

PROGRAM of MEWS

38

Date: 2025/10/23-24

Venue: Tsukuba Int'l Congress Center

Host: Japan Aerospace Exploration Agency



DAY 1 | Agenda

Thursday, October 23rd, 2025

10:00 am	DAY1 Venue OPEN	
10:20 am	Welcome Greeting	Noriyuki Inaba JAXA
DAY1-1 10:30 am – 11:00 am		p. 3
10:30 am	Elevating the Future of Europe in Space	Britta Schade & Sylvain Bouchart ESA
Break & Exhibition (Start)		
DAY1-2 11:10 am – 12:10 pm		p. 4
11:10 am	Research and development of new EEE component technologies for JAXA's new medium/long-term plan	Hiroyuki Shindo JAXA
11:30 am	Introduction of Space-Grade Microprocessors, SOI-SOC series	Daisuke Matsuura MHI
11:50 pm	Accelerated Computing for Space Applications: Reconfigurable GR765 Octa-core and GR801 edge AI processor	Christian Sayer Frontgrade
Lunch & Exhibition (p.32) 12:10 pm – 1:40 pm		
DAY1-3 1:40 pm – 2:30 pm		p. 7
1:40 pm	DLR Update on EEE-Components	Arianit Preci & Burak Gökgöz DLR
2:10 pm	Pioneering Radiation-Tolerant SoC FPGAs for Space with Low Power RISC-V® Architecture	Minh Nguyen Microchip Technology
Break		
DAY1-4 2:40 pm – 3:40 pm		p. 9
2:40 pm	Modern FPGAs for SWAP-C Constrained Mission Critical Applications	Esam Elashmawi & Jim Tavecchi Lattice Semiconductor
3:00 pm	Custom eFPGA IP for Mission-Critical Space Applications Using Australis IP Generator	Ichiro Tajima QuickLogic
3:20 pm	Teledyne e2v Space Semiconductors	Mariano Fantini Teledyne e2v
Break & Exhibition (30 min.)		
DAY1-5 4:10 pm – 5:30 pm		p. 12
4:10 pm	Synthetic Aperture Radar Processing in Space with AMD Versal™ Adaptive SoCs	Ken O'Neill AMD
4:30 pm	CASPEX: A Generic Camera Heads Family for Space Imaging Applications	Julien Bezzine 3D PLUS
4:50 pm	Monolithic and hybrid integrated on chip optical filters for compact multi-and hyperspectral imaging payloads	Bavo Delauré imec
5:10 pm	European Dual Band Beamformer IC	Frank Henkel IMST
5:30 pm	Adjourn for the day	
6:00 pm	WELCOME RECEPTION (in Room 102) [Fee: 7,000 JPY]	

DAY 2 | Agenda

Friday, October 24th , 2025

9:00 am	DAY2 Venue OPEN	
DAY2-1 9:20 am – 10:30 am		p. 16
9:20 am	Inside ESA's EEE Strategy: Evolving Standards, Mission Classification and EEE Sovereignty Alongside Collaboration with JAXA	Leo Farhat ESA
9:50 am	Next Generation Space Power Products from 12V-500V	Jutta Heinzelmann & Helmut Puchner Infineon Technologies
10:10 am	New space grade power management ICs for all space missions	Mark Toth Texas Instruments
Break		
DAY2-2 10:40 am – 11:40 am		p. 19
10:40 am	Vicor's Radiation Tolerant Factorized Power Modules for LEO & MEO Applications	Yutaka Mizutani Vicor
11:00 am	Lead-free Transition for the European Space Sector (LETTERSS):a new EU-funded R&D project	Agustin Coello-Vera ReachLaw
11:20 am	Advanced High Power Hermetic Sealed Package for Space Applications	Mikiya Tamaru TECNISCO
Lunch & Exhibition (p.31) 11:40 am – 1:00 pm		
DAY2-3 1:00 pm – 1:45 pm		p. 22
1:00 pm	CNES Components activities: Focus on the challenges of testing complex components	Florence Malou & Guillaume Bascoul CNES
1:15 pm	NASA EEEE Parts Activities Update A: The NASA Report B: NASA Efforts Towards a Holistic COTS Approach for Space Avionics	A: Shri Agarwal (JPL) B: Peter Majewicz (GSFC) NASA
Break & Exhibition (End)		
DAY2-4 2:10 pm – 3:30 pm		p. 25
2:10 pm	MLCC product lineup for automotive applications and expansion into space products	Hiroya Fujii FUKUI MURATA Mfr.
2:30 pm	Sub-Micrometer-Thickness Plastic Film Capacitor Technology	Daisaku Mukaiyama Rubycon
2:50 pm	Initiatives to Promote the Utilization of COTS Parts in Satellites	Yoichiro Kusuda ASTEC
3:10 pm	Design Approach for High-Performance COTS FPGAs in Photonic-Electronic Devices for Satellite Systems	Yuzo Yajima MELCO
Break		
DAY2-5 3:40 pm – 4:50 pm		p. 29
3:40 pm	High Speed + High Density + High Reliability How does Base Material Support Modern Space PCBs	Monique Mayr Panasonic Industry
4:00 pm	GREEN SPACE and ZERO DEBRIS-EEE(E) EVALUATIONS	Michael Moesken TESAT
4:20 pm	Tradeoffs to optimize radiation efforts on COTS components	Jeremy Guillermin TRAD
4:40 pm	Wrap-up & Closing Remark	Hiroyuki Shindo JAXA
4:50 pm	Adjourn for the day	

Elevating the Future of Europe in Space

Sylvain Bouchart / Britta Schade
European Space Agency

In this talk Britta Schade and Sylvain Bouchart will cover ESA's achievements so far in 2025; the preparation of the 2025 Council of Ministers ('CMin') and the main priorities promoted by the Agency and the ESA Strategy 2040.

The keynote also includes an update from the Technology Engineering & Quality Directorate (TEC).

Research and development of new EEE component technologies for JAXA's new medium/long-term plan

H.Shindo*

* Japan Aerospace Exploration Agency (JAXA)

In order to sustainably develop future space activities, JAXA is continuously engaged in research and development of EEE component technologies for space applications. In addition, our new medium/long-term plan has been launched from this fiscal year to incorporate the results of our R&D into the social system and to serve the public. R&D system itself has recently been strengthened, and collaboration with component companies is underway, not only for space but also for applications in the terrestrial industry.

This presentation will introduce the latest status of JAXA's research and development efforts, including new Atom-switch non-volatile FPGAs and related technologies, next generation microprocessors, and power devices utilizing wide bandgap semiconductor technologies. Current status of a feasibility study of new technologies such as Silicon-photonics, Diamond devices for power management applications and new methods for predicting the effects of radiation on semiconductor devices will also be presented.

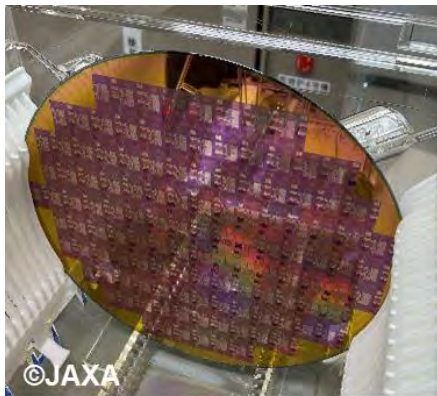


Fig. 1 Trial production of 12nm SoC NB-FPGA

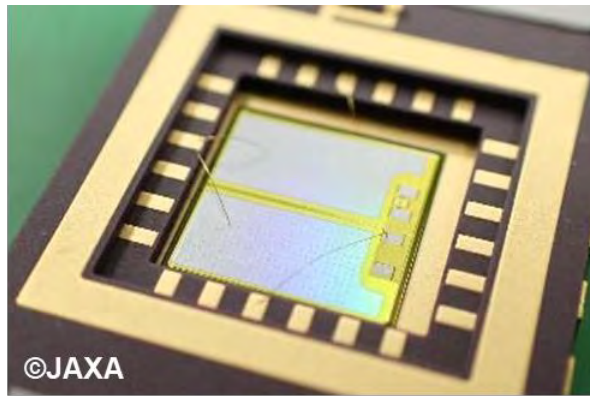


Fig. 2 Prototype sample of SiC MOSFETs with a new radiation-resistant reinforced structure. (Patent pending)

Introduction of Space-Grade Microprocessors, SOI-SOC series

Daisuke Matsuura*, Kazunori Mochizuki*, Shigeru Ishii*, Daisuke Takahashi*,
Masaki Kusano*, Yoshiharu Mori*, Hirotaka Yamada*

* Mitsubishi Heavy Industries, Ltd.

Mitsubishi Heavy Industries(MHI), has been developing radiation-hardened microprocessors using silicon on insulator technology (SOI-SOC series), under cooperation with JAXA. In this presentation, 2 types of SOI-SOC series microprocessors, SOI-SOC2 and SOI-SOCX are described.

SOI-SOC2 is a flight-proven microprocessor which had already been applied to over 10 satellites (e.g. Arase (ERG), XRISM).

Based on technologies obtained from SOI-SOC2, MHI was developed, under JAXA, the next generation microprocessor, SOISOC4. Performance and communication interfaces of the SOISOC4 are upgraded, aiming at meeting the needs of future space mission. SOISOC4 is designed with world's top-class power efficiency.

Qualification model chips, manufactured in JFY2023, showed good results in terms of radiation and electrical characteristics. Qualification JAXA-QTS-2010 test was completed by the end of JFY2024.

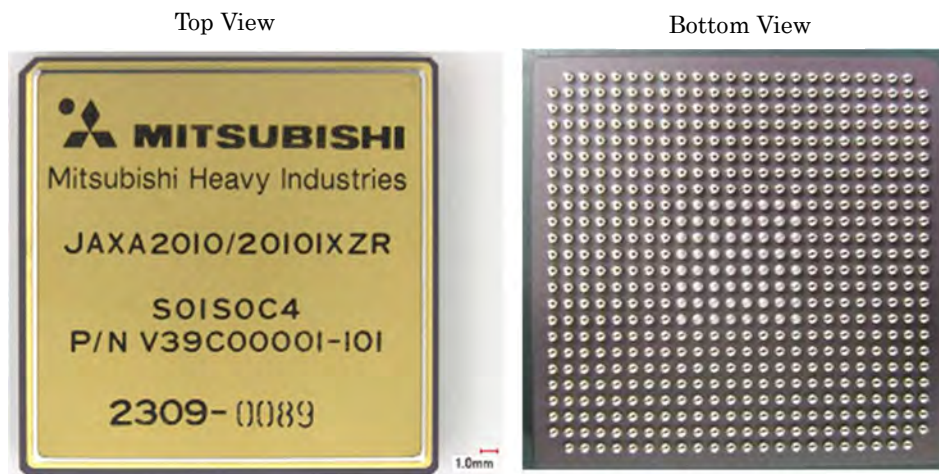


Fig. 1 Photo of SOISOC4 (Ceramic Ball Grid Array package)

Accelerated Computing for Space Applications: Reconfigurable GR765 Octa-core and GR801 edge AI processor

Christian Sayer, Juan Pedro Cobos, Kenneth Östberg
Frontgrade Gaisler, Göteborg, Sweden

Modern on-board processing aims to perform tasks well beyond the classic AOCS/GNC of the on-board computer and the linear data processing of traditional payloads. Autonomous landing and docking, object detection and tracking in EO data as well as for debris detection, and on-board data triage are only some of the most prominent examples. AI-driven, accelerated edge computing is setting the requirements for new space grade semiconductor components.

Frontgrade Gaisler is enabling design and efficient implementation of such applications with two new components: The GR765 octa-core system-on-chip (SoC) with embedded FPGA, and a neuromorphic processor – the GR801.

The GR765 is a radiation-hardened, fault-tolerant octa-core system-on-chip (SoC) with a variety of on-chip functionalities aiming for highest performance and flexibility. An embedded NanoXplore FPGA fabric can be configured at start-up to implement hardware acceleration, additional interfaces, custom protocols, glue logic and more. The device implements both most prominent instruction set architectures currently used in high-rel spaceflight: RISC-V and SPARC V8. The entire system is initialized into one or the other mode during the reset and boot phase. High-speed serial interfaces including Spacefibre and PCI Express Gen3 are complemented by traditional spacecraft interfaces such as MIL-STD1553 and a SpaceWire router. An ONFI 4.0 compliant NAND flash controller enables high-density mass storage, and volatile memory is supported by a DDR2/3/4 controller.

The GR801 SoC combines a neuromorphic processing engine (BrainChip Akida™ 1.0) with a fault-tolerant RV64GC RISC-V processor. A versatile set of communication interfaces allows it to be used as a near-sensor edge processing node, as well as a power-efficient accelerator connected to a larger SoC, such as the GR765. Besides traditional data streams, the Akida engine also supports event-based processing to achieve highest energy efficiency in sensor applications.

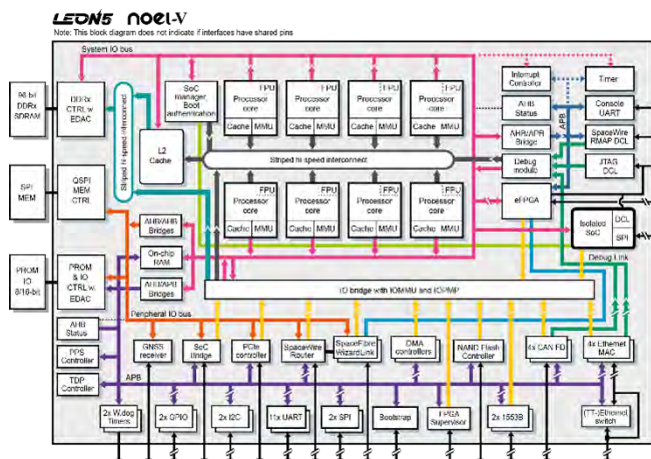


Fig. 1: GR765

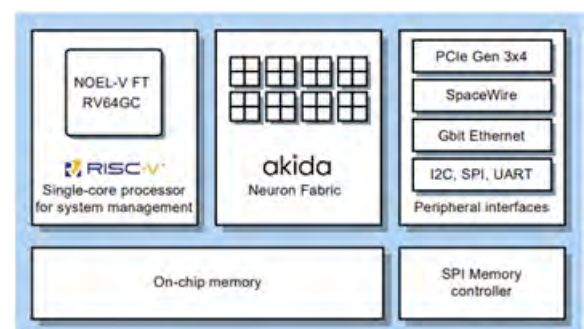


Fig. 2: GR801

DLR Update on EEE-Components

Presenters Mr. Burak Gökgöz * and Mrs Anita Weinschrott-Schaaf **

* German Space Agency at DLR, ** Tesat-Spacecom GmbH & Co. KG

This talk will begin with a brief introduction to the German Aerospace Center at DLR.

DLR will provide an overview of the activities of the EEE-Components Division, including ongoing national development and ESCC qualification projects, as well as planned future EEE components projects. The national exchange platforms 'Gallium Nitride' and 'Optoelectronics' will be introduced, and the status and interim results of these initiatives and stakeholder workshops will be presented.

In addition, the speech will provide an update on the 'Space2Motion' working group, which was initiated by the German Space Agency at DLR and focuses on the use of automotive components in space applications. Serving as a national exchange platform between the automotive and space sectors in Germany, Space2Motion focuses on technology transfers and R&D cooperation. DLR will also provide an insight into COTS activities in general.

The speech will conclude by addressing the German-Japanese collaboration in the field of automotive EEE components.

Pioneering Radiation-Tolerant SoC FPGAs and PIC64-HPSC MPUs with Low Power RISC-V® Architecture

Minh Nguyen, Microchip Technology

This presentation will provide an overview of Microchip Technology's key enabling FPGA and High-Performance Spaceflight Computing (HPSC) technologies, addressing the increasing demands for enhanced signal processing in next generation space systems without sacrificing reliability or performance.

The PolarFire® FPGA, PolarFire SoC and RT PolarFire families already deliver the industry's best thermal and power efficiency in the mid-range segment. Optimized for deploying systems with high-compute performance in small form factors, the families have reduced the size and weight of power-constrained systems in applications including imaging, robotics, smart defense and aerospace systems. Our future technology will go even further up the performance and power-efficiency curve and add new RISC-V-based high-performance compute elements. The benefits which Microchip FPGA families bring to enable high-performance spaceflight computing will be discussed.

The RT PolarFire family of SoC FPGAs specifically represents a new generation of radiation-tolerant embedded systems. Built on Microchip's flight-proven RT PolarFire FPGA fabric, these devices offer outstanding power efficiency, high reliability, best-in-class security and enhanced radiation performance, making them ideal for deployment in demanding environments with broad offerings for Low Earth Orbit (LEO), deep space or anything in between.

This abstract summarizes the key features, capabilities, and radiation resilience characteristics of these SoC FPGAs. The RT PolarFire SoC FPGA leverages the RISC-V® architecture, supporting not only the flexibility of Linux®-based systems but also ensures the determinism required for real-time control systems. Its multi-core processor, coherent with the memory subsystem, provides central satellite processing capabilities akin to single-board computers widely used in the space industry for command and data handling, platform avionics, and payload control. This versatility enables the development of highly integrated designs that are customizable and adaptable over time while optimizing size, weight, and power considerations.

Designed to withstand the harsh radiation conditions of space, the RT PolarFire SoC FPGA eliminates the need for external scrubbers by achieving zero configuration memory upsets, reducing both system complexity and cost. By consuming up to 50% less power compared to competing solutions, it simplifies satellite design, easing thermal dissipation challenges and power management requirements.

In addition, the PIC64-HPSC series of 64-bit microprocessors (MPUs) represents a revolutionary step forward in radiation-hardened and radiation-tolerant processors for space exploration applications. The PIC64-HPSC series offers a 100 times improvement in processing capability compared to traditional space processors. These MPUs also bring new capabilities to space applications, such as virtualization, Artificial Intelligence/Machine Learning (AI/ML), Ethernet Time-Sensitive Networking (TSN), Remote Direct Memory Access over Converged Ethernet (RoCE) v2, PCIe®, Compute Express Link® (CXL®) 2.0 and post-quantum cryptography. The PIC64-HPSC enables autonomous missions by bringing intelligent edge computing to LEO, GEO and deep space.

Finally, coupled with Microchip's Mi-V ecosystem, which supports a wide range of operating systems such as Linux, VxWorks®, and Zephyr®, designers can accelerate development timelines for mission-critical applications. Mi-V is a comprehensive suite of tools and design resources, developed with numerous third parties, to support RISC-V designs. The Mi-V ecosystem aims to increase adoption of the RISC-V instruction set architecture (ISA) and support Microchip's SoC FPGA and PIC64 portfolio.

Backed by over six decades of expertise in powering spaceflight missions and a path to achieving the Qualified Manufacturers List (QML) qualification, the RT PolarFire SoC FPGA and PIC64-HPSC deliver a reliable, high-performance, and radiation-tolerant platform for advancing the frontiers of space exploration.

Modern FPGAs for SWaP-C Constrained Mission Critical Applications

Esam Elashmawi / SVP, Mktg & Strategy, Lattice Semiconductor
Jim Tavacoli / Sr Dir Product Mktg, Lattice Semiconductor

The space industry is undergoing an unprecedented expansion to offer new capabilities and services. Lattice leverages the experience to build power efficient, small form factor and reliable FPGAs to deliver a scalable portfolio of inherently radiation tolerant FPGAs in support of the emerging field of small satellites for governments and businesses worldwide.

Especially for the rapid growth of low-earth orbit satellites, much of the volume is in LEO where there are no DLA qualification requirements. Lattice FPGA has some performance features that we see people need in SPACE(LEO) & AVIONICS.

Lattice Semiconductor provides a new FPGA technology platform for its low-power FPGAs based on 28nm fully depleted silicon-on-insulator (FD-SOI) process technology.

We are using FD-SOI to enable the development of some FPGA families that provide up to 75% reduction in power compared with competing families, are 100 times more reliable in terms of soft error rate, can deliver the smallest form factor.

Lattice strives to provide the most reliable FPGAs for space and other harsh environment applications. Lattice NEXUS FPGA reliability and quality have been independently verified by multiple agencies in the United States and Europe to meet the performance, reliability and lifecycle demands of space systems by taking advantage of the following results:

Immunity to single event latch-up, tested to high LET

High Total Ionizing Dose Immunity

Instant-on feature configures I/O in under 4ms with full FPGA configured in less than 30ms

Interleaved SRAM memory architecture with no Multiple-Bit Upsets detected

In addition to characterizing radiation effects in reconfigurable FPGAs, Lattice offers mitigation techniques including built-in error detection and correction as well as Triple Modular Redundancy.

Working with a wide array of developers and subject matter experts, Lattice participates in an open radiation test consortium to facilitate industry cooperation, accelerate the development of test platforms and enable public awareness and access to test results.

Lattice focuses on SWaP-C Optimization. (SWaP-C refers to the concept of optimizing size, weight, power, and cost.)

Lattice products have been launched into space by multiple companies in the USA and Europe including US government agencies. And there are some public test reports conducted by US Government agency such as NASA.



Fig. 1 Target Application 1



Fig. 2 Target Application 2

Custom eFPGA IP for Mission-Critical Space Applications Using Australis IP Generator

Presenter: Tajima, Ichiro Co-author: Wang, Mao

In mission-critical domains such as aerospace, defense, and high-reliability industrial systems, flexibility, reliability, and long-term availability are essential. Traditional fixed-function silicon often cannot meet the evolving requirements of these applications due to rigid architecture and limited lifecycle support.

This presentation introduces a customizable embedded FPGA (eFPGA) IP solution, generated using QuickLogic's Australis eFPGA IP generator and tailored specifically for mission-critical and space applications. Australis enables rapid creation of right-sized, power-efficient, and radiation-tolerant eFPGA IPs for integration into ASICs and SoCs.

We will present key architectural features including support for formal verification, fault tolerance, and space-grade security capabilities such as anti-tamper and secure boot. Case studies will demonstrate how our methodology shortens silicon design cycles while improving adaptability and system resilience. Benchmark results will illustrate trade-offs in performance, silicon area, and power consumption, highlighting the advantages of this technology for long-duration and reconfigurable space missions.

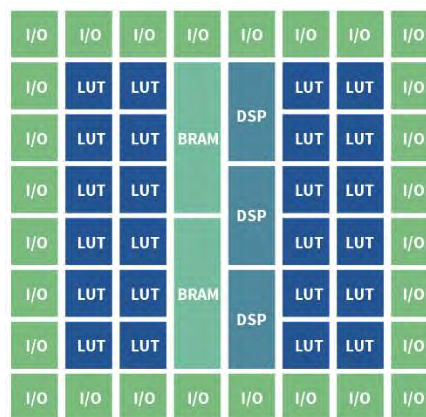


Fig. 1 eFPGA Architecture

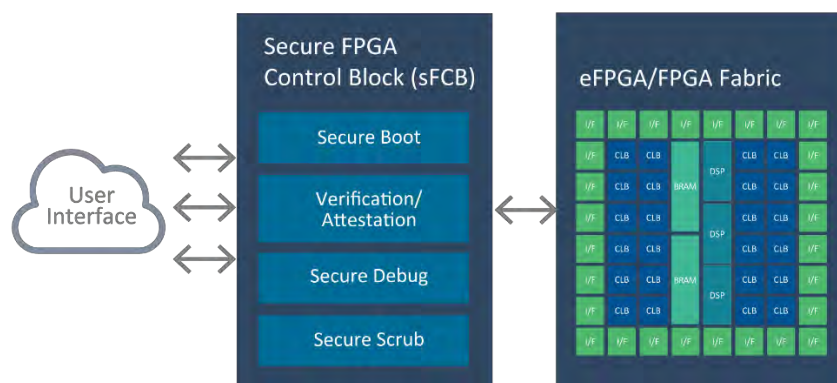


Fig. 2 Built-in features protect data and IP

Teledyne e2v Space Semiconductors

Mariano Fantini, Marc Stacler

Field application engineer (EMEA), Field application engineer (USA)

Teledyne e2v is a global leader in advanced technologies that span semiconductors and imaging systems. As part of Teledyne Technologies Inc., the company plays a pivotal role in enabling innovation across industries such as aerospace, defense, medical and space exploration.

Headquartered in Grenoble, FR, Teledyne e2v designs and manufactures high-reliability components and subsystems tailored for demanding environments. Its semiconductor division produces radiation-tolerant microprocessors, data converters and memory modules, which are critical for aerospace and defense applications.

We delivered the world first broadband ADC and DAC in NASA space systems back in the 1995 and we are the first to introduce Radiation Hardened ADC and DAC enabling Direct Conversion till Ka Band. Our Data converters enable deep RF softwarization allowing multi-band digitization and signal generation critical for resilient satellite communication, navigation and Earth observation systems.

Teledyne e2V is also the industry leader on Space qualified High Performance, Low Power Microprocessor and Memory Solutions. Our gigahertz clock rate, low power, CMOS multicore microprocessors featuring proven reliability, extended temperature range operation, robust packaging and radiation testing are used in many Space and Defense programs in the US and in Europe. We are introducing now the first to introduce a space qualified 16 cores ARM72, called LX2160. Teledyne e2v has been the first to introduce a Space Grade DDR4. Our DDR4 is the most deployed in Space worldwide and enable flexible and ultracompact design with all Space processors and FPGA.

Teledyne e2v's commitment to innovation is reflected in its collaborations with academic institutions and industry leaders, as well as its involvement in high-profile programs like the Airbus A380, Eurofighter Typhoon, and multiple space missions. With a workforce of over 400 employees and a strong emphasis on quality, reliability, and long-term partnerships, Teledyne e2v continues to deliver cutting-edge solutions that touch lives and shape the future of technology.

In this session, Teledyne e2v will showcase its latest high-performance processing technologies, including DDR4 memory solutions, multi-core ARM processors, and the advanced Qormino processing modules. The presentation will also feature updates on the company's newest K-band capable data converters.



Fig. 1 Teledyne e2v's products

Synthetic Aperture Radar Processing in Space with AMD Versal™ Adaptive SoCs

Ken O'Neill, Jason Timpe, Mark Rollins
Advanced Micro Devices

Synthetic Aperture Radar (SAR) is a technique whereby high resolution radar images can be created using a relatively small radar antenna, simulating the effect of a much larger and more expensive antenna. The technique relies on the motion of the radar platform relative to the target, and uses multiple samples of radar returns from the target to build up high resolution images. Several different algorithms exist for SAR processing, however they all require large amounts of high performance compute resources. In conventional satellite and airborne applications, the raw SAR data is returned to the ground for processing. This creates a large communications bottleneck, and limits the amount of SAR data that can be collected during the mission. With modern space-grade adaptive SoCs, SAR data can be processed efficiently on board the radar platform, and finished images can be transmitted to the ground which avoids the communications bottleneck and allows more SAR images to be sampled as the spacecraft or aircraft flies over the earth.

In this presentation, we examine range/doppler processing and back-projection, which are two separate processing algorithms for SAR which are useful in space applications, and summarize the implementation of both algorithms in an AMD Versal adaptive SoC.

We will also provide an update on the space qualification of the XQR Versal adaptive SoCs, and provide the latest reliability and radiation data.

CASPEX: A Generic Camera Heads Family for Space Imaging Applications

Julien BEZINE*

* 3D PLUS

Reducing the size and mass, but also the cost and delivery time, of space payloads – including optical instruments – is a growing priority for the space industry. As achieving this goal cannot come at the expense of quality and reliability, which remain critical to meeting mission requirements, it introduces complex design constraints and trade-offs. This presentation introduces 3D PLUS CASPEX product family, its specific design strategy, testing and qualification results, and how it answers these new challenges.

3D PLUS has developed, in the framework of its R&D activities, a family of highly miniaturized, radiation tolerant, and off-the-shelf modules for space imaging applications, called CASPEX (CAmera heads for SPace EXploration). CASPEX camera heads leverage 3D PLUS 3D packaging technologies, refined over more than 30 years for its standard products, to offer all-in-one, space grade, solutions. These compact modules enable users to significantly reduce the complexity, size, and mass of optical payloads, by integrating all proximity electronics alongside high-resolution visible or SWIR image sensors, into one compact module with specifications ensuring suitability for wide range of applications.

Each CASPEX camera head integrates alongside its image sensor a complex electronic architecture providing processing, power and radiation protection functionalities. The electronic architecture is FPGA based, incorporating a generic processing core with volatile and non-volatile memories for operation of the image sensor and processing or storage of the image and video data before transmission through standard interfaces such as SpaceWire. Power conversion is fully integrated, requiring only a 5V input to power all components. Radiation mitigation techniques such as triple modular redundancy, latch-up protections, or drift compensation are employed to ensure high reliability in harsh space environments. Special attention is given to optimizing optical, mechanical and thermal interfaces to ensure high performance over a wide range of mission profiles. The CASPEX design strategy, applying careful selection and evaluation of EEE parts including radiation testing (TID, TNID, SEL, SEE), coupled with strategic stock management for both EEE part and CASPEX modules, and space grade FPGA design development allows 3D PLUS to offer generic, cost-effective, low lead time and off-the-shelf imaging solutions for space applications.

The CASPEX camera heads family includes two CMOS visible-range camera heads - 4Mpx for 62g and 12Mpx for 120g (Fig.1) - and one InGaAs SWIR camera head - 1.3Mpx for 140g. Both visible camera heads passed qualification successfully (Thermal cycling, Life Test, Endurance, Mechanical testing) guaranteeing the product performances with regards to reliability, temperature, radiations (TID > 30-40 krad(Si), SEL LET th > 62.5 MeV.cm²/mg). CASPEX SWIR camera head is expecting full qualification by end of 2025.

The CASPEX family is gaining increasing space heritage, being part of high-profile science missions, benefitting from its high level of miniaturization and radiation tolerant design, such as **JAXA's** DESTINY+, **JAXA/CNES/DLR's** MMX mission, **NASA's** Perseverance (SUPERCAM instrument) and DART (LICIACube) missions, as well as multiple other commercial missions such as OneWeb constellation (SODERN's Auriga star tracker). The CASPEX family addresses all imaging applications, from observation or spectrometry to detection and tracking, or navigation and rendezvous.



Fig. 1 CASPEX 4M and CASPEX 12M Camera Heads

Monolithic and hybrid integrated on chip optical filters for compact multi-and hyperspectral imaging payloads

B. Delauré*, B. Berteloot, W. Charle*, B. Geelen*, N. Nguyen, and K. Tack*

* imec, Kapeldreef 75, 3001 Leuven, Belgium,

Over the past decade, improved access to space has unlocked vast opportunities for Earth observation, highlighting the potential of compact, lightweight optical payloads aboard small satellites. Emerging satellite constellations now enable high temporal, spatial, and spectral resolution monitoring of our planet. A key enabler of this progress is the miniaturization of optical instruments—though this brings challenges in balancing compactness with performance.

A promising solution lies in the highly integrated design of thin-film optical filters directly combined with image sensors. This approach enhances compactness, robustness, and design flexibility. At imec, we leverage our expertise in semiconductor fabrication and process technology to develop wafer-level, interference-based optical filters. These filters can be deposited and patterned directly on image sensor pixels or on glass substrates integrated into the detector package.

Thanks to lithographic precision, filters can be defined at the single-pixel level, enabling highly optimized geometric layouts that minimize transition zone losses in the focal plane. This eliminates the need for complex alignment between the detector and external filters, paving the way for versatile, multipurpose imaging systems.

Two common filter architectures have been developed: line-based patterns for Time Delay Integration (TDI) to enhance signal-to-noise ratios, and mosaic patterns (e.g., 4×4 or 5×5 filter matrices) for real-time video operation. These configurations are particularly advantageous for dynamic scene monitoring in space exploration missions, such as rovers or asteroid missions like Hyperscout-H aboard ESA's HERA mission.

Our CMOS-based platform enables compact, robust, and scalable filter integration with high yield and low cost. The baseline Fabry-Pérot filter design consists of a transparent cavity layer sandwiched between two Bragg reflector mirrors—multi-layer stacks of alternating high and low refractive index materials. Mirror reflectivity defines spectral characteristics such as bandwidth (FWHM) and quality, while cavity thickness determines the central wavelength. This platform also supports more complex filter stacks, including multi-cavity and high optical density (OD) designs.

This presentation will showcase imec's latest developments in multi- and hyperspectral filters on CMOS and InGaAs sensors, including a 96-band hyperspectral imager covering 450–900 nm. We will also present examples of on-chip spectral imagers currently operating in orbit or scheduled for launch later this year.

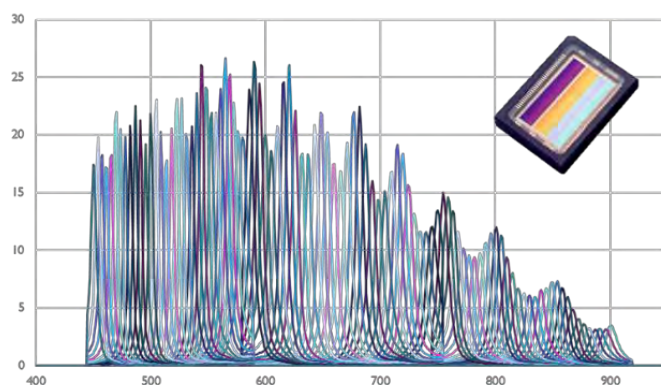


Fig. 1 96 band hyperspectral imager

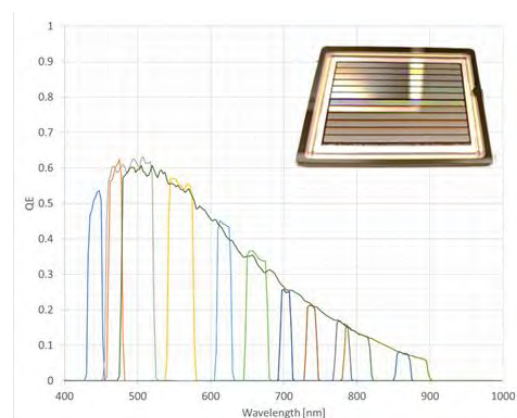


Fig. 2 11 band + PAN multispectral imager

European Dual Band Beamformer IC

Frank Henkel*, Tobias van Rey* and Alexander Hees**

* IMST GmbH, Germany ** Airbus Defence & Space GmbH, Germany

IMST GmbH, Germany is a design house and a supplier of radiation hard (RH) ASICs. The company obtained full ESA ESCC certification of its mixed-signal ASIC supply chain by February 2024. At the moment, IMST together with Airbus DS are working on a radiation hard Dual Band Beamformer IC for space applications which supports the C-Band and the X-Band as well. The design is implemented on a high speed SiGe-BiCMOS process from Infineon (B11HFC) and is using an organic package. The presentation will cover the architecture and system approach of the IC and the implementation of important target specifications related to phased arrays for radar and telecom applications. Tradeoffs will be presented and first ideas on the circuit design are shown. An outlook will be given on the next project steps and the planned way towards a fully qualified EEE component under the ESA ESCC system. The project is running under the ESA GSTP program and is supported by the German aerospace research and technology centre DLR.

Inside ESA's EEE Strategy: Evolving Standards, Mission Classification and EEE Sovereignty - Alongside Collaboration with JAXA

Léo Farhat, Karin Lundmark, Ali Zadeh
European Space Agency

This presentation provides an overview of the ongoing evolution of ESA's strategy for Electrical, Electronic, and Electromechanical (EEE) components, highlighting both technical developments and international collaboration.

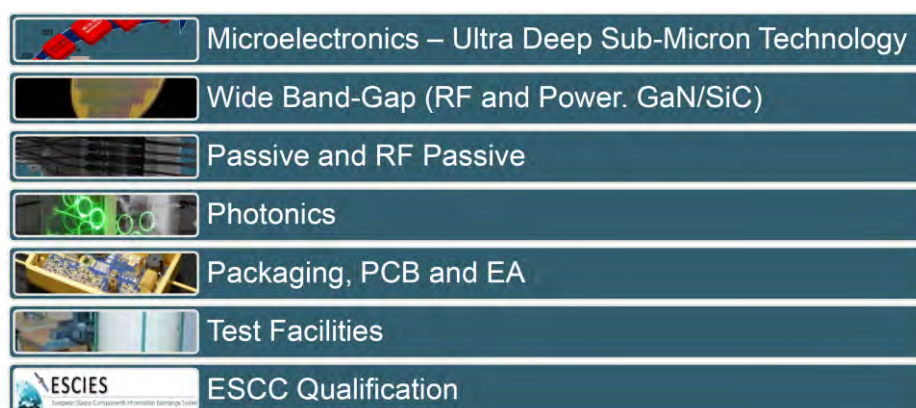
The update of the ECSS-Q-ST-60 standard marks a significant milestone, as it now integrates Japanese QTS-qualified parts, strengthening the harmonization of component assurance practices across space agencies. In parallel, the ESCC system has undergone restructuring with the introduction of a three-part European Preferred Parts List (EPPL). This new approach not only improves the classification of EEE parts but also opens the possibility for manufacturers to have COTS+ components certified under the Enhanced Grade Qualified Manufacturers List (EG-QML).

The presentation also addresses the recent evolution of ESA's mission classification, with new categories for satellites (Alpha, Beta, Gamma, Delta) linked to EEE class levels (Class 1, 2, and 3). This framework ensures a more consistent balance between cost, performance, and reliability across mission types.

Looking ahead, the outcomes of CMIN2025 are discussed, emphasizing the strategic objective of strengthening European sovereignty in EEE components and consolidating long-term development activities.

Additionally, an overview is provided of how ESA is supporting European manufacturers in developing new technologies for space, particularly in the field of passive components, as well as upcoming ESA-organized conferences dedicated to EEE components.

Finally, the collaborative dimension of ESA's EEE work is highlighted through joint missions with JAXA, including EarthCARE and BepiColombo. Particular attention is given to our EEE team's contribution in resolving an in-orbit anomaly on BepiColombo, traced to a component issue, which demonstrated the critical role of EEE expertise in ensuring mission success.



ESA Technology lines for European Sovereignty

Next Generation Space Power Products from 12V-500V

Jutta Heinzelmann*, Dr. Martin Göllner*, Dr. Tudor Chirilla* and Dr. Helmut Puchner**

* Infineon Technologies, Munich, Germany

** Infineon Technologies, San Jose, USA

The increasing demand for reliable and efficient power systems in New Space and LEO missions has driven the need for radiation tolerant power solutions. However, designing and manufacturing such components poses significant challenges due to the harsh radiation environment in space. We continuously expanding our solution portfolio with innovative and novel solutions. We will present a general and adaptable digital controlled power solution based on PMBus for processing payloads based on 12V input voltages. Reliability can be customized for each orbit with added hot standby power rails to ensure failsafe power rails.

To address DC-DC conversion applications the industry's first radiation tolerant power MOSFETs, were released in 2024. The 60V and 150V n-channel MOSFETs with low RDSON ratings are based on Infineon's COOLMOS™ technology and come in SMD and Through Hole plastic packages. The parts are qualified to withstand TID of up to 30krad and a SEE of 46MeV·cm²/mg. We are expanding the portfolio with -30V/-60V p-channel MOSFETs and a LS-Driver IC. All radiation tolerant components will meet TID of 30krad and a SEL immunity of 46MeV·cm²/mg.

Beyond the radiation tolerant product portfolio Infineon HiRel division, in partnership with the German Aerospace Center and the European Space Agency, launched the European Power SiC Supply Chain (EPOSIC) research project, the first of its kind. This ambitious project will lay the foundation for exploring and developing Silicon Carbide (SiC) based semiconductor solutions for space applications for the first time. DLR and ESA foresee a trend towards high-power platforms in space applications, with bus voltages up to 300V. To address this requirement, a high-performance power MOSFET technology is necessary, capable of reliable operation at 300V at high junction temperatures. Within the EPOSIC project the performance of wide-band-gap SiC technology will be evaluated and improved to meet also the necessary radiation performance for such kind of missions. We will provide an project overview and the current status.

NOTE1: The submitted PDF will be published as-is.

NOTE2: The copyright of submitted abstracts shall be transferred to the MEWS Secretariat.

New space grade power management ICs for all space missions

Mark Toth
Texas Instruments, Inc.

An overview of new space-grade products from TI bringing modern power management capabilities to the space industry will be presented. Key new product types for payload applications include wide-input voltage and multi-channel buck point of load (PoL) converters, ultra-low-noise and wide-input linear regulators, along with power supply sequencers and supervisors. For satellite bus power, solutions include PWM controllers with integrated Gallium Nitride (GaN) driver, gate drivers for GaN solutions, and GaN Power stage.

Product categories include QML-V (hermetic) and QML-P (plastic) packaged devices for high-reliability, GEO missions, along with Space EP devices for LEO and shorter missions. Total Ionizing Dose (TID) test levels range from 30krad(Si) to 100krad(Si), while single-event-effect characterization levels range from 43 MeV·cm²/mg to 75 MeV·cm²/mg

Complete power solutions for popular space FPGAs will also be presented. Reference designs for power converters of multiple types such as synch. buck, boost, flyback, forward, zero-voltage-switched (ZVS) full-bridge covering power levels from 5W to 300W will be presented as well.

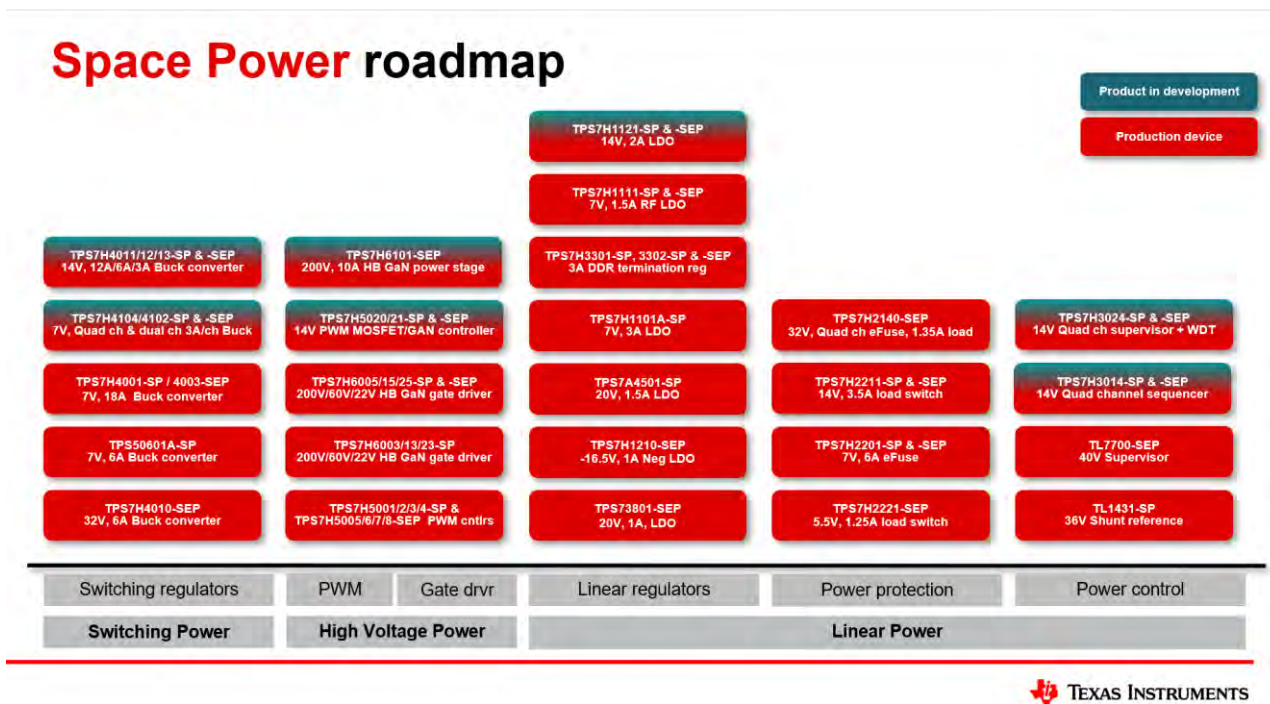


Fig. 1. TI space power roadmap

Vicor's Radiation Tolerant Factorized Power Modules for LEO & MEO Applications

Presenter: Yutaka Mizutani

Affiliation: Vicor K.K.

Satellites are increasingly incorporating high-performance computing (HPC) placing new demands on radiation tolerant power delivery networks (PDNs). These PDNs must deliver hundreds of amps of current at less than 1V to supply advanced processors for AI and other applications as satellites become more sophisticated. To meet this growing need, Vicor developed and evaluated a satellite power solution featuring a 100V input and 0.8V/150A output.

This power board, measuring approximately 150 x 40 x 15mm, comprises 3 key power modules: PRM2919 with regulation functionality (18.2g), VTM2919 (13.3g) with voltage transformation functionality, and BCM3423 (Bus Converter Module) with isolation functionality (25.9g), along with passive components like LRCs. Each module is remarkably compact, with PRM2919 and VTM2919 measuring 29 x 19 mm, BCM3423 measuring 34 x 23 mm.

The FPA (Factorized Power Architecture) comprises 2 core modules: PRM (Pre-regulation Module) and VTM (Voltage Transformation Module). The PRM converts an unregulated input source into a regulated output voltage, which then supplies power to VTM. The VTM efficiently transforms this voltage to the precise level required by the load. This FPA achieves high efficiency, up to approximately 94% by applying current resonance technology and over 1 MHz switching frequency to separate power regulation from power conversion.

Another key characteristic of the FPA is its PoL (Point of Load) placement, by positioning the VTM as close as possible to the load, the FPA minimizes I²R power consumption caused by current and PCB trace resistance. This approach enables a compact power system with high overall efficiency by significantly reducing I²R power consumption within the PDN (Power Delivery Network).

Although this power board is a remarkably compact solution for satellites, measuring approximately 150 x 40 x 15mm. Each of BCM3423, PRM2919, and VTM2919 modules is radiation tolerant.

These modules support TID of 50krad. Additionally, to mitigate SEE (Single Event Effects), each of BCM3423, PRM2919, and VTM2919 modules integrates 2 redundant power circuits. Thereby providing high reliability.

We evaluated the thermal performance of this board and present the findings.

Lead-free Transition for the European Space Sector (LETTERSS): a new EU-funded R&D project

Agustin Coello-Vera
REACHLaw, FINLAND

The global electronics industry's shift toward lead-free solutions poses significant challenges for the space sector, particularly in managing risks associated with Electrical, Electronic, and Electromechanical (EEE) components featuring lead-free finishes. The growing adoption of Commercial Off-The-Shelf (COTS) components, driven by the expanding satellite constellation market, has increased the use of lead-free finishes in European space projects, even when high-reliability leaded alternatives are available. Although the space sector is exempt from RoHS regulations, compliance with REACH and evolving market dynamics may limit the future availability of leaded solder paste, necessitating proactive strategies to ensure reliability and performance.

The LETTERSS project (Lead-free Transition for the European Space Sector), funded by the European Commission's EU Space R&D Programme, addresses the critical challenges of transitioning to lead-free soldering, as outlined in the 2020 ESCC Task Force Roadmap. This presentation will detail the project's methodologies to overcome barriers to integrating COTS components into space projects, which currently rely on qualified leaded solder assembly processes. Furthermore, it will showcase a comprehensive evaluation of two promising lead-free solders for space applications, including the development of reliability models to support their adoption in high-reliability environments.



**Funded by
the European Union**

Advanced High Power Hermetic Sealed Package for Space Applications

Mikiya Tamaru^{*}, Mikiya Tamaru^{*}, Benjamin Falk^{**} and Alexander Renz^{***}
^{*} TECNISCO, LTD., ^{**} Tesat-Spacecom GmbH & Co. KG., ^{***} HAILTEC GmbH

The rising demand for high-power RF components in space, driven by GaN semiconductor technology, has led to the development of a novel hermetically sealed high-power RF package. This collaborative effort between Tesat-Spacecom GmbH & Co. KG, Tecnisco Ltd., and Hailtec GmbH focuses on integrating silver-diamond (AgD) heat sinks for superior thermal management, achieving conductivity values exceeding 900 W/(m·K).

Key Innovations:

AgD Heat Sink Manufacturing: Traditional waterjet cutting results in rough surfaces unsuitable for RF applications. Advanced laser cutting techniques—particularly quasi-continuous wave multimode fiber lasers—allow precise, rapid processing with surface roughness below Rz 36 µm.

Surface Treatment and Coating: A Physical Vapor Deposition (PVD) process applies a three-layer metal coating (Ti/Ni/Au), ensuring strong adhesion, solderability, and corrosion resistance. Successful solderability and shear tests confirmed high mechanical integrity and bonding strength.

Thermal and RF Testing: An existing 50W X-band package was modified with AgD heat sinks (using adhesive bonding for initial trials). Thermal simulations and measurements showed a significant junction temperature reduction from 178°C (CuW) to 124°C (AgD) in the simulation and 179°C (CuW) to 129°C (AgD) in the measurement. RF performance also improved, with up to 6% gain in Power Added Efficiency (PAE).

LTCC Integration: The LTCC-based hybrid package design uses precise eutectic die attach methods and laser-welded lids to ensure hermeticity and high thermal performance.

Conclusion and Next Steps:

This first phase validated AgD laser processing and its thermal benefits. Future work will focus on hermetically sealed modules and evaluating thermomechanical impacts on RF performance. Two types of packages—mechanical and RF-representative—will be developed, with pressure sensors aiding hermeticity testing.

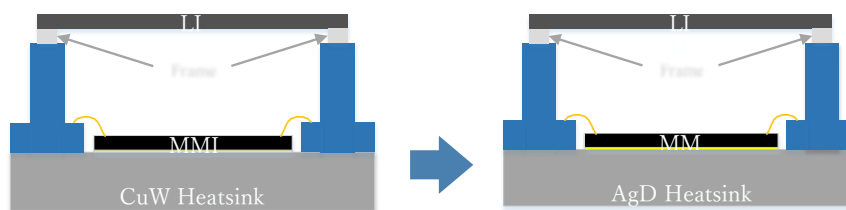


Fig1. CuW and AgD LTCC Package

	Thermal Analysis [°C]		Measurement [°C]	
	CuW-Package	AgD Package	CuW-Package	AgD Package
NTC1	87	70	95	81
NTC2	70	65	77	75
T _{NTC1} -T _{NTC2}	17	5	18	6
Junction Temp.	178	125	179*	129*

Fig2. Results Analysis vs. Measurement (*after calibration)

CNES Components activities : Challenges of testing complex components

Florence Malou and Guillaume Bascoul
Quality & Expertise Department, CNES

Mrs. Florence Malou is Senior components expert. Dr Guillaume Bascoul is Electrical analysis expert. We are working in Quality & Expertise Department in CNES Technical Directorate.

This talk will present CNES activities on EEE component development, test and qualification with a focus on UDSM technologies.

CNES with the French Space ecosystem defined the strategy to access to UDSM (Ultra Deep SubMicron) technologies. The results is the ETOILE project. ETOILE objective is to define chiplet strategy and to develop and validate building blocks in 7nm for next European rad-hard FPGA & ASIC chiplet components in System-In-Package. The development of next FPGA and ASIC on UDSM technology is coordinated between CNES, European Commission and ESA.

In CNES labs, we have invested in new equipment to address UDSM challenges. We want to keep our technical expertise at the state of the art. An overview of our equipment and expertise will be shown.

In parallel, we have a very fruitful collaboration with JAXA on radiation characterization of UDSM technology. Together CNES and JAXA will face the new challenges.

ABSTRACT

Conference Name: MicroElectronic Workshop, MEWS38

Organizer: Japan Aerospace Exploration Agency, JAXA

Meeting Dates: October 23-24, 2025

Title: The NASA Report

Authors: Co-Author 1: Shri Agarwal, NASA-Jet Propulsion Laboratory, California Institute of Technology

Co-Author 2: Peter Majewicz, NASA Goddard Space Flight Center

Co-Author 3: Susana Douglas, NASA Goddard Space Flight Center

Abstract:

This year we celebrate the silver jubilee of NEPAG (NASA Electronic Parts Assurance Group). And JAXA is very much a part of it. It has been 25 years that NASA has worked with domestic and international space agencies; JC-13 (the manufacturers of government products); CE-11 and CE-12 (the users of passive and active devices); DLA (Defense Logistics Agency); the Aerospace Corporation; and others. A lot has been accomplished by working together - sharing parts failure experiences, inserting new technology into military standards, and much more. This presentation will highlight some of those achievements. We'll also talk about the challenges ahead of us. Status of NASA's initiative to address the workforce development in electronic parts engineering (the "School") will be provided. Updates on ILPM (Industry Leading Parts Manufacturers) and PEAL (Parts Evaluation & Assessment Laboratory) will be given as well.

NASA Efforts Towards a Holistic COTS Approach for Space Avionics

Peter Majewicz, Ph.D.

NASA Electronic Parts & Packaging (NEPP) Program

Aerospace electrical hardware systems are required to withstand and reliably operate in harsh environments that include, for example, temperature extremes, intense vibrational stress, drastic temperature cycling and high radiation exposure. The nature of aerospace electronics also demands high initial reliability since, with very few exceptions, there is no chance for servicing and repairs. Common risk mitigation techniques for this type of situation are to use electrical components that are regarded as “high reliability” because of additional controls and requirements applied in their design, manufacturing, and testing. That methodology has been successful for decades, but limited availability of space-grade MIL-SPEC parts and a need for using the most current technologies in system designs have necessitated the incorporation of commercial electronics into space flight hardware.

This presentation presents the methodology championed at NASA to utilize more commercial-off-the-shelf (COTS) electronics. This includes fostering relationships with high-quality manufacturers, who are producing very reliable devices in high volume, using automated production equipment and use statistical process controls to establish “zero defect” workmanship. After verification of these criteria, these companies are designated as “Industry Leading Parts Manufacturers (ILPMs)”. Additional testing may also be needed to ensure the parts meet the project’s Mission, Environment, Application and Lifetime (MEAL), including radiation testing, that is accomplished by the NASS Parts Evaluation and Assessment Laboratory (PEAL). The presentation will conclude with the latest updates of the ILPM and PEAL efforts.

MLCC product lineup for automotive applications and expansion into space products

Hiroya Fujii
Ceramic Capacitor Business Unit
Murata Manufacturing Co.,Ltd.

Murata contributes to the advancement of the electronics society through the creation of innovative technologies and solutions. By establishing an integrated production system from materials to finished products, we lead trends in the electronics industry such as miniaturization, high functionality, and thinner designs. More than 90% of its products are sold overseas, providing technologies, products, and services to customers worldwide across all regions.

Our company handles a wide variety of capacitors, including ceramic, polymer aluminum, single-layer microchip, silicon, and film types. We offer the industry's No.1 extensive lineup of multi-layer ceramic capacitors (MLCCs), meeting diverse needs and providing optimal solutions.

Among these, automotive MLCCs meet high reliability requirements, and space-use MLCCs are developed based on automotive MLCCs. In the automotive market, recent advancements in autonomous driving technology and the expansion of the EV/HEV market have driven the increase and high-performance development of systems installed in vehicles. As safety and high-functionality requirements for systems grow, the performance requirements for MLCCs are also diversifying. This report introduces the latest technological trends in MLCCs centered on automotive applications and reports on their potential expansion into space products.

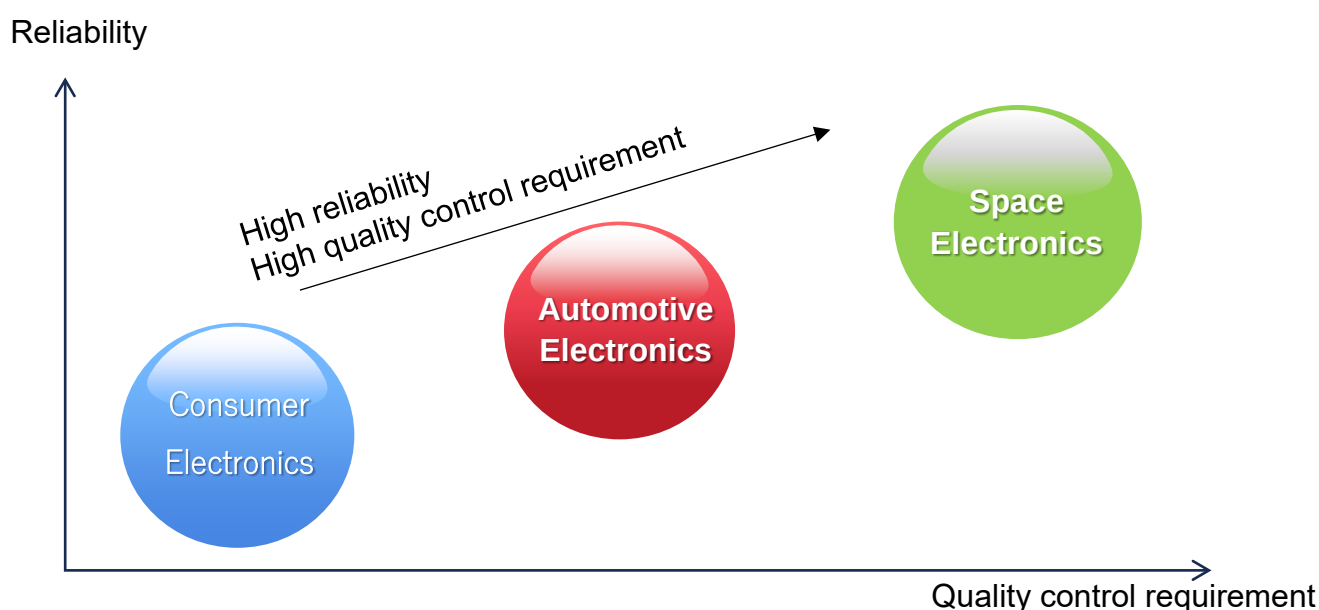


Fig. Reliability and Quality requirement in each market

Sub-Micrometer-Thickness Plastic Film Capacitor Technology

Daisaku Mukaiyama^{*,**}, Chiharu Ito^{*}

^{*} Rubycon Corporation

^{**} Nagoya University

PMLCAP (Polymer Multi-layer Capacitor) technology enables capacitors composed of submicron-thick plastic films. This is a technology in which three processes are continuously performed in a vacuum chamber: i) liquid monomers deposition as dielectric raw materials, ii) polymerization of monomers by electron beams, and iii) formation of internal electrodes by aluminum deposition. The maximum thickness of the base element of PMLCAP is approximately 2mm, meaning that several thousand layers form in one element.

The SMD-type PMLCAP, developed using this technology, has been manufactured for approximately 17 years for the audio market and measurement equipment. In the NASA Mars inspection mission "INSIGHT" in 2018, PMLCAPs were used for the LPF of the seismometer, and it operated completely in the Mars environment.

Rubycon Corporation has been developing high-voltage PMLCAP technology for seven years, basing our mass production experience on SMD products. As a result, we will release high-voltage PMLCAP products (box type) as "HPB-series" this year. The advantages of High-voltage PMLCAP technology to conventional film capacitor technologies will be presented in terms of SOA (refer to Fig.1), thermal conductivity, and capacitance density.

The PMLCAP technology allows the dielectric thickness to be adjusted to the appropriate value even in a voltage range below 500 V, providing many advantages for high-voltage space applications such as satellite ion engines.

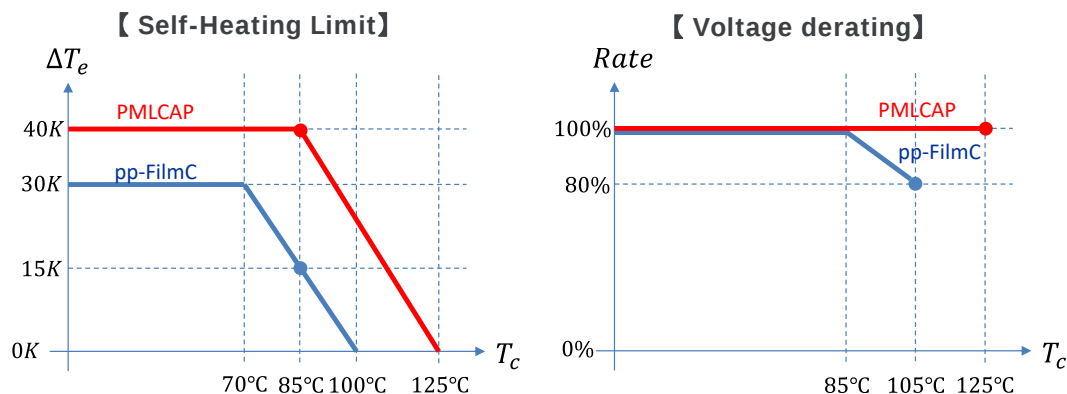


Fig. 1 Comparison of SOA

Initiatives to Promote the Utilization of COTS Parts in Satellites

Yoichiro Kusuda, Yoshiyuki Morihara, Hideto Kurasawa, Hirotaka Yamamoto, Ryuta Suzuki

Advanced Satellite Systems Technology Center (ASTEC)

In recent years, the growing demand for small satellites has accelerated the global adoption of commercial off-the-shelf (COTS) parts. Since 2020, new guidelines have been established by ESA and NASA in Europe and the United States. The active introduction of COTS, balancing risk and performance, is contributing to the strengthening of the space industry's competitiveness. In contrast, despite Japan has the world-class electronics industry, the use of COTS parts in the space sector remains limited, and the benefits of these parts are not being fully leveraged in satellite development.

To address this issue, our initiatives were selected in the first phase of the Space Strategy Fund under the theme "Development and verification of parts and components for establishing satellites supply chain". In 2025, we launched activities focusing on the following three key areas:

- (1) Developing technical guidelines for utilizing COTS parts in satellites
- (2) Developing contractual guidelines for utilizing COTS parts in satellites
- (3) Identification of other issues related to promoting the use of COTS parts

First, regarding (1) Technical guidelines, based on a survey of relevant domestic and international standards, we aim to develop a draft COTS utilization guideline in satellites with high usability that can be tailored to each mission, from small to large satellites, based on risk tailoring. We will collaborate with related companies and proceed with discussions while reflecting a wide range of opinions through exchanges with external companies and organizations.

Regarding (2) Contractual guidelines, we address the contractual hesitation of COTS suppliers due to ambiguous liability scopes and risk aversion. In collaboration with a law firm, we are developing a contract guideline and contract templates based on the perspectives of both suppliers and users.

Finally, regarding (3) identification of other issues, we will hold a meeting with COTS suppliers, users and distributors to gather comments on COTS utilization barriers through discussions. The goal of this process is to identify issues hindering the promotion of COTS utilization except technical and contractual guidelines.

This activity aims to enhance the flexibility and competitiveness of satellite development in Japanese space industry by promoting the utilization of COTS parts in satellites. The outcomes of this activity are expected to be widely used in Japanese space industry, and we plan to report on its progress of this activity at the time of its announcement.

Design Approach for High-Performance COTS FPGAs in Photonic-Electronic Devices for Satellite Systems

Yuzo YAJIMA*, Eisuke HARAGUCHI*, Shigenori TANI*, Sato KOBAYASHI*, Yasuhiro FUKUTA**, and Hiroshi KINODA**

* Mitsubishi Electric Information Technology R&D Center, ** Mitsubishi Electric Kamakura Works

Satellites play an indispensable role in meteorological observation, disaster monitoring, positioning, and communications, where the demand for higher speed and larger bandwidth in data transmission continues to increase as Fig.1. To support such requirements, advanced onboard processing and high-speed transmission technologies, including optoelectronic integration, are becoming essential. Among the candidate devices, commercial off-the-shelf (COTS) field-programmable gate arrays (FPGAs) have attracted attention due to their high functionality, flexibility, and cost-effectiveness.

However, the application of COTS devices to space missions faces significant challenges. In particular, the harsh space environment imposes requirements for long-term reliability that are difficult to satisfy with devices originally designed for terrestrial use. Radiation effects represent one of the most critical concerns, as they can induce functional degradation or even permanent damage in advanced semiconductor devices. Therefore, comprehensive evaluation and the implementation of effective countermeasures are necessary steps before these devices can be confidently applied to satellite systems.

This study addresses these challenges by developing methodologies for the assessment and mitigation of radiation-induced risks in COTS FPGAs. Based on detailed evaluations, design measures were identified to enhance their robustness for space use. The results demonstrate the feasibility of applying COTS FPGAs in geostationary satellite missions while ensuring the required reliability. These findings contribute to establishing practical guidelines for the reliable integration of COTS components into next-generation satellite communication subsystems.

High Speed + High Density + High Reliability

How does Base Material Support Modern Space PCBs

Monique Mayr* and Markus Maringer*

* Panasonic Industrial Devices Materials Europe GmbH

Modern space printed circuit boards (PCBs) are becoming increasingly complex!

High-density interconnect (HDI) printed circuit boards (PCBs) going hand in hand with the demand for fast signal transmission to support high end components.

This abstract demonstrates how advanced base material for PCB can support the increased functionality, and compact designs.

High Speed:

- The presentation compares different resin systems including epoxy, polyphenylene ether (PPE), and polyimide, elaborating on their distinct electrical performance.
- It discusses the selection criteria for glass cloth, reviewing various cloth types and their properties, such as weave structure, and illustrates the influence of glass fabric on electrical performance, notably the fiber-weave effect that impacts signal integrity at high frequencies, is also assessed.
- Furthermore, it examines different copper foil options highlighting roughness comparisons and their implications on electrical performance. Additionally, the skin effect phenomenon and its contribution to transmission loss across various copper foils are clearly explained.

High Density

- The second part of the presentation analyzes the challenges of complex HDI technology and how robust HDI PCB designs can meet the stringent reliability requirements of space applications. This will include examining material selection, particularly glass fabric and copper thickness, which helped address some of the conflicting requirements, such as 2-layer prepreg constructions versus aspect ratio and copper thickness versus prepreg thickness.

High Reliability

The presentation concludes with the confirmation of the statements by utilizing the MEGTRON®7 qualification as an example:

- MEGTRON7 qualified for PCB at European Space Agency (ESA):
The abstract addresses the thermal resistance of PPE-based materials, summarizing their performance and reliability according to testing standards defined by the European Cooperation for Space Standardization (ECSS), ensuring suitability for rigorous and demanding applications.
- And concludes with the Japan Experiment Module “Kibo” as shown in figure 1 in cooperation with Japan Aerospace Exploration Agency (JAXA) where the material was exposed to Space at the International Space Station (ISS).

The extremely harsh environment where microgravity, a powerful vacuum, cosmic radiation, and wide-ranging temperature changes occur simultaneously; conditions that are difficult to replicate on Earth. The experiments were conducted to meet this challenge, aiming to expose electronic materials developed by Panasonic Industry Co., Ltd. to space conditions and assess their performance under adverse conditions.



Fig. 1 Japan Experiment Module Kibo on board the ISS

GREEN SPACE and ZERO DEBRIS – EEE(E) EVALUATIONS

Michael Moesken*, Dr. Frederik Kuechen* and Dennis Michael Joeckel*

* TESAT EEE Parts Agency

On 22 May, the ESA and a dozen European countries signed a new Space Debris Mitigation Policy and Requirements document, which will apply to all future ESA missions, as well as mission extensions. Furthermore, NASA has established a sustainability department and the UN is stepping up its efforts to develop guidelines for the long-term sustainability of outer space activities.

As a consequence, the EEE(E) sector has to apply those rules as well. In this speech, the TESAT Parts Agency will present the current status of its research into how EEE(E) components can be evaluated with regard to these requirements.

Results are derived from experiments simulating atmospheric EEE(E) re-entries and are combined to a life cycle assessment in different impact categories.

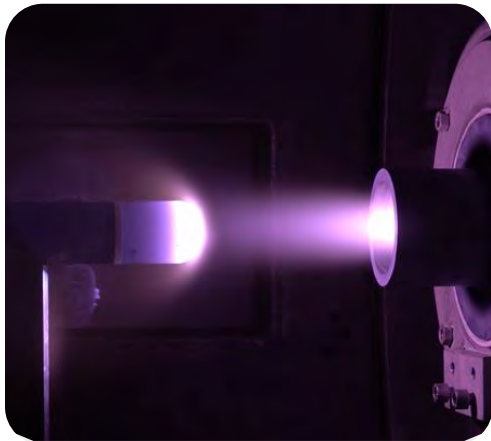


Fig. 1: DUT plasma exposure

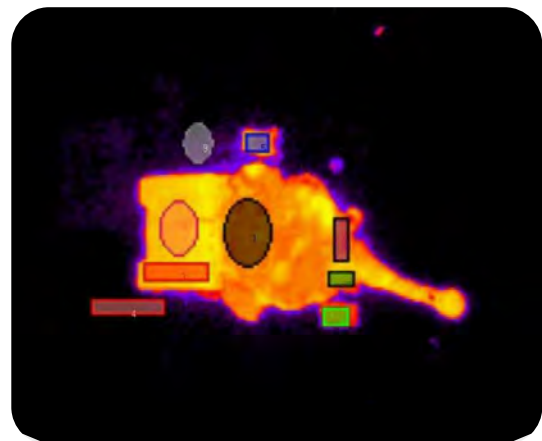


Fig. 2: OES heat map of DUT

Tradeoffs to optimize radiation efforts on COTS components

Jeremy GUILLERMIN*, Leo COIC*, Alexandre ROUSSET*, Christian CHATRY*

* TRAD, Tests & radiations

The consideration of radiation effects on electronic components is often at odds with the budget and time constraints of New Space applications. Even when willing to acknowledge these risks, it is seldom viable in this frame to rely on full Rad-Hard HiRel designs and/or complete qualification of parts according to the usual standards. Tradeoffs are a certainty and may take the form of the adoption of COTS elements in the design along with reduced and tailored test constraints. The characterization of radiation effects is thus less standardized and aims at alleviating the most critical risks while simply mitigating or accepting the rest. This presentation focuses on outlining possible optimization methods that may help navigating these tradeoffs in an efficient manner.

Efforts can be made at different stages, beginning with the reduction of unnecessary margins when defining environment constraints and received TID levels. Mapping the received dose in a simplified equipment 3D geometry as in Fig.1 may lead to significant reductions of the estimated levels compared to a 1-dimensional calculations with an Aluminium shielding assumption. This presentation will discuss ways to optimize these efforts, addressing the benefits and constraints of these intermediate steps.

When relying on COTS parts, characterization responsibilities rely solely on the user. For some missions, this characterization may be tailored as it may not be necessary to go to the same extent than a full standard qualification. Efficient tailoring reduces the amount of needed beam time and test bench complexity to focus only on critical aspects, saving time and money. These approaches and their limitations have to be carefully examined to find an optimized path fulfilling project requirements. Different possibilities, along with alternative test methods and facilities will be illustrated in this talk with a focus on the use of laser facilities as derisking solutions as shown in Fig.2 and Fig.3.

Finally, hybrid solutions for COTS sourcing will be highlighted where high performance industrial parts can be upscaled with an added layer of radiation qualification, reliability and traceability guarantees necessary for space applications as a turnkey solution concerning New Space part procurement. The need for such solutions has been emphasized by the industry at large and is being addressed in the frame of the R2COTS project and the long-term collaboration with the CNES aiming to provide the community with alternatives to Rad-hard and Rad-tolerant devices while considering budget and time constraints inherent to New Space projects. This approach will be a core part of this talk.

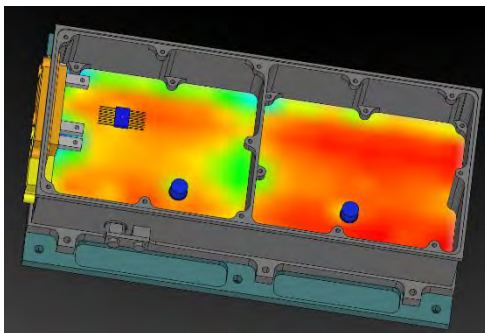


Fig.1: Mapping of received TID in an equipment

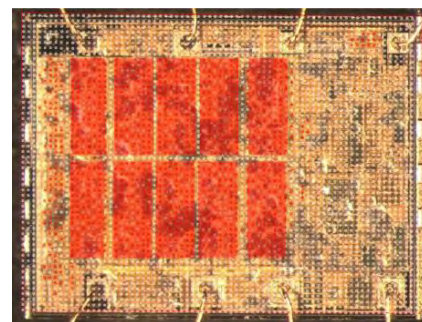


Fig.2: LASER test mapping highlighting SEL sensitive volumes

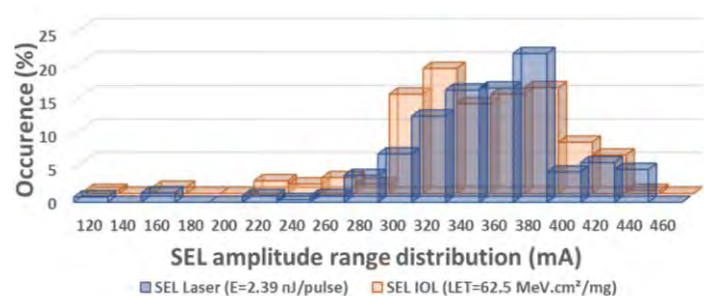
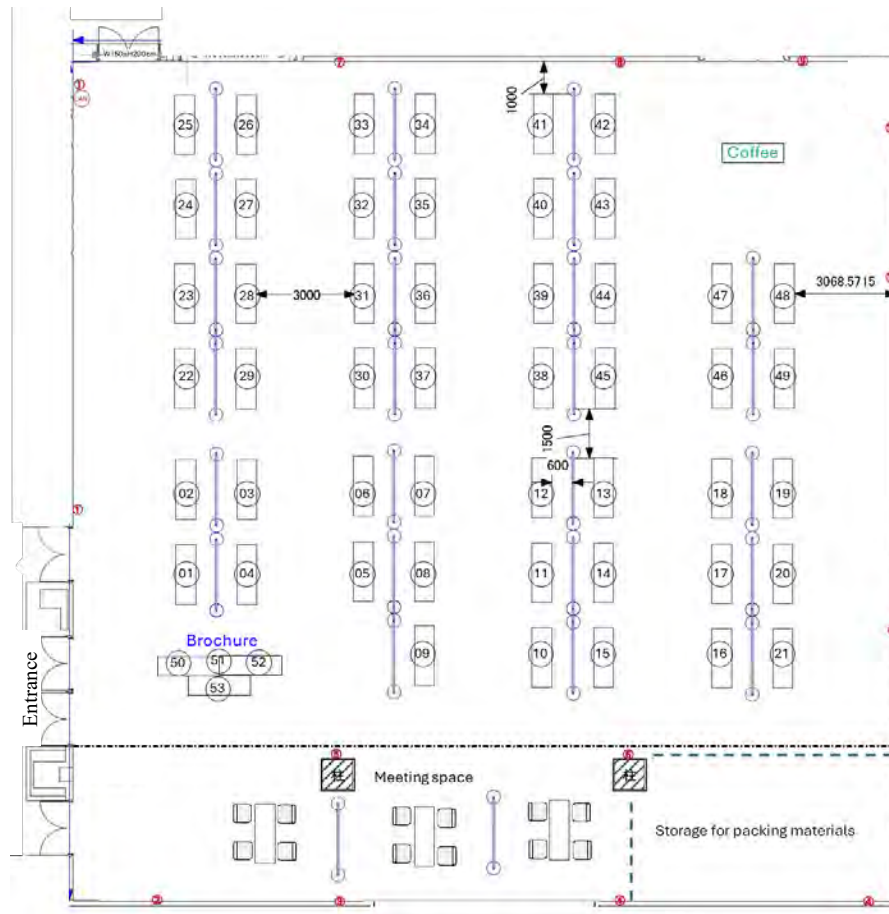


Fig.3: Distribution of LASER and HI SEL amplitudes

Space Components & Parts Exhibition

- ◆ Venue: Multi-Purpose Hall (1F)
- ◆ Open Hour
 - DAY1 October 23 11:00 – 17:30
 - DAY2 October 24 9:15 – 14:30
- ◆ Booth Layout



Booth #	Brand / Company Name	Booth #	Brand / Company Name	Booth #	Brand / Company Name
1	Glenair	18	Marubeni Ele-Next	36	DAIMARU STEEL INDUSTRY
2	AIO Core	19	TATEYAMA	37	Marubun
3	HIREC	20	SHOSHIN	38	CHRONIX
4	JEPICO	21	NTK CERAMIC / Niterra group	39	Mach Corporation
5	JC ELECTRONICS	22	imec	40	Iwase Kogaku
6	RIKEN DENGU SEIZO	23	TECNISCO	41	Microchip Technology
7	Caeleste bv	24	SANADA KOA	42	Rubycon
8	DDC/ Power Device Corporation	25	STMicroelectronics	43	TAKITEK
9	PEI Genesis	26	Hokuriku Electric Industry	44	ASINE
10	Thermo Graphitics	27	SUNTECHNO	45	Panasonic Industry
11	TAMURA	28	SIJTechnology	46	NanoBridge FPGA
12	Kanematsu	29	NASAM Japan	47	Industrial Technology Innovation Center of Ibaraki Prefecture
13	IR Hirel, Micross, Exxelia, ISOBAUD	30	SHINNETSU	48	Littelfuse
14	Samtec Japan LLC	31	[SCS] KIKUCHISEIKI	49	BizLink Special Cables Germany
15	OKI Circuit Technology	32	GLIT	50	*Isogai Mfr.
16	Isabellenuette	33	STAR ENGINEERING	51	*NITTOCORP
17	NAITO DENSEI KOGYO	34	TOBATA SeISaKUSHO	52	*QuickLogic
		35	Shirato Printed Circuit Board	53	*German Aerospace Center (DLR)

