Registration No. 1294

JAXA-QTS-2220
18 March 2025

CRYSTAL OSCILLATORS, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: 8 September 2025

Revision history

Rev.	Date	Description
NC	18 Mar. 2025	Original

Contents

CRYSTAL OSCILLATORS, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the general requirements for space use, high reliability, crystal oscillators (hereinafter referred to as “crystal oscillator”) used for electronic equipment installed on spacecrafts.

1.2 Definition of Terms

The definitions for terms and symbols used herein are provided in paragraph 6.1 and appendixes of this specification, JAXA-QTS-2000, MIL-STD-883, MIL-HDBK-1331, MIL-STD-202 and MIL-PRF-55310.

1.3 Part Number

An example of the part number of crystal oscillator is shown below. The details shall be specified in the detail specification.

Example:

JAXA [(1)]	2220/101	-	1	CB	C	R	100M0000
	Individual Identification (paragraph 1.3.1)		Device type (paragraph 1.3.2)	Package configuration (paragraph 1.3.3)	Lead material and finish (paragraph 1.3.4)	Radiation hardness (paragraph 1.3.5)	Nominal frequency (paragraph 1.3.6)

Note: [(1)] "JAXA" indicates the common part for space use and may be abbreviated to “J.”

1.3.1 Individual Identification

Individual identification shall be individual number specified in the detail specification. Individual identification shall be indicated by a three-digit number. First digit identifies certified manufacturer and shall be provided by Japan Aerospace Exploration Agency (hereinafter referred to as “JAXA”) and last two numbers shall be provided by certified manufacturer. Certified manufacturer shall specify provision rule and list of individual identification in quality assurance program plan.

1.3.2 Device Type

The device type shall be the number assigned to the individual device type in the detail specification and shall be a one-digit number from 1 to 9.

1.3.3 Package Configuration

The package configuration shall be designated by two capital letters. Details shall be specified in appendix F, the detail specification and the design specification.

1.3.4 Lead Material and Finish

The lead material and finish identification shall be designated by a capital letter as follows.

Finish letter (1)	Lead material	Finish
C	Type A, B or C	Gold plating
Z	As specified in detail specification	As specified in detail specification

Note: (1) Finish letter "X" may be used in the detail specifications when all of the lead materials and finishes C or Z are applicable. However, the actual lead material and finish letter shall be marked on the product and its package, and the letter “X” shall not be marked.

1.3.5 Radiation Hardness (Total Dose Hardness)

The radiation hardness (total dose hardness) shall be identified by a single capital letter and indicates the radiation hardness assurance level. The designator shall be used for the inspection lots that have passed the radiation hardness test (total dose test) of the subgroup 2, radiation hardness (total dose), qualification test and quality conformance inspection specified in appendix C of this specification, and shall be used for the inspection lots that have passed the radiation hardness test (total dose test) of lot evaluation test for semiconductor chips.

Letter	Radiation hardness assurance level
R	1000 Gy (Si) {$1x10^5$ rad (Si)}

1.3.6 Nominal Frequency

Nominal frequency shall be specified in detail specification.
Nominal frequency shall be identified by a single capital letter (K, M and G) indicating the frequency range and numbers indicating significant digits.

a) When the frequency is greater than or equal to 1,000Hz and less than one megahertz (MHz), the letter “K” shall be used.
b) When the frequency is greater than or equal to one MHz, the letter “M” shall be used.
c) When the frequency is greater than or equal to one gigahertz (GHz), the letter “G” shall be used.

All digits before and after the letter (K, M, G) shall represent significant digits.

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents

The documents listed below form a part of this specification to the extent specified herein. These documents are the latest issues available at the time of contract award or application.
If a specific issue needs to be used, the issue shall be specified in the detail specification.

a) JAXA-QTS-2000	Common Parts/Materials, Space Use, General Specification for
b) ISO 14644-1:1999	Cleanrooms and Associated Controlled Environments - Part 1: Classification of Air Cleanliness
c) ISO 14644-2:2000	Cleanrooms and Associated Controlled Environments - Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1
d) MIL-STD-38534	Hybrid Microcircuits, General Specification for
e) MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
f) MIL-PRF-55310	Oscillator, Crystal Controlled, General Specification for
g) MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
h) MIL-STD-750	Test Method Standard Test Methods for Semiconductor Devices
i) MIL-STD-883	Test Methods Standard Microelectronics
j) MIL-HDBK-1331	Handbook for Parameters to be Controlled for the Specification of Microcircuits
k) ASTM F1192	Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices
l) JESD57	Test Procedure for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation
m) ESCC5000	Generic Specification for Discrete Semiconductor Components
n) ESCC9000	Integrated Circuits: Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits with Non-Organic Substrate, Hermetically and Non-Hermetically Sealed and Die
o) ECSS-Q-ST-70-60	Qualification and Procurement of Printed Circuit Boards

2.2 Reference Documents

The following documents are the reference documents for this specification.

a)	JAXA-QTS-2010	Integrated Circuits, High Reliability, Space Use, General Specification for
b)	JAXA-QTS-2030	Semiconductor Devices, High Reliability, Space Use, General Specification for
c)	JAXA-QTS-2040	Capacitors, Fixed, High Reliability, Space Use, General Specification for
d)	JAXA-QTS-2050	Resistors, High Reliability, Space Use, General Specification for

e) JAXA-QTS-2140 Printed Wiring Boards, High Reliability, Space Use, General Specification for
f) JAXA-QTS-2070 Crystal Units, Quartz, High Reliability, Space Use, General Specification for
g) JERG-0-035 JAXA Parts Application Handbook (limited to JAXA)
h) JERG-0-039 High Reliability Soldering Requirements
i) JERG-0-043 Standard for Surface Mount Soldering Process
j) JMR-012 Electrical, Electronic, And Electromechanical Parts Program Standard
k) ESCC3503 issue5 Crystal Controlled Oscillators ESCC Generic Specification

2.3 Order of Precedence

In the event of a conflict between requirements specified in applicable specifications, the following order of precedence shall apply.

a) Detail specification
b) This specification
c) JAXA-QTS-2000
d) Applicable documents of this specification (paragraph 2.1) (except for JAXA-QTS-2000)

2.4 Design Specification and Detail Specification

a) Preparation of design specification
When manufacturer acquires certification, the manufacturer shall prepare design specification which specifies qualification coverage (including construction and design limit values) of crystal oscillator in accordance with appendix D, and shall submit the design specification attached to quality assurance program plan to qualification audit acting agency.
b) Preparation of detail specification
Certified manufacturer shall provide detail specification number in accordance with paragraph 2.4.1, prepare and establish detail specification in accordance with appendix E and submit the detail specification to qualification audit acting agency. JAXA will issue the detail specification.

2.4.1 Detail Specification Number

Detail specification number shall be assigned in accordance with paragraph A.2.2.2 of JAXA-QTS-2000. An example is shown below. Individual identification shall be a three-digit number with first digit representing certified manufacturer and remaining two digits representing series number.

Example: JAXA-QTS-2220 / 101 A

- A — Revision letter
- 101 — Individual identification
- JAXA-QTS-2220 — This specification number

2.4.2 Revision letter of Detail Specification

Revision letter in detail specification number shall be assigned in accordance with paragraph A.2.2.2.4 of JAXA-QTS-2000.

2.4.3 Independency of Detail Specification

Detail specification shall be a stand-alone document with a unique number in accordance with paragraph 2.4.1.

2.4.4 Formats of Design Specification and Detail Specification

a) Format of design specification shall be as specified in appendix D.
b) Format of detail specification shall be as specified in appendix E.

3. REQUIREMENTS

3.1 Certification

3.1.1 Qualification Coverage

Qualification shall be valid for crystal oscillators that are designed within the range of designing limit values specified in the design specifications, produced by the manufacturing line that conforms to quality assurance programs. The qualification coverage shall be within the range of that are typified by evaluation elements or samples which have passed the qualification test. Within this coverage, certified manufacturer is allowed to supply qualified products in compliance with the detail specification.

3.1.2 Initial Qualification

To acquire qualification of crystal oscillators in compliance with this specification, a manufacturer shall establish a quality assurance program in accordance with paragraph 3.2.1 of this specification, perform qualification tests specified in paragraph 4.6 of this specification and acquire a certification as specified in paragraph 3.4.1 of JAXA-QTS-2000. The manufacturer shall be listed on the Certified Manufacturers List of JAXA (JAXA QML).

To acquire qualification, the manufacturer shall also prepare a design specification (to be attached to quality assurance program plan) in accordance with appendix D and a detail specification in accordance with appendix E and submit them to qualification audit acting agency.

3.1.3 Retention of Qualification

To continue supplying crystal oscillators in accordance with this specification, certified manufacturer shall apply for QML qualification retention in accordance with paragraph 3.4.2.1 of JAXA-QTS-2000 prior to expiration date of certification period specified in paragraph 3.1.4 of this specification.
If the crystal oscillators were not manufactured during the effective period of qualification and a quality conformance inspection was not performed, certified manufacturer may apply for the retention of qualification without performing quality conformance inspection.

3.1.4 Effective Period of Qualification

Effective period of qualification granted in compliance with this specification shall be three years.

3.1.5 Requalification

In the case of changes affecting design limit values, functions, performance, reliability and quality of crystal oscillators, certified manufacturer shall apply for requalification in accordance with paragraph 3.4.3 of JAXA-QTS-2000.

3.2 Quality Assurance Program

3.2.1 Establishment of a Quality Assurance Program

To acquire a qualification in accordance with this specification, manufacturer shall establish a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall establish a quality assurance program plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to qualification audit acting agency for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.

3.2.2 TRB Formation

To acquire a qualification for products in accordance with this specification, manufacturer shall form and operate the Technical Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.

3.3 Design and Construction

Design and construction of crystal oscillators shall specify materials, processes and design rules as a whole and design limit values specified for at least following items a) to f) in accordance with appendix D shall be specified in the design specification.

Design and construction of each product shall be specified in the detail specification in accordance with appendix E.
Details of design specification and detail specification shall be in accordance with paragraphs 3.3.1 to 3.3.8.

a) Operating temperature
   1) Case temperature
b) Substrate
   1) Material (e.g., Alumina)
c) Pattern formation and metallization
   1) Minimum element spacing (spacing between conductor-to-conductor, conductor-to-resistor, resistor-to-resistor and elements)
   2) Minimum pattern width (conductor and resistor)
   3) Minimum and maximum length of an element (resistor)
   4) Film forming method (thin- or thick- film)
   5) Film material (e.g., NiCr, Ta, Au, Pd-Ag)
   6) Trimming method
d) Mounted elements
   1) Type of elements (e.g., semiconductor, capacitor)
   2) Mounting configuration (e.g., face-up, eutectic bonding and adhesion)
   3) Mounting material (e.g., molybdenum tablet, Au-Si eutectic, solder, nonconductive or conductive adhesive)
   4) Maximum area and weight of mounted elements
   5) Derating of mounted elements
e) Internal lead wires
   1) Material (e.g., gold, aluminum)
   2) Configuration (e.g., wire, ribbon) and dimensions
   3) Bonding method (e.g., thermocompression, ultrasonic, parallel gap welding)
   4) Maximum wire (or ribbon) length (or bonding spacing)
f) Packaging
   1) Packaging material
   2) Package configuration (e.g., 16-pin metal flat, package)
   3) Sealing process (e.g., welding, brazing)
   4) Lead material and finish

3.3.1 Operating Temperature

Operating temperature of crystal oscillators shall be within the case temperature range. Minimum and maximum operating temperatures shall be specified in the design specification and detail specification.

3.3.2 Substrates

Unless otherwise specified in the design specification and the detail specification, thin-film ceramic substrate and thick-film ceramic substrate shall be made of alumina (Al_2O_3) with the minimum purity of 99.5% and 96%, respectively.

3.3.3 Metallization

Unless otherwise specified in the design specification and the detail specification, metallization shall meet the following requirements.

3.3.3.1 Conductors

a) Thin-film conductors

Thin-film conductors on the substrates shall be designed such that, when assumed to be properly built up, the current density shall not exceed the following maximum allowable current density when operated under the worst conditions specified in the design specification and the detail specification.

Conductor material	Maximum allowable current density
Gold	$6 \times 10^5 A/cm^2$
Others (unless otherwise specified in the detail specification)	$2 \times 10^5 A/cm^2$

1) Use a current value equal to the maximum continuous current (at full fan-out for digital devices or at the maximum load for linear devices) or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value at the point(s) of the maximum current density. This current value shall be determined at the maximum recommended rating voltage(s) and with the current assumed to be uniform over the entire conductor cross-sectional area.
2) Use the minimum allowable metallization thickness within controls.
3) Use the minimum actual design metallization width (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.
4) Areas of the barrier metals and nonconductive material shall not be included in the calculation of the metallization cross section.
5) In order to compensate for reduction of the cross section due to thinning, voids or scratches, use the cross section obtained from steps 2) through 4) of this paragraph and multiplied by 0.75, to calculate the maximum current density.

b) Thick-film conductors

Thick-film conductors (such as wiring by metallization and bonding pads) on substrates shall be designed such that, when assumed to be properly built up, the power loss shall not exceed $4W/cm^2$ if the maximum design current is applied.

3.3.3.2 Resistors

Unless otherwise specified in the design specification and the detail specification, the maximum power consumption of resistors shall meet the following requirements.

a) Thin-film resistors
Thin-film resistors on substrates shall be designed such that, when assumed to be properly built up, the maximum power consumption shall not exceed $93W/cm^2$.

b) Thick-film resistors
Thick-film resistors on substrates shall be designed such that, when assumed to be properly built up, the maximum power consumption shall not exceed $7.75W/cm^2$.

3.3.4 Mounted Elements

Mounted elements of crystal oscillator shall be selected to meet the following requirements:

a) Finished terminals
Considering the risk of whisker growth, parts with tin plating (lead containing 3 percent or less, by mass) finished terminals shall not be used in principle. When tin plating (lead containing 3 percent or less, by mass) finished terminals are used, certified manufacturer shall evaluate any risks for whisker growth and obtain a purchaser's approval. The procedures and criteria for risk evaluation shall be approved by TRB.

b) Selection of mounted elements
Mounted elements for crystal oscillator shall be selected in accordance with paragraphs 3.3.4.1 to 3.3.4.4 of this specification.

3.3.4.1 Passive Elements

a) Chip capacitors, chip resistors and chip inductors
Chip capacitors, chip resistors and chip inductors shall be selected in accordance with paragraph A.2.4.1 of this specification and shall be specified in the design specification and the detail specification.

b) Quartz crystal units
Quartz crystal units shall be selected in accordance with paragraph A.2.4.2 of this specification and shall be specified in the design specification and the detail specification.

3.3.4.2 Semiconductors

a) Semiconductor chips
Semiconductor chips shall be selected in accordance with requirements in appendix A and shall be specified in the design specification and the detail specification.

b) Surface mounting semiconductor parts
Surface mounting semiconductor parts shall be selected with reference to the

requirements in appendix A and shall be specified in the design specification and the detail specification.

3.3.4.3 Printed Wiring Boards

Printed wiring boards shall be selected in accordance with paragraph A.2.4.3 and shall be specified in the design specification and the detail specification.

3.3.4.4 Other Mounted Elements

When any other mounted elements are used, the requirements for the elements shall be specified in the design specification and the detail specification.

3.3.5 Organic and Polymeric Materials

When organic and polymeric materials (e.g., coatings, adhesives) are used inside a package of crystal oscillator as assembling or coating materials, they shall not exhibit blister, crack, outgas, softening, outflow or other defects under the test conditions specified in the detail specification.
Organic and polymeric materials shall be specified in the design specification and the detail specification.

3.3.6 Mounting Materials for Substrates, Semiconductor Chips and Passive Elements

Glass shall not be used for mounting substrate, semiconductor chips or passive elements.
Mounting materials for substrate, semiconductor chips or passive elements shall be specified in the design specification and the detail specification.

3.3.7 Internal Lead Wires

Internal lead wires or other conductors which are not in thermal contact with the substrate along the entire length shall be designed such that the maximum rated current (continuous current for direct currents, effective value for alternating currents and peak current divided by $\sqrt{2}$ for pulsed currents) shall not exceed the maximum allowable current calculated by the following formula.

$$I = \frac{1}{128} \times K \times d^{\frac{3}{2}}$$

where, I = Maximum allowable current (A)
d = Wire diameter (mm) (When the cross section is not circular, use the diameter of a circular wire or conductor of the same cross section area)
K = A constant obtained from the length and composition of the wire or conductor as shown in Table 1.

Table 1. "K" value

Material	"K" value for bond-to-bond total conductor length	
	Length ≤ 1.0mm	Length > 1.0mm
Aluminum	22000	15200
Gold	30000	20500
Copper	30000	20500
Silver	15000	10500
All other	9000	6300

3.3.8 Package

Unless otherwise specified in the detail specification, package shall be such that the leads have stress relief when mounted on printed wiring board, such as a flat package. Packages shall be selected in accordance with paragraph A.2.4.4 of this specification.

a) Package configuration
Qualification coverage of package configuration shall be specified in design specification in accordance with appendix D. Package configuration of each product shall be specified in detail specification in accordance with appendix E.

b) Package material
External metal surfaces of the package shall be corrosion resistant. External leads shall meet the requirements of c) below. Nonmetallic materials of the package and coatings materials including markings shall be non-nutrient to fungus and shall not exhibit any blister, crack, outgas, softening, outflow or other defects under the test conditions specified in detail specification. Details shall be specified in the detail specification.

c) Lead material and finish
1) Lead material
Lead material shall be one of the following types unless otherwise specified in detail specification.

1.1) Type A

Iron	53% nominal
Nickel	29±1%
Cobalt	17±1%
Manganese	0.65% max.
Silicon	0.20% max.
Carbon	0.06% max.
Aluminum	0.10% max.
Magnesium	0.10% max.
Zirconium	0.10% max.
Titanium	0.10% max.

(The sum of aluminum, magnesium, zirconium, and titanium contents shall be 0.20% as a maximum.)

1.2) Type B

Nickel	40.00% to 43.00%
Cobalt	0.500% max.
Manganese	0.800% max.
Silicon	0.300% max.
Carbon	0.100% max.
Aluminum	0.100% max.
Chrome	0.250% max.
Phosphorus	0.025% max.
Sulfur	0.025% max.
Iron	Remainder

1.3) Type C (Copper-core, Fe-Ni52 alloy)

Copper (core)	99.96% min.
Nickel	48% to 52%
Carbon	0.02% max.
Manganese	0.2% to 1.0%
Silicon	0.1% to 0.5%
Sulfur	0.025% max.
Phosphorus	0.025% max.
Iron	Other

2) Lead Finish

Unless otherwise specified in the detail specification, lead finish shall be one of the following options from 2.1) to 2.3).

2.1) Solder dip

Solder dip shall be homogeneous with the minimum thickness of 5.08μm at the major flats of solder (Sn60 to Sn63) over a primary finish in accordance with type 2.2) below or nickel plating (with the thickness between 2.54μm and 7.62μm).

2.2) Gold plating

Purity of gold plating shall be a minimum of 99.7% gold (i.e., the sum of impurities and other metals shall be 0.3% as a maximum). Gold plating thickness shall be a minimum of 1.27μm. This finish requires electrolytic nickel or copper base plating with a thickness between 1.27μm and 7.62μm.

2.3) Tin lead plating

Percentage of lead shall be between 3% and 50%. Tin lead plating thickness shall be minimum 7.62μm. Electroless nickel or electrolytic nickel base plating may be used for this finish. Thickness of the base plating shall be between 1.27μm and 8.89μm.

3.4 Marking

3.4.1 Marking Items

At least the following marking items shall be specified in the detail specification.

a) Index point (paragraph 3.4.1.1)
b) Part number (paragraph 1.3)
c) Inspection lot identification code (paragraph 3.4.1.2)
d) Serial number (paragraph 3.4.1.3)
e) Certified manufacturer's identification (paragraph 3.4.1.4)

3.4.1.1 Index Point

Index point indicates the start of lead numbers or mechanical orientation and shall be shown by a stamp, tab, notch or groove, among other means. The index point shall be visible from the top when the product is mounted in a normal manner. Certified manufacturer's identification code shall not be used for this purpose.

3.4.1.2 Inspection Lot Identification Code

An inspection lot identification code shall be assigned to each inspection lot (refer to 2) of (paragraph 4.3.1 l)) and shall be marked.

3.4.1.3 Serial Number

A serial number shall be assigned to each crystal oscillator in inspection lot prior to screening test (refer to paragraph 4.7).

3.4.1.4 Certified manufacturer's Identification

Certified manufacturer's identification shall be the certified manufacturer's name, abbreviation or trademark.

3.4.2 Marking Location and Layout

Unless otherwise specified in the detail specification, part number and inspection lot identification code shall be located on the top surface of packages. Each marking item may be placed in any way as long as it satisfies the marking requirement and does not interfere with other markings.

3.4.3 Marking Option

Certified manufacturer shall complete markings by the start of external visual inspection of screening test.

3.4.4 Exemption of Marking Items

When the surface area of crystal oscillator is not sufficient to place all the marking items specified in paragraph 3.4.1, marking items may be exempted in the following order or priority. Details shall be specified in detail specification.

a) "2220-" of part number
b) Package configuration and lead material/finish designator of part number. (In this case, both designators shall be exempted).
c) Certified manufacturer's identification

3.5 Radiation Hardness

3.5.1 Total Dose Radiation Hardness

Total dose radiation hardness of crystal oscillator shall be specified in the detail specification. When total dose radiation hardness is required for semiconductor chip, the semiconductor chip shall be selected in accordance with appendix A and shall be specified in the detail specification.

3.5.2 Single Event Characteristics

As for single event characteristics of crystal oscillator, characteristics selected from the following items relating to product shall be specified in the detail specification. When single event characteristics are required for semiconductor chip, the semiconductor chip shall be selected in accordance with appendix A and shall be specified in the detail specification.

a) SEU
b) SEL
c) Others

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

Certified manufacturer shall be responsible for implementing quality assurance program specified in paragraph 3.2 of this specification and operating TRB.

4.2 Incoming Parts and Materials Control

Incoming parts and materials shall be subject to an appropriate incoming inspection and controlled to ensure that each part and material is traceable to incoming inspection lot. Certified manufacturer shall establish and implement procedures to store and retrieve received parts and materials and to remove limited-life parts and materials.

4.2.1 Incoming Inspection

Test items, test methods and pass/fail criteria of incoming inspection for each part and material used for crystal oscillator shall be specified in detail specification.

4.2.2 Record of Incoming Parts and Materials Control

The records of incoming parts and materials shall be categorized into incoming inspection records and storage, retrieval and disposal records. These records shall include the following items as a minimum.

a) Incoming inspection records
   1) Part and Material name
   2) Inspection items
   3) Lot size
   4) Lot identification code
   5) Document number and established date of inspection instructions
   6) Pass or fail of each lot and quantity of failed parts and materials
   7) Date of inspection and name or identification code of the inspector

b) Storage, retrieval and disposal records
   1) Part and Material name
   2) Storage conditions
   3) Lot identification code
   4) Storage date and quantity of storage materials
   5) Retrieval date and quantity, lot identification code of finished or semi-finished products for which the part and material are used.
   6) Disposal date and quantity

4.3 Manufacturing Process Control

Certified manufacturer shall establish and maintain procedures of manufacturing processes, control parameters and methods.

4.3.1 Control of Manufacturing Process Works

Certified manufacturer shall define and control each manufacturing process works including the items listed below as a minimum. Rework shall be performed in accordance with paragraph 4.3.2 of this specification. Certified manufacturer shall also establish and implement a storage method for finished or semi-finished products between each manufacturing process work.

a) Formation of substrate lots
   1) Formation procedure of substrate lots
   2) Assignment of substrate lot identification codes

b) Metallization process
   1) Manufacturing process of thin-film substrates
      1.1) Mask control
      1.2) Metallization material

1.3) Forming method
1.4) Forming conditions
1.5) Method and frequency of chamber cleaning

2) Electrolytic plating process
2.1) Metallization material
2.2) Plating solution and control of plating bath
2.3) Plating conditions

3) Manufacturing process of thick-film substrates
3.1) Screen control
3.2) Paste material
3.3) Forming method
3.4) Forming conditions
3.5) Furnace control

c) Pattern formation process

1) Masking method
When photolithography is used, the following items on handling of photo resist shall be specified.
1.1) Preparation method
1.2) Evaluation methods for specific gravity, viscosity, solid residues and pinholes
1.3) Storage conditions
1.4) Coating conditions
1.5) Baking conditions
1.6) Exposure conditions
1.7) Developing conditions

2) Etching technique
When wet etching is used, the following items shall be specified.
2.1) Preparation method
2.2) Composition, grade, temperature, etc., of etching solution
2.3) Frequency of etching solution change
2.4) Etching conditions
2.5) Washing and drying

3) Inspection process
3.1) Method of visual inspection and pass/fail criteria

d) Trimming of resistors

1) Trimming method and facility type
2) Trimming conditions
3) Inspection for resistance and film stability
4) Method of visual inspection and pass/fail criteria

e) Scribing and substrate separation

1) Scribing method and conditions
2) Dicing method and conditions
3) Method of visual inspection and pass/fail criteria

f) Formation of production lots

1) Formation of production lots(1)
2) Assignment of production lot identification code

Note (1) Production lot should be prepared such that inspection sub-lots are able to be easily prepared (paragraph 4.3.1 k)).

g) Substrate and parts mounting process
   1) Mounting material and package material in the mounting area
   2) Mounting structure
   3) Mounting conditions
   4) Visual inspection method for mounting
   5) Control method of adhesive strength

h) Interconnection bonding
   1) Material
   2) Lead type
   3) Bonding method
   4) Bonding conditions
   5) Visual inspection for bonding
   6) Nondestructive bond pull test method
   7) Control method of bond strength

i) Pre-seal visual inspection
   1) Procedure and pass/fail criteria of visual inspection

j) Sealing process
   1) Package and sealing materials
   2) Sealing method
   3) Stabilization bake prior to sealing
   4) Sealing conditions

k) Formation of inspection sub-lots
   1) Formation of inspection sub-lots(1)
   2) Assignment of inspection sub-lot identification code

   Note (1) Inspection sub-lots shall meet the following requirements.
      i. An inspection sub-lot shall consist of crystal oscillators of a single part number and single device type with identical package type and lead finish.
      ii. All products of an inspection sub-lot shall be manufactured using a single substrate lot.
      iii. Each inspection sub-lot shall consist of semiconductor chips made from a single wafer lot.
      iv. Each inspection sub-lot shall be manufactured using the same machines in each production process.
      v. The entire assembly process from assembly start (such as substrate attachment and MOSFET mounting) to package sealing shall be completed within the same 12-week period.
      vi. Each inspection lot shall consist of 500 crystal oscillators as a maximum.

l) Formation of inspection lots
   1) Formation of inspection lots(1)
   2) Assignment of inspection lot identification code

   Note (1) Inspection lots shall satisfy the following requirements.
      i. An inspection lot shall consist of crystal oscillators of a part number with identical identification number, selected from a maximum of five

inspection sub-lots. The case configuration, package types, and lead finish shall be identical.

ii. The entire assembly process from assembly start (such as substrate attachment and MOSFET mounting) to package sealing shall be completed within the same 16-week period.

4.3.2 Rework Control

When rework specified below is performed, the rework results shall be documented in records as specified in paragraph 4.3.5. Reworked products shall be clearly identifiable from other products. After final sealing, rework shall be limited to re-cleaning, correction of defective marking and lead straightening (e.g., reshaping of leads such as correction of lead tip shape which does not degrade for seal of the product.). In addition, opening operations shall not be performed after final sealing.

4.3.2.1 Re-Bonding and Element Replacement

Unless otherwise specified in detail specification, re-bonding and replacement of attached elements should be allowed under the following conditions.

a) Re-bonding shall not be performed on bonding pads that have been damaged to the extent that the top layer of metallization in the area being bonded is lifted or peeled away or the underlying metallization or substrate is exposed.
b) The total number of re-bonding shall be limited to a maximum of 10% of the total number of bonds in the crystal oscillator. Re-bonding of wires to substrate pads or package posts for replacing elements shall not be limited to this maximum number.
c) The total number of internal connection bonding or element replacements shall be limited to three times. Element replacements shall only be for the elements which are mounted by adhesive or solder.

4.3.2.2 Rework of Conductors on Substrate

Rework shall be allowed to repair scratches, breaking, discontinuation of conductors on substrates using bonding wires or ribbons which have current capacity of 3.5 times the maximum operating load current (refer to paragraph 3.3.3). Repair shall be limited to one area per substrate area of 323mm^2.

4.3.2.3 Replacement of Substrates and Packages

Unless otherwise specified in the detail specification, substrates and packages of crystal oscillator shall not be replaced.

4.3.3 Environmental Control

Temperature, relative humidity and dust counts shall be controlled for manufacturing processes (such as substrate manufacturing processes and assembly operations) which are significantly affected by the environments. The particle counting shall be performed in accordance with ISO 14644-1 and ISO 14644-2.

4.3.4 Water Purity Control

Purity of water shall be controlled with respect to the minimum specific resistively, maximum total solids, maximum organic impurity, maximum bacteria quantity and maximum chlorine contents at room temperature.

4.3.5 Records of Manufacturing Processes

Records of manufacturing processes shall be categorized as either work records for the manufacturing processes or control records for the environmental conditions. Records of manufacturing processes shall include at least the following items.

a) Work records for the manufacturing process
   1) Name of work
   2) Lot identification code of materials and products (including semi-finished products)
   3) Document number and issue date of the document that ordered the work to be performed.
   4) Quantity of incoming and outgoing products (including semi-finished products) for each work and disposition
   5) Date of work and name or identification code of operator
   6) Identification of facility used
b) Control records such as for environmental conditions
   1) Document number and issue date of the document directing the control method
   2) Date of measurement and name or identification code of operator

4.4 Classification of Inspections and Tests

Inspections and tests shall include screening test in addition to three categories specified in paragraph 4.3 of JAXA-QTS-2000.

a) In-process inspection
b) Qualification test
c) Screening test
d) Quality conformance inspection

4.5 In-Process Inspection

Certified manufacturer shall perform in-process inspections specified below during the manufacturing process of crystal oscillator to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize

properties which cannot be measured on the finished products. Test items, test methods, pass/fail criteria and sample quantity shall be shown in manufacturing process flowchart and shall be specified in detail specification.

a) Internal visual inspection of semi-finished products (100% non-destructive or sampled inspection)
   Final visual inspection prior to sealing shall be conducted to all sample.
b) Physical or chemical inspection of semi-finished products (sampled destructive or non-destructive inspection)
   1) Bond pull strength test
   2) Die shear strength test
c) Characterization of semi-finished products (100% non-destructive or sampled inspection)

4.5.1 In-Process Inspection Records

Certified manufacturer shall specify in-process inspection records in quality assurance program as specified in paragraph 3.2.1.

4.6 Qualification Test

Qualification test shall be performed on the inspection lot which passed the screening test in accordance with Appendix C using evaluation elements or samples which were produced using the same design, construction, materials and manufacturing line as those to be qualified.

4.6.1 Evaluation Elements or Samples

Evaluation elements or samples shall be produced using design, construction, materials and manufacturing line specified in quality assurance program and shall have sufficient functions and performance to evaluate construction and design limits of the products. Therefore evaluation elements or samples shall be identical in critical constructions to the crystal oscillators to be qualified. When all critical construction and design limits are not able to be represented by a single evaluation element or sample, multiple evaluation elements or samples may be used.

4.7 Screening Test

To supply crystal oscillators in compliance with this specification, certified manufacturer shall perform screening test in accordance with appendix B. Prior to the screening test, production lots shall be re-grouped into inspection lots.
Screening test may be initiated after final sealing process has been completed. Products shall be serialized within each inspection lot prior to screening test to provide traceability between each measurement and product.

4.8 Quality Conformance Inspection

Quality conformance inspection shall be performed in accordance with appendix C on inspection lots which passed screening tests. Sampled products shall be disposed of in accordance with paragraph C.3.6. When products to be shipped and qualification test sample are within same inspection lot, qualification test results may be used as quality conformance inspection results for the first article.

4.9 Long-Term Storage

4.9.1 Disposition of Products Stored for a Long Term at Certified manufacturer's Site

When products have been stored at certified manufacturer's site for 24 months or longer after the quality conformance inspection, certified manufacturer may conduct the electrical characteristics test (Table C-1) as a retest prior to delivery to the purchaser, and deliver the products that pass the test. If products fail in any subgroup inspection, 100% inspection shall be performed for items in that subgroup. The crystal oscillators which are judged acceptable can be delivered as products. Failed products shall be removed from the lot and shall be declared defective. Paragraph 4.3.4.1 of JAXA-QTS-2000 shall also be applicable.

4.9.2 Storage by Purchasers

Conditions and period of storage by purchasers shall be specified in the detail specification, if necessary.

4.10 Change of Tests and Inspections

Any change to the in-process inspection, screening test and quality conformance inspection as specified in this specification shall be in accordance with paragraphs 4.3.5 and A.4.4.2 of JAXA-QTS-2000.

5. PREPARATION FOR DELIVERY

5.1 Packaging

Certified manufacturer shall package the products individually prior to delivery. The package shall have a construction to hold the products securely and protect the products from mechanical shocks. The package shall protect the products from moisture and be free of sharp edges or burrs on the external surfaces. It is desirable that the package allows visual inspection without opening the package. The packaging materials shall not break, peel off, crumble, loosen, accumulate static electricity or corrode. Tapes or adhesives shall not be used to secure the products. Proper protection shall be provided to ESD sensitive products. Individual shipping packages shall be placed in a shipping container to protect the products from possible damages during shipment.

5.2 Marking on Package

Each shipping package shall have the markings specified in b) through e) of paragraph 3.4.1. However, when the markings on the products are clearly visible from outside of the shipping package, those markings on the package may be exempted. For packages with ESD protection, a marking “ESD sensitive” shall be added. All markings shall be waterproof.
The marking requirements for each shipping package shall also apply to the shipping container. However, the quantity, applicable specification number, year and month of packaging and inspection results shall be marked additionally except for the marking specified in paragraph 3.4.1d).

6. NOTES

6.1 Definition of Terms

The following definition of terms is used in this specification.

a) Chip:
Circuit elements used in crystal oscillator without a package and leads.

b) Substrate:
The base element on which the element is formed or mounted.

c) Device type:
Refers to a specific configuration of crystal oscillator. For example, products made by different certified manufacturers using different mechanical arrangements and materials are referred to as “the same device type” if those devices are functionally and physically interchangeable at the semiconductor chip or substrate level.

d) Package type:
Refers to a specific package configuration. Packages with the same package configuration, materials (including mounting materials such as bonding wires and semiconductor chips), components and assembly processes are of the same package type.

e) Final seal:
Manufacturing process that do not allow processing related to the internals without disassembling the crystal oscillator.

f) Delta limit:
The maximum value at which a specified parameter is allowed to vary from its pre-test measured value as a criteria for acceptance in a specified test.
Note: If represented in percentage, delta limit shall indicate a percentage with respect to a pre-test value.

g) Wafer lot:
A group of wafers processed together in each process.

h) Substrate lot:
A group of substrates formed together in each process.

i) Production lot:
A group of crystal oscillators manufactured (or being manufactured) using the same manufacturing technology, materials, controls, design and production line. When

multiple device types are manufactured in the same processes up to the final seal process, the production lot may include those device types.

j) Inspection lot:
A group of crystal oscillators with the same package type and lead finish. An inspection lot may include multiple device types. Inspection lots are usually divided into inspection sub-lots.

k) Inspection sub-lot:
A group of single device type crystal oscillators with the same package type and lead finish. Inspection sub-lots are processed together in all manufacturing processes.

l) Thin-film:
Film formed on substrate surface by vacuum deposition, ion sputtering or gas phase reaction, among other methods.

m) Thick-film:
Film formed by baking, among other methods, after ink paste is coated, sprayed or printed on substrate surface.

n) Ferrite core:
Ferrite core is produced by forming and baking materials that are made of several layers of various metal oxide films. The primary ingredient of those metal oxide films is iron oxide. The chemical composition of ferrite core is $MOFe_2O_3$ (M indicates metals).

o) Single event characteristics:
Specific characteristics that cause malfunction or permanent damage in circuit elements by the incidence of a single high-energy particle.

p) Design specification:
Document providing qualification coverage for design of crystal oscillator.

q) Procurement specification:
Document prepared by certified manufacturer and applicable to purchase of materials for crystal oscillator manufacturing (refer to paragraph 4.2). This document is included in product assurance documents.

r) First article:
Product delivered at first time for detail specification.

s) Crystal oscillator XO:
A crystal oscillator without temperature control or temperature compensation. The frequency-temperature characteristics of the oscillator depend on the quartz crystal units.

6.2 Notes for Certified manufacturer

6.2.1 Preparation and Registration of Application Data Sheet

Certified manufacturer shall prepare application data sheet in accordance with appendix G of JAXA-QTS-2000 and register it with JAXA.

In the case of products based on purchaser's individual requirements (refer to paragraph 6.3.1), certified manufacturer may be exempt from preparing the application data sheet, when certified manufacturer takes counsel with the purchaser about necessity of the

application data sheet and the exemption is approved by certified manufacturer's TRB (refer to paragraph 3.2.2).

6.3 Notes for Purchaser

6.3.1 Items to be specified at Procurement

To purchase crystal oscillators in accordance with this specification, following items shall be specified:

a) Part number
b) This specification number
c) Detail specification number
d) Test data to be submitted for the delivery and whether the source inspection is performed or not.
e) Others

Requirements other than those defined in this specification may be specified for specific applications as item e). However, if the requirements conflict with the existing requirements in this specification, the purchaser shall not request certified manufacturer to indicate that the crystal oscillator complies with this specification.

6.3.2 Review of Application Data Sheet

Application data sheets contain detailed data at the time of qualification of crystal oscillators and contain more detailed information than the detailed specifications, which is required for selection and design tasks. Purchaser shall review the application data sheet prior to procurement.

APPENDIX A

REQUIREMENTS FOR SEMICONDUCTOR CHIPS, SUBASSEMBLY AND SEMI-ASSEMBLY CRYSTAL OSCILLATORS

APPENDIX A

REQUIREMENTS FOR SEMICONDUCTOR CHIPS, SUBASSEMBLY AND SEMI-ASSEMBLY CRYSTAL OSCILLATORS

A.1. Scope

This appendix establishes the requirements for semiconductor chips, subassembly and semi-assembly crystal oscillators. From semiconductor chips acceptance to crystal oscillator assembly is shown in Figure A-1.

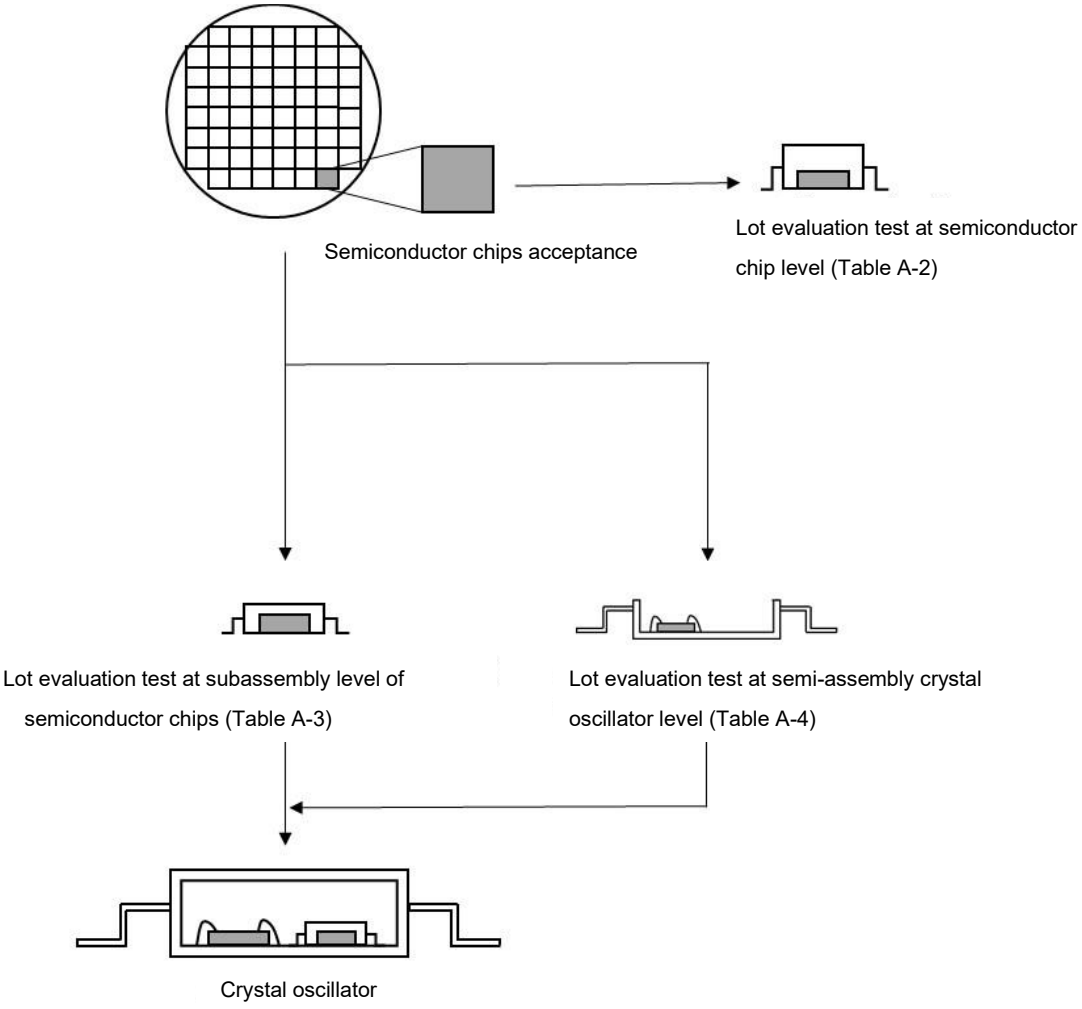


Figure A-1: From semiconductor chips acceptance to crystal oscillator assembly

A.2. Requirements

Certified manufacturer shall verify quality of semiconductor chips used for crystal oscillators through lot evaluation tests for each lot before the semiconductor chips are used. Specification shall be prepared to establish electrical parameters, test methods, etc.

A.2.1 Design and Construction of Semiconductor Chips

Certified manufacturer shall verify that design and construction of semiconductor chips meet the following requirements.

A.2.1.1 Current Density of Metallization

Unless otherwise specified, the metallization shall be designed so that, when assumed to be properly built up, the current density through it, under the worst case operating conditions, does not exceed the maximum allowable current densities shown in Table A-1.

Table A-1. Maximum Allowable Current Density of Metallization

Metallization material	Maximum allowable current density (A/cm^2)
Aluminum (99.99% purity or doped)	2×10^5
High melting point metal (Mo, W, Ti-W, Ti-N)	5×10^5
Gold	6×10^5
All other (unless otherwise specified)	2×10^5

Maximum current densities shall be calculated using current and cross section areas which are determined as follows.

a) Use a current value equal to the maximum continuous current (at full fan-out for digital or at the maximum load for linear) or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value. Currents shall be calculated on the assumption that currents flow uniformly through the conductor's cross section driven by the maximum recommended rating voltage.
b) Use the minimum allowable metallization thickness within the range specified in the manufacturing specification and controls.
c) Use the minimum actual design metallization widths, not mask widths, including appropriate allowance for narrowing or undercutting experienced in metal etching.
d) Areas of the barrier metals and nonconductive materials shall not be included in the calculation of the metallization cross section.
e) Use the cross section obtained from steps b) through d) multiplied by 0.75 for calculation of the maximum current density to compensate for reduction of the metallization cross section due to thinning, bond or scratches.

A.2.1.2 Glassivation

Unless otherwise specified in the detail specification, all semiconductor chips shall be glassivated. The glassivation thickness shall be a minimum of 0.40μm for SiO_2 or a

minimum of 0.20μm for Si_3N_4 unless otherwise specified in the detail specification. The glassivation shall cover all conductor surfaces except for bonding pads.

A.2.1.3 Semiconductor Chip Thickness

Unless otherwise specified in detail specification, the minimum semiconductor chip thickness shall be 0.15mm.

A.2.1.4 Plating for Back Surface of Semiconductor Chip

When the back surface of semiconductor chip is plated with gold, the thickness shall be between 0.10μm and 1.00μm. Electrolytic plating shall not be used for gold plating on the back surface of semiconductor chips.

A.2.1.5 Radiation Hardness Assurance

Semiconductor chips used for radiation hardened crystal oscillators shall pass the lot evaluation tests of subgroup 4 in Tables A-2 to A-4.
When total dose test has been performed on the same lot of semiconductor chips used, the test data may be used. Single event test results shall be evaluated on a semiconductor chip basis in accordance with appendix A. When test data on semiconductor chips of the same design is available, the test data may be used.

A.2.2 Lot Evaluation Test of Semiconductor Chips

Certified manufacturer shall verify for each wafer lot that the semiconductor chips pass the lot evaluation tests specified in Tables A-2 to A-4. Unless otherwise specified in the detail specification, Table A-2 shall be applied for lot evaluation test. Table A-3 or Table A-4, which performs some tests as in-process tests of crystal oscillators, may be applied when semiconductor chips are mounted such that they can be characterized as separate chips. In this case, tests specified in Table A-3 shall be performed for subassembly parts. Tests specified in Table A-4 shall be performed for semi-assembly products of crystal oscillators. Paragraph A.2.3 may apply to MIL, ESA and JAXA qualified semiconductor chips.
Certified manufacturer may modify or optimize the content of this evaluation test by clarifying the basis on which the quality assurance requirements are met in accordance with paragraph 4.3.5 of JAXA-QTS-2000.

A.2.2.1 Samples and Sampling Methods

a) Samples for the lot evaluation test shall be as follows.
Samples shall be randomly selected from semiconductor chips produced from the single wafer lot.
b) Samples for the subgroups 2c) and 2d) shall be prepared using the same materials and techniques of semiconductor mounting and wire bonding as those used in the crystal oscillator.

c) Unless otherwise specified in detail specification, samples for the subgroups 3, 4a) and 5 of Table A-2, subgroups 3, 4a) and 5 of Table A-3 and subgroups 4a) and 5 of Table A-4 shall be packaged and sealed in compliance with paragraph 3.3.8 (except for the requirement specified in paragraph 3.3.8 c)).

A.2.2.2 Failure and Retest

If lot evaluation test failed because of an equipment failure or an operator error, the cause and problem shall be documented in detail and the failed chips may be replaced with chips made from the same wafer. The replaced chips shall pass all tests performed previously with the failed chips. The remaining tests shall then be performed.

A.2.2.3 Lot Evaluation Test Records

Records of lot evaluation tests shall contain a minimum of the following items and shall be managed in accordance with quality assurance program requirements specified in paragraph 3.2.1.

a) Test items
b) Document number and issue date of test methods
c) Quantity of passed and failed chips
d) Date of test and name or identification code of the operator
e) Records accompanying the tests (e.g., temperature charts)
f) Quantitative data including electrical parameter tests

A.2.3 Lot Evaluation Test for MIL, ESA and JAXA Qualified Semiconductor Chips

When certified manufacturer procures the semiconductor chips corresponding to a) or b) specified below in accordance with paragraph C.3.3, appendix C of MIL-PRF-38534, ESCC 5000 or ESCC 9000 qualified products c) and JAXA qualified products d) or e), subgroups 2b) Inspection for external dimensions (semiconductor chips), d) Die shear strength test, 4a) Radiation hardness test (1) and 5a) Electrostatic discharge sensitivity test (1) of Table A-2 shall be performed as lot evaluation test.
The test shall be performed as specified in paragraphs A.2.2.1, A.2.2.2 and A.2.2.3.
When total dose test has been performed on the same lot of semiconductor chips used, the test data may be used. Single event test results shall be evaluated on a chip-by-chip basis in accordance with appendix A. When test data on the same lot of semiconductor chips of the same design are available, they may be used.

a) JANKC chips qualified by MIL-PRF-19500 (listed on QML-19500) or Class V chips qualified by MIL-PRF-38535 (listed on QML-38535).
b) Chips other than JANKC products qualified by MIL-PRF-19500 (listed on QML-19500) and class V chips qualified by MIL-PRF-38535 (listed on QML-38535),

which are semiconductor chips that have been evaluated and passed in accordance with TABLE C-II for Class K, appendix C of MIL-PRF-38534.

c) ESCC 5000 or ESCC 9000 qualified Level 1 chip
d) JAXA-QTS-2010 qualified chip
e) JAXA-QTS-2030 qualified chip

Note: (1) The radiation hardness test and/or electrostatic discharge sensitivity test may be exempted when the semiconductor chips listed on QML-19500 or QML-38535, ESCC 5000 or ESCC 9000 qualified chips and JAXA-QTS-2010 or JAXA-QTS-2030 qualified chips meet the requirements for crystal oscillator.

A.2.3.1 Notice of Procurement

The following items shall be specified in procurement specification for purchase of semiconductor chips.

a) Designation of radiation hardness test and electrostatic discharge sensitivity test (if required by the application of crystal oscillator).
b) At least the following data as a record:
    1) Certificate of compliance
    2) Test results indicating the conformance to a) to e) of paragraph A.2.3, and/or results of lot evaluation (figures and/or measurements)

A.2.4 Selection and Procurement of Parts such as Passive Elements

A.2.4.1 Capacitor Chips, Resistor Chips and Inductor Chips

Capacitor chips, resistor chips and inductor chips to be used shall be selected in principle from the following:

a) JAXA qualified parts
b) MIL failure rate levels S, R, D and C
c) GSFC S311
d) ESCC Levels B and C

When a part passes lot evaluation test required for MIL-PRF-55310 Level S parts in accordance with paragraph B.3.3.3 of MIL-PRF-55310, the part may be used.

When the tests to be performed in this evaluation test are under the same conditions as the tests performed on the crystal oscillator, the tests in this evaluation test may be exempted. Certified manufacturer may modify or optimize the content of this evaluation test by clarifying the basis on which the quality assurance requirements are met in accordance with paragraph 4.3.5 of JAXA-QTS-2000.

A.2.4.2 Quartz crystal units

Quartz crystal units to be used shall be selected in principle from the following:

a) JAXA qualified parts
b) MIL failure rate levels S and R
c) GSFC S311
d) ESCC Levels B and C

When a part passes lot evaluation test required for MIL-PRF-55310 Level S parts in accordance with paragraph B.3.3.3 of MIL-PRF-55310, the part may be used.

When the tests to be performed in this evaluation test are under the same conditions as the tests performed on the crystal oscillator, the tests in this evaluation test may be exempted. Certified manufacturer may modify or optimize the content of this evaluation test by clarifying the basis on which the quality assurance requirements are met in accordance with paragraph 4.3.5 of JAXA-QTS-2000.

A.2.4.3 Printed Wiring Boards

Printed wiring boards to be used shall be selected in principle from the following:

a) JAXA qualified parts
b) MIL qualified printed wiring boards
c) Printed wiring boards qualified by ESA in accordance with ECSS-Q-ST-70-60.

When a part passes lot evaluation test in accordance with paragraph B.3.3.5 of MIL-PRF-55310, the part may be used.

When the tests to be performed in this evaluation test are under the same conditions as the tests performed on the crystal oscillator, the tests in this evaluation test may be exempted. Certified manufacturer may modify or optimize the content of this evaluation test by clarifying the basis on which the quality assurance requirements are met in accordance with paragraph 4.3.5 of JAXA-QTS-2000.

A.2.4.4 Packages

Certified manufacturer may use the package, which passes lot evaluation test required for MIL-PRF-55310 Level S parts in accordance with paragraph B.3.3.8 of MIL-PRF-55310.

When the tests to be performed in this evaluation test are under the same conditions as the tests performed on the crystal oscillator, the tests in this evaluation test may be exempted. Certified manufacturer may modify or optimize the content of this evaluation test by clarifying the basis on which the quality assurance requirements are met in accordance with paragraph 4.3.5 of JAXA-QTS-2000.

Evaluation methods for packages to be used shall be specified in quality assurance program plan.

Table A-2. Lot Evaluation Test for Semiconductor Chips

Sub-group	Test item	Test method/conditions [1]	Sample size (accept no.)
1	a) DC parameters	a) As specified in the procurement specification.	100%
	b) Visual inspection	b) 2010 [2] 2072 [3] 2073 [3]	100%
2	a) SEM inspection	a) As specified in the procurement specification.	As specified in the procurement specification.
	b) Inspection for external dimensions (semiconductor chip)	b) As specified in the procurement specification.	3 (0)
	c) Bond strength	c) 2011	3 (0) [4]
	1) Thermocompression	1) Condition C or D	
	2) Ultrasonic	2) Condition C or D	
	3) Flip-chip	3) Condition F	
	4) Beam lead	4) Condition H	
	5) Thermosonic	5) Condition C or D	
	6) Resistance to welding	6) Condition C or D	
	d) Die shear strength	d) 2019	3 (0)
3	a) Stabilization bake	a) 1008/Condition C	10 (0)
	b) Temperature cycling	b) 1010/Condition C	
	c) Electrical parameter test	c) As specified in the procurement specification.	
	d) High temperature reverse bias life test [5]	d) As specified in the procurement specification (72 hrs. at 150ºC).	
	e) Electrical parameter test [5]	e) As specified in the procurement specification.	
	f) Steady-state operating life test	f) As specified in the procurement specification (min. 240 hrs. at 125ºC).	
	g) Electrical parameter test	g) As specified in the procurement specification.	
4 [5]	a) Total dose test	a) 1019, and as specified in the procurement specification.	5 (0)
	b) Single event test (except for power, discrete semiconductor)	b) As specified in ASTM F 1192, JESD 57, 1080 [3] or the procurement specification.	b) As specified in the procurement specification.
	c) SEB test (power, discrete semiconductor)	c) 1080 [3]	c) As specified in the procurement specification.
	d) SEGR test (power, discrete semiconductor)	d) 1080 [3]	d) As specified in the procurement specification.
5 [5] [6]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0) [7]

Notes:

[1] Four-digit number refers to the test method number used in MIL-STD-883.

[2] Condition A shall be applied.

(3) The number refers to the test method number used in MIL-STD-750.
(4) 15 samples of wire or bonding shall be tested for each chip. When sample size is less than 15, all samples shall be tested.
(5) The tests shall be performed when specified in procurement specification.
(6) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other crystal oscillators is already evaluated, these tests are not needed (not considered as first procurement lot).
(7) Tests with the same pin combination shall be performed on each sample.

Table A-3. Lot Evaluation Test for Semiconductor Chips at Subassembly level

Sub-group	Test item	Test method/conditions [1]	Sample size (accept no.)
1	a) DC parameters b) Visual inspection	a) As specified in the procurement specification. b) 2010 [2] 2072 [3] 2073 [3]	100% 100%
2	a) SEM inspection b) Inspection for external dimensions (semiconductor chip) c) Bond strength 1) Thermocompression 2) Ultrasonic 3) Flip-chip 4) Beam lead 5) Thermosonic 6) Resistance to welding d) Die shear strength	a) As specified in the procurement specification. b) As specified in the procurement specification. c) 2011 1) Condition C or D 2) Condition C or D 3) Condition F 4) Condition H 5) Condition C or D 6) Condition C or D d) 2019	a) As specified in the procurement specification. 3 (0) 3 (0) [4] 3 (0)
3 [5][6]	a) Stabilization bake [7] b) Temperature cycling c) Sealing test d) Particle Impact Noise Detection Test e) Radiograph inspection f) Interim electrical parameter test (Ta=25 ºC) g) Burn-in h) Final electrical parameter test (Ta=25 ºC) i) External visual inspection	a) 1008/Condition C (24 hours at 150ºC) b) 1010/Condition C (10 minutes at -65ºC, 10 minutes at +150ºC) c) 1014 [8] d) 2020/Condition A e) 2012 only for Y-axis f) As specified in the detail specification [9] g) As specified in 1015 and the detail specification (240 hours at minimum 125ºC). h) As specified in the detail specification [9]. i) 2009	100%
4 [10]	a) Total dose test b) Single event test (expect for power, discrete semiconductor) c) SEB test (power, discrete semiconductor) d) SEGR test (power, discrete semiconductor)	a) 1019, and as specified in the procurement specification. b) As specified in ASTM F 1192, JESD 57, 1080 [2] or the procurement specification. c) 1080 [3] d) 1080 [3]	a) 5 (0) b) As specified in the procurement specification. c) As specified in the detail specification. d) As specified in the detail specification.
5 [10] [11]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0) [12]

Notes:

(1) Four-digit number refers to the test method number used in MIL-STD-883.

(2) Condition A shall be applied.

(3) The number refers to the test method number used in MIL-STD-750.

(4) 15 samples of wire or bonding shall be tested for each chip. When sample size is less than 15, all samples shall be tested.

(5) Unless otherwise allowed, the test items shall be performed in this order.

(6) Semiconductor chips shall be sealed and package shall be mounted by certified manufacturer.

(7) This test may be performed before sealing.

(8) Only the gross leak test shall be performed. Test condition C1 shall apply except for the vacuum/pressurization cycles.

(9) When specified in detail specification, changes of electrical parameter measurements between pre- and post-burn-in test shall be calculated. When the changes exceed the specified delta limits, the product shall be rejected. For subassembly parts, the PDA (percent defective allowable) of the burn-in test shall be 5% for all failures (same failure mode) (or one subassembly, whichever is greater) and 3% for functional failures (or one subassembly, whichever is greater). The lots that failed to meet these PDA requirements shall be disposed in accordance with paragraph B.3.2.

(10) The tests shall be performed when specified in the procurement specification.

(11) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other crystal oscillators is already evaluated, these tests are not needed (not considered as first procurement lot).

(12) Tests with the same pin combination shall be performed on each sample.

Table A-4. Lot Evaluation Test for Semiconductor Chips at Semi- Assembly Crystal Oscillators Level

Sub-group	Test item	Test method/conditions [1]	Sample size (accept no.)
1	a) DC parameters b) Visual inspection	a) As specified in the procurement specification. b) 2010 [2] 2072 [3] 2073 [3]	100% 100%
2	a) SEM inspection b) Inspection for external dimensions (semiconductor chip) c) Bond strength 1) Thermocompression 2) Ultrasonic 3) Flip-chip 4) Beam lead 5) Thermosonic 6) Resistance to welding d) Die shear strength	a) As specified in the procurement specification. b) As specified in the procurement specification. c) 2011 1) Condition C or D 2) Condition C or D 3) Condition F 4) Condition H 5) Condition C or D 6) Condition C or D d) 2019	As specified in the procurement specification. 3 (0) 3 (0) [4] 3 (0)
3 [5][6][7]	a) Internal visual inspection b) Interim electrical parameter test (Ta=25 ºC) c) Burn-in test d) Final electrical parameter test (Ta=25 ºC) e) Internal visual inspection	b) Table C-1 Subgroup 1 [8] c) As specified in 1015 and the detail specification. 240 hours at minimum 125ºC d) Table C-1 Subgroup 1 [8]	100%
4 [9]	a) Total dose test b) Single event test (expect for power, discrete semiconductor) c) SEB test (power, discrete semiconductor) d) SEGR test (power, discrete semiconductor)	a) 1019, and as specified in the procurement specification. b) As specified in ASTM F 1192, JESD 57, 1080 [2] or the procurement specification. c) 1080 [3] d) 1080 [3]	a) 5 (0) b) As specified in the procurement specification. c) As specified in the detail specification. d) As specified in the detail specification.
5 [9] [10]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0) [11]

Notes:

[1] Four-digit number refers to the test method number used in MIL-STD-883.

[2] Condition A shall be applied.

[3] The number refers to the test method number used in MIL-STD-750.

(4) 15 samples of wire or bonding shall be tested for each chip. When sample size is less than 15, all samples shall be tested.
(5) Unless otherwise allowed, the test items shall be performed in this order.
(6) Since test sample is unsealed, burn-in test shall be performed in inert gas atmosphere.
(7) Semiconductor chips shall be mounted on the substrates by certified manufacturer.
(8) When specified in detail specification, changes of electrical parameter measurements between pre- and post-burn-in test shall be calculated. When the changes exceed the specified delta limits, the product shall be rejected. For semi-assembly of crystal oscillators, the PDA (percent defective allowable) of the burn-in test shall be 5% for all failures (same failure mode) (or one semi-assembly of crystal oscillator, whichever is greater) and 3% for functional failures (or one semi-assembly of crystal oscillator, whichever is greater). The lots that failed to meet these PDA requirements shall be disposed in accordance with paragraph B.3.2.
(9) The tests shall be performed when specified in the procurement specification.
(10) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other crystal oscillators is already evaluated, these tests are not needed (not considered as first purchase lot).
(11) Tests with the same pin combination shall be performed on each sample.

APPENDIX B

PROCEDURE FOR SCREENING

APPENDIX B

PROCEDURE FOR SCREENING

B.1. Scope

This appendix establishes screening test procedure.

B.2. General Test Conditions

Screening test shall be performed under the general test conditions specified herein.

B.2.1 Environmental Conditions

Unless otherwise specified in the detail specification, all tests shall be performed at ambient temperatures between 20 and 30°C, relative humidity between 20% and 90% and atmospheric pressure between 86.7kPa and 106.7kPa. Whenever the specified parameters shall be closely controlled to obtain reproducible results, the test shall be performed using appropriate control center values and tolerance parameters as established in detail specification or quality assurance program.

B.2.1.1 Performance of Constant Temperature Chamber

Performance of constant temperature chamber used such as stabilization bake and burn-in tests shall meet the following requirements.

a) Temperature distribution in the operating temperature range
Temperature distribution in the operating temperature range shall be 6°C or 6% of the set temperature, whichever is greater.

b) Temperature variation in the operating temperature range
Temperature variation in the operating temperature range shall be ±2°C or ±4% of the set temperature, whichever is greater.

B.2.2 Orientation

Crystal oscillator orientation for tests that require application of external mechanical forces shall be as shown in Figure B-1.

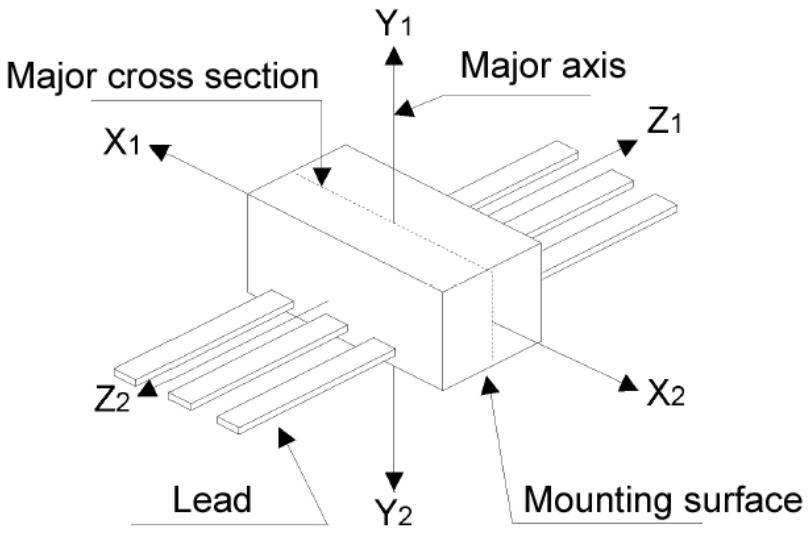


Figure B-1. Orientation

Remark: Y_1 is a force to lift semiconductor chip off the substrate or the wires off the semiconductor chip.

B.2.3 Test Frequency

Unless otherwise specified in the detail specification, electrical tests shall be performed at the lowest and highest frequencies of the specified range when the frequency range is specified in electrical tests.

B.2.4 Accuracy

Unless otherwise specified in the detail specification, specified tolerances shall be for true values under specified test conditions. Certified manufacturer shall re-establish appropriate tolerances in quality assurance program (or the detail specification) based on the accuracy (for test conditions and measurements) of their test apparatus.

B.3. Procedure for Screening Test

All crystal oscillators in inspection lot shall be subject to screening test. Unless otherwise specified in the detail specification, screening test shall be performed in accordance with Table B-1 under the conditions specified in paragraph B.2. When additional test items not specified in Table B-1 are required to effectively perform screening a specific crystal oscillator, the test items shall be specified in the detail specification. After completion of seal in screening test, lead forming that may adversely degrade the effectiveness (hermeticity) of the seal shall not be performed except for minor modifications such as correction of lead tips.

B.3.1 Disposition of Failed Products

If a product failed any of screening test, it shall be properly identified as a defective product and disposed. A product that failed the electrical tests and is to be used in subgroups of qualification test or quality conformance inspection, in which electrically defective products can be used, shall be properly identified and returned to the inspection lot for exposure to the same thermal environments as those applicable to good samples.

B.3.2 Burn-in Screen Failures and Reselection

Inspection lots that failed to meet the specified PDA (percent defective allowable) for the burn-in tests shall be disposed in accordance with paragraph B.3.1. The inspection lot may be re-selected only once, provided that the following conditions are met:

a) Percent defective does not exceed twice the specified PDA (for all failures).
b) Failure analysis is performed and failure causes are identified.
c) Identified failure causes and re-selecting are reviewed and approved by TRB, qualification audit acting agency and purchaser.

The PDA of reselection shall be 3% for all failures (or for one failure, whichever is greater) and 2% for functional failures (or for one failure, whichever is greater).

B.3.3 Failures Due to Test Apparatus Failure or Operator Error

If a product failed the burn-in test due to test apparatus failure or operator error, which resulted in a lot failure, certified manufacturer shall record the failure with detailed description of reasons and conduct a failure analysis. When TRB determine from the results that the remaining product has not been damaged or degraded, certified manufacturer may continue screening test.

B.3.4 Records of Screening Tests

Screening records shall include a minimum of the following items and shall be controlled in accordance with quality assurance program specified in paragraph 3.2.1 of this specification.

a) Test item
   1) Inspection lot identification code
   2) Document number and issue date of test instructions
   3) Quantity and disposition of passed and failed products
   4) Test date and operator’s name or identification code
   5) Measurements of electrical parameters before and after burn-in test or reverse bias burn-in when specified in the detail specification. (This data shall be traced to each product by serial number.)

Table B-1. Screening Test

Order	Test item (3)	Test method/condition (1) (2)
1	Stabilization bake (4)	1008/C (24 hours at 150ºC)
2	Temperature cycling	1010, 10cycles (9)
3	Constant acceleration or Mechanical shock	2001/B (5), Y_1 direction only 2002/B, Y_1 direction only
4	Visual inspection	(6)
5	Particle Impact Noise Detection test	2020/A
6	Radiography	2012 Flat packages: Y direction only
7	Interim electrical parameters (subgroup 1, electrical characteristics, Table C-1, pre burn-in)	In accordance with the detail specification (7)
8	Burn-in test	1015, in accordance with the detail specification.
9	Interim electrical parameters (subgroup 1,electrical characteristics, Table C-1, post burn-in)	In accordance with the detail specification (7)
10	Frequency ageing	More than or equal to 30 days at 70ºC (10)
11	Seal	1014
12	Final electrical parameter test 25ºC (subgroup 1, electrical characteristics, Table C-1) Maximum and minimum operating temperature (subgroups 2 and 3, electrical characteristics, Table C-1)	In accordance with the detail specification (8).
13	External visual	2009

Notes:

(1) Four-digit number refers to the test method number specified in MIL-STD-883.

(2) Three-digit number refers to the test method number used in MIL-STD-202.

(3) Unless otherwise allowed, the test items shall be performed in this order.

(4) The test may be performed immediately before sealing.

(5) Use condition A when the internal sealing of the package exceeds 50.8mm.

(6) The crystal oscillators shall be inspected for damages such as any loss of leads, damage to the package and separation of lids.

(7) When specified in detail specification, the variation value of electrical parameter measurements between pre- and post-burn-in test shall be calculated for crystal oscillator. If a variation value exceeds the specified delta limits, the crystal oscillator shall be rejected. The PDA of the burn-in test of crystal oscillator shall be 5% on all failures (one failure is allowed) and 3% on functional failures (one failure is allowed). The lots that fail to pass these requirements shall be disposed of in accordance with paragraph B.3.2.

(8) Subgroups, in which electrical parameters of the crystal oscillators are not included, may be exempted.

(9) The test temperature (upper and lower limits) shall be the maximum and minimum storage temperature.

(10) The test method shall be in accordance with paragraph 4.8.35 of MIL-PRF-55310. The variation value of the frequency in the frequency ageing test shall be calculated. If a

variation value exceeds the specified delta limits, the crystal oscillator shall be rejected. The PDA of crystal oscillator shall be 5% on all failures (one failure is allowed).

APPENDIX C

PROCEDURES FOR QUALIFICATON TEST AND QUALITY CONFORMANCE INSPECTION

APPENDIX C

PROCEDURES FOR QUALIFICATION TEST AND QUALITY CONFORMANCE INSPECTION

C.1. Scope

This appendix establishes the procedures for qualification test and quality conformance inspection.

C.2. General Test and Inspection Conditions

Qualification test and quality conformance inspection shall be performed under the following conditions.

C.2.1 Environmental Conditions

Unless otherwise specified in the detail specification, all tests and inspections shall be performed at ambient temperatures between 20°C and 30°C, relative humidity between 20% and 90% and atmospheric pressure between 86.7kPa and 106.7kPa. Whenever the parameters specified herein shall be closely controlled in order to obtain reproducible results, the test and the inspection shall be performed using appropriate control center values and tolerance parameters established in the quality assurance program.

C.2.1.1 Performance of Constant Temperature Chamber

Performance of constant temperature chamber used for tests such as steady-state life test shall meet the following requirements.

a) Temperature distribution in the operating temperature range
Temperature distribution in the operating temperature range shall be 6°C or 6% of the set temperature, whichever is greater.

b) Temperature variation in operating temperature range
Temperature variation in the operating temperature range shall be ±2°C or ±4% of the set temperature, whichever is greater.

C.2.2 Orientation

Crystal oscillator orientation for tests that require application of external mechanical forces shall be as shown in Figure C-1.

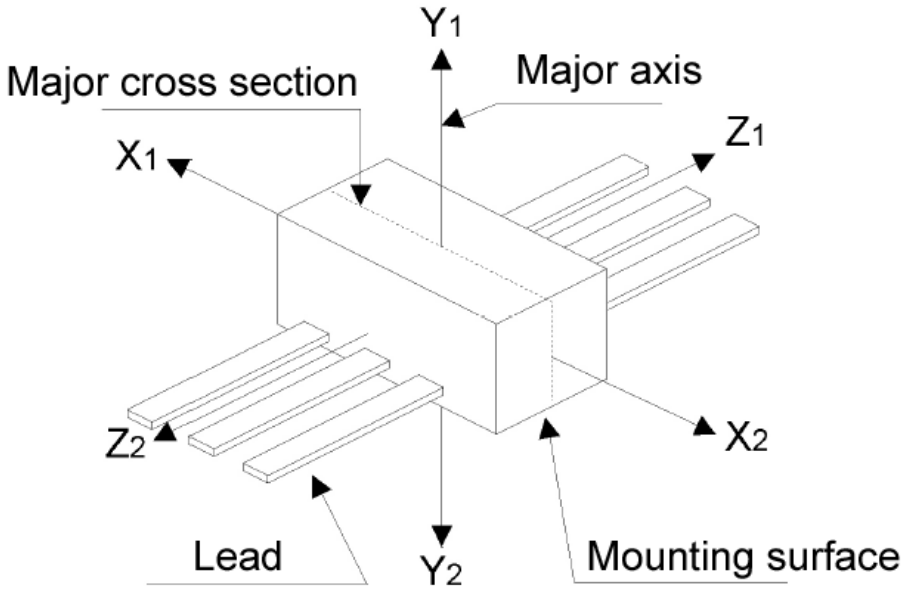


Figure C-1. Orientation

Remark: Y_1 is a force to lift semiconductor chip off substrate or the wires off semiconductor chip.

C.2.3 Test Frequency

Unless otherwise specified in the detail specification, electrical tests shall be performed at the lowest and highest frequencies of the specified range when frequency range is specified for electrical tests.

C.2.4 Accuracy

Unless otherwise specified in the detail specification, specified tolerances shall be for true values under specified test conditions. Certified manufacturer shall re-establish appropriate tolerances in quality assurance program (or the detail specification) based on the accuracy (for test conditions and measurements) of their test apparatus.

C.3. Qualification Test and Quality Conformance Inspection

Qualification test and quality conformance inspection shall be performed under the conditions of paragraph C.2 and in accordance with the procedures specified below.

a) Qualification Test

Qualification test shall be performed using evaluation elements or samples manufactured by design, construction, materials and manufacturing line for qualification (refer to paragraph 4.6.1) under the conditions of paragraph C.2 and in accordance with paragraphs C.3.1, C.3.2 and C3.3.

b) Quality Conformance Inspection

In addition to the procedures specified in paragraphs C.3.1, C.3.2 and C.3.3 under the conditions of paragraph C.3.2, quality conformance inspection shall be performed in accordance with the following.

Quality conformance inspection shall be performed once every year after qualification (or retention of qualification). However, as a result of the TRB review, when TRB determines that both of the following conditions are met, quality conformance inspection may be performed once every two year.

1) Certified manufacturer shall have a manufacturing experience that confirms the stability of the process for at least three years. When manufacturing experience of a product whose design, process, etc. are basically the same exists, this may be added to the manufacturing experience.
2) Critical defects have not occurred after product delivery for the past three years.

C.3.1 Sampling Methods of Qualification Test and Quality Conformance Inspection

Qualification test and quality conformance inspection shall be as sampling tests or inspections using samples taken from an inspection lot.

If samples are damaged due to test apparatus failure or operator error, spare crystal oscillators may be tested or inspected with any subgroups of samples as a substitute (refer to paragraph C.3.5.2). Order of using these spare crystal oscillators shall be specified in advance.

C.3.2 Qualification Test and Quality Conformance Inspection Procedures

Qualification test and quality conformance inspection shall be performed in accordance with Table C-2 for products of an inspection lot manufactured in accordance with quality assurance program for crystal oscillator and which have passed screening test.

Samples for qualification test and quality conformance inspection shall consist of samples from inspection lots that have passed testes specified in Table C-1 (electrical characteristic tests).

Unless otherwise specified in the detail specification, subgroup 2 and subsequent subgroups of qualification test may be performed in any order. Individual tests within a subgroup shall be performed in the order shown in Tables C-2. Samples subjected to the non-destructive test may be subjected to other subgroups.

C.3.2.1 Sample Allocation for Qualification Test and Quality Conformance Inspection

When an inspection lot consists of multiple inspection sublots, the number of samples taken from each inspection sublot shall be equal (or as equal as possible) for each subgroup.

When one inspection sub-lot passes one of the subgroups, the other inspection sub-lots may be considered to have passed that subgroup.

C.3.2.1.1 Radiation Hardness Test

Radiation hardness test shall be performed for each inspection sublot. However, when an inspection lot consists of semiconductor chips in a single wafer lot, if one inspection sublot passes the radiation hardness test, the other inspection sublots may be considered to have passed the radiation hardness test.

C.3.3 Exemption of Qualification Test and Quality Conformance Inspection

When one of the following conditions is satisfied, the test may be exempted by utilizing test data.

a) Exemption of radiation hardness test by utilization of data

1) Total dose test

Unless otherwise specified in the detail specification, when a crystal oscillator of the same design and structure and performance using the same wafer lot of semiconductor chips as the semiconductor chips used has passed the total dose test, that test data may be used as the data for the lot considered (when the wafer lots of some semiconductor chips built in are different, the different wafer lot chips shall be tested individually).

When total dose tests are performed on a chip-by-chip basis, existing data may be utilized if the wafer lot is the same.

2) Single event test

Single event tests shall be evaluated on a semiconductor chip basis in accordance with appendix A. When data from tests performed on semiconductor chips of the same design is available, it may be used. Details shall be specified in the detail specification.

C.3.4 Electrical Characteristics Test

Electrical characteristics tests shall be performed in accordance with Table C-1, at the time of manufacturing of all products (after screening specified in appendix B) and in the subgroups specified in qualification test and quality conformance inspection (Table C-2). Details shall be specified in the detail specification.

C.3.5 Determination of Pass or Fail

When a lot passed all test and inspection items, the lot shall be considered to pass the qualification test or quality conformance inspection. When any lot has failed during any subgroup tests of qualification test, certified manufacturer shall dispose of the crystal oscillators in the inspection lot in accordance with paragraph C.3.6, cancel the tests, and follow the procedure specified in paragraph 3.4.1.6 of JAXA-QTS-2000. When any lot has failed during any subgroups of quality conformance inspection, certified manufacturer shall dispose of the crystal oscillators in the inspection lot in accordance with paragraph C.3.6.

C.3.5.1 Re-inspection

When any lot has failed during any subgroups of quality conformance inspection, the samples reselected from the failed inspection lot may be used for re-inspection. This re-inspection may be done only once and shall be as follows.

a) Failed samples shall be subjected to a failure analysis. A re-inspection may be performed when the TRB has determined that the failure meets the following conditions:
   1) Random failures which are not related to basic design or processes of crystal oscillators.
   2) Failures due to defects that can be effectively removed by inspecting the entire lot.

C.3.5.2 Failure Due to Test Equipment Failure or Operator Error

If a sample failed due to test apparatus failure or operator error, which resulted in lot rejection in qualification test, quality conformance inspection and electrical characteristics test, a crystal oscillator from the same inspection lot shall be used as a substitute sample. To use a substitute sample, certified manufacturer shall perform a failure analysis and the TRB shall determine that the failure was caused due to test apparatus failure or operator error. The substitute crystal oscillator shall pass all tests that were performed with the failed samples prior to subsequent tests and inspections.

C.3.6 Disposition of Sample

Samples shall be properly identified as defective and disposed of, when used in the destructive tests (refer to paragraph C.3.6.1), have failed any test, inspection, or are in rejected lots.
The samples subjected to qualification test or quality conformance inspection shall not be delivered.

C.3.6.1 Destructive Test

Unless otherwise specified in the detail specification, the following tests shall be categorized as destructive tests.

a) Solderability
b) Thermal shock
c) Lead integrity
d) Moisture resistance
e) Electrostatic discharge sensitivity test
f) Radiation hardness test (total dose test)
g) Radiation hardness test (single event test)
h) All tests and inspections that require disassembling crystal oscillator

All other tests and inspections other than the ones defined as non-destructive (refer to paragraph C.3.6.2) shall initially be treated as destructive. However, when

sufficient data are obtained to indicate that those tests are non-destructive, they may be considered as a non-destructive test. A test is considered to be non-destructive if repeated five times using the same samples and all samples pass every run of the test without any indication of cumulative degradation or failure.

C.3.6.2 Non-Destructive Test

Unless otherwise specified in the detail specification, the following tests shall be categorized as non-destructive tests.

a) Electrical parameter test
b) Steady-state operating life test
c) Constant acceleration
d) External dimensions
e) Seal
f) Visual inspection
g) Particle impact noise detection (PIND) test
h) Radiography
i) Mechanical shock
j) Thermal cycling

C.3.7 Radiation Hardness Test

A minimum of the following items shall be specified in the detail specifications for a radiation hardness test.

C.3.7.1 Total Dose Test

a) Radiation hardness assurance level
The radiation hardness assurance level specified in paragraph 1.3.5 shall be specified.
b) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the irradiation shall be specified.
c) Conditions during irradiation to end-point electrical parameter measurements after irradiation
Considering annealing effect, the time from irradiation to post-irradiation measurements shall be specified.
d) Bias circuit
The bias circuit for the radiation hardness test shall be specified.

C.3.7.2 Single Event Effects Test

a) Type of single event phenomena and threshold value
Type of single event phenomena and threshold value shall be specified.
b) Sample

Samples (products or evaluation elements) for single event test shall be specified to associate with types of single event phenomena.

c) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the single event test shall be specified.

d) Bias circuit
The bias circuit for single event effects test shall be specified.

C.3.8 Records of Qualification Test, Quality Conformance Inspection and Electrical Characteristics Test

Qualification test, quality conformance inspection and electrical characteristics test records shall include a minimum of the following items and shall be managed in accordance with quality assurance program specified in paragraph 3.2.1.

a) Test or inspection items
b) Inspection lot identification code
c) Document number and issue date of test instructions
d) Quantity and disposition action of passed and failed products
e) Test or inspection date(s) and operator's name or identification code
f) Records associated with the tests and inspections including temperature and relative humidity charts, and shock pulse waveforms

Qualification test records shall also include the following items.

g) Measurement data of electrical characteristics tests for the specified sample
h) Measurement data of electrical parameters (at pre- and post-test) required at the end of the steady-state operating life test
i) Measurement data of external dimensions
j) Applied force at failure and failure category in bond strength testing
k) Applied force at failure and failure category in die shear testing
l) Measurement data of electrical parameters (at pre- and post-test) required at the end of the radiation hardness test
m) Measurement data of electrical parameters (at pre- and post-test) required at the end of the electrostatic discharge sensitivity test

Records for inspection lots of a device type initially subjected to quality conformance inspection shall also include the following items.

n) Measurement data of electrical characteristics tests for the specified sample
o) Measurement data of electrical parameters (at pre- and post-test) required at the end of the steady-state operating life test

Data g) to o) shall be identified by individual crystal oscillator serial numbers.

Table C-1. Electrical Characteristics Test (1) (2) (3)

Subgroup	Test conditions and limits	Sample size (accept number)
Subgroup 1 (Tc = +25 ºC)	As specified in the detail specification.	All (0)
Subgroup 2 (Tc = Maximum operating temperature) (4)		All (0)
Subgroup 3 (Tc = Minimum operating temperature) (5)		All (0)

Notes:

(1) Electrical parameters, measuring conditions and limits values shall be specified in the detail specification.

(2) Provided that when all the electrical parameters specified in the subgroups of this table are measured at the final electrical parameter tests of the screening tests specified in appendix B, the measurement data of the final electrical parameter test of crystal oscillators which have passed the screening test may also be used as measurement data supplied for the electrical characteristics test.

(3) The same sample may be used for all subgroups.

(4) Measurements at the maximum operating temperature shall be performed after the temperatures of all internal elements (the junction temperature for semiconductor chips) are in thermal equilibrium and the package temperature has reached at least 80% of the maximum operating temperature.

(5) Measurements at the minimum operating temperature shall be performed after the junction temperature is in the thermal equilibrium and the package temperature has reached within 20% of the minimum operating temperature.

Table C-2. Qualification Test and Quality Conformance Inspection

Sub-group	Test or inspection item [10]	Test method or condition [2]	Sample size (accept no.) [1]	
			Qualification test	Quality conformance inspection
1	a) Vibration, high frequency	204	16 (0)	8 (0)
	b) Shock (specified pulse)	213, test condition I		
	c) Acceleration [9]	212, test condition C		
	d) Random vibration	2026, test conditions I - J		
	e) Seal 1) Fine 2) Gross	1014 Test condition A_2 Test condition C_1		
	f) Electrical characteristics	As specified in Table C-1 (subgroup 1)		
2	a) Thermal shock	107, 100 cycles [3]	4 (0)	2 (0)
	b) Seal [9] 1) Fine 2) Gross	1014 Test condition A_2 Test condition C_1		
	c) Radiation hardness [4] 1) Total dose	1019		
	d) Electrical characteristics	As specified in Table C-1 (subgroup 1)		
3	a) Resistance to soldering heat [5]	210, in accordance with the detailed specification	3 (0)	2 (0)
	b) Moisture resistance	106, step 7b shall not apply.		
	c) Electrical characteristics	As specified in Table C-1 (subgroup 1)		
4	a) Terminal strength	211 [6]	2 (0) [7]	
	b) Solderability	208, 245 ± 5ºC		
	c) Resistance to solvents	215		
5	a) Internal gas analysis	1018	3 (0) [7]	-
6	a) Steady state operating life	1005, 1000 hours at case temperature:125 ºC	5 (0)	2 (0)
	b) Electrical characteristics	As specified in Table C-1 (subgroups 1, 2 and 3)		
7	a) Electrostatic discharge sensitivity	3015 [8]	3 (0)	-
	b) Electrical characteristics	As specified in Table C-1 (subgroup 1)		

Notes:

(1) After the completion of subgroup 1, samples shall be divided into subgroups 2, 3, 4, 5, 6 and 7 for qualification test, and subgroups 2, 3, 4 and 6 for quality conformance inspection. However, for subgroups 4 and 5, note (7) may be applicable.

(2) Four-digit number refers to the test method number in MIL-STD-883. Three-digit number refers to the test method number in MIL-STD-202.

(3) The test temperature (upper and lower limits) shall be the maximum and minimum storage temperature.

(4) When total dose tests have been performed on the same lot of semiconductor chips used, the data may be utilized. Single event effect tests shall be evaluated on a semiconductor chip basis in accordance with appendix A. If data from tests performed on semiconductor chips of the same design is available, it may be used. Details shall be specified in the detail specification.

(5) Test conditions such as temperature, time, etc. shall be specified in the detail specification based on soldering conditions.

(6) When the diameter or width of the pin (terminal) is 0.8 mm or less, condition C shall be applied.

(7) Subgroups 4 and 5 may use samples from the same inspection lot, including electrical defective products. However, for subgroup 4, the samples shall be subjected to the same thermal conditions as the thermal tests (stabilization bake, temperature cycling and burn-in test) that good products are subjected to in screening prior to the tests.

(8) Tests with the same pin combination shall be performed on each sample.

(9) This test shall be performed when specified in the detail specification.

(10) Except for the steady state operating life test in subgroup 6, all other tests and inspections shall be as a non-operating condition (without bias). However, tests and inspections with operating condition (with bias) shall be specified in the detail specification.

APPENDIX D

PREPARATION OF DESIGN SPECIFICATION

APPENDIX D

PREPARATION OF DESIGN SPECIFICATION

D.1 Scope

This appendix provides formats and contents of the design specification.

D.2 Design Specification

Design specification based on paragraph 2.4 a) of this specification shall include at least contents specified in paragraph 3.3 of this specification and shall be in accordance with paragraph 3.1.1 to represent construction and design limit values indicating qualification coverage. Example of design specification is shown in Format D-1 (1).

To supply crystal oscillators based on this specification, manufacturer shall attach design specification which was prepared in accordance with this appendix to quality assurance program plan and submit to qualification acting agency at qualification (requalification) test application.

Note (1) Contents of example are for example only.

Attachment-○

Crystal Oscillators, High Reliability, Space Use

Design Specification

Prepared: dd/mmm/yyyy

Format D-1 (Cover)

Note (1) Contents are for example only (the same shall apply hereinafter).

Crystal Oscillators, High Reliability, Space Use
Design Specification

1. General

This specification establishes qualification coverage of design on space use, high reliability, crystal oscillators used for electronic equipment installed on spacecrafts. Other requirements resulting from specific use may be specified in detail specification.

2. Applicable Documents

Unless otherwise specified, the latest issues of documents listed below form a part of this specification to the extent specified herein.

JAXA-QTS-2000 Common Parts/Materials, Space Use, General Specification for
JAXA QTS-2220 Crystal Oscillators, High Reliability, Space Use, General Specification For
MIL STD-883 Test Methods standard, Microelectronics

3. Requirements

3.1 Design and Construction

Design and construction of crystal oscillators shall be in compliance with the following "Construction and design limit values" and paragraph 3.3 of JAXA-QTS-2220. In the event of a conflict between this specification and JAXA-QTS-2220, this specification shall take precedence.

Format D-1 (Text)

Construction and Design Limit Values

1. Part number _____
2. Manufacturer's name _____
2.1 Factory location and manufacturing line

Line (or process) name	Factory name	Location

3. Operating case temperature range: Min. _____ºC Max. _____ºC
4. Substrate
   a) Material _____
   b) Film formation process ☐Thin-film ☐Thick-film
   c) Membrane composition (Metallization and glassivation)

	Level No. (1)	Material	Forming Method	Thickness	
				Min.	Max.
Metallization material					
Glassivation					

Note (1) When the metallization or glassivation is multi-layered, the layer closest to the substrate shall be numbered level 1, and descriptions shall be made for all levels.

   d) Conductor
      Maximum current density (thin-film): _____ A/cm^2
      Maximum power consumption (thick-film): _____ W/cm^2
   e) Maximum power consumption of resistors
      1) Thin-film resistor: _____ W/cm^2
      2) Thick-film resistor: _____ W/cm^2

5. Pattern form
   a) Minimum element spacing
      1) Conductor – Conductor: _____
      2) Conductor – Resistor: _____
      3) Resistor – Resistor: _____
      4) Spacing of element mount: _____

b) Minimum pattern width
1) Conductor _____
2) Resistor _____
c) Element dimension
1) Resistors Min.:_____ Max.: _____
2) Chip capacitors Min.:_____ Max. : _____
3) Chip resistors Min.: _____ Max. : _____
4) Semiconductor chips Min.: _____ Max. : _____
5) Quartz crystal units Min.: _____Max. :_____

d) Trimming ☐Laser ☐Sand-blast ☐Anodic treatment
☐Others _____
e) Scribing ☐Diamond ☐Laser ☐Saw

6. Mounted element and mounting structure

Element type (mounting structure)	Mounting material	Maximum area (mm^2)	Maximum weight (mg)	Derating	Number of elements used (pcs)
a) Substrate					
b) Chip capacitor					
c) Chip resistor					
d) Semiconductor chips ☐Face-up ☐Eutectic bonding ☐Adhesive ☐Others					
e) Quartz crystal units					
f) Other items					

7. Internal connection

	Material	Dimensions/ configuration of wire (or ribbon)	Connecting method	Maximum wire length (or bond spacing)	Maximum current
a) Semiconductor chips / substrate					
b) Chip capacitor / substrate					
c) Chip resistor / substrate					
d) Quartz crystal units / substrate					
d) Substrate / substrate					
e) Substrate / package leads					
f) Other items					

8. Package and packaging material

a) Package configuration _____

b) Number of pins _____

c) Material _____

Header	Material	Plating material
Post to be bonded		
Cap or lid		
External leads		

9. Final seal

a) Atmosphere at sealing _____

b) Sealing method ☐Welding ☐Brazing ☐Others

c) Sealing material (except when welding) _____

Melting point _____

Maximum temperature _____

10. Sheet transformer

a) Material: _____

b) Number of layer: _____

c) Winding pattern: _____

1) Minimum pattern width : _____ mm

2) Minimum pattern spacing : _____ mm

3) Temperature rising: _____ max.

11. Typical construction illustration

Typical construction illustration of crystal oscillator is as follows:

APPENDIX E

PREPARATION OF DETAIL SPECIFICAITON

APPENDIX E

PREPARATION OF DETAIL SPECIFICATION

E.1. Scope

This appendix establishes instructions for preparation of the detail specification of crystal oscillators as specified in this specification.

E.2. General

This specification (JAXA-QTS-2220) establishes the general requirements for space use, high reliability crystal oscillators. To manufacture crystal oscillators using qualification acting agency-qualified production lines in accordance with this specification, the detail specification which specifies individual and specified requirements for the crystal oscillator shall be prepared.

E.3. Contents

Detail specification shall contain the following items in accordance with paragraph A.4 of JAXA-QTS-2000. Format of detail specifications (cover and contents) shall be as specified in Format E-1.

a) Revision record
b) General
c) Applicable documents
d) Requirements
e) Quality assurance provisions
f) Preparation for delivery
g) Notes

E.3.1 General

General shall specify the following items.

a) Scope
b) Part number
c) Absolute maximum ratings
d) Recommended operating conditions

E.3.1.1 Scope

Scope shall contain applicable general specification and specify scope of the detail specification.

E.3.1.2 Part Number

Part number shall be specified in accordance with paragraph 1.3.

E.3.1.3 Absolute Maximum Ratings

Absolute maximum ratings applied to crystal oscillators shall be specified in table format.

E.3.1.4 Recommended Operating Conditions

Recommended operating conditions for crystal oscillators shall be specified in table format.

E.3.2 Applicable Documents

Applicable documents shall be in accordance with paragraph A.3.2.1 of JAXA-QTS-2000. Applicable documents shall include at least quality assurance program plan.

E.3.3 Requirements

E.3.3.1 Design and Construction

In addition to referring to paragraph 3.3, design and construction requirements shall specify at least the following items.
It shall be clarified that product design and construction shall be in compliance with quality assurance program plan.

a) Mounted elements (paragraph 3.3.4)
b) Organic and Polymeric materials (paragraph 3.3.5)
c) Mounting materials for substrate, semiconductor chips and passive elements (paragraph 3.3.6)
d) Package (paragraphs 3.3.8 a), b) and E.3.3.1.1)
e) Lead material and finish (paragraphs 3.3.8 c) and E.3.3.1.2)
f) Electrical characteristics (paragraph E.3.3.1.3)
g) Pin connections (paragraphs E.3.3.1.4)

E.3.3.1.1 Package Configuration

Package configuration shall be shown with a package outline drawing, dimensions and external lead numbers of crystal oscillator.

E.3.3.1.2 Lead Material and Finish

Lead material and finish shall be specified. The lead finish shall be specified including adequate control limits.

E.3.3.1.3 Electrical Characteristics

Requirements for electrical characteristics shall reflect the intended function of the circuit according to the circuit function. Test conditions and limits (maximum, minimum or both) shall be specified for all required electrical parameters to represent intended function and assure interchangeability. In addition, a table shall be provided to define the relationship between the lead numbers and input/output signals of crystal oscillator specified in Table C-1.

E.3.3.1.4 Pin Connections

Pin connections shall be specified with a figure that clarifies the relationship between the external lead numbers.

E.3.3.2 Marking

Requirements for marking shall refer to paragraph 3.4. However, when radiation hardness (total dose radiation hardness) assurance level letter and the beryllium oxide package identification code are indicated on crystal oscillator, the details shall be specified.

E.3.3.3 Qualification

In addition to referring to paragraph 3.1, requirements for qualification test shall specify electrical parameters to be measured, steady state life test circuit and test conditions for electrostatic discharge sensitivity (refer to paragraph E.3.4.6). When certified manufacturer determines to perform radiation hardness test, the certified manufacturer shall specify the radiation hardness test.

E.3.4 Quality Assurance Provision

Requirements for quality assurance provision shall specify following eight items:

a) General requirements
b) Incoming materials control
c) Manufacturing process control
d) In-process inspection
e) Screening test
f) Qualification test and quality conformance inspection
g) Long-term storage
h) Change and optimization of tests and inspections

E.3.4.1 General Requirements

General requirements shall be specified by referring to paragraph 4.1.

E.3.4.2 Incoming Materials Control

Incoming materials control shall be specified by referring to paragraph 4.2.

E.3.4.3 Manufacturing Process Control

Manufacturing process control shall be specified by referring to paragraph 4.3.

E.3.4.4 In-process Inspection

In-process inspection shall be specified by referring to paragraph 4.5.
Inspection items, inspection methods, pass/fail criteria, and number of samples, etc., applicable to in-process inspection shall be specified.

E.3.4.5 Screening Test

In addition to referring to paragraph 4.7, requirements for screening test shall specify following items:

a) Electrical parameters to be measured
b) Test circuits and conditions for burn-in
c) Delta limits

E.3.4.5.1 Electrical Parameter Test to be measured

The following items shall be specified as electrical parameter tests to be measured at screening test. When an electrical parameter test (subgroup) that corresponds to an electrical characteristic test is not specified for circuit function reasons, the electrical parameter test (subgroup) may be exempted.

Electrical Parameter Test	Subgroup Number of Electrical Characteristics Test
Interim electrical parameter test	1
Final electrical parameter test	1, 2 and 3

E.3.4.5.2 Burn-in Test Circuit

The burn-in test circuit shall be configured to operate all internal elements in the crystal oscillator as close as possible to actual use conditions, to induce initial failures based on their potential defects, and to remove the defective product.

E.3.4.5.3 Delta Limits

Delta limits of crystal oscillator shall be specified in detail specification.

E.3.4.6 Qualification Test and Quality Conformance Inspection

In addition to referring to paragraphs 4.6 and 4.8, requirements for qualification test and quality conformance inspection shall specify external dimensions to be measured, electrical parameters, circuits for steady-state operating life test and test

conditions for electrostatic discharge sensitivity. When the product is qualified as radiation-hardened crystal oscillator, radiation hardness tests shall be specified for the product.

E.3.4.6.1 External Dimensions to be measured

The following symbols defined in paragraph F.3.2 at least shall be specified as the external dimensions to be measured in the quality conformance inspection. However, if the applicable symbol is not specified on the package outline drawing shown in Appendix F due to the type of package outline, the symbol shall not be applied.

Package Outline	Dimension Symbol
Flat package	A, D, D1, E, E1, e and L

E.3.4.6.2 Electrical parameters to be measured

In addition to electrical characteristic test, at least the following items shall be specified as electrical parameters to be measured. When no applicable subgroup is specified in the electrical characteristics test for circuit function reasons, the subgroup may be exempted.

Endpoint Electrical Parameter Test	Subgroup Number of Electrical Characteristics Test
Subgroup 1 of qualification test and quality conformance inspection	1
Subgroup 2 of qualification test and quality conformance inspection	1
Subgroup 3 of qualification test and quality conformance inspection	1
Subgroup 6 of qualification test and quality conformance inspection	1, 2 and 3
Subgroup 7 of qualification test and quality conformance inspection	1

E.3.4.6.3 Steady state Operating Life Test Circuit

Steady state operating life test circuit shall be configured to operate all internal elements in the crystal oscillator as close as possible to actual use conditions. In general, the same test circuit as the burn-in test circuit may be used (refer to paragraph E.3.4.5.2).

E.3.4.6.4 Radiation Hardness Test

a) When radiation hardness test (total dose test) is required for the crystal oscillator, radiation hardness assurance level shall be specified in accordance with paragraph 1.3.5 of this specification and test conditions shall be specified. When radiation hardness test (total dose test) is performed on semiconductor chips, the test shall be specified by referring to appendix A.

b) When radiation hardness test (single event effects test) is required for the crystal oscillator, test conditions shall be specified. When radiation hardness test (single event test) is performed on semiconductor chips, the test shall be specified by referring to appendix A.

E.3.4.6.5 Electrostatic Discharge Sensitivity Test

Pin combination shall be specified for performing the electrostatic discharge sensitivity test.

E.3.4.7 Long-term Storage

Delivery of products stored for more than or equal to 24 months shall be specified by referring to paragraph 4.9.1.

E.3.4.8 Change and Optimization of Tests and Inspections

When in-process inspection, screening test and quality conformance inspection specified in this specification are changed, exempted and/or optimized, the change, exemption and/or optimization shall be specified in the detail specification in accordance with paragraph 4.10.

E.3.5 Preparation for Delivery

Preparation for delivery shall be specified by referring to paragraph 5 of this specification.

E.3.6 Notes

Notes shall be specified by referring to the relevant items in paragraph 6 of this specification. In addition, handling precautions shall be specified as necessary and appropriate.

Format E-1 (Cover sheet)

Registration No.xxxx

JAXA-QTS-2220/xxxxA
(date)

Superseding
JAXA-QTS-2220/xxxx
Cancelled
(date)

CRYSTAL OSCILLATORS, HIGH RELIABILITY, SPACE USE, DETAIL SPECIFICATION FOR

Prepared and Established by ABCD CORPORATION

Issued by Japan Aerospace Exploration Agency

Format E-1 (Table of contents 1/2)

Contents

Format E-1 (Table of contents 2/2)

APPENDIX F

PACKAGE CONFIGURATION

APPENDIX F

PACKAGE CONFIGURATION

F.1 Scope

This appendix applies to package configuration of crystal oscillators.

F.2 Definition of Terms

Definition of terms used in this appendix shall be as follows.

a) Shape:
Physical form of a package excluding dimensions.

b) Package configuration:
Physical form of a package including dimensions.

c) Base plane:
Reference plane, parallel to the nominal seating plane, containing the lowest point of the package body.

d) Seating plane:
Reference plane which designates the interface of the case outline with the mounting surface.

e) Flat package:
A package in which the base and top planes are flat and parallel and leads are parallel to the base plane (refer to Figure F-1).

f) Index:
A reference mark such as a stamp, tab and notch that identifies the location of the first external lead position.

g) Index area:
Area in which all or a portion of the index must be located.

h) Dual in-line package:
A square package with leads arranged in two rows and leads are vertical to the side plane (refer to Figure F-2).

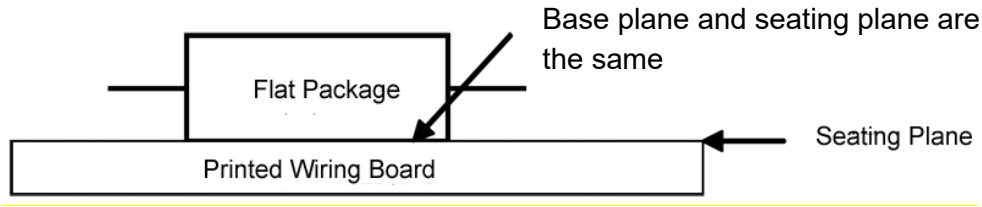


Figure F-1. Flat package

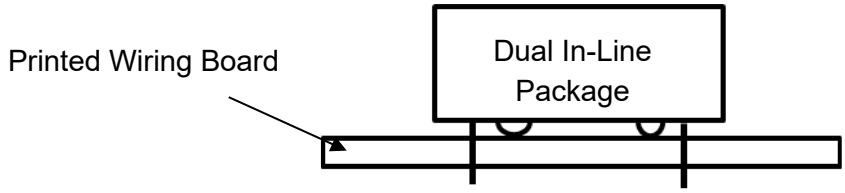


Figure F-2. Dual In-Line Package

F.3 Definition of Package Configuration

Package configuration shall be specified to meet the following requirements.

F.3.1 External Leads Numbering

For flat packages and dual in-line packages, external lead 1 shall be on the closest point to the index when viewed from the top (If the index is between two leads at equal distances, external lead 1 is located immediately adjacent to and counterclockwise from the index). The lead numbers shall increase in a counterclockwise direction.

F.3.2 Dimensions

Minimum value, maximum value or both shall be specified for dimensions identified with one of the symbols defined below.

A	Body height
Φb	External lead diameter
b	External lead width
c	External lead thickness
ΦD	Body diameter
D	Body length
D_1	Spacing of external lead row in the length direction
E	Body width
E_1	Spacing of external lead row in the width direction
e	External lead spacing
F	Flange dimension
k	Index dimension
L	External lead length
Q	Standoff height (the height from the seating plane to the base plane)
S	Distance between external leads and body edge
α	Angle of external leads spread

F.3.3 Illustration of Package Configuration

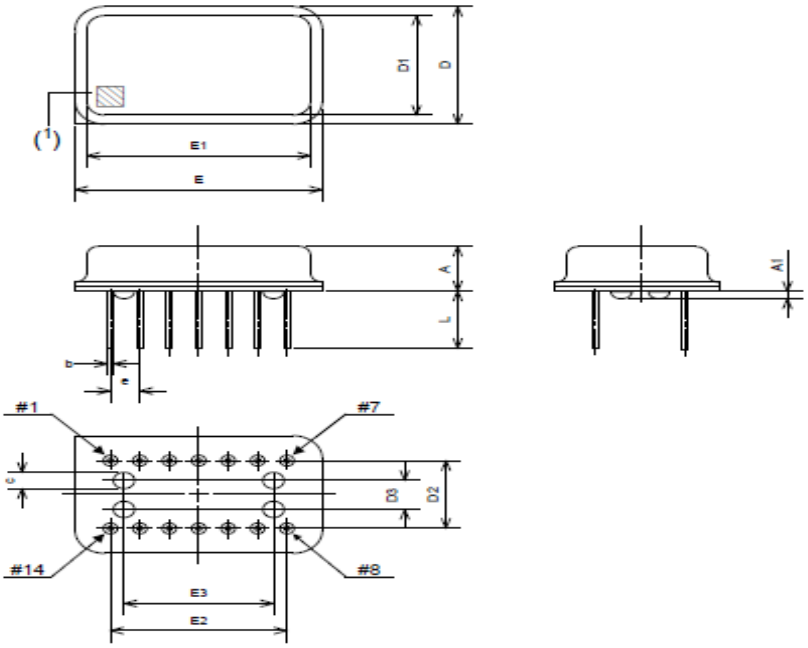
For flat packages, front, top, and side views shall be provided in orthogonal projections. For dual in-line packages, front, bottom and side views shall be provided in orthogonal projections. Dimension symbols (refer to paragraph F.3.2) shall be

shown in drawings and actual dimensions (minimum, maximum or both) with corresponding symbols shall be provided in table format.

F.3.4 Package Outline Drawings

This section provides drawings of the typical package configurations as follows.

	Package configuration	Number of leads	Figure no.
Dual in-line packages	CA	14	Figure F-3
Flat packages	CB	20	Figure F-4

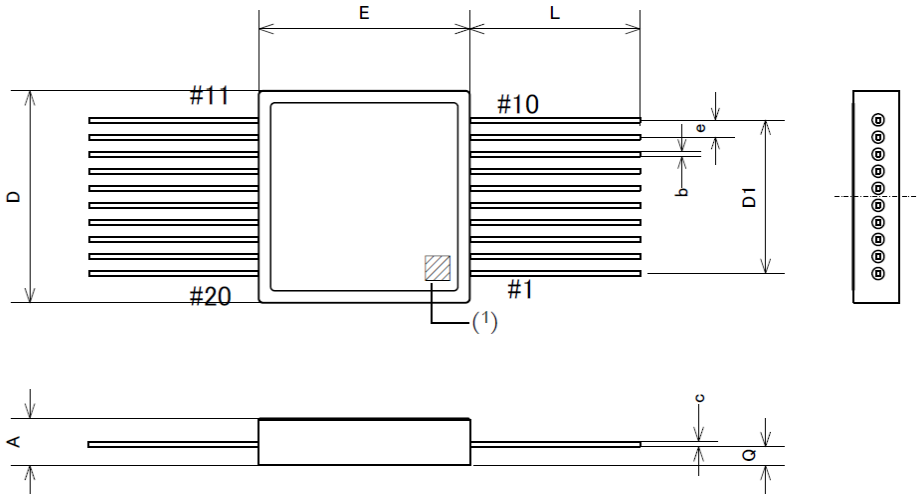


Unit: mm

Symbol	Dimensions (5)		Notes
	Min.	Max.	
A	4.5	5.1	
A1	(0.8)		(5)
b	0.35	0.55	(3)
c	(1.8)		(5)
D	12.0	13.0	(4)
D1	10.4	11.0	
D2	7.32	7.92	
D3	(3.2)		
E	19.6	20.6	(4)
E1	18.1	18.7	
E2	14.94	15.54	
E3	(12.7)		
e	2.54 STD		
L	5.85	6.85	

Notes: (1) Index area
(2) Applicable to all leads.
(3) Dimension of the off-center lid and any brazing material overflow produced during the sealing process shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 2.54±0.25mm.
(5) Applicable to all standoffs.

Figure F-3. Package Outline Drawing CA (14 pin DIP)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.2	3.8	
b	0.35	0.55	(2)
c	0.2	0.3	(2)
D	15.6	16.0	(3)
D1	11.13	11.73	
E	15.6	16.0	(3)
e	1.27 STD		(4)
L	12.7		

Notes:
(1) Index area.
(2) Applicable to all leads.
(3) Dimension of the off-center lid and any brazing material overflow produced during the sealing process shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

Figure F-4. Package Outline Drawing CB (20 lead flat package)