Registration No. 1288

JAXA-QTS-2140/B601A 13 June 2024

Superseding JAXA-QTS-2140/B601 Canceled 13 June 2024

FINE PITCH PRINTED WIRING BOARDS,
GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL,
HIGH RELIABILITY, SPACE USE,
DETAIL SPECIFICATION FOR

Prepared and Established by CMK CORPORATION

Issued by Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: 24 September 2025

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#### Record of revisions

Rev.	Date	Description
NC	24 Aug.	Original
	2023	Issued by CMK CORPORATION, Document number: CM84802.
Α	13 Jun.	Reflected the changes issued by CMK CORPORATION, Document number:
	2024	CM84803.
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Revision history

Revision history		
Rev.	Date	Description
NC 2 Dec. Original 2022		Original
01	17 Jan. 2023	Paragraph 3. Requirements  Added the wording "The inner layer copper foil with SVH shall be at least 12µm (nominal)" in the text to clarify the difference of the requirements between this specification and the generic specification.  Paragraph 3.a Performance  Added the wording "The inner layer copper foil with SVH shall be at least 12µm (nominal)" in the column "Specifications" of item "Metal-cad laminate and prepreg" in Table 4.  Paragraph 5. Preparation for delivery  Replaced the packaging marking with a printed circuit board shipping inspection report that corresponds to paragraph 5 of JAXA-QTS-2000.  Paragraph 6. Notes  Corrected the wrong description of the standard title.
02	7 July 2023	Changed the name (Consistency of the qualified products.)  Paragraph 1.GENERAL  a) Scope  Corrected the part name  b) Part number  Changed substrate applicable standard to IPC-4101 in Table 1.  c) Ratings  Changed the qualified part name to Fine Pitch Printed Wiring Boards, Glass  Oven Base Epoxy Resin Base Material. (Consistency of the qualified products)  Changed substrate applicable standard to IPC-4101.  Added the description of the mounting pad width restrictions on conductors for the prevention of solder bridges.  Assigned the applicable document as JAXA-QTS-2140.  Paragraph 2. Applicable Documents  Corrected the wrong document name.  Paragraph 3. a. Performance  Changed the specification for metal-cad laminate and prepreg to IPC-4101 in Table 4.  Paragraph 4. a. In-process inspection  Changed the descriptions in Table 5 to align with paragraph B.4.1 of JAXA-QTS-2140.  Deleted paragraphs B.3.2.1, B.3.3.5, B.3.3.6, B.3.3.7 and B.3.5, and replaced to B.3.4.1, B.3.4.2, B.3.4.3 and B.3.7 in Table 5.

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Rev.	Date	Description	
03	13 June 2024	Paragraph 4.a. In-Process Inspection Changed the name of the equipment from the Omega meter to CONTAMINOMETER™ in note (1) of Table 5.  Paragraph 4.d. Change of Tests and Inspections Changed the name of the measurement equipment from the Omega meter to CONTAMINOMETER™.  Reflected the change of the equipment due to the deterioration of the Omega meter in the text.	

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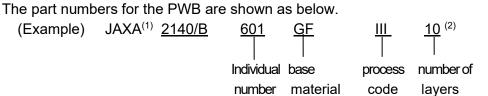
# FINE PITCH PRINTED WIRING BOARDS, GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL, HIGH RELIABLILITY, SPACE USE, DETAIL SPECIFICATION FOR

#### 1. GENERAL

#### 1.a) Scope

This specification applies to fine pitch printed wiring boards, glass base woven epoxy resin base material (hereinafter referred to as PWB), which are manufactured by CMK CORPORATION, certified by JAXA in accordance with JAXA-QTS-2140.

#### 1.b) Part Number



Note:<sup>(1)</sup> "JAXA" indicates the common part for space use and may be abbreviated to "J." Note:<sup>(2)</sup> Shows number of the conductor layers.

The base material code is shown in Table 1.

Table 1. Base Material Code

Base material code	Base material
GF	Glass base epoxy resin in accordance with IPC-4101 🔯

The processing code is shown in Table 2.

Table 2. Processing Code

Processing code	Construction	Remark
III	Multilayer	

The maximum number of layers is shown in Table 3.

#### 1.c) Ratings

Ratings are shown on Table 3.

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## Table 3. Ratings

Qualified products	Fine Pitch Printed Wiring Boards, Glass Base Woven Epoxy Resin Base Material.
Applicable standard for the base material	IPC-4101 🗘
Material	GF
Number of layers	10 layers as a maximum
Board thickness	1.6mm as a maximum
Conductor width	0.13mm as a minimum     * The minimum conductor spacing of the external layer with solder coat shall be 0.25mm when no solder resist is applied between the conductors of the external layer and the conductor of the external layer are located in vertical, horizontal, and diagonal directions.
Connection resistance	As specified in paragraph B.3.8.3, appendix B of JAXA-QTS-2140
Terminal pull strength	As specified in paragraph B.3.9, appendix B of JAXA-QTS-2140
Thermal shock	Test condition: MIL-STD-202 Method 107
Temperature range (°C)	-30 to 125°C
Number of cycles 1.000 (1,200 as a reference)	

#### 2. APPLICABLE DOCUMENTS

The applicable documents shall be in accordance with paragraph B.2, appendix B of JAXA-QTS-2140.

#### 3. REQUIREMENTS

The requirements shall be in accordance with paragraph B.3, appendix B of JAXA-QTS-2140.

The inner layer copper foil with SVH shall be at least 12µm (nominal).  $\triangle$ 

#### 3.a Performance

Performance shall be shown in Table 4.

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# Table 4. Performance (1/3)

ltem	Requirement paragraph of JAXA-QTS- 2140	Specification
Materials	B.3.2	As specified in appendix B of JAXA-QTS-2140
Metal-clad laminate and prepreg	B.3.2.1	As specified in IPC-4101  The board thickness shall be equal to or more than 0.05mm (nominal)  The inner layer copper foil with SVH shall be equal to or more than 12µm (nominal)
Solder coating	B.3.2.2	Sn content ratio 50% to 70%
Solder resist	B.3.2.3	Equivalent to IPS-SM-840 Class H
Marking ink	B.3.2.4	Epoxy based ink
Plating	B.3.2.5	-
(1) Electroless copper plating	B.3.2.5.1	Perform pretreatment to form electrolytic copper plating
(2) Electrolytic copper plating	B.3.2.5.2	Copper purity 99.5% min.
Design and construction	B.3.3	-
Manufacturing drawing and artwork master	B.3.3.1	As specified in appendix B of JAXA-QTS-2140
Connector for PWB	B.3.3.2	Do not use direct-shaped PWB connectors
Interlayer connection	B.3.3.3	Process by through-holes including small via holes (min. drill diameter 0.35mm), IVH (min. drill diameter 0.2mm) and SVH (min. drill diameter 0.2mm)
Conductor width	B.3.3.4	As specified in appendix B of JAXA-QTS-2140
Conductor Spacing	B.3.3.5	As specified in appendix B of JAXA-QTS-2140
Land diameter	B.3.3.6	As specified in appendix B of JAXA-QTS-2140
Plating thickness and others	B.3.3.7	
(1) Electroless copper plating	-	Enough and sufficient thickness for electrolytic copper plating in the next process.
(2) Electrolytic copper plating	-	Parts hole: 25µm min. Small via hole: 30µm min. IVH and SVH: 15µm min.
(3) Solder coat	-	As specified in appendix B of JAXA-QTS-2140
Operating temperature range	B.3.3.8	-65 to +125°C
Externals, dimensions, marking and others	B.3.4	-
Conductive pattern	B.3.4.1.1 a)	As specified in appendix B of JAXA-QTS-2140
Conductor	B.3.4.1.1 b)	As specified in appendix B of JAXA-QTS-2140
Annular ring	B.3.4.1.1 c)	Plated through hole: 0.05mm as a minimum. Non-plated-through hole: 0.38mm as a minimum.
Dielectric layer between conductor layers	B.3.4.1.1 d)	The surface of the insulator shall be free of unwanted residual conductors or foreign materials.
Electrolytic solder plating and solder coating	B.3.4.1.1 e)	Complete coverage of conductors with no pinholes, pits and others.
Edges of PWB	B.3.4.1.1 f)	As specified in appendix B of JAXA-QTS-2140

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## Table 4. Performance (2/3)

Item	Requirement paragraph of JAXA-QTS-2140	Specification
Surface of PWB	B.3.4.1.1 g)	As specified in appendix B of JAXA-QTS-2140
Solder resist	B.3.4.1.1 h)	As specified in appendix B of JAXA-QTS-2140.
Dimensions	B.3.4.2	As specified in appendix B of JAXA-QTS-2140.
Marking	B.3.4.3	As specified in appendix B of JAXA-QTS-2140.
Marking on split board	B.3.4.3.1	As specified in appendix B of JAXA-QTS-2140.
Through holes	B.3.4.4	-
a) Voids	B.3.4.4 a)	As specified in appendix B of JAXA-QTS-2140.
b) Conductive interface	B.3.4.4 b)	As specified in appendix B of JAXA-QTS-2140.
c) Layer-to-layer registration	B.3.4.4 c)	0.20mm max.
d) Dielectric layer thickness	B.3.4.4 d)	0.08mm min.
e) Plating thickness	B.3.4.4 e)	As specified in appendix B of JAXA-QTS-2140.
f) Annular ring	B.3.4.4 f)	As specified in appendix B of JAXA-QTS-2140.
Workmanship	B.3.5	As specified in appendix B of JAXA-QTS-2140.
Bow and twist	B.3.5.1	0.8% max.
Repair	B.3.5.2	As specified in appendix B of JAXA-QTS-2140.
Plating adhesion and overhang	B.3.6	As specified in appendix B of JAXA-QTS-2140.
Cleanliness	B.3.7	Resistivity of solvent extract: 2x10 <sup>6</sup> Ω · cm min.
Electrical performance	B.3.8	-
Dielectric withstanding voltage	B.3.8.1	As specified in appendix B of JAXA-QTS-2140.
Circuitry	B.3.8.2	As specified in appendix B of JAXA-QTS-2140.
Connection resistance	B.3.8.3	As specified in appendix B of JAXA-QTS-2140.
Mechanical performance	B.3.9	As specified in appendix B of JAXA-QTS-2140.
Terminal pull strength	B.3.9.1	As specified in appendix B of JAXA-QTS-2140.
a) Bond strength	B.3.9.1 a)	As a minimum of 89.2N or 1380N/cm <sup>2</sup> , whichever is smaller
b) Conductor and land	B.3.9.1 b)	As specified in appendix B of JAXA-QTS-2140.
c) Microsection of through hole	B.3.9.1 c)	As specified in appendix B of JAXA-QTS-2140.
Solderability	B.3.9.2	-
Hole solderability	B.3.9.2 a)	As specified in appendix B of JAXA-QTS-2140.
Surface solderability	B.3.9.2 b)	As specified in appendix B of JAXA-QTS-2140.
Environmental performance	B.3.10	-
Thermal shock (I)	B.3.10.1.1	As specified in appendix B of JAXA-QTS-2140.
Thermal shock (II)	B.3.10.1.2	As specified in appendix B of JAXA-QTS-2140.

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Table 4. Performance (3/3)

Item	Requirement paragraph of JAXA-QTS-2140	Specification
Humidity and insulation resistance	B.3.10.2	As specified in appendix B of JAXA-QTS-2140.
Hot oil resistance	B.3.10.3	As specified in appendix B of JAXA-QTS-2140.
Thermal stress	B.3.10.4	As specified in appendix B of JAXA-QTS-2140.
a) Externals	B.3.10.4.a)	As specified in appendix B of JAXA-QTS-2140.
b) Copper foil	B.3.10.4 b)	As specified in appendix B of JAXA-QTS-2140.
c) Laminated voids	B.3.10.4 c)	As specified in appendix B of JAXA-QTS-2140.
Radiation hardness	B.3.10.5	As specified in appendix B of JAXA-QTS-2140.

#### 4. QUALITY ASSURANCE PROVISIONS

The quality assurance provisions shall be as specified in paragraph B.4, appendix B of JAXA-QTS-2140.

### 4.a In-Process Inspection

The in-process inspection shall be as specified in Table 5 with no changes from paragraph B.4.1, appendix B of JAXA-QTS-2140.

Table 5. In-Process Inspection 🖄

NI-	I	Requirement	Test method	Number o	of samples
No.	Inspection item	paragraph	paragraph	Products	Test coupon
1	Visual inspection of		B.4.4.2.1		
	inner layers,	B.3.4.1		A II	Not emplicable
	construction and	B.3.4.2		All	Not applicable
	dimensions	B.3.4.3			
2	Cleanliness (1)	B.3.7	B.4.4.5	1	Not applicable

Note <sup>(1)</sup> For products from which chips generated during the router process have been removed, one sample per lot is measured using a Contaminometer.

### 4.b Qualification test

The qualification test shall be no changes from paragraph B.4.2, appendix B of JAXA-QTS-2140.

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## Table 6. Qualification Test

		Test			Determin	ation of pass	and fail
			Requirement	Test method	Quantity of	samples <sup>(1)</sup>	Quantity
Group	Order	Item	paragraph	paragraph	Production PWBs	Test coupon (2)	of allowable defects
	1	Design and construction	B.3.3	B.4.4.2			
		Externals, dimensions, marking and others.		B.4.4.2.1		A, B, C,	
I	2	Externals and construction	B.3.4.1		No. 1 to No. 6	No. 1 to D, E, F, No. 6 G, H, K	
		Dimensions	B.3.4.2		and L <sup>(</sup>	and L <sup>(4)</sup>	
		Marking	B.3.4.3				
	3	Workmanship (3)	B.3.5.	B.4.4.3			
II	1	Plating adhesion and overhang	B.3.6	B.4.4.4	No. 1 to	С	
	2	Bow and twist	B.3.5.1	B.4.4.3.1	No. 6	Not applicable	
Ш	1	Through holes	B.3.4.4	B.4.4.2.2	No. 1	A, F and K	
Ш	2	Terminal pull strength	B.3.9.1	B.4.4.7.1	INO. I	F	
	3	Solder resist thickness	B.3.4.5	B.4.4.2.3		J	
	1	Connection resistance	B.3.8.3	B.4.4.6.3			
IV	2	Hot oil resistance	B.3.10.3	B.4.4.8.3	No. 2	D	
	3	Connection resistance	B.3.8.3	B.4.4.6.3			0
	1	Circuitry	B.3.8.2	B.4.4.6.2			
	2	Connection resistance	B.3.8.3	B.4.4.6.3		F 1 O	
V	3	Thermal shock (I)	B.3.10.1.1	B.4.4.8.1 a)	No. 3	E and G	
	4	Circuitry	B.3.8.2	B.4.4.6.2			
	5	Connection resistance	B.3.8.3	B.4.4.6.3			
VI	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	No. 4	E	
VI	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1	110. 4	<u> </u>	
	1	Thermal stress	B.3.10.4	B.4.4.8.4		A, B. and L	
VII	2	Solderability	B.3.9.2	B.4.4.7.2	No. 5	B and H	
VIII	1	Radiation hardness	B.3.10.5	B.4.4.8.5	No. 6	Not applicable	
-	1	Material	B.3.2	Not applicable	(7	·)	Not applicable

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#### Notes:

- (1) The number of test coupons submitted for group I test shall be a summation of the test coupons for group II through VIII tests. For group II through VII tests, one test coupon shall be provided for each coupon type specified above.
  - In order to quality split boards, sprit board specimens shall be submitted as the production samples.
- (2) Test coupons and sample product shall be fabricated simultaneously. For group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test..
- Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the second test of group II test.
- Group I test shall be performed on the test coupons which are to be provided for group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.
- Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.
- (6) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress.
- (7) Data to meet the design specifications shall be submitted.

### 4.c Quality Conformance Inspection

Quality conformance inspection shall be as specified in Table 7 with no changes from paragraph B.4.3 of JAXA-QTS-2140.

**Table 7. Quality Conformance Inspection (Group A)** 

		C.		<b>-</b> .	Deterr	mination of pass a	ınd fail
	Inspe	ection		Test	Quantit	y of samples	Quantity
Group	Order	Item	Requirement paragraph	Method paragrap h	Production PWBs	Test coupon	of allowable defects
		Externals, Dimensions, marking and others		D 4 4 0 4			
I	1	Externals and construction	B.3.4.1	B.4.4.2.1	All	Not applicable	
		Dimensions	B.3.4.2				
		Marking	B.3.4.3				
	2	Workmanship	B.3.5.	B.4.4.3			
II	1	Bow and twist	B.3.5.1.	B.4.4.3.1	All	Not applicable	0
III	1	Circuity	B.3.8.2	B.4.4.6.2	All	Not applicable	U
IV	1	Thermal stress	B.3.10.4	B.4.4.8.4	Not	A, F and K <sup>(2)</sup>	
					applicable		
	2	Through hole	B.3.4.4	B.4.4.2.2	Not	A, B and L <sup>(2)</sup>	
		Conductive	b)	a) and d)	applicable		
		interface	c)	c)			
		Through hole	B.3.4.4	B.4.4.2.2	Not	A, B and L <sup>(2)</sup>	
		Plating	b)	A and d)	applicable		
		thickness	c)	c)			
V	1	Solderability	B.3.9.2	B.4.4.7.2	Not applicable	B and H <sup>(3)</sup>	

Notes: (1) Bow and twist (paragraph B.3.5.1) shall be inspected in order 1 of group II.

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**Table 8. Quality Conformance Inspection (Group B)** 

	In	spection	Requirement	Test method	Criteria for pass/fail	Quantity of
Group	Order	Item	Paragraph	paragraph	Test coupon	allowable defects
I	1	Plating adhesion and overhung	B.3.6	B.4.4.4.4	С	
	1	Terminal pull strength	B.3.9.1	B.4.4.7.1	F	
	2	Connection resistance	B.3.8.3	B.4.4.6.3		
II	3	Hot oil resistance	B.3.10.3	B.4.4.8.3	D	
	4	Connection resistance	B.3.8.3	B.4.4.6.3		
	1	Circuitry	B.3.8.2	B.4.4.6.2		
	2	Connection resistance	B.3.8.3	B.4.4.6.3		0
III	3	Thermal shock (II)	B.3.10.1.2	B.4.4.8.1 b)	E and G <sup>(1)</sup>	
	4	Circuitry	B.3.8.2	B.4.4.6.2		
	5	Connection resistance	B.3.8.3	B.4.4.6.3		
D./	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	_	
IV	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1	E	

Note <sup>(1)</sup> The circuitry shall be inspected with test coupon "G" for continuity and shall be inspected with test coupon (E) for circuit shorts.

#### 4.d Change of Tests and Inspections

In-Process Inspection

Cleanliness Method:

For products from which chips generated during the router process have been removed, one sample per lot is measured using an Contaminometer.

Reasons:

- In the case of sampling after circuit formation, expecting waste samples per working unit.
- When making samples, there is a concern that the correct cleanliness will
  not be reflected due to the risk of contamination from handling because
  sample cutting by router processing is a nonsteady operation. Therefore,
  the products processed through solder resist, solder leveling, and router
  are cleaned and used as samples.
- The number of samples should be kept to a minimum because the sampling targets are to be discarded.

<sup>(2)</sup> For a multilayer printed wiring board, test coupon A shall be inspected, when the corresponding product is provided with small via holes. Test coupons K and L shall be inspected when the corresponding products have IVH or SVH.

<sup>(3)</sup> Test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.

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5.	PREPARATION FOR DELIVERY			
	A shipping (buy-off) inspection report of PWBs associated in paragraph 5 of JAXA-QTS-2000 shall be Included in the shipment.   The materials for packaging shall be free from any harmful effects to PWBs.			
6.	Notes shall be as specified in paragraph 6 of JAXA-QTS-2000. $\triangle$			