Cancelled

Title:	FINE PITCH PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL HIGH RELIABILITY,SPACE USE, DETAIL SPECIFICATION FOR
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FINE PITCH PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL, HIGH RELIABILITY, SPACE USE,

DETAIL SPECIFICATION FOR

Prepared and Established by OKI Circuit Technology Co., Ltd.

Issued by Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: June 24, 2021

Revision Log

Rev.	Date	Description
Original	26 Jan. 2001	• NASDA-QTS-2140/B301 as original
A	25 Nov. 2004	• Changed the registration number. • Changed from NASDA-QTS-2140/B301 to JAXA-QTS-2140/B301. • Modified due to the transition to ISO-9001 (2000). • Changed the name of organization from NASDA to JAXA. • Table 3 Qualification Coverage: Added Metal Foil printed wiring boards under qualification coverage.
B	21 Nov. 2007	• Paragraphs 5.2 Marking on Package: Changed the definition for (d) Lot Identifier from "Last three digits of the lot number of lot card" to "The serial number in 3-digit number".
C	2 Aug. 2011	• Table 3 Qualification Coverage: Added IPC4101 to No. 1. Base materials applicable standard. • Table 3 Qualification Coverage: Changed from “1.27mm from edge of the board” to “0.3mm from edge of the board” for general board of Pattern-prohibited area.
D	6 Sept. 2012	• Table 3 Qualification Coverage: Added "Type1: modified polyimide" to general purpose of qualification coverage. • Table 4 Copper-Clad Laminate and Prepreg: Added standard, IPC4101.
E	1 Oct. 2012	• Cover sheet: Changed the name of the company. • Paragraph 5.2 Marking on Package: Changed the name of the manufacturer in Example: production lot number,
F	1 April 2014	• Cover sheet: Changed the name of the company. • Deleted the description of native polyimide due to discontinuation of production.
G	28 Aug. 2015	• Table 3 Qualification Coverage: Clarified the tolerance value for the qualification coverage of metal-foil printed wiring boards conductor width (105μm→105 ± 10μm) • Paragraph 5.2 Marking on Package: d) Corrected an error on the description about production lot number.
H	5 June 2017	• Changes associated with qualification coverage expansion 1) Added Tables 3, 4, and 5 (later table numbers were moved up) 2) Table 3: Changed board thickness of conventionally qualified range for B-1(GI) and B-2(GF) from 1.6mm to 1.8mm. 3) Changed the number of layer of B-5, metal foil board (GI type) from 10 layer to 12 layer. 4) Added the structures of B-3, B-4, and B -6 as newly qualified range. 5) Added paragraph 4.5 6) Added Figures 4 to 6. • Table 7: Reviewed performance list • Added Tables 8 to 10 to clarify the items of qualification test and quality conformance inspection

Revision Log

Rev.	Date	Description
J	14 Nov. 2017	• Tables 3 through 5 Qualification Coverage: Deleted specific structure numbers B-1 through B-6 • Table 3 Qualification Coverage: Added conventional material E679 and newly qualified material, R1766 to the table. • Tables 7 through 9: Added reference paragraph for side plating. • Reviewed paragraph 4.5 in associated with additional requirement for side plating.
K	27 April 2018	▪ Table 2, paragraph B.3.8.3: Changed “Conductor resistance” to “Connection resistance” to align with the term in the general specification. ▪ Table 3 Qualification coverage: Changed the minimum drill diameter of general purpose 10-layer GF epoxy (R1766) from ϕ0.30mm to ϕ0.20mm. ▪ Table 7, paragraph B.3.3.1 Modified “Drawings and artwork master” to “Manufacturing drawing and artwork master” to align with the general specification. ▪ Paragraph 4.5.4.2 Thermal stress: Changed the terms “plated-through hole barrel wall” to “sideplating wall”, “plated-through hole” to “sideplating” to clarify the statement. ▪ Table 5, Figure 3: Unified the term, “metal foil” within the table and the figure.
L	31 Oct. 2019	▪ Table 8, Table 10: Added test coupon C1 for metal foil board (thick copper foil). ▪ Added Paragraph 4.5.5 Metal Foil Printed Wiring Boards and Figure 8 Test coupons C and C1 ▪ Moved Figures 4 through 7 to be placed under the appropriate paragraph.

Contents

FINE PITCH PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL, HIGH RELIABILITY, SPACE USE, DETAIL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the general requirements and quality assurance provisions for the fine pitch printed wiring boards which use glass base woven polyimide resin or glass base woven epoxy resin as a base material (hereinafter referred to as “printed wiring boards”).

1.2 Part Number

The part number of the printed wiring boards shall be in accordance with Paragraph B.1.3, Appendix B of JAXA- QTS-2140 and as shown in the example below.

Example: JAXA([1]) 2140/B301 - GF - III - **([2])

Base material code | Processing code | Number of layers

Notes:
([1]) "JAXA" indicates the common part is for space use and may be abbreviated to “J”.
([2]) Number of conductor layers

Table 1 Part Number

Item	JAXA-QTS-2140 Applicable paragraph	Requirement
Base material code	B.1.3.1	GF (glass base woven epoxy resin) GI (glass base woven polyimide resin)
Processing code	B.1.3.2	I (single-sided printed wiring board) II (double-sided printed wiring board) III (multilayer printed wiring board)
Number of layers	B.1.3.3	The maximum number of layer is specified in Tables 3 and 4.

1.3 Ratings

Table 2. Ratings

Test item	JAXA-QTS-2140 Paragraph	Description
Operating temperature range	B.3.3.8	GF: -65°C to +125°C GI: -65°C to +170°C
Connection resistance	B.3.8.3	Ri (mΩ) max. calculated from the next equation $Ri = 2\rho\frac{l}{W \cdot t}\ (m\Omega)$ ρ = 1.72 X 10^{-2} (mΩ· mm) (Volume resistivity of copper at 20°C) l = Distance between lands (mm) w = Conductor width (mm) t = Conductor thickness (mm)
Through hole pull strength	B.3.9.1	1380N/cm^2 as a minimum and calculated from the next equation. $L \geqq 1380\frac{\pi\{(d_2)^2 - (d_1)^2\}}{4}$ L = Pull strength (N) d_1 = Hole diameter (cm) d_2 = Land diameter (cm)
Change in connection resistance due to temperature	--	Changes in connection resistance due to the temperature of conductor pattern is Rx (mΩ) provided by the next equation. Rx = Rc {1 + 0.00377(Tx-20)} Rc = 1.72 X 10^{-2} (mΩ· mm) (Volume resistivity of copper at 20°C)(mΩ) Tx = Temperature (°C)

2. APPLICABLE DOCUMENTS

The applicable documents shall be in accordance with Paragraph B.2.1, Appendix B of JAXA-QTS-2140.

3. REQUIREMENTS

The requirements shall be in accordance with Paragraph B.3, Appendix B of JAXA-QTS-2140 and as follow.

3.1 Qualification Coverage

The qualification coverage shall be as shown in Tables 3 through 5, and Figures 1 through 3.

Table 3. Qualification Coverage

Specification		General purpose 10-layer	General purpose 10-layer	General purpose 10-layer	General purpose 10-layer
Base material		GF Epoxy (E679)	GI Polyimide (I671)	GF Epoxy (R1766)	GI Polyimide (I671)
Base materials applicable standard		IPC4101,JPCA/NASDA-SCL01			
Maximum number of layer	Through hole	10 layers	10 layers	10 layers	10 layers
	SVH/IVH	2 layers	2 layers	2 layers	2 layers
Maximum number of buildup		One	One	One	One
Maximum board thickness		1.6mm	1.6mm	1.8mm	1.8mm
Minimum drill diameter	Through hole	Φ0.35mm	Φ0.35mm	Φ0.35mm	Φ0.35mm
	SVH/IVH	Φ0.20mm	Φ0.20mm	Φ0.20mm	Φ0.20mm
Minimum plating thickness	Through hole	30μm	30μm	35μm	35μm
	SVH/IVH	15μm	15μm	15μm	15μm
Conductor width		0.13mm min.	0.13mm min.	0.13mm min.	0.13mm min.
Conductor spacing		0.18mm min.	0.18mm min.	0.18mm min.	0.18mm min.
Pattern-prohibited area from edge of the board		0.3mm min.	0.3mm min.	0.3mm min.	0.3mm min.
Solder resist ink		Equivalent to IPC-SM-840 class H			
Side-plating	Annular ring on outer layer	-	-	2.0mm	2.0mm
	Inner layer connection for reinforcement	-	-	2 layers min. for 6-(or less) layer boards	
		-	-	4 layers min. for more than 6-layer boards	
Surface processing		Solder coating, electrolytic nickel gold plating (partial), electrolytic nickel gold plating (entire surface)			

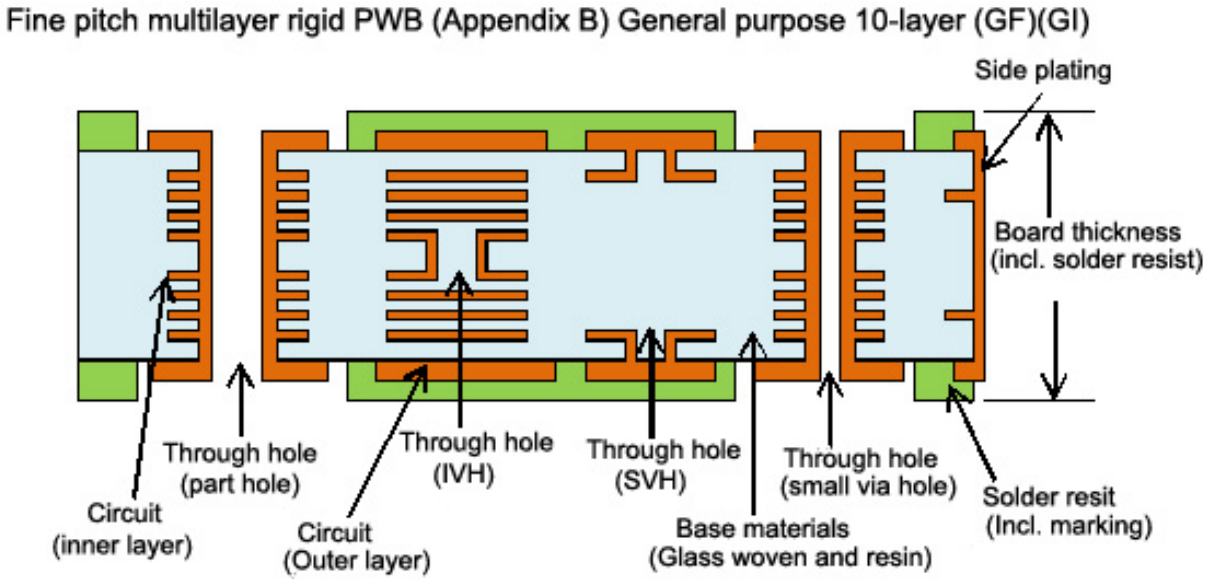


Figure 1. Cross Sectional View of General Purpose Boards

Table 4. Qualification Coverage

Specification		Multilayer SVH 16 layers (8+8)	Multilayer IVH 16 layers (1+14+1)
Base material		GI Polyimide	GI Polyimide
Base materials applicable standard		IPC4101,JPCA/NASDA-SCL01	
Maximum number of layer	Through hole	16 layers	16 layers
	Multilayer SVH	8 layers	--
	Multilayer IVH	2 layers	14 layers
Maximum number of buildup		Two	Two
Maximum board thickness		2.6mm	2.6mm
Minimum drill diameter	Through hole	Φ0.35mm	Φ0.35mm
	SVH/IVH	Φ0.20mm	Φ0.20mm
	Multilayer SVH/IVH	Φ0.20mm	Φ0.20mm
Minimum plating thickness	Through hole	30μm	30μm
	SVH/IVH	15μm	15μm
	Multilayer SVH/IVH	35μm	35μm
Conductor width		0.13mm as a minimum	0.13mm as a minimum
Conductor spacing		0.18mm as a minimum	0.18mm as a minimum
Pattern-prohibited area from edge of the board		0.3mm as a minimum	0.3mm as a minimum
Solder resist ink		Equivalent to IPC-SM-840 class H	
Side-plating	Annular ring on outer layer	2.0mm	2.0mm
	Inner layer connection for reinforcement	2 layers as a minimum for 6 (or less) layer boards	
		4 layers as a minimum for more than 6-layer boards	
Surface processing		1, Solder coating, 2, electrolytic nickel gold plating (partial), 3, electrolytic nickel gold plating (entire surface)	

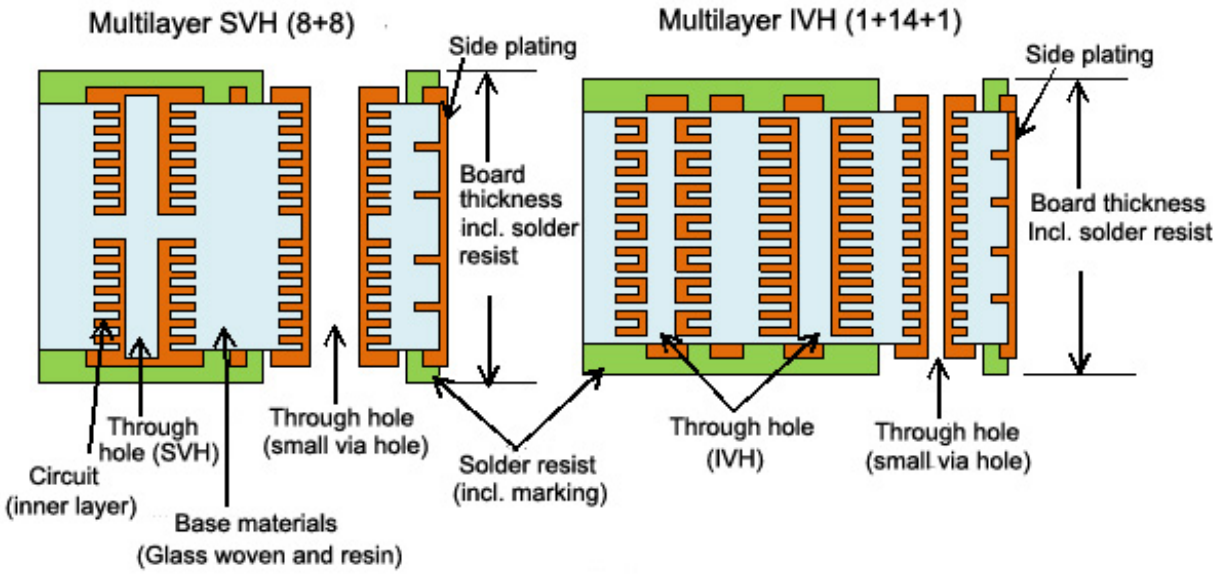


Figure 2. Cross Sectional View of Multilayer SVH/IVH Boards

Table 5. Qualification Coverage

Specification		Metal foil 10 layers (5+5) (conventional)	Metal foil 12 layers (6+6)	Metal foil 12 layers (1+10+1)
Base material		GI Polyimide	GI Polyimide	GI Polyimide
Base materials applicable standard		IPC4101, JPCA/NASDA-SCL01		
Maximum number of layer	Through hole	10 layers	12 layers	12 layers
	Multilayer SVH	5 layers	6 layers	--
	Multilayer IVH	2 layers	2 layers	10 layers
Maximum number of buildup		Two	Two	Two
Maximum board thickness		2.5mm	3.4mm	3.4mm
Conductor thickness		105μm ± 10μm	105μm ± 10μm	105μm ± 10μm
Minimum drill diameter	Through hole	Φ0.70mm	Φ0.35mm	Φ0.35mm
	SVH/IVH	Φ0.20mm	Φ0.20mm	Φ0.20mm
	Multilayer SVH/IVH	Φ0.20mm	Φ0.20mm	Φ0.20mm
Minimum plating thickness	Through hole	63μm	35μm	35μm
	SVH/IVH	15μm	15μm	15μm
	Multilayer SVH/IVH	15μm	35μm	35μm
Conductor width		0.15mm min.	0.15mm min.	0.15mm min.
Conductor spacing		0.18mm min.	0.18mm min.	0.18mm min.
Pattern-prohibited area from edge of the board		0.3mm min.	0.3mm min.	0.3mm min.
Solder resist ink		Equivalent to IPC-SM-840 class H		
Plating on side surface	Annular ring on outer layer	-	2.0mm	
	Inner layer connection for reinforcement	-	2 layers min, for 6 (or less) layer boards	
		-	4 layers min, for more than 6-layer boards	
Surface processing		1.Solder coating, 2.Electrolytic nickel gold plating (partial)	1.Solder coating, 2.Electrolytic nickel gold plating (partial), 3.Electrolytic nickel gold plating (entire surface)	

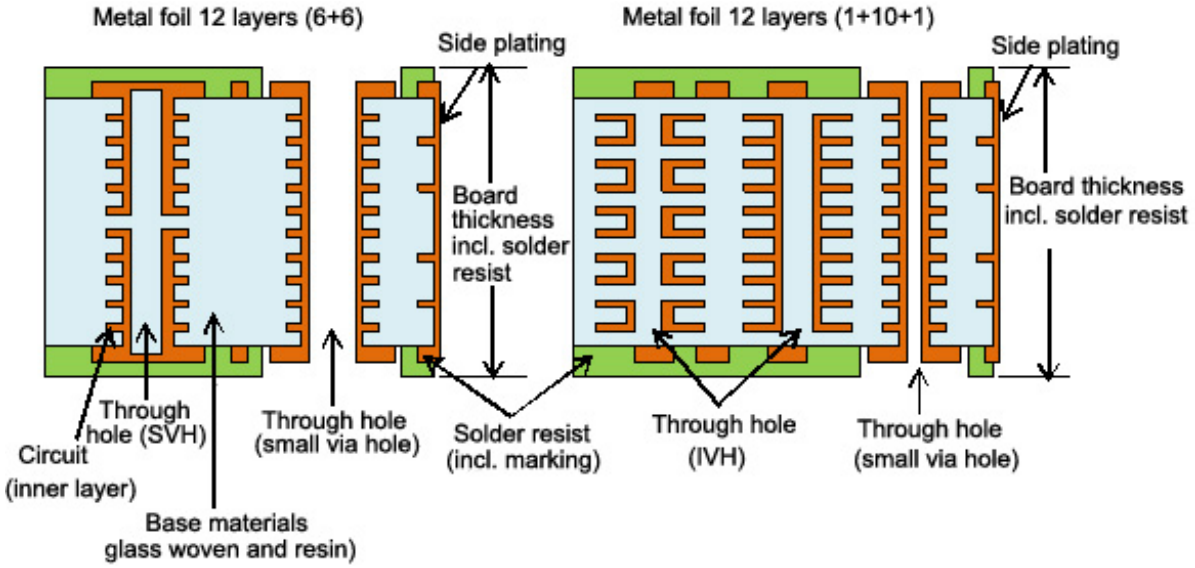


Figure 3. Cross Sectional View of Metal Foil Printed Wiring Boards

3.2 Materials

The materials shall be in accordance with Paragraph B.3.2, Appendix B of JAXA-QTS-2140 and as follows.

3.2.1 Copper-Clad Laminate and Prepreg

The copper-clad laminates and prepregs used for the printed wiring boards shall be in accordance with the applicable standards (IPC-4101 or JPCA/NASDA-SCL01) and specified in Table 6.

Table 6. Copper-Clad Laminate and Prepreg

Base material	Copper-clad laminate	Prepreg	Notes
GF	• IPC4101 • JPCA/NASDA-SCL01 (Space use 2140GF1) (Space use 2140GF2)	• IPC4101 • JPCA/NASDA-SCL01 (Space use 2140GF3)	1) The minimum board thickness for copper-clad laminate shall be 0.1mm (nominal) as a minimum. 2) The minimum copper foil thickness of the outermost layer shall be 18μm (nominal) as a minimum, and for printed wiring boards with SVH, it shall be 9μm (nominal) as a minimum. 3) The minimum copper foil thickness for the inner layer shall be 35μm (nominal) as a minimum. For printed wiring boards with SVH or IVH, the copper foil thickness shall be 18μm (nominal) as a minimum.
GI	• IPC4101 • JPCA/NASDA-SCL01 (Space use 2140GI1) (Space use 2140GI2)	• IPC4101 • JPCA/NASDA-SCL01 (Space use 2140GI3)	

GF1: Single-sided material, double-sided material GF2: Multilayer material GF3: Prepreg
GI 1: Single-sided material, double-sided material GI 2: Multilayer material GI 3: Prepreg

3.3 Performance

The performance shall be shown in Table 7.

Table 7. Performances (1/3)

Item	Requirements of JAXA-QTS-2140	Requirements
Materials	B.3.2	As specified in Appendix B of JAXA-QTS-2140.
Metal-clad laminate and prepreg	B.3.2.1	In accordance with IPC-4101
Solder coating	B.3.2.2	Tin content: 50% to 70%
Solder resist	B.3.2.3	IPC-SM-840 Class H or equivalent
Marking ink	B.3.2.4	Epoxy ink
Plating	B.3.2.5	–
(1) Electroless copper plating	B.3.2.5.1	Create copper undercoat in preparation for electrolytic copper plating.
(2) Electrolytic copper plating	B.3.2.5.2	Minimum purity: 99.9%
(3) Electrolytic gold plating	B.3.2.5.3	Minimum purity: 99.7%, hardness: 91 ≦Hk ≦129
(4) Electrolytic nickel plating	B.3.2.5.4	SAE-AMS-QQ-N-290 or equivalent: low stress
Design and construction	B.3.3	–
Manufacturing drawings and artwork master	B.3.3.1	As specified in Appendix B of JAXA-QTS-2140
Interlayer connection	B.3.3.3	As specified in Appendix B of JAXA-QTS-2140
Conductor width	B.3.3.4	As specified in Appendix B of JAXA-QTS-2140
Conductor spacing	B.3.3.5	As specified in Appendix B of JAXA-QTS-2140
Land diameter	B.3.3.6	As specified in Appendix B of JAXA-QTS-2140
Plating thickness and others	B.3.3.7	–
(1) Electroless copper plating	–	Necessary and sufficient amount of thickness for the next process (electrolytic copper plating)
(2) Electrolytic copper plating (1)	–	Through hole: 30μm (conventional general purpose; E679, I671) Through hole: 63μm (conventional metal foil; I671) Through hole: 35μm (general purpose; R1766, I671)) Through hole: 30μm (multilayer/ SVH) Through hole: 35μm (metal foil) IVH and SVH: 15μm as a minimum Multilayer IVH/Multilayer SVH: 35μm as a minimum Sideplating thickness: 30μm
(3) Electrolytic gold plating	–	1.3 to 4.0μm
(4) Electrolytic nickel plating	–	5μm as a minimum
(5) Solder coating	–	As specified in Appendix B of JAXA-QTS-2140
Operating temperature range	B.3.3.8	As specified in Appendix B of JAXA-QTS-2140
Externals, dimensions, marking and others	B.3.4	–
a) Conductive pattern	B.3.4.1.1 a)	As specified in Appendix B of JAXA-QTS-2140
b) Conductor	B.3.4.1.1 b)	As specified in Appendix B of JAXA-QTS-2140

Table 7. Performances (2/3)

Item	Requirements of JAXA-QTS-2140	Requirements
c) Annular ring	B.3.4.1.1 c)	Through hole: 0.05mm as a minimum Non-through hole: 0.38mm as a minimum
d) Dielectric layer between conductor layers	B.3.4.1.1 d)	As specified in Appendix B of JAXA-QTS-2140
e) Electrolytic solder plating and solder coating	B.3.4.1.1 e)	The electrolytic solder plating shall be uniform, free of pinholes or pits, and completely cover conductive patterns. This provision shall not apply to vertical conductor edges.
f) Edges of printed wiring board	B.3.4.1.1 f)	As specified in Appendix B of JAXA-QTS-2140.
g) Surface of printed wiring board	B.3.4.1.1 g)	As specified in Appendix B of JAXA-QTS-2140.
h) Solder resist	B.3.4.1.1 h)	As specified in Appendix B of JAXA-QTS-2140.
Dimensions	B.3.4.2	As specified in Appendix B of JAXA-QTS-2140.
Marking	B.3.4.3	As specified in Appendix B of JAXA-QTS-2140.
Marking on split board	B.3.4.3.1	As specified in Appendix B of JAXA-QTS-2140.
Workmanship	B.3.5	As specified in Appendix B of JAXA-QTS-2140.
Repair	B.3.5.2	As specified in Appendix B of JAXA-QTS-2140.
Bow and twist	B.3.5.1	0.8% as a maximum
Through holes	B.3.4.4	As specified in Appendix B of JAXA-QTS-2140.
a) Voids	B.3.4.4. a)	As specified in Appendix B of JAXA-QTS-2140.
b) Conductive interface	B 3.4.4. b)	As specified in Appendix B of JAXA-QTS-2140.
c) Layer-to-layer misregistration	B 3.4.4. c)	As specified in Appendix B of JAXA-QTS-2140.
d) Dielectric layer thickness	B 3.4.4. d)	0.08mm as a minimum
e) Plating thickness	B 3.4.4. e)	As specified in Appendix B of JAXA-QTS-2140.
f) Annular ring	B 3.4.4. f)	As specified in Appendix B of JAXA-QTS-2140.
g) Resin filling of multilayer IVH and multilayer SVH	–	90% as a minimum.
h) Resin recession for the plating of multilayer SVH resin-filled part	–	Depth: 0.08mm as a maximum.
Plating adhesion and overhang	B.3.6	As specified in Appendix B of JAXA-QTS-2140.
Dielectric withstanding voltage	B.3.8.1	As specified in Appendix B of JAXA-QTS-2140.
Circuitry (continuity, circuit shorts)	B.3.8.2	As specified in Appendix B of JAXA-QTS-2140.
Thermal shock	B.3.10.1	Resistance change rate after 1000 cycles: withiin10%
Moisture and insulation resistance	B.3.10.2	As specified in Appendix B of JAXA-QTS-2140.
Terminal pull strength	B.3.9.1	1380N/cm^2 as a minimum
Solderability	B.3.9.2	–
a) Hole solderability	B.3.9.2 a)	As specified in Appendix B of JAXA-QTS-2140.
b) Surface solderability	B.3.9.2 b)	As specified in Appendix B of JAXA-QTS-2140.

Table 7. Performances (3/3)

Item	Requirements of JAXA-QTS-2140	Requirements
Hot oil resistance	B.3.10.3	Room temperature ←→260°C, resistance change rate after 10 cycles: withiin10%
Connection resistance	B.3.8.3	As specified in Appendix B of JAXA-QTS-2140.
Thermal stress	B.3.10.4	–
a) External view	B.3.10.4 a)	As specified in Appendix B of JAXA-QTS-2140.
b) Copper foil	B.3.10.4 b)	As specified in Appendix B of JAXA-QTS-2140.
c) Laminate void	B.3.10.4 c)	As specified in Appendix B of JAXA-QTS-2140.
Radiation hardness	B.3.10.5	Insulation resistance after irradiation: 500MΩ as a minimum
Cleanliness	B.3.7	Resistance of extracts: 2 x 10^6 Ω· cm
Solder resist thickness	B.3.4.5	17.5μm as a minimum (at the center of conductor)

Note (1): For the qualification coverage of any products manufactured per the revision G or before of this detail specification, “conventional” specification shall be referred.

4. QUALITY ASSURANCE PROVISIONS

The quality assurance provisions shall be in accordance with Paragraph B.4, Appendix B of JAXA-QTS-2140 and as follows.

4.1 In-Process Inspection

The In-process inspection shall be in accordance with Paragraph B.4.1, Appendix B of JAXA-QTS-2140.

4.2 Qualification Test

The qualification test shall be in accordance with Paragraph B.4.2, Appendix B of JAXA-QTS-2140.

Table 8. Qualification Test (1/2)

Test			Requirement paragraph	Test method paragraph	Accept/reject criteria		
					Sample (1)		Sample size/accept number
Group	Order	Test item			Production printed wiring boards	Test coupon (2)	
I	1	Design and construction	B.3.3	B.4.4.2	No. 1 to No. 6	A, B, C, D, E, F, G, H, K, L, D2, G2, K2, L2 and O (4) (8)	100%(0)
	2	Externals, dimensions, marking and others Externals and construction Dimensions Marking	B.3.4.1 B.3.4.2 B.3.4.3	B.4.4.2.1			
	3	Workmanship(3)	B.3.5	B.4.4.3			
II	1	Plating adhesion and overhang	B.3.6	B.4.4.4	No. 1 to No. 6	C and C1	
	2	Bow and twist	B.3.5.1	B.4.4.3.1		N/A	
III	1	Through holes	B.3.4.4	B.4.4.2.2	No. 1	A, F, K and K2	
	2	Terminal pull strength	B.3.9.1	B.4.4.7.1		F	
	3	Solder resist thickness	B.3.4.5	B.4.4.2.3		J	

Table 8. Qualification Test (2/2)

Test			Requirement paragraph	Test method paragraph	Accept/reject criteria		
					Sample (1)		Sample size /accept number
Group	Order	Test item			Production printed wiring boards	Test coupon (2)	
IV	1	Connection resistance	B.3.8.3	B.4.4.6.3	No. 2	D and D2	100%(0)
	2	Hot oil resistance	B.3.10.3	B.4.4.8.3			
	3	Connection resistance	B.3.8.3	B.4.4.6.3			
V	1	Circuitry	B.3.8.2	B.4.4.6.2	No. 3	E, G and G2(5)	
	2	Connection resistance	B.3.8.3	B.4.4.6.3			
	3	Thermal shock (I)	B.3.10.1.1	B.4.4.8.1 a)			
	4	Circuitry	B.3.8.2	B.4.4.6.2			
	5	Connection resistance	B.3.8.3	B.4.4.6.3			
VI	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	No. 4	E	
	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1			
VII	1	Thermal stress	B.3.10.4	B.4.4.8.4	No. 5	A, B, L2, and O(8)	
	2	Solderability	B.3.9.2	B.4.4.7.2		B and H(6)	
VIII	1	Radiation hardness	B.3.10.5	B.4.4.8.5	No.6	N/A	
-	1	Materials	B.3.2	N/A	(7)		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. In order to qualify split boards, split board specimens shall be submitted as the production samples.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the second test of Group II tests.

(4) Group I test shall be performed on the test coupons which are to be provided for Group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(5) Under the circuitry test, the test coupons G and G2 shall be subjected to the continuity test and test coupon E shall be subjected to circuit shorts test.

(6) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

(7) Data to certify compliance with design specifications shall be submitted.

(8) The test coupon O shall be tested when the sideplating is required.

4.3 Quality Conformance Inspection

The quality conformance inspection shall be in accordance with Paragraph B.4.3, Appendix B of JAXA-QTS-2140.

Table 9. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Accept/reject criteria		
					Sample		
Group	Order	Inspection item			Production printed wiring boards	Test coupon(1)	Sample size /accept number
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	B.3.4.1 B.3.4.2 B.3.4.3	B.4.4.2.1	100%	N/A	100%(0)
	2	Workmanship(2)	B.3.5	B.4.4.3			
II	1	Bow and twist	B.3.5.1	B.4.4.3.1	100%	N/A	
III	1	Circuitry	B.3.8.2	B.4.4.6.2	100%	N/A	
IV	1	Thermal stress	B.3.10.4	B.4.4.8.4	N/A	A, F, K and K2 (A, B, F)(3)(4) and O(6)	
	2	Through holes Conductive interface Plating thickness	B.3.4.4 b) e)	B.4.4.2.2 a) and d) c)		A, B, L and L2 (A, B and F)(3)(4)	
V	1	Solderability	B.3.9.2	B.4.4.7.2	N/A	B and H (A and D)(5)	

Notes:

(1) A letter inside the parentheses shows the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

(2) Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the first test of Group II tests.

(3) For a multilayer printed wiring board, test coupon A shall be inspected when the corresponding product is provided with small via holes. Test coupons K, L, K2 and L2 shall be inspected when the corresponding products have IVH or SVH.

(4) For a single-sided or double-sided printed wiring board, test coupon F shall be inspected, only when the corresponding product is provided with small via holes.

(5) Test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.

(6) The test coupon O shall be tested when the sideplating is required.

Table 10. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Accept/reject criteria	
Group	Order	Inspection item			Test coupon	Sample size /accept number
I	1	Plating adhesion and overhang	B.3.6	B.4.4.4	C and C1	100%(0)
II	1	Terminal pull strength	B.3.9.1	B.4.4.7.1	F	
	2	Connection resistance	B.3.8.3	B.4.4.6.3	D	
	3	Hot oil resistance	B.3.10.3	B.4.4.8.3		
	4	Connection resistance	B.3.8.3	B.4.4.6.3		
III	1	Circuitry	B.3.8.2	B.4.4.6.2	E, G and G2(1)	
	2	Connection resistance	B.3.8.3	B.4.4.6.3		
	3	Thermal shock (II)	B.3.10.1.2	B.4.4.8.1 b)		
	4	Circuitry	B.3.8.2	B.4.4.6.2		
	5	Connection resistance	B.3.8.3	B.4.4.6.3		
IV	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	E	
	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1		

Note: (1) Under the circuitry test, the test coupons G and G2 shall be used for the continuity test and the test coupon E shall be used for circuit shorts test.

4.4 Long Term Storage

The long-term storage shall not be applicable.

4.5 Change of Tests and Inspections

The following test items shall be added to the requirements of Appendix B in JAXA-QTS-2140.

4.5.1 Plating Thickness and Others

Plating thickness and others (paragraph B.3.3.7): For electrolytic copper, the through hole plating shall be 30μm or 35μm as a minimum, and multilayer IVH and multilayer SVH plating shall be 35μm as a minimum.

4.5.2 Through Holes

Through holes (paragraph B.3.4.4): The requirements for resin filling of multilayer IVH and multilayer SVH, and for resin recession at the filled resin of multilayer SVH shall be added. (See table 7)

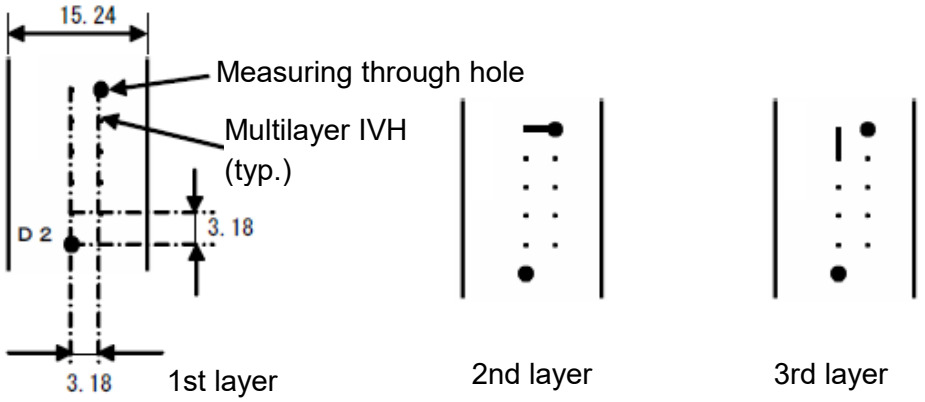
4.5.3 Multilayer IVH or Multilayer SVH Structure

In the application of multilayer IVH or multilayer SVH structure, the following test coupons other than the coupons (see Figure B-9) specified in Appendix B of JAXA-QTS-2140 shall be used.

a) Test coupons D2 and G2 (which are equivalent to the coupons D and G, respectively, of Appendix B of JAXA-QTS-2140) shall be added (see Figures 4 and 5).

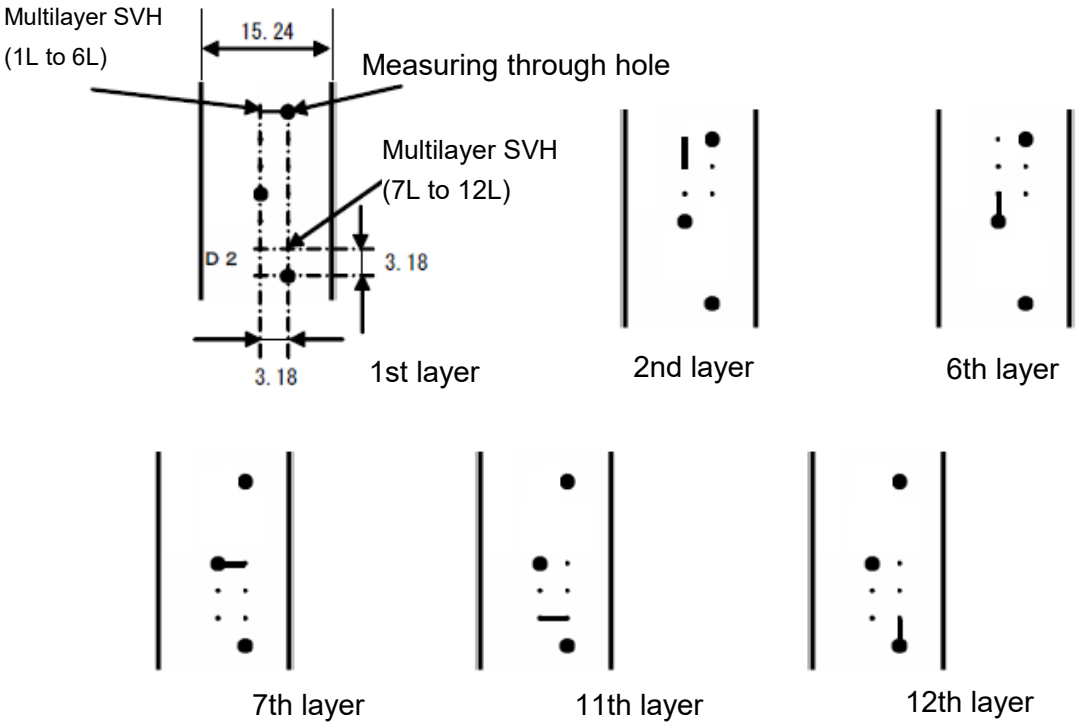
b) Test coupons K2 and L2 (which are equivalent to the coupons K and L, respectively, of Appendix B of JAXA-QTS-2140) shall be added (see Figure 6).

Refer to the notes of Figure B-9, Appendix B of JAXA-QTS-2140 when the test coupons K2 or L2 are selected.



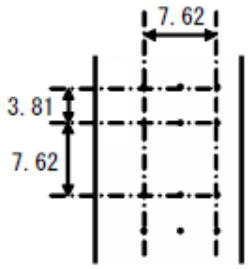
The figure is an example of multilayer IVH with 10 layers which connects 2nd layer through 11th layer.
Lands with the same diameter as the IVH shall be provided on the external layers.

Figure 4. Test Coupons D2 and G2 for Multilayer IVH



The figure is an example of multilayer SVH with 6 layers + 6 layers

Figure 5. Test Coupons D2 and G2 for Multilayer SVH

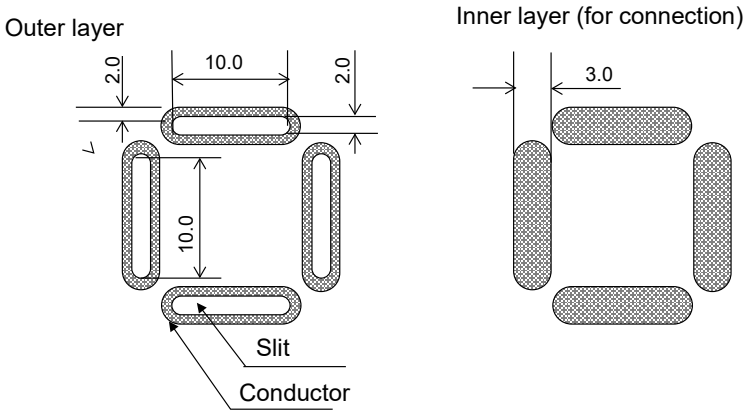


On the test coupons K2 and L2, land shall only be placed on the layer which consists of IVH or SVH forming IVH and/or SVH by creating through hole at the end points.

Figure 6. Test Coupons K2 and L2

4.5.4 Sideplating

For the structure with sideplating, the test coupon O shall be tested as follows. (See Figure 7)



Test coupon O shall be placed on the products with sideplating.

Figure 7. Test Coupon O

4.5.4.1 Externals, Dimensions, Marking and Others

When printed circuit boards are tested as specified in paragraph B.4.4.2.1, Appendix B of JAXA-QTS-2140, the sideplating shall not exhibit any cracks, lifting, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land.

4.5.4.2 Thermal Stress

When tested as specified in paragraph B.4.4.8.4, Appendix B of JAXA-QTS-2140, printed wiring boards shall not exhibit any measling, cracks, separation between plating and inner-layer conductors, or between plating and the board, blistering or delamination.

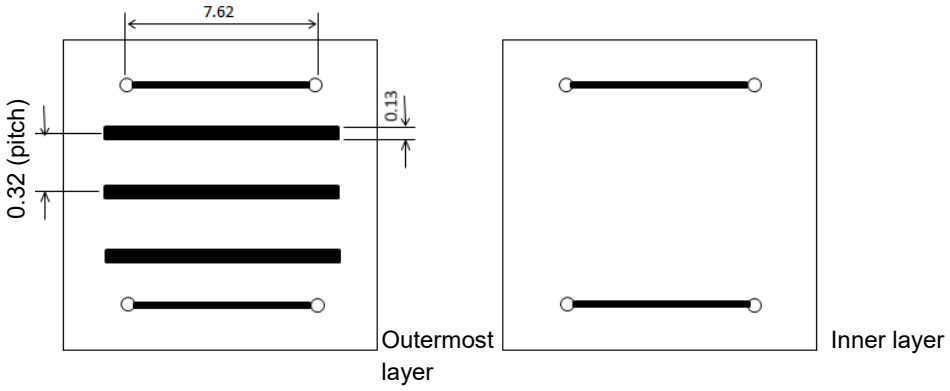
Resin recession at the outer surface of the sideplating of the board shall be permitted, provided the maximum depth as measured from the sideplating wall does not exceed

80μm, and the resin recession along the line of the sideplating does not exceed 40 percent of the cumulative base material thickness on the sideplating being evaluated

4.5.5 Metal Foil Printed Wiring Boards

The external visual, plating adhesion and overhang for metal foil printed wiring boards (copper foil thickness: 105Ωm) shall be performed using test coupon C1 (see Figure 8).

Test coupon C



Test coupon C1 (for metal foil printed wiring boards)

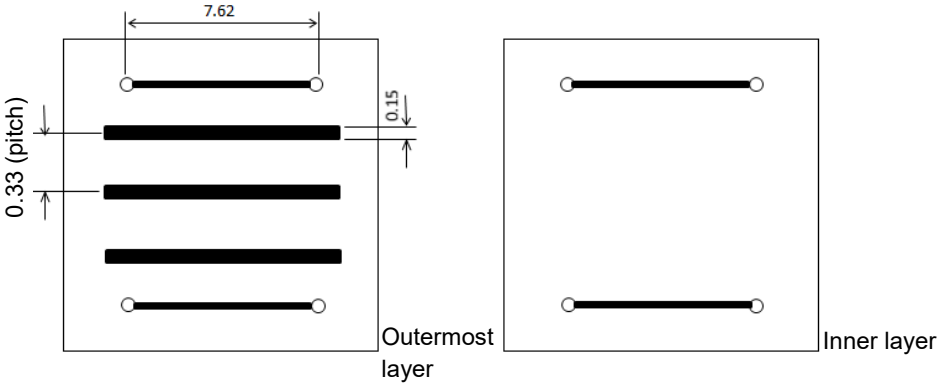


Figure 8. Test Coupons C and C1

5. PREPARATION FOR DELIVERY

The products shall be prepared for delivery as follows and as specified in Paragraph 5 of JAXA-QTS-2140 and as follows.

5.1 Packaging

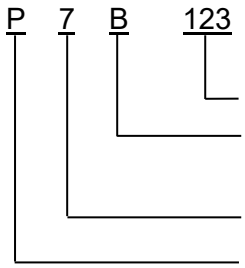
The printed wiring boards shall be packaged with a material that will not affect the insulation area and conductors of the printed wiring board, and in an appropriate manner that will protect the products from any damage during handling and transportation. The product shall be placed in an aluminum bag, vacuumed and sealed with nitrogen gas, and packed in a cardboard box with cushion.

5.2 Marking on Package

The following items shall be marked on the package.

a) Part name
b) Part number
c) Applicable specification number
d) Manufactured date and production lot number

Example: production lot number



The serial number in 3-digit number
Month manufactured (January:A, February:B, March:C· · · .
October:K, November:L, December:M, “I” shall not be used.)
Last digit of year manufactured (e.g. 7 for the year 2017)
Abbreviation for OKI Circuit Technology Co., Ltd.

e) Purchaser’s name
f) Manufacturer’s name (supplier’s name)
g) Unit number in the package
h) Date of inspection
i) Inspection result

6. NOTES

As specified in Paragraph 6 of JAXA-QTS-2140.