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18 March 2020

POWER MOSFET, N-CHANNEL,
RADIATION HARDENED,
HIGH RELIABILITY, SPACE USE,
DETAIL SPECIFICATION FOR

JAXA R 2SK1A01

Prepared and Established by Fuji Electric Co., Ltd.
Issued by Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

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Revision Log

Rev.	Date	Description
----	29 March 2012	Original
A	18 March 2020	▪ Cover: Changed the corporate name. ▪ Paragraph 3.2.1: Added marking for inspection lot identification code and serial number. ▪ Modified the wording in each paragraph in the document. ▪ Paragraph 6.1: Added Terms and definitions. ▪ Table 1b Group A inspection (A-3b): Corrected test condition error of gfs from "$V_{GS}=25V$" to "$V_{DS}=25V$". ▪ Table 2a Group B inspection (B-3g) and Table 2b Group B inspection (B-6g): Corrected test condition error of Bond strength from "condition A" to "condition D".

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**POWER MOSFET, N-CHANNEL, RADIATION HARDENED,
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JAXA R 2SK1A01

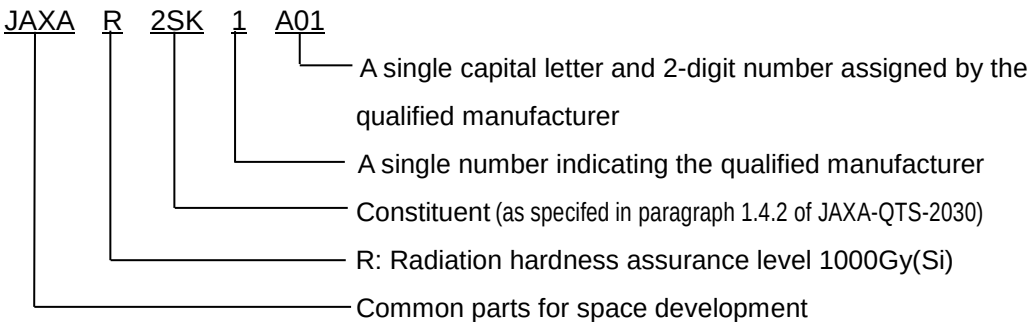
1 GENERAL

This specification establishes the detailed requirements for space use, high reliability, N channel power MOSFET (600V for TO-257 package types) used for electronic equipment installed on spacecrafts. The products specified in this specification are as follows.

1.1 Part Number

The part numbers for the products are provided in accordance with JAXA-QTS-2030 and shall be shown as the following example.

(Example)



The part numbers for the products covered by this specification are assigned as follows:

JAXA R 2SK1A01

1.2 Absolute Maximum Ratings

The absolute maximum ratings of the products specified in this specification are as follows.

Unless otherwise specified, T_A is +25°C.

Part No.	V_{DS} (V)	I_D (A)	$I_{D(pulse)}$ (A)	V_{GS} (V)	P_D $T_C=25^\circ\text{C}$ (W)	P_D $T_A=25^\circ\text{C}$ (W)	$T_{ch}^{(1)}$ (°C)	T_{stg} (°C)	$R_{th(ch-c)}$ (°C/W)	$R_{th(ch-a)}$ (°C/W)	SOA
JAXA R 2SK1A01	600	3.9	15.6	±20	70 Fig.5	2.55 Fig.6	150	-55 to 150	1.67	49.0	Fig.7

Note⁽¹⁾ The channel temperature T_{ch} is given by the following equations:

$$T_{ch}=T_C + R_{th(ch-c)} \times P_D$$

$$T_{ch}=T_A + R_{th(ch-a)} \times P_D$$

Where T_C : Case temperature (°C)

T_A : Ambient temperature (°C)

$R_{th(ch-c)}$: Thermal resistance between junction and case (°C/W)

$R_{th(ch-a)}$: Thermal resistance between channel and ambient (°C/W)

P_D : Power dissipation (W)

1.3 Primary Electrical Characteristics

The primary electrical characteristics of the products specified in this specification are as follows. Unless otherwise specified, T_A is +25°C.

Electrical Characteristics (1/3)

Part No.	$V_{(BR)DSS}$ (V)	I_{DSS} (μ A)	I_{GSS} (nA)	$V_{GS(th)}$ (V)	$R_{DS(on)}^{(1)}$ (Ω)	$gfs^{(1)}$ (S)	E_{AS} (mJ)
	$I_D=1mA$ $V_{GS}=0V$	$V_{DS}=480V$ $V_{GS}=0V$	$V_{GS}=\pm 20V$ $V_{DS}=0V$	$I_D=1mA$ $V_{DS}=V_{GS}$	$I_D=1.95A$ $V_{GS}=12V$	$I_D=1.95A$ $V_{DS}=25V$	$I_D=3.9A$ $V_{DD}=48V$, $V_{GS}=12V$
	Min	Max	Max	Min-Max	Max	Min	Max
JAXA R 2SK1A01	600	10	± 100	2.5-4.5	1.9	2.5	122

Note⁽¹⁾ Pulse test: Pulse width $\leq 1ms$, Duty cycle $\leq 2\%$

Electrical Characteristics (2/3)

Part No.	Q_{GS} (nC)	Q_{GD} (nC)	Q_G (nC)	$t_{d(on)}$ (ns)	t_r (ns)	$t_{d(off)}$ (ns)	t_f (ns)
	$V_{DS}=300V$, $I_D=3.9A$, $V_{GS}=12V$			$V_{DD}=300V$, $I_D=3.9A$, $V_{GS}=12V$, $R_G=10\Omega$			
	Max	Max	Max	Max	Max	Max	Max
JAXA R 2SK1A01	14	14	48	55	10	100	15

Electrical Characteristics (3/3)

(Body Diode Characteristics)

Part No.	$V_{SD}^{(1)}$ (V)	t_{rr} (ns)	Q_{rr} (μ C)
	$I_F=3.9A$ $V_{GS}=0V$	$I_F=3.9A$, $V_{GS}=0V$, $-di/dt=100A/\mu s$, $T_{ch}=25^\circ C$	
	Max	Typ	Typ
JAXA R 2SK1A01	1.6	800	11

Note⁽¹⁾ Pulse test: Pulse width $\leq 1ms$, Duty cycle $\leq 2\%$

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1.4 Radiation Hardness

The radiation hardness of the products specified in this specification is as follows.

Symbol	Radiation hardness assurance level
R	1000 Gy(Si) { 1×10^5 rad(Si)}
	(Dose Rate 36Gy(Si)/ h to 360Gy(Si)/ h)

2 APPLICABLE DOCUMENTS

The latest issues of documents listed below at the time of contract award or application form a part of this specification the extent specified herein.

- a) JAXA-QTS-2030 Semiconductor Devices, High Reliability, Space Use, General Specification for
- b) MIL-STD-750 Test Methods Standard for Semiconductor Devices

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3 REQUIREMENTS

3.1 Design and Construction

The design and construction of the products shall meet the requirements specified in this paragraph and paragraph 3.3 of JAXA-QTS-2030.

3.1.1 Package Configuration and Lead Connection

The package configuration and lead connection shall meet the requirements specified in Figure 1.

3.1.2 Lead Materials and Finish

The leads shall be made of Fe-Ni (Ni-Au plating) covered OCF (Oxygen-Free Copper) and plated with Au as specified in the paragraph 3.3.7 c) 2) 2.3) or with Pb-Sn solder dipping as specified in the paragraph 3.3.7 c) 2) 2.1) of JAXA-QTS-2030.

3.1.3 Electrical Characteristics

The electrical characteristics shall meet the requirements specified in Tables 1a and 1b.

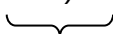
3.2 Marking

The marking shall be in accordance with paragraph 3.4 of JAXA-QTS-2030, and Figure 2.

3.2.1 Marking for Inspection Lot Identification Code and Serial Number

The marking for inspection lot identification code and serial number shall be as follows.

Example:

19	01	001
a)	b)	c)
		
Inspection lot identification code		Serial number

- a) The last two digit number indicating the year the inspection started
- b) The two digit number indicating the week of sealing for the first inspection subplot (production lot) of each inspection lot. The week number is counted from the first week of January of the year.
- c) Unique three-digit number from 001 to 999 consecutively assigned for each product within the inspection lot

3.3 Certification

The requirements for the products to be certified shall be in accordance with paragraph 3.1 of JAXA-QTS-2030

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4 QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The general requirements shall be in accordance with paragraph 4.1 of JAXA-QTS-2030.

4.2 Incoming Materials Control

The incoming materials control shall be in accordance with paragraph 4.2 of JAXA-QTS-2030.

4.3 Manufacturing Process Control

The manufacturing process control shall be in accordance with paragraph 4.3 of JAXA-QTS-2030.

4.4 In-process Inspection

The in-process inspection shall be in accordance with paragraph 4.5 of JAXA-QTS-2030.

4.5 Screening

The screening shall be in accordance with paragraph 4.7 of JAXA-QTS-2030. The electrical characteristics to be measured, test conditions and delta limits shall be as follows.

4.5.1 Electrical Characteristics to be Measured

The following parameters shall be measured during the interim and final electrical characteristics tests for screening.

(1) Interim electrical characteristic tests

$T_A = +25^\circ\text{C}$

Measuring item	$V_{(BR)DSS}$ (V)	I_{DSS} (μA)	I_{GSS} (nA)	$V_{GS(th)}$ (V)	$R_{DS(on)}^{(1)}$ (Ω)	$gfs^{(1)}$ (S)	$V_{SD}^{(1)}$ (V)
MIL-STD-750 Test Method No.	3407	3413	3411	3404	3421	3475	---
Test conditions	Bias Condition C $I_D = 1\text{mA}$ $V_{GS} = 0\text{V}$	Bias Condition C $V_{DS} = 480\text{V}$ $V_{GS} = 0\text{V}$	Bias Condition C $V_{GS} = \pm 20\text{V}$ $V_{DS} = 0\text{V}$	$I_D = 1\text{mA}$ $V_{DS} = V_{GS}$	$I_D = 1.95\text{A}$ $V_{GS} = 12\text{V}$	$I_D = 1.95\text{A}$ $V_{DS} = 25\text{V}$	$I_F = 3.9\text{A}$ $V_{GS} = 0\text{V}$
	Min	Max	Max	Min-Max	Max	Min	Max
JAXA R 2SK1A01	600	10	± 100	2.5-4.5	1.9	2.5	1.6

Note⁽¹⁾ Pulse test: Pulse width $\leq 1\text{ms}$, Duty cycle $\leq 2\%$

(2) Final electrical characteristics test: As specified in the subgroups 1, 2, and 3 of Tables 1a and 1b.

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4.5.2 Test Conditions

The conditions of gate stress test, avalanche energy test, temperature cycling test, reverse bias burn-in test and burn-in test for screening test shall be as follows.

(Gate stress test is performed as part of In-process inspection.)

Gate stress test: $V_{GS}=35V$, $t=1ms$, $T_A=25^{\circ}C$

Single pulse avalanche energy (E_{AS}) test: $I_{D(pulse)} = \text{rated } I_D$, $V_{DD}=48V$, $V_{GS}=12V$

Initial $T_C = +25_{-5}^{+10}^{\circ}C$

$$L(mH) = \left[\frac{2E_{AS}}{(I_D)^2} \right] \left[\frac{BV_{DSS} - V_{DD}}{BV_{DSS}} \right] \quad \bullet \bullet \text{ Equation (1)}$$

Temperature cycling test: Condition G, 20 cycles

Reverse bias burn-in test (GS): $T_A=150^{\circ}C$, $V_{GS}=16V$
 $V_{DS}=0V$, 48hr

Burn-in test (DS): $T_A=150^{\circ}C$, $V_{DS}=80\%$ of rated V_{DS}
 $V_{GS}=0V$, 240hr

4.5.3 Delta Limits

The delta limits for reverse bias burn-in test and burn-in test shall be as follows.

$$\Delta I_{GSS} \leq |20nA|$$

$$\Delta I_{DSS} \leq |10\mu A|$$

$$\Delta R_{DS(on)} \leq |20\%|$$

$$\Delta V_{GS(th)} \leq |20\%|$$

4.6 Qualification Test and Quality Conformance Inspection

The qualification test and the quality conformance inspection shall be in accordance with paragraphs 4.6 and 4.8 of JAXA-QTS-2030. External dimensions, electrical characteristics, test conditions and limits shall be as specified in Figures 1, 3, Tables 1, 2, 3, 4 and 5.

4.6.1 Electrostatic Discharge Sensitivity Test

Electrostatic discharge sensitivity test in the qualification test shall be performed with the following lead combination:

Gate and Source

4.6.2 Radiation Hardness Test

Radiation test (TID: Total Dose Irradiation) level, electrical characteristics, test conditions and limits in the qualification tests and the quality conformance inspections shall be as specified in Table 5. The bias shall be maintained during the irradiation and post-irradiation electrical characteristics test. The post-irradiation electrical characteristics

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test shall be performed within 24 hours after the completion of irradiation.

4.7 Change of Tests and Inspections

No change has been made to any test or inspection specified in appendixes A, B or C of JAXA-QTS -2030.

4.8 Shipment after Long-term Storage

Shipment of the products stored at the manufacturer's site for 24 months or longer shall be in accordance with paragraph 4.9.1 of JAXA-QTS-2030.

5 PREPARATION FOR DELIVERY

Preparation for delivery shall be in accordance with Section 5 of JAXA-QTS-2030.

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6 NOTES

6.1 Terms and Definitions

The terms and definitions used herein shall be in accordance with paragraph 1.2 of JAXA-QTS-2030 and as follows.

6.2 Notes for Purchasers

The precautions to be taken by the purchaser shall be in accordance with paragraph 6.2 of JAXA-QTS-2030 and as follows.

6.2.1 Handling Instructions

The products specified in this specification contain thin oxide films and can be damaged due to electrostatic discharge (ESD). ESD protection measures shall be implemented to avoid ESD between the gate and source and between the gate and drain during transportation and other handling environments.

6.2.2 Beryllium Warning

The products of TO-257 package contain beryllium. Disintegration or chemical processing of the products that may produce dusts or fumes shall be prohibited. Disposition of the products shall be performed in accordance with applicable regulations.

Table 1a. Group A Inspection ⁽¹⁾

Gr.No	MIL-STD-750			JAXA R 2SK1A01
Sub	Test Item	Method		
A -1 Static Characteristics (T _A =25°C)			Sample Size	LTPD 3
-1a	Breakdown Voltage Drain to Source V _{DSS}	3407	Conditions	Bias Condition C I _D =1mA , V _{GS} =0V
			Limits	min 600V DC
-1b	Gate Current I _{GSS}	3411	Conditions	Bias Condition C V _{GS} =±20V , V _{DS} =0V
			Limits	max ±100nA DC
-1c	Drain Current I _{DSS}	3413	Conditions	Bias Condition C V _{DS} =480V , V _{GS} =0V
			Limits	max 10μA DC
-1d	Gate to Source Voltage (Threshold) V _{GS(th)}	3404	Conditions	Bias Condition C V _{GS} =V _{DS} , I _D =1mA
			Limits	2.5 - 4.5V DC
-1e	Static Drain to Source On-State Resistance R _{DS(on)}	3421	Conditions	Pulse Test ⁽²⁾ , V _{GS} =12V
			Limits	I _D 1.95A max 1.9Ω
-1f	Forward Transconductance g _{fs}	3475	Conditions	Pulse Test ⁽²⁾ , V _{DS} =25V
			Limits	I _D 1.95A min 2.5S
-1g	Forward Voltage V _{SD}	---	Conditions	Pulse Test ⁽²⁾ , V _{GS} =0V
			Limits	I _D 3.9A max 1.6V DC
A -2 Static Characteristics (T _A =125°C)			Sample Size	LTPD 5
-2a	Gate Current I _{GSS} (125°C)	3411	Conditions	Bias Condition C V _{GS} =±20V , V _{DS} =0V
			Limits	max ±100nA DC
-2b	Drain Current I _{DSS} (125°C)	3413	Conditions	Bias Condition C V _{DS} =480V , V _{GS} =0V
			Limits	max 25μA DC
-2c	Gate to Source Voltage (Threshold) V _{GS(th)} (125°C)	3404	Conditions	Bias Condition C V _{GS} =V _{DS} , I _D =1mA
			Limits	min 1.5V DC
-2d	Static Drain to Source On-State Resistance R _{DS(on)} (125°C)	3421	Conditions	Pulse Test ⁽²⁾ , V _{GS} =12V
			Limits	I _D 1.95A max 3.3Ω

Notes ⁽¹⁾ The same sample may be used for all subgroups.

⁽²⁾ Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

Table 1b. Group A Inspection ⁽¹⁾

Gr.No	MIL-STD-750			JAXA R 2SK1A01
Sub	Test Item	Method		
A -3	Static Characteristics (T_A=-55°C)		Sample Size	LTPD 5
-3a	Gate to Source Voltage (Threshold) V _{GS(th)} (-55°C)	3404	Conditions	Bias Condition C V _{GS} =V _{DS} , I _D =1mA
			Limits	max 5.0V DC
-3b	Forward Transconductance g _{fs} (-55°C)	3475	Conditions	Pulse Test ⁽²⁾ , V _{DS} =25V
			Limits	1.95A min 3.0S
A -4	Dynamic Characteristics (T_A=25°C)		Sample Size	LTPD 3
	Switching Time Test (1) Turn-on delay time t _{d(on)} Rise time: t _r (2) Turn-off delay time t _{d(off)} Fall time: t _f	3472	Conditions	Test circuit and waveform shall be as specified in Figure 3.
			Limits	I _D 3.9A
			t _{d(on)}	max
			t _r	55ns
			t _{d(off)}	10ns
			t _f	100ns
			t _f	15ns
A -6a	Safe Operating Area Test⁽³⁾		Sample Size	LTPD 5
-6b	End-Point Electrical Measurements	3474	Conditions	---
		---	Conditions	Same as Gr.A-1
A -7	Other Characteristics (T_A=25°C)⁽⁴⁾		Sample Size	LTPD 10
-7a	Gate Charge (1) Gate Charge: Q _g (2) Gate to Drain Charge: Q _{gd} (3) Gate to Source Charge: Q _{gs}	3471	Conditions	V _{GS} =12V V _{DS} =300V
			Limits	I _D 3.9A
			Q _g	max
			Q _{gd}	48nC
			Q _{gs}	14nC
-7b	Reverse Recovery Characteristics (1) T _{rr} (2) Q _{rr}	3473	Conditions	I _F = I _D 3.9A V _{GS} =0V -di/dt=100A/μs
			Limits	max
			T _{rr}	1200ns
			Q _{rr}	16.5μs

Notes⁽¹⁾ The same sample may be used for all subgroups.

⁽²⁾ Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%

⁽³⁾ The samples used for subgroups A-1, A-2, and A-3 tests shall be used.

⁽⁴⁾ The samples used for subgroups A-6 tests shall be used.

Table 2a. Group B Inspection

Gr.No	MIL-STD-750			JAXA R 2SK1A01
Sub	Test Item	Method		
B -1	External Dimensions⁽¹⁾		Sample	Level I ⁽²⁾ 3p
			Size	Level II ⁽²⁾ 3p
		2066	Conditions	See Fig. 1
B -2	Resistance to Solvents⁽³⁾ ⁽⁴⁾		Sample	Level I 3p
			Size	Level II 3p
		1022	Conditions	Solvent a, b, c
B -3b	Temperature Cycling (Air to Air)		Sample	Level I 6p
			Size	Level II 6p
		1051	Conditions	-55 ⁺⁰ ₋₅ °C ↔ 25 ⁺¹⁰ ₋₅ °C ↔ 150 ⁺⁵ ₋₀ °C 100 cycles
-3c	Surge Test (1) Gate Shock	4066	Conditions	V _{GS} =35V
		4066	Conditions	V _{DS} =48V, L= See paragraph 4.5.2 Equation (1)
				I _{D(pulse)} 3.9A
-3d	Hermetic Seal (1) Fine	1071	Conditions	Condition H
			Limits	max 1×10 ⁻³ Pa·cm ³ /s
		1071	Conditions	Condition C
-3e	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1
-3f	Decap-Internal Visual and mechanical inspection	2075 2071	Conditions	---
-3g	Bond Strength	2037	Conditions	Condition D
			Limits	Gate Wire >90gf
				Source Wire >90gf
-3h	SEM⁽¹⁾	2077	Conditions	---
-3i	Die Shear		Sample	Level I 3p
			Size	Level II 3p
		2017	Conditions	---
			Limits	min 2.5kgf
B -4	Solderability⁽³⁾ ⁽⁴⁾		Sample	Level I, 6 leads ⁽⁵⁾
			Size	Level II, 6 leads ⁽⁵⁾
		2026	Conditions	---

Notes ⁽¹⁾ The test may be performed using the samples prior to inspection lot formation.

⁽²⁾ Level I and Level II shall be applicable to the qualification test and the quality conformance inspection, respectively. (See paragraphs C.3.2 and C.3.3 of JAXA-QTS-2030)

⁽³⁾ Electrical reject products from the same inspection lot may be used.

⁽⁴⁾ When electrical reject products are used, the samples shall be exposed to the same thermal environments as the certified samples experience in all thermal tests required as part of the screening test.

⁽⁵⁾ This test shall be performed for each 3 leads from 2 devices.

Table 2b. Group B Inspection

Gr.No	MIL-STD-750			JAXA R 2SK1A01
	Sub	Test Item	Method	
B -5a		Intermittent Operation Life	Sample Size	Level I LTPD 10 Level II 12p
			1042 Conditions	Condition D, 2000 cycles ⁽¹⁾ Minimum On time: 30 seconds
-5b		End-Point Electrical Measurements	---	Conditions Same as Gr.A-1
B -6c		Accelerated Steady-state Gate Stress (High Temp. GS)	Sample Size	Level I LTPD 10 Level II 12p
			1042 Conditions	$V_{GS}=20V, T_A=150^{\circ}C, 48hr$ or $V_{GS}=20V, T_A=175^{\circ}C, 24hr$
-6d		End-Point Electrical Measurements	---	Conditions Same as Gr.A-1
-6e		Accelerated Steady-state Reverse Bias (High Temp. DS)	1042 Conditions	$V_{DS}=600V, T_A=150^{\circ}C, 240hr$ or $T_A=175^{\circ}C, 120hr$
-6f		End-Point Electrical Measurements	---	Conditions Same as Gr.A-1
-6g		Bond Strength	Sample Size	20 wires
			2037 Conditions	Condition D
			Limits	Gate Wire >90gf Source Wire >90gf
B -7		Thermal Impedance $Z_{th(ch-c)}(\Delta V_{SD})$	Sample Size	Level I LTPD 10 Level II 8p
			3161 Conditions	$T_A=25^{\circ}C$
			Limits	max 1.67°C/W

Note⁽¹⁾ If the samples are also used for "Intermittent operating life test" of C1-1 in the Group C test, the test shall be performed up to 6000 cycles.

Table 3. Group C Inspection

Gr.No	MIL-STD-750			JAXA R 2SK1A01
Sub	Test Item	Method		
C 1-1a	Intermittent Operation Life		Sample Size	Level I LTPD 10 Level II LTPD 10
		1042	Conditions	Condition D, 6000 cycles ⁽¹⁾ Minimum On time: 30 seconds
		---	Conditions	Same as Gr.A-1
1-1b	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1
C 1-2a	Steady-state Bias Life Test (High Temp GS) ⁽²⁾		Sample Size	Level I LTPD 5 Level II NA
		1042	Conditions	V _{GS} =16V T _A =150°C, 1000hr
		---	Conditions	Same as Gr.A-1
1-2b	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1
1-2c	Steady-state Bias Life Test (High Temp. DS) ⁽²⁾	1042	Conditions	V _{DS} =480V T _A =150°C, 1000hr
1-2d	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1
C -2a	Temperature Cycling		Sample Size	Level I 12p Level II NA
		1051	Conditions	-55 ⁺⁰ ₋₅ °C↔25 ⁺¹⁰ ₋₅ °C↔150 ⁺⁵ ₋₀ °C 500 cycles
		1071	Conditions	Condition H
-2b	Hermetic Seal (1) Fine		Limits	max 1×10 ⁻³ Pa·cm ³ /s
		1071	Conditions	Condition C
		---	Conditions	Same as Gr.A-1
-2c	End-Point Electrical Measurements ⁽³⁾		Sample Size	Level I LTPD 10 Level II 8p
		3161	Conditions	T _A =25°C
			Limits	max 1.67°C/W
C -4a	Safe Operating Area Test ⁽⁶⁾		Sample Size	Level I LTPD 10 Level II LTPD 10
		3474	Conditions	---
		---	Conditions	Same as Gr.A-1
-4b	End-Point Electrical Measurements ⁽⁶⁾		Sample Size	Level I 3p Level II NA
		1020	Conditions	V _{GS} ±500V
		---	Conditions	Same as Gr.A-1
C -6a	Electric Discharge Sensitivity Classification	1020	Conditions	V _{GS} ±500V
-6b	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1

Notes⁽¹⁾ For the quality conformance inspection, the cycles may be reduced to 2000 cycles as a minimum.

⁽²⁾ The legibility of the marking shall not apply.

⁽³⁾ This test may be conducted prior to the hermetic seal.

⁽⁴⁾ Thermal impedance curve shall be obtained during the qualification test.

⁽⁵⁾ This test may be exempted if performed in the Group B test.

⁽⁶⁾ This test may be exempted if performed in the Group A test.

Table 4a. Group D Inspection

Gr.No	MIL-STD-750			JAXA R 2SK1A01	
	Sub	Test Item			Method
D-1a	Thermal Shock (Glass Strain)		Sample Size	Level I LTPD 15 Level II LTPD 15	
		1056	Conditions	Condition B, 15 cycles	
	-1b	Temperature Cycling	1051	Conditions	-55 ⁺⁰ ₋₅ °C↔25 ⁺¹⁰ ₋₅ °C↔150 ⁺⁵ ₋₀ °C 45 cycles
	-1c	Lead Strength	2036	Conditions	Condition A 1.5kg, 30s
	-1d	Moisture Resistance	1021	Conditions	(MIL-STD-202, Method 106)
	-1e	Hermetic Seal (1) Fine	1071	Conditions	Condition H
				Limits	max 1×10 ⁻³ Pa·cm ³ /s
		(2) Gross	1071	Conditions	Condition C
	-1f	Visual Inspection	1051 1021	Conditions	---
	-1g	End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1
D-2a	Shock ⁽¹⁾		Sample Size	Level I LTPD 15 Level II LTPD 15	
		2016	Conditions	No Operating, 14700m/s ² (1500G) 5 blows in each orientation, X ₁ , Y ₁ , Y ₂ and Z ₁ The orientation is shown in Figure 4.	
	-2b	Vibration, Variable Frequency ⁽¹⁾	2056	Conditions	100 to 2000 Hz, 4min 196 m/s ² (20G) 4 times in each orientation, X, Y, and Z
	-2c	Constant Acceleration ⁽¹⁾	2006	Conditions	98100m/s ² (10000G) X ₁ , Y ₁ , Y ₂ and Z ₁ orientation The orientation is shown in Figure 4.
	-2d	Hermetic Seal ⁽¹⁾ (1) Fine	1071	Conditions	Condition H
				Limits	max 1×10 ⁻³ Pa·cm ³ /s
		(2) Gross	1071	Conditions	Condition C
	-2e	End-Point Electrical Measurements ⁽¹⁾	---	Conditions	Same as Gr.A-1
D-3a	Salt Atmosphere ⁽²⁾		Sample Size	Level I LTPD 15 Level II LTPD 15	
		1041	Conditions	35°C, 24hr Rate of salt deposit=10 to 50g/m ² /24hr	
	-3b	Visual Inspection	1051 1021	Conditions	---

Notes ⁽¹⁾ Samples used for subgroup 1 may be used.

⁽²⁾ Electrical reject products from the same inspection lot may be used.

Table 4-b. Group D Inspection

Gr.No	MIL-STD-750				JAXA R 2SK1A01
	Sub	Test Item	Method		
D -4		Barometric Pressure (reduced)	Sample Size		Level I 3p Level II NA
			1001 Conditions		8mmHg, 60sec (minimum) $V_{DS}=600V$, $V_{GS}=0V$
D -5		Internal Water Vapor⁽¹⁾	Sample Size		Level I 3p Level II 3p
			1018 Conditions		---
D -6a		Resistance to Soldering Heat	Sample Size		Level I 3p Level II NA
			2031 Conditions		250°C, 10s
-6b		Visual Inspection	---	Conditions	---
-6c		Hermetic Seal (1) Fine	1071 Conditions		Condition H
			Limits		max $1 \times 10^{-3} \text{Pa-cm}^3/\text{s}$
		(2) Gross	1071 Conditions		Condition C
-6d		End-Point Electrical Measurements	---	Conditions	Same as Gr.A-1

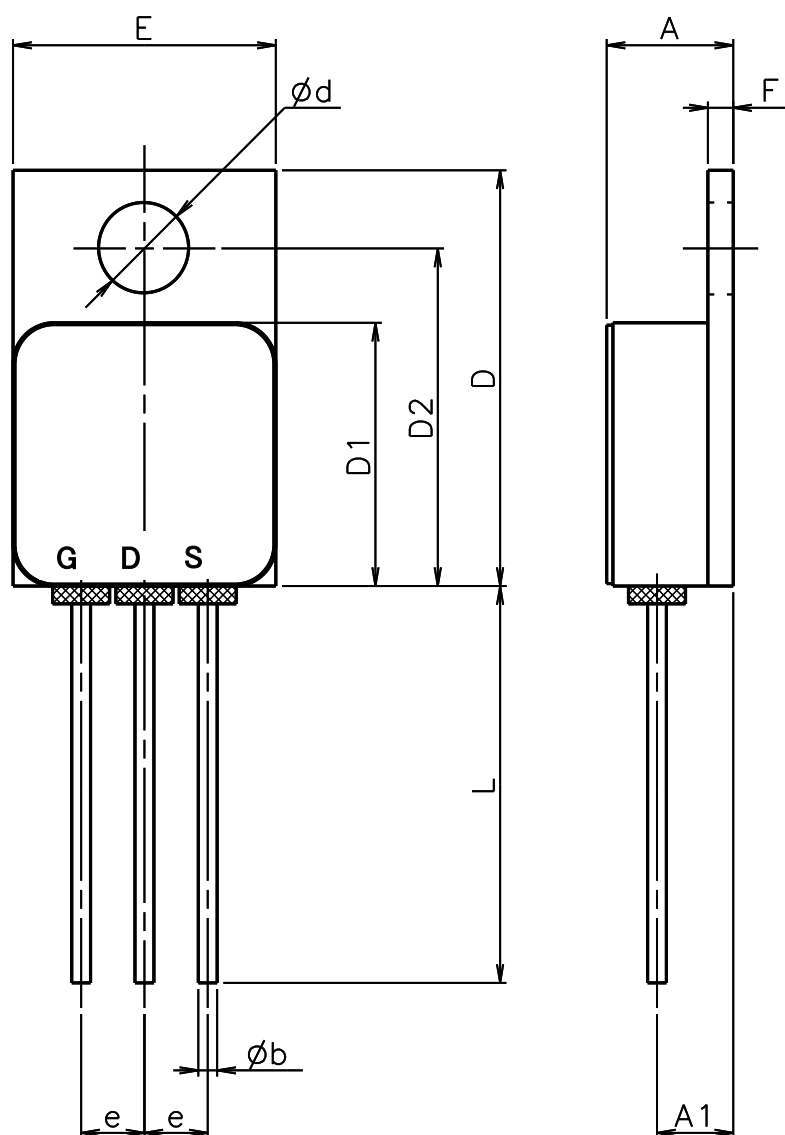
Note⁽¹⁾ Electrical reject products from the same inspection lot may be used.

Table 5. Group E Inspection

Gr.No	MIL-STD-750			JAXA R 2SK1A01
Sub	Test Item	Method		
E -1a	Total Dose Irradiation (TID)		Sample Size	Level I 4p ⁽¹⁾ Level II 4p ⁽¹⁾
		1019	Conditions	Total Dose 1×10 ³ Gy(Si) Dose Rate 36Gy(Si)/h to 360Gy(Si)/h Bias Condition (during irradiation, after irradiation) (a)V _{DS} =0V , V _{GS} =20V (b)V _{DS} =0V , V _{GS} =-20V (c)V _{DS} =480V , V _{GS} =0V
-1b	End-Point Electrical Measurements			Within 24hr after irradiation
(1)	Breakdown Voltage Drain to Source V _{DSS}	3407	Conditions	Bias Condition C I _D =1mA , V _{GS} =0V
			Limits	600V DC
(2)	Gate Current I _{GSS}	3411	Conditions	Bias Condition C V _{GS} =±20V , V _{DS} =0V
			Limits	max ±100nA DC
(3)	Drain Current I _{DSS}	3413	Conditions	Bias Condition C V _{DS} =480V , V _{GS} =0V
			Limits	max 10μA DC
(4)	Gate to Source Voltage (Threshold) V _{GS(th)}	3404	Conditions	Bias Condition C V _{GS} =V _{DS} , I _D =1mA
			Limits	min 1.5V DC ΔV _{GS(th)} max 2.0V
(5)	Static Drain to Source On-State Resistance R _{DS(on)}	3421	Conditions	Pulse Test ⁽²⁾ , V _{GS} =12V I _D
			Limits	1.95A max 1.9Ω

Notes ⁽¹⁾ This test shall be performed for each single wafer lot. When an inspection lot consists of multiple inspection sublots, one inspection subplot may be performed this test.

⁽²⁾ Pulse test: Pulse width ≤ 1ms, Duty cycle ≤ 2%



Symbol	Dimension (mm)	
	Min	Max
A	4.76	5.11
A1	2.92	3.18
ϕb	0.64	0.89
D	16.51	16.76
D1	10.41	10.67
D2	13.39	13.64

Symbol	Dimension (mm)	
	Min	Max
ϕd	3.56	3.81
E	10.41	10.67
e	2.48	2.60
F	0.89	1.14
L	15.24	16.51

Note: All leads are isolated from the case.

Figure 1. Package Configuration and Lead Connection

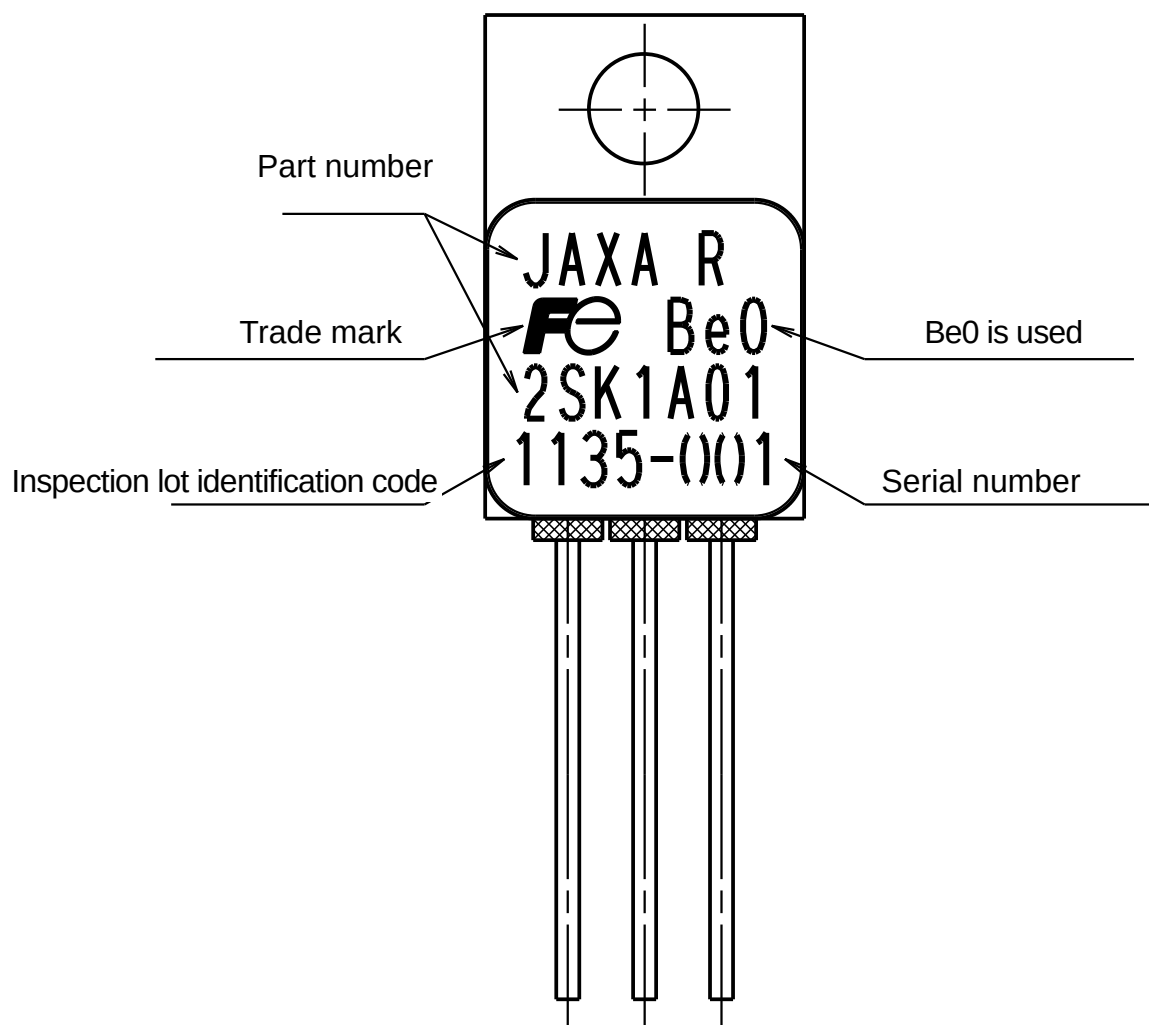


Figure 2. Marking

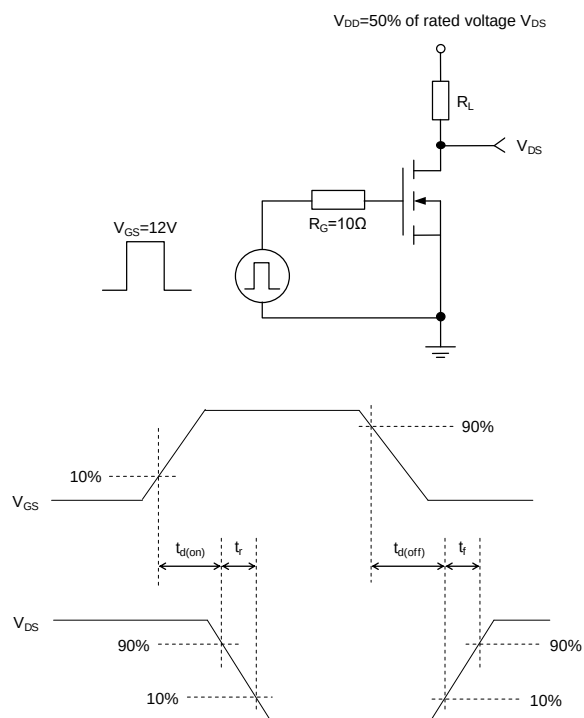


Figure 3. Switching time test circuit and waveforms

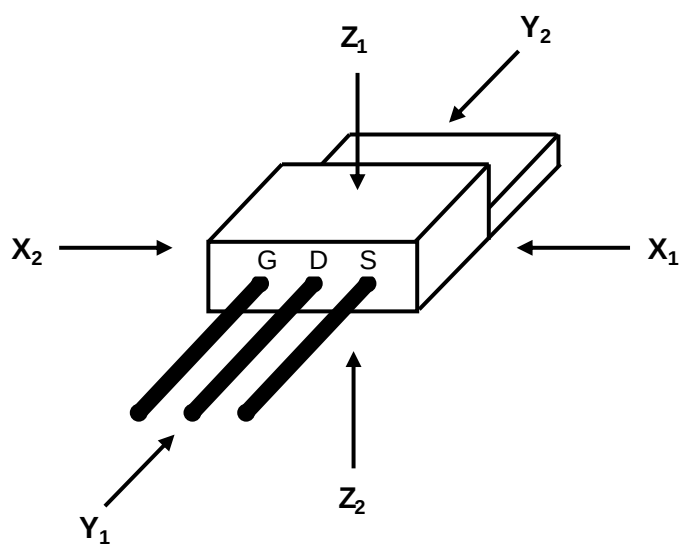


Figure 4. Orientation

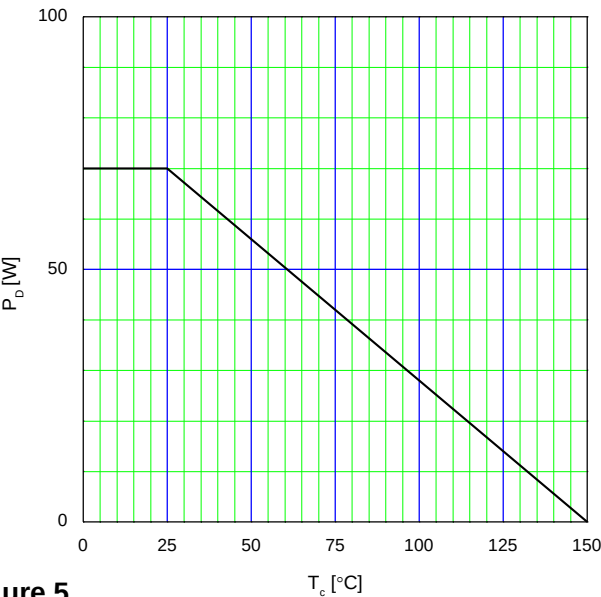


Figure 5.
Allowable power dissipation P_D – Case temperature T_c

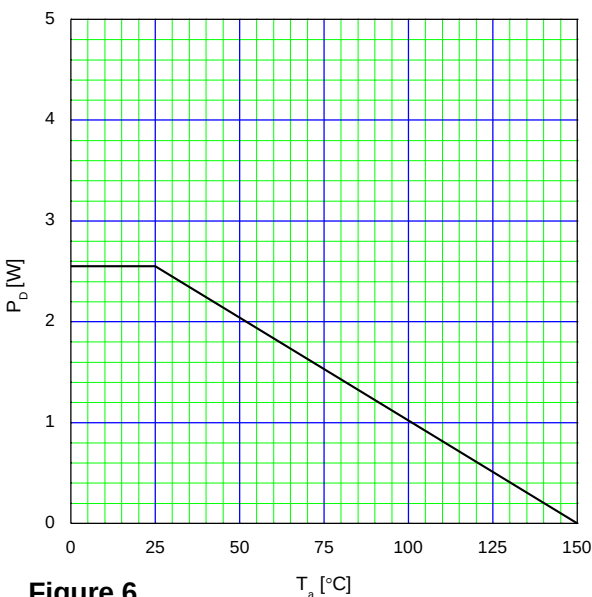


Figure 6.
Allowable power dissipation P_D – Ambient temperature T_a

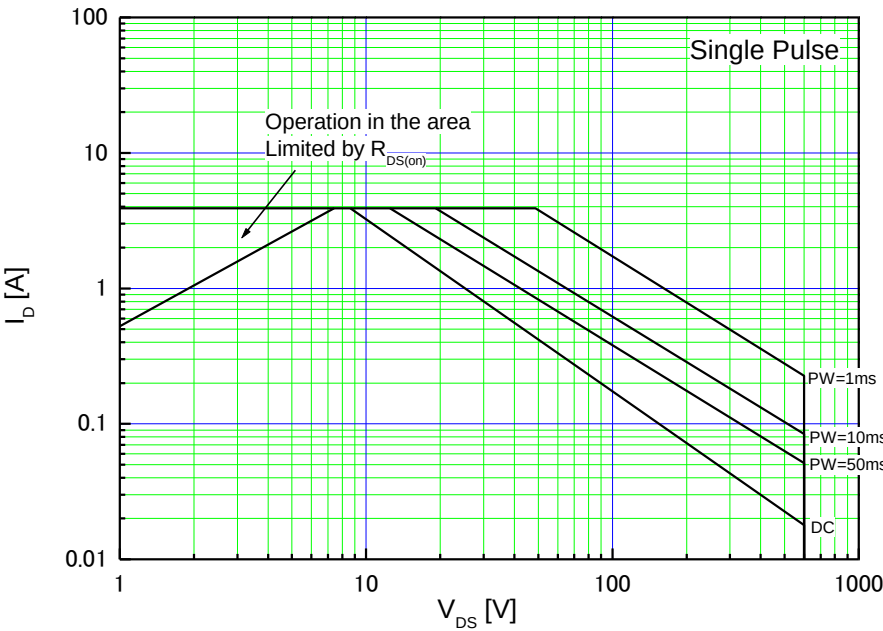


Figure 7. Maximum safe operating area