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INTEGRATED CIRCUITS, HYBRID, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

JAXA
JAPAN AEROSPACE EXPLORATION AGENCY

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: December 24, 2021

Revision Log		
Revision	Date	Description
NC	31 March 2003	Original
A	31 March 2004	Revised to reflect the organizational change from NASDA to JAXA • Changed the Specification identification from NASDA-QTS-2020 to JAXA-QTS-2020 • Changed from NASDA to JAXA in the text.
B	22 June 2007	Revised to reflect the revision of JAXA-QTS-2000 from revision B to revision C • Paragraph 1.3: Changed “NASDA 2020****” to “JAXA 2020****” in the part number definition. Made the same change to the part number in the example of Format F-1. Changed the requirements to cover DC-to-DC converters • Paragraph 3.3.4: Added surface mount semiconductor, sheet transformer and flexible printed wiring board to the elements. Added requirements on tin finish. • Paragraph 3.3.8: Added copper-core, Fe-Ni52 alloy as type C to the lead materials. • Paragraph A.2.2: Added lot evaluation test on semiconductor chips mounted on substrate. • Table C-2 and other places.: Defined frequency for conducting RGA. Added the shock test method for hybrid IC including sheet transformer. Deleted the electrical parameter test and changed the sample size for Group D. • Format E-1: Added design criteria for sheet transformer wiring to the design documents. • Figure G-14: Added “Package configuration DA.” Unification of terminology • Changed from ”HIC” to “Hybrid IC” because HIC is a registered trademark • Changed from “die” to “semiconductor chip.” Other changes to clarify the requirements and to correct inconsistency. • Paragraph 1.3: Deleted paragraph “Reference to detail specification.” Renumbered the subsequent paragraphs. • Paragraph 4.2.1: Deleted paragraph “Requirements for dies.”. Renumbered the subsequent paragraphs. •Paragraph A.2.1.2.1: Deleted paragraph “Verification of Glassivation layer integrity.” Deleted the same item from Table A-1, Lot evaluation test. • Figure G-13: Corrected errors in the drawing of “Package configuration HM.”
C	30 March 2021	Revised to reflect JAXA-QTS-2025. • Paragraph 1.1: Added “design specification” to specify qualification coverage. Furthermore, added definition of Class I hybrid IC and Class II hybrid IC. • Paragraph 1.3: Added part number of Class II hybrid IC.

Revision Log		
Revision	Date	Description
		• Paragraph 1.3.1: Added assign method of individual number and management of assignment list. • Paragraph 1.3.3: Added design specification. • Paragraph 1.3.4: Deleted symbol “B”. Added symbol “D”. Reconsidered note (1) description. • Paragraph 1.3.5: Changed paragraph title and text. Reflected JAXA-QTS-2020B Notice 1. • Paragraph 2.1: Corrected specification title of k) and l). Added n) ASTM F1192, o) JESD57, and p) CAA-2020055. • Paragraph 2.2: Added “limited to JAXA” to a). Corrected specification title of b) and c). Added d) JMR-012. • Paragraph 2.4: Corrected paragraph title. Added preparation of design specification and detail specification. • Paragraph 2.4.4: Corrected paragraph title. Added format of design specification and detail specification. • Paragraph 3.1.1: Corrected description. • Paragraph 3.1.1.2: Added paragraph. Added description of quality assurance level for Class I hybrid IC and Class II hybrid IC. • Paragraphs 3.1.2 and 3.1.3: Corrected description. • Paragraph 3.1.5: Corrected paragraph title. Corrected description. • Paragraphs 3.3, 3.3.1, 3.3.2, 3.3.3, 3.3.3.1 and 3.3.3.2: Corrected description. • Paragraph 3.3.4: Added “Selection of mounted element”. • Paragraphs 3.3.4.1 a), 3.3.4.1 b), 3.3.4.2 a), 3.3.4.2 b), 3.3.4.3, 3.3.4.4, 3.3.4.5, 3.3.5, 3.3.6, 3.3.8 a), 3.3.8 c) 2), 3.3.8 c) 2.1) and 3.3.8 c) 2.2): Corrected description. • Paragraph 3.3.8 c) 2.3): Added paragraph. • Paragraphs 3.4.1, 3.4.1.2, 3.4.1.3 and 3.4.4: Corrected description. • Paragraphs 3.5, 3.5.1 and 3.5.2: Added radiation hardness. • Paragraphs 4.2 and 4.2.1: Corrected description. • Paragraph 4.2.2: Corrected paragraph title and description. • Paragraph 4.3.1 k) Note (1) ii, iii and vi: Corrected description. • Paragraphs 4.3.2, 4.3.2.1 and 4.3.2.3: Added description of Class II. • Paragraphs 4.3.2.1, 4.5, 4.5.1, 4.7 and 4.8: Corrected description. • Paragraph 6.1: Corrected paragraph title. • Paragraphs 6.1 b) 3) and 6.1 i): Corrected description. • Paragraphs from 6.1 s) to 6.1 x): Added terms. • Paragraphs 6.2.1 and 6.3.1: Corrected description. • Paragraph 6.3.1 c): Added paragraph. Changed item name from “d) ~ e)” to “e) ~ f)”. • Figures 1, 2, 3 and 4: Added. • Appendix A: Reconsidered Appendix A as a whole to clarify requirements for “subassembly parts”, in which procured semiconductor chip are assembled

Revision Log		
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		in the firm, and “semi-assembly products of hybrid IC”. • Figure A-1: Added illustration showing from acceptance of semiconductor chip to hybrid IC assembly. • Paragraphs A.1, A.2.1.2, A.2.1.3 and A.2.1.5: Corrected description. • Table A-1: Added table number and title to table of maximum allowable current density. • Paragraph A.2.2: Corrected description. • Paragraph A.2.2.1: Added requirements for sample and sampling of class I and class II. • Paragraph A.2.2.2: Unified terms. • Paragraph A.2.3: Added standards applicable to ESA and JAXA certified semiconductor chip. Corrected paragraph title. • Table A-2: Corrected title as “lot evaluation test at semiconductor chip”. Added requirements for class II. Changed “sample size” to “number of chips for tests”. Integrated LTPD into number. • Table A-2 subgroup 4: Added requirements for “single event test (except for power discrete semiconductor)”, “SEB test (power discrete semiconductor) and “SEGR test (discrete semiconductor)”. • Table A-2 notes: Corrected description. • Table A-3: Corrected title as “lot evaluation test of semiconductor chip subassembly”. Corrected item name. Applied the latest version of applicable documents. Changed from “sample size” to “number of chips for tests”. Integrated LTPD into number. • Table A-3 subgroup 4: Added requirements for “single event test (except for power discrete semiconductor)”, “SEB test (power discrete semiconductor) and “SEGR test (discrete semiconductor)”. • Table A-3 notes: Corrected description. • Table A-4: Corrected title as “lot evaluation test of semiconductor chip of semi-assembly products of hybrid IC”. Corrected item name. Applied the latest version of applicable documents. Changed “sample size” to “number of chips for tests”. Integrated LTPD into number. • Table A-4 subgroup 4: Added requirements for “single event test (except for power discrete semiconductor)”, “SEB test (power discrete semiconductor) and “SEGR test (discrete semiconductor)”. • Table A-4 notes: Corrected description. • Paragraph B.3.2: Corrected description of reselection. • Paragraph B.3.4: Added description that screening record had to be controlled in accordance with quality assurance program. • Table B-1: Added class II hybrid IC to table. Assigned number 6 “serialization” as deleted number. Corrected description of interim electrical parameters and final electrical parameter test. • Table B-1: Deleted note (9) stabilization bake. Reconsidered PDA allowance. • Paragraph C.2.1.1: Corrected errors (steady-state operating life test).

Revision Log		
Revision	Date	Description
		• Paragraph C.3: Classified test into qualification test and quality conformance inspection and added procedures for each test. • Paragraph C.3.2: Added description that “Level I” had to be applied to qualification test. • Paragraph C.3.3: Added description that “level I” had to be applicable to first article and “level II” had to be applicable to previously procured products. • Paragraph C.3.3.2 a) to c): Corrected description. • Paragraph C.3.5: Deleted description of disposition of samples that were subject to destructive test. • Paragraph C.3.5.1 h) to i): Deleted “salt atmosphere”. Added radiation hardness test (single event test, SEB test and SEGR test) and corrected item number. • Paragraph C.3.5.2 h): Added radiograph inspection to non-destructive test. • Paragraph C.3.6.1: Added paragraph “total dose test”. • Paragraph C.3.6.2: Added paragraph “single event test”. • Paragraph C.3.6.3: Added paragraph “SEB test”. • Paragraph C.3.6.4: Added paragraph “SEGR test”. • Table C-1: Added class II. Classified sample size into “level I” and “level II”. Corrected errors of subgroup number (subgroups 10 and 11). • Table C-2: Added class II. Classified number of sample into “level I” and “level II”. Changed name of subgroup 1b) as “internal gas analysis inspection”. Add following test to subgroup 2. Corrected notes. c) Bond strength test 3) Flip-chip 4) Beam lead • Table C-3: Added class II. Classified sample size into “level I” and “level II”. Added resistance to soldering heat test to subgroup 2. Corrected to conduct mechanical shock and constant acceleration tests in succession. Corrected end-point electrical parameter test. Added notes $^{(12)}$ and $^{(13)}$. • Table C-4: Added class II. Classified sample size into “level I” and “level II”. Deleted subgroup 3 a) salt atmosphere test. Deleted group D test subgroup 2. Deleted subgroup 1d) visual inspection. Deleted notes $^{(2)}$ to $^{(6)}$. • Table C-5: Added class II. Classified sample size into “level I” and “level II”. Corrected sample size as number of sample. Added single event test for power semiconductor and that except for power semiconductor. Corrected notes (^{1}) and (^{2}) and added notes (^{6}) to (^{11}). • Appendix E: According to change title to design specification, corrected title of appendix E as “Preparation of Design Specifications”. • Paragraph E.1: Corrected design documents as design specifications. • Paragraph E.2: Corrected description of requirements for design specifications. • Format E1: Deleted formats of design documents and added formats of design specifications. • Paragraph F.3.2: Added quality assurance program plan as applicable

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Revision	Date	Description
		document. • Paragraph F.3.3.1: Corrected description of requirements. • Paragraph F.3.3.1 a) to c): Added following requirements of main rules. a) Mounted element (paragraph 3.3.4) b) Organic and polymeric material (paragraph 3.3.5) c) Mounting materials for substrate, semiconductor chip and passive element chip (paragraph 3.3.6). • Tables F-1 to F-4: Moved to another portions. • Paragraph F.3.3.2: Added description of total dose radiation hardness. • Paragraph F.3.4: Added “c) Manufacturing process control” and “h) Change of test and inspection”. Corrected item number. • Paragraphs F.3.4.1 to F.3.4.5: Corrected description. • Paragraph F.3.4.5.1: Corrected to conduct all interim electrical parameter test at room temperature and to conduct all final electrical parameter test at room / high/ low temperature. • Table F-5 and Figures F-1 to F-11: Deleted. • Paragraph F.3.4.5.2: Deleted table F-5 and figures F-1 to F-11. • Paragraph F.3.4.5.3: Specified class I – specific requirements. • Table F-5: Corrected table F-6 as table F-5. • Paragraph F.3.4.6.2: Corrected electrical parameter test items to be measured and corrected subgroups corresponding to group A test of each test. • Paragraph F.3.4.6.3: Corrected paragraph title and description. • Paragraph F.3.4.6.4: Added total dose test, single event test, SEB test and SEGR test to radiation hardness test. • Paragraph F.3.6: Corrected description. • Format F1: Reconsidered as a whole. • Paragraph G.2 i): Added dual in-line package. • Figure G-3: Added dual in-line package. • Paragraph G.3.1: Added dual in-line package. • Paragraph G.3.3: Added dual in-line package to package configuration. • Paragraph G.3.4: Added package configuration (symbols DB, CA and CB). • Figure G-16: Added package configuration (symbol DB). • Figure G-17: Added package configuration (symbol CA). • Figure G-18: Added package configuration (symbol CB). • Appendix Z: Newly established appendix Z “Procedure after Revision of JAXA-QTS-2020”.

Contents

INTEGRATED CIRCUITS, HYBRID, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the general requirements and quality assurance provisions for space use, high reliability, hybrid integrated circuits (hereinafter referred to as “hybrid ICs”) used for electronic equipment installed on spacecrafts. Qualification coverage of hybrid ICs (construction, limits of design, etc.) shall be specified in the design specification. Detailed requirements for individual part types shall be specified in the detail specification. This specification provides following classes of hybrid ICs:

a) Class I hybrid IC
Hybrid IC with the highest quality level and at the lowest risk.

b) Class II hybrid IC
Hybrid IC with next-highest quality level. Burn-in time of screening test for class II hybrid IC is shorter than that of screening test for class I hybrid IC and delta judgement of electrical parameters is not applicable to class II.

1.2 Definition of Terms

The definitions for terms and symbols used herein are provided in paragraph 6.1, appendixes of this specification, JAXA-QTS-2000, MIL-STD-883 and MIL-HDBK-1331.

1.3 Part Number

An example of the part number of hybrid IC is shown below. The details shall be specified in the detail specification.

a) Class I hybrid IC
Example:

JAXA[(1)]	2020/	1001	1	HA	C	R
		Individual Identification (paragraph 1.3.1)	Device type (paragraph 1.3.2)	Package configuration (paragraph 1.3.3)	Lead material and finish (paragraph 1.3.4)	Radiation hardness (paragraph1.3.5)

Note: [(1)] "JAXA" indicates the common part for space use and may be abbreviated to “J.”

b) Class II hybrid IC
Example:

JAXA[(1)]	2025/	1001	1	HA	C	R
		Individual Identification (paragraph 1.3.1)	Device type (paragraph 1.3.2)	Package configuration (paragraph 1.3.3)	Lead material and finish (paragraph 1.3.4)	Radiation hardness (paragraph1.3.5)

Note: [(1)] "JAXA" indicates the common part for space use and may be abbreviated to “J.”

1.3.1 Individual Identification

Unless otherwise specified, the individual identification for the part number shall be the individual number of the detail specification. The individual identification is indicated by a four-digit number. The first digit identifies the manufacturer and shall be provided by Japan Aerospace Exploration Agency (hereinafter referred to as “JAXA”) on the basis of CAA-2020055 and the last three numbers shall be provided by the manufacturer. The manufacturer shall specify provision rule and list of individual identification in quality assurance program plan.
When the manufacturer acquires certification of class I and class II hybrid ICs and design, construction and performance of class I hybrid IC are identical to those of class II hybrid IC, the manufacturer shall ensure that individual identification of class I hybrid IC is not different from individual identification of class II hybrid IC.

1.3.2 Device Type

The device type number shall be a single number from 1 to 9 defined in the detail specification.

1.3.3 Package Configuration

The package configuration is designated by two capital letters. The package configuration shall be defined in Appendix G, the detail specification and the design specification.

1.3.4 Lead Material and Finish

The lead material and finish identification is designated by a capital letter as follows.

Finish letter[(1)]	Lead material	Finish
A	Type A, B or C	Solder dip
B	(not used)	(not used)
C	Type A, B or C	Gold plating
D	Type A, B or C	Tin lead plating
Z	As specified in the detail specification	As specified in the detail specification

Note: (1) Finish letter "X" can be used only in detail specifications where lead finishes A, C, D and Z are all considered acceptable. It shall not be marked on the product or its package and actual lead material and finish letter shall be marked on the product or its package.

1.3.5 Radiation Hardness (Total Dose Radiation Hardness)

The radiation hardness (total dose) shall be identified by a single capital letter and indicates the radiation hardness assurance level. The designator shall be used for the inspection lots that have passed the radiation test (total dose test) of the subgroup 1, Group E of Appendix C or the lot evaluation test of semiconductor chips. When the radiation hardness test (total dose test) is performed at the semiconductor chip level, the lowest radiation hardness (total dose) level result shall be the radiation hardness (total dose) level of the hybrid IC. The manufacturer shall prove that other elements have higher radiation hardness (total dose) levels than the semiconductor chip.

Letter	Radiation hardness assurance level
M	30 Gy (Si) {3x103 rad (Si)}
D	100 Gy (Si) {1x104 rad (Si)}
P	300 Gy (Si) {3x104 rad (Si)}
L	500 Gy (Si) {5x104 rad (Si)}
R	1000 Gy (Si) {1x105 rad (Si)}
F	3000 Gy (Si) {3x105 rad (Si)}
G	5000 Gy (Si) {5x105 rad (Si)}
H	10000 Gy (Si) {1x106 rad (Si)}

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents

The documents listed below form a part of this specification to the extent specified herein. These documents are the latest issues available at the time of contract award or application. If a specific issue needs to be used, the issue shall be specified in the detail specification.

a) JAXA-QTS-2000 Common Parts/Materials, Space Use, General Specification for
b) JAXA-QTS-2010 Microcircuits, High Reliability, Space Use, General Specification for
c) JAXA-QTS-2030 Semiconductor Devices, High Reliability, Space Use, General Specification for
d) JAXA-QTS-2040 Capacitors, Fixed, High Reliability, Space Use, General Specification for
e) JAXA-QTS-2050 Resistors, High Reliability, Space Use, General Specification for
f) JAXA-QTS-2140 Printed Wiring Boards, High Reliability, Space Use, General Specification for

g) ISO 14644-1:1999 Cleanrooms and Associated Controlled Environments - Part 1: Classification of Air Cleanliness
h) ISO 14644-2:2000 Cleanrooms and Associated Controlled Environments - Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1
i) MIL-STD-38534 Hybrid Microcircuits, General Specification for
j) MIL-STD-202 Test Method Standard, Electronic and Electrical Component Parts
k) MIL-STD-750 Test Method Standard Test Methods for Semiconductor Devices
l) MIL-STD-883 Test Methods Standard Microelectronics
m) MIL-HDBK-1331 Handbook for Parameters to be Controlled for the Specification of Microcircuits
n) ASTM F1192 Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices
o) JESD57 Test Procedure for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation
p) CAA-2020055 Provision and management of individual identification for Integrated circuits, hybrid, high reliability, space use

2.2 Reference Documents

The following documents are the reference documents for this specification.

a) JERG-0-035 JAXA Parts Application Handbook (limited to JAXA)
b) JERG-0-039 High Reliability Soldering Requirements
c) JERG-0-043 Standard for Surface Mount Soldering Process
d) JMR-012 Electrical, Electronic, And Electromechanical Parts Program Standard

2.3 Order of Precedence

In the event of a conflict between requirements specified in applicable specifications, the following order of precedence shall apply.

a) Detail specification
b) This specification
c) JAXA-QTS-2000
d) Applicable documents of this specification (paragraph 2.1) except for JAXA-QTS-2000

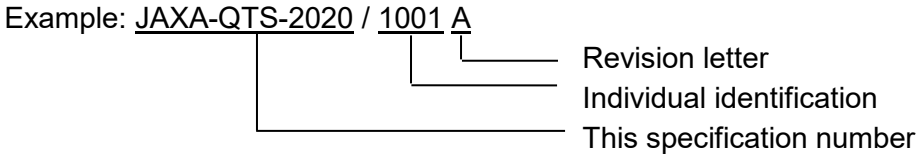
2.4 Design Specifications and Detail Specifications

a) Preparation of design specification
When the manufacturer acquires certification, the manufacturer shall prepare design specification which specifies qualification coverage (including construction and design limit values) of hybrid IC in accordance with Appendix E, and shall submit the design specification attached to quality assurance program plan to JAXA.
b) Preparation of detail specification
The QML manufacturer shall provide detail specification number in accordance with paragraph 2.4.1, prepare and establish detail specification in accordance with

Appendix F and submit the detail specification to JAXA. JAXA will review the submitted detail specification and issue. When detail specification, which was established by purchaser's individual requirements, is published on database of JAXA qualified EEE parts and materials, the QML manufacturer shall cooperate with JAXA after obtaining purchaser's agreement.

2.4.1 Detail Specification Number

The detail specification number shall be assigned in accordance with paragraph A.2.2.2 of JAXA-QTS-2000. An example is shown below. The individual identification shall be a four-digit number with the first digit representing the QML manufacturer and the remaining three digits representing the series number.



2.4.2 Revision letter of the Detail Specification

A revision letter in the detail specification number is assigned in accordance with paragraph A.2.2.2.4 of JAXA-QTS-2000.

2.4.3 Independency of Detail Specification

The detail specification shall be a stand-alone document with a unique number in accordance with paragraph 2.4.1.

2.4.4 Format of Detail Specification

a) The format of the design specification shall be as specified in Appendix E.
b) The format of the detail specification shall be as specified in Appendix F.

3. REQUIREMENTS

3.1 Certification

3.1.1 Qualification Coverage

Qualification shall be valid for hybrid ICs that are designed within the range of designing limit values specified in design specifications, produced by the manufacturing line that conforms to quality assurance programs. The qualification coverage shall be within the range of that are typified by evaluating circuits or samples which have passed the qualification test. Within this coverage, the manufacturer is allowed to supply qualified products in compliance with the detail specification.

3.1.1.1 Qualification System of Hybrid IC

Unless otherwise specified, unlike monolithic integrated circuits, performance and characteristics of hybrid ICs such as circuit functions and electrical parameters are determined according to the specific requirements of each purchaser. Therefore, hybrid ICs must be uniquely designed to satisfy each purchaser's requirements. For this reason, this specification requires that the manufacturer acquire certification from JAXA on a particular manufacturing line (including design standards, materials selection standards and manufacturing technologies). Consequently, the QML manufacturer can respond to individual requirements of each purchaser within the range of certified manufacturing line (including design standards, materials selection standards and manufacturing technologies).

3.1.1.2 Quality Assurance Level of Hybrid IC

a) Class I Hybrid IC

Components (such as chip parts) used for class I hybrid IC shall be class I or equivalent (produced from single wafer lot). At lot evaluation test of semiconductor chip and screening, hybrid IC which exceeded delta limit of electrical parameters before and after burn-in test (burn-in time shall be 240hr) shall be removed from conforming articles. Class I hybrid IC shall pass class I quality conformance inspection and shall be delivered. Class I hybrid IC shall not be unsealed.

b) Class II Hybrid IC

Components (such as chip parts) used for class II hybrid IC shall be class II or equivalent (non-single wafer lot may be allowed). When SOI chips are used, single event resistance shall be evaluated at each wafer lot. At lot evaluation test of semiconductor chip and screening, evaluation of delta limit are not applicable to class II hybrid IC and test requirements (including burn-in test (burn-in time shall be 168hr)) for class II hybrid IC are looser than that for class I hybrid IC. Class II hybrid IC shall pass class II quality conformance inspection and shall be delivered. Only one-time unsealing of class II hybrid IC is allowed.

3.1.2 Initial Qualification

To acquire certification of hybrid ICs in compliance with this specification, a manufacturer shall establish a quality assurance program in accordance with paragraph 3.2.1 of this specification, perform the qualification tests specified in paragraph 4.6 of this specification and acquire a certification status from JAXA as specified in paragraph 3.4.1 of JAXA-QTS-2000. The manufacturer shall be listed on the Qualified Manufacturers List of the Japan Aerospace Exploration Agency (JAXA QML).
To acquire certification, the manufacturer shall also prepare a design specification (to be attached to quality assurance program plan) in accordance with Appendix E and a detail specification in accordance with Appendix F and submit them to JAXA. Initial qualification flow is shown in Figure-1.

3.1.3 Retention of Qualification

To continue supplying hybrid ICs in accordance with this specification, a manufacturer must apply for QML qualification retention in accordance with paragraph 3.4.2.1 “Application for Retention of Qualification” of JAXA-QTS-2000 prior to the expiration date of the certification period specified in paragraph 3.1.4 of this specification.
If the hybrid ICs were not manufactured during the effective period of certification and a quality conformance inspection was not conducted, the manufacturer may apply for the retention of qualification without conducting the quality conformance inspection.

3.1.4 Effective Period of Certification

The effective period of certification granted in compliance with this specification shall be three years.

3.1.5 Requalification

In the case of changes affecting design limit values, functions, performance, reliability and quality of hybrid IC, the manufacturer shall apply for requalification in accordance with paragraph 3.4.3 of JAXA-QTS-2000. Requalification flow is shown in Figure-2.

3.2 Quality Assurance Program

3.2.1 Establishment of a Quality Assurance Program

To acquire a certification in compliance with this specification, the manufacturer shall be responsible for establishing a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall generate a quality assurance program plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to JAXA for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.

3.2.2 TRB Formation

To acquire a certification status of products in compliance with this specification, the manufacturer shall form and operate the Technical Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.

3.3 Design and Construction

The design and construction of hybrid ICs shall specify materials, processes and rules as a whole and design limit values specified for at least following items a) to f) in accordance with Appendix E shall be specified in design specification.
Design and construction of each product shall be specified in detail specification in accordance with Appendix F.
Details of design specification and detail specification shall be in accordance with paragraphs 3.3.1 to 3.3.8.

a) Operating temperature
   1) Case temperature
b) Substrate
   1) Material (e.g., Alumina)
c) Pattern formation and metallization
   1) Minimum element spacing (spacing between conductor to conductor, conductor to resistor, resistor to resistor and element)
   2) Minimum pattern width (conductor and resistor)
   3) Minimum and maximum length of an element (resistor)
   4) Film forming method (thin or thick film)
   5) Film material (e.g., NiCr, Ta, Au, Pd-Ag)
   6) Trimming method
d) Element mounting
   1) Type of elements (e.g., semiconductor, capacitor)
   2) Mounting configuration (e.g., face-up, beam-lead bonding)
   3) Mounting material (e.g., molybdenum tablet, Au-Si eutectic, solder, nonconductive or conductive adhesive)
   4) Maximum area and weight of mounted elements
   5) Derating of mounted elements
e) Internal lead wires
   1) Material (e.g., gold, aluminum)
   2) Configuration (e.g., wire, ribbon) and dimensions
   3) Bonding method (e.g., thermocompression, ultrasonic, parallel gap welding)
   4) Maximum wire (or ribbon) length (or bonding spacing)
f) Packaging
   1) Material
   2) Package configuration (e.g., 16-pin, metal flat package)
   3) Sealing process (e.g., welding, brazing)
   4) Lead material and finish

3.3.1 Operating Temperature

The operating temperature of hybrid ICs shall be within the case temperature range. Unless otherwise specified in the design specification and detail specification, the minimum and maximum operating temperatures shall be -55ºC and +125ºC, respectively.

3.3.2 Substrates

Unless otherwise specified in the design specification and detail specification, thin-film ceramic substrate and thick-film ceramic substrate shall be made of alumina (Al_2O_3) with the minimum purity of 99.5% and 96%, respectively.

3.3.3 Metallization

Unless otherwise specified in the design specification and detail specification, metallization shall meet the following requirements.

3.3.3.1 Conductors

a) Thin film conductors

The properly manufactured thin film conductors on substrates shall be designed such that the current density shall not exceed the following maximum allowable current density when operated under the worst conditions specified in design specification and detail specification.

Conductor material	Maximum allowable current density
Gold	$6x10^5 A/cm^2$
Others (unless otherwise specified in the detail specification)	$2x10^5 A/cm^2$

1) Use a current value equal to the maximum continuous current (at full fan-out for digital devices or at the maximum load for linear devices) or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value at the point(s) of the maximum current density. This current value will be determined at the maximum recommended supply voltage(s) and with the current assumed to be uniform over the entire conductor cross-sectional area.
2) Use the minimum allowed metallization thickness within controls.
3) Use the minimum actual design metallization width (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.
4) Areas of the barrier metals and nonconductive material shall not be included in the calculation of the metallization cross section.
5) In order to compensate for reduction of the cross section due to thinning, voids or scratches, use the cross section obtained from steps 2) through 4) of this paragraph and multiplied by 0.75, to calculate the maximum current density.

b) Thick film conductors

The properly manufactured thick film conductors (such as wiring by metallization and bonding pads) on substrates shall be designed such that the power loss shall not exceed $4W/cm^2$ when the maximum design current is applied.

3.3.3.2 Resistors

Unless otherwise specified in the design specification and detail specification, the maximum power consumption of resistors shall meet the following requirements.

a) Thin film resistors
The properly manufactured thin film resistors on substrates shall be designed such that the maximum power consumption shall not exceed 93W/cm^2.

b) Thick film resistors
The properly manufactured thick film resistors on substrates shall be designed such that the maximum power consumption shall not exceed 7.75W/cm^2.

3.3.4 Mounted Elements

Mounted elements of hybrid IC shall be selected to meet the following requirements:

a) Finished terminals
If tin plating finished terminals are used, the manufacturer shall evaluate any risks for whisker growth and obtain a purchaser's approval. The procedures and criteria for risk evaluation shall be approved by TRB.

b) Selection of mounted elements
Mounted elements for class I hybrid IC shall be selected in accordance with paragraphs 3.3.4.1 to 3.3.4.5. For class II hybrid IC, mounted elements, whose quality assurance levels are exceeding or equivalent to class II parts required in paragraph 5.1.2.2 of JMR-012, shall be selected.

3.3.4.1 Passive Elements

a) Chip capacitor
Chip capacitors shall be selected from JAXA-QTS-2040 qualified products or equivalent and as specified in the design specification and detail specification.

b) Chip resistors
Chip resistors shall be selected from JAXA-QTS-2050 qualified products or equivalent and as specified in the design specification and detail specification.

3.3.4.2 Semiconductor Chips

a) Semiconductor chips
Semiconductor chips shall be selected in compliance with requirements in Appendix A and as specified in the design specification and detail specification.

b) Surface mounting semiconductor parts
Surface mounting semiconductor parts shall be specified in the design specification and detail specification, referring to the requirements in Appendix A.

3.3.4.3 Sheet Transformers

Sheet transformers shall be specified in the design specification and detail specification in consideration of the requirements in JAXA-QTS-2140.

3.3.4.4 Flexible Printed Wiring Boards

Flexible printed wiring boards shall be specified in the design specification and detail specification in consideration of the requirements in JAXA-QTS-2140.

3.3.4.5 Other Mounted Elements

When any other mounted elements are used, the requirements for the elements must be specified in the design specification and detail specification.

3.3.5 Organic and Polymeric Materials

When organic and polymeric materials (e.g., coatings, adhesives) are used inside a package of hybrid IC as assembling or coating materials, they shall not exhibit blister, crack, outgas, softening, outflow or other defects under the specified test conditions. Organic and polymeric materials shall be as specified in the design specification and detail specification.

3.3.6 Mounting Materials for Substrate and Semiconductor Chips

Glass shall not be used for mounting substrate or semiconductor chips. Mounting materials for substrate or semiconductor chips shall be specified in the design specification and detail specification.

3.3.7 Internal Lead Wires

Internal lead wires or other conductors which are not in thermal contact with the substrate along the entire length shall be designed such that the maximum rated current (continuous current for direct currents, effective value for alternating currents and peak current divided by $\sqrt{2}$ for pulsed currents) shall not exceed the maximum allowable current calculated by the following formula.

$$I = \frac{1}{128} \times K \times d^{\frac{3}{2}}$$

where, I = Maximum allowable current (A)
d = Wire diameter (mm) (When the cross section is not circular, use the diameter of a circular wire or conductor of the same cross section area)
K = A constant obtained from the length and composition of the wire or conductor as shown in Table 1.

Table 1. "K" value

Material	"K" value for bond-to-bond total conductor length	
	Length ≤ 1.0mm	Length > 1.0mm
Aluminum	22000	15200
Gold	30000	20500
Copper	30000	20500
Silver	15000	10500
All other	9000	6300

3.3.8 Package

Unless otherwise specified in the detail specification, packages shall be designed to provide stress relief for leads such as flat pack package when mounted to a printed wiring board.

a) Package configuration
Qualification coverage of package configuration shall be defined in the design specification in accordance with Appendix E. Package configuration of each product shall be specified in the detail specification in accordance with Appendix F.

b) Package material
External metal surfaces of the package shall be corrosion resistant. External leads shall meet the requirements of c) below. Nonmetallic materials of the package and coatings including markings shall be non-nutrient to fungus and shall not exhibit any blister, crack, outgas, softening, outflow or other defects under the test conditions specified in the detail specification. Details shall be specified in the detail specification.

c) Lead material and finish

1) Lead material
The lead material composition shall satisfy one of the following types unless otherwise specified in the detail specification.

1.1) Type A

Iron	53% nominal
Nickel	29±1%
Cobalt	17±1%
Manganese	0.65% max.
Silicon	0.20% max.
Carbon	0.06% max.
Aluminum	0.10% max.
Magnesium	0.10% max.
Zirconium	0.10% max.
Titanium	0.10% max.

(The sum of aluminum, magnesium, zirconium, and titanium contents shall be 0.20% as a maximum.)

1.2) Type B

Nickel	40.00% to 43.00%
Cobalt	0.50% max.
Manganese	0.80% max.
Silicon	0.30% max.
Carbon	0.10% max.
Aluminum	0.10% max.
Chrome	0.25% max.
Phosphorus	0.025% max.
Sulfur	0.025% max.
Iron	Remainder

1.3) Type C (Copper-core, Fe-Ni52 alloy)

Copper (core)	99.96% min.
Nickel	48% to 52%
Carbon	0.02% max.
Manganese	0.2% to 1.0%
Silicon	0.1% to 0.5%
Sulfur	0.025% max.
Phosphorus	0.025% max.
Iron	Other

2) Lead Finish

Unless otherwise specified in the detail specification, the lead finish shall be one of the following options from 2.1) to 2.3).

2.1) Solder dip

The solder dip shall be homogeneous with the minimum thickness of 5.08μm at the major flats of solder (Sn60 to Sn63) over a primary finish in accordance with type 2.2) below or nickel plating (with the thickness between 2.54μm and 7.62μm).

2.2) Gold plating

The purity of gold plating shall be a minimum of 99.7% gold (i.e., the sum of impurities and other metals shall be 0.3% as a maximum). Gold plating thickness shall be a minimum of 1.27μm. This finish requires electrolysis nickel or copper undercoating with a thickness between 1.27μm and 7.62μm.

2.3) Tin lead plating

Percentage of lead shall be between 3% and 50%. Tin lead plating thickness shall be minimum 7.62μm. Electrolysis nickel or nickel electrodeposit underplating may be used for this finishing. Thickness of the underplating shall be between 1.27μm and 8.89μm.

3.4 Marking

3.4.1 Marking Items

At least the following marking items shall be specified in the detail specification.

a) Index point (paragraph 3.4.1.1)
b) Part number (paragraph 1.3)
c) Inspection lot identification code (paragraph 3.4.1.2)
d) Serial number (paragraph 3.4.1.3)
e) Manufacturer's identification (paragraph 3.4.1.4)

3.4.1.1 Index Point

The index point indicates the start of lead numbers or mechanical orientation and shall be shown by a stamp, tab, notch or groove, among other means. The index point shall be visible from the top when the product is mounted in a normal manner. The manufacturer's identification code shall not be used for this purpose.

3.4.1.2 Inspection Lot Identification Code

An inspection lot identification code shall be assigned to each inspection lot (see 2) of paragraph 4.3.1 l)) and shall be marked.

3.4.1.3 Serial Number

A serial number shall be assigned to each hybrid IC in the inspection lot prior to the screening test (see paragraph 4.7).

3.4.1.4 Manufacturer's Identification

The manufacturer's identification shall be the certified manufacturer's name, abbreviation or trademark.

3.4.2 Marking Location and Layout

Unless otherwise specified in the detail specification, the part number and inspection lot identification code shall be located on the top surface of flat packages and on either the top or the side of cylindrical packages. Each marking item may be placed in any way as long as it satisfies the marking requirement and does not interfere with other markings.

3.4.3 Marking Option

The manufacturer shall complete markings on all hybrid ICs in the inspection lot by the start of the external visual inspection of the screening test or shall be marked on the samples for the Groups B, C, D and E qualification test or quality conformance inspection. When the manufacturer chooses the latter, the procedure is as follows.

a) Sample products shall be marked prior to conducting the Group B, C, D or E qualification test or quality conformance inspection.
b) All products in the inspection lot represented by the samples shall be marked when the sample has passed all the tests. The external visual inspection of the screening test shall then be performed.

3.4.4 Exemption of Marking Items

When the surface area of hybrid IC is not sufficient to place all the marking items specified in paragraph 3.4.1, marking items may be exempted in the following order or priority.

a) When “2020-” of part number (for class I hybrid IC) or “2025-“ of part number (for class II hybrid IC) is omitted, identification code “C1” indicating class I or “C2” indicating class II shall be located on the proper place.
b) Package configuration and lead material/finish designator of part number. (In this case, both designators shall be omitted).
c) Manufacturer’s identification

3.5 Radiation Hardness

3.5.1 Total Dose Radiation Hardness

Total dose radiation hardness of hybrid IC shall be specified in detail specification. When total dose radiation hardness is required for semiconductor chip, the semiconductor chip shall be selected on the basis of requirements in Appendix A and as specified in detail specification.

3.5.2 Single Event Characteristics

As for single event characteristics of hybrid IC, characteristics selected from the following items relating to product shall be specified in detail specification. When single event characteristics are required for semiconductor chip, the semiconductor chip shall be selected on the basis of requirements in Appendix A and as specified in detail specification.

a) SEU
b) SEL
c) SEB
d) SEGR
e) SEDR
f) SET
g) SEFI
h) Others

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The manufacturer shall be responsible for implementing the quality assurance program specified in paragraph 3.2 and operating the TRB.

4.2 Incoming Parts and Materials Control

Incoming parts and materials shall be subject to an appropriate incoming inspection and controlled to ensure that each part and material is traceable to the incoming inspection lot. The manufacturer shall establish and implement procedures to store and retrieve received parts and materials and to remove limited-life parts and materials.

4.2.1 Incoming Inspection

Test items, test methods and criteria of incoming inspection for each part and material used for hybrid IC shall be specified in detail specification.

4.2.2 Record of Incoming Parts and Materials Control

The records of incoming parts and materials shall be categorized into incoming inspection records and storage, retrieval and disposal records. These records shall include the following items as a minimum.

a) Incoming inspection records
   1) Part and Material name
   2) Inspection items
   3) Lot size
   4) Lot identification code
   5) Document number and established date of inspection instructions
   6) Pass or fail of each lot and quantity of failed parts and materials
   7) Date of inspection and name or identification code of the inspector

b) Storage, retrieval and disposal records
   1) Part and Material name
   2) Storage conditions
   3) Lot identification code
   4) Storage date and quantity of storage materials
   5) Retrieval date and quantity, lot identification code of finished or semi-finished products for which the part and material are used.
   6) Disposal date and quantity

4.3 Manufacturing Process Control

The manufacturer shall establish and maintain procedures of manufacturing processes, control parameters and methods.

4.3.1 Manufacturing Process

The manufacturer shall define and control each manufacturing process including the items listed below as a minimum. Rework shall be performed in accordance with paragraph 4.3.2. The manufacturer shall also establish and implement a storage method for finished or semi-finished products between processes.

a) Formation of substrate lots
   1) Formation procedure of substrate lots
   2) Assignment of substrate lot identification codes

b) Metallization process
   1) Manufacturing process of thin-film substrates
      1.1) Mask control
      1.2) Metallization material
      1.3) Forming method
      1.4) Forming conditions
      1.5) Method and frequency of chamber cleaning
   2) Electrolytic plating process
      2.1) Metallization material
      2.2) Plating solution and control of plating bath
      2.3) Plating conditions
   3) Manufacturing process of thick-film substrates
      3.1) Screen control
      3.2) Paste material
      3.3) Forming method
      3.4) Forming conditions
      3.5) Furnace control

c) Pattern formation process
   1) Masking method
      When photolithography is used, the following items on handling of photo resist shall be specified.
      1.1) Preparation method
      1.2) Specific gravity, viscosity, evaluation methods for solid residues and pinholes
      1.3) Storage conditions
      1.4) Coating conditions
      1.5) Baking conditions
      1.6) Exposure conditions
      1.7) Developing conditions
   2) Etching technique
      When the wet etching is used, the following items shall be specified.
      2.1) Preparation method
      2.2) Composition, grade, temperature, among others, of etching solution
      2.3) Frequency of etching solution change
      2.4) Etching conditions
      2.5) Washing and drying
   3) Inspection process
      3.1) Method of visual inspection and pass/fail criteria

d) Trimming of resistors
   1) Trimming method and facility type
   2) Trimming conditions
   3) Inspection for resistance and film stability
   4) Method of visual inspection and pass/fail criteria

e) Scribing and substrate separation
   1) Scribing method and conditions
   2) Dicing method and conditions
   3) Method of visual inspection and pass/fail criteria

f) Formation of production lots
   1) Formation of production lots(1)
   2) Assignment of production lot identification code

   Note(1) Production lot shall be prepared such that inspection sublots can be easily prepared (paragraph 4.3.1k)).

g) Substrate and parts mounting
   1) Mounting material and package material in the mounting area
   2) Mounting structure
   3) Mounting conditions
   4) Visual inspection method for mounting
   5) Control method of adhesive strength

h) Interconnection bonding
   1) Material
   2) Lead type
   3) Bonding method
   4) Bonding conditions
   5) Visual inspection for bonding
   6) Nondestructive bond pull test method
   7) Control method of bond strength

i) Pre-seal visual inspection
   1) Procedure and pass/fail criteria of visual inspection

j) Sealing process
   1) Package and sealing materials
   2) Sealing method
   3) Stabilization bake prior to sealing
   4) Sealing conditions

k) Formation of inspection sublots
   1) Formation of inspection sublots(1)
   2) Assignment of inspection sublot identification code

   Note (1) Inspection sublots shall meet the following requirements.
      i. An inspection sublot shall consist of hybrid ICs of a single part number and single device type with identical package type and lead finish.
      ii. All products of an inspection sublot shall be manufactured using a single substrate lot. This requirement is not applicable to class II.
      iii. Each inspection sublot shall consist of semiconductor chips made from a single wafer lot. This requirements is not applicable to class II.

iv. Each inspection sublot shall be manufactured using the same machines in production processes.
v. The entire assembly process from assembly start such as substrate attachment and MOSFET mounting to package sealing shall be completed within the same 12-week period.
vi. Each inspection lot shall consist of 500 class I hybrid ICs as a maximum. This requirement is not applicable to class II hybrid IC.

l) Formation of inspection lots
1) Formation of inspection lots(1)
2) Assignment of inspection lot identification code

Note (1) Inspection lots shall satisfy the following requirements.
i. An inspection lot shall consist of hybrid ICs of a part number with identical identification number, selected from a maximum of five inspection sublots. The case configuration, package types, and lead finish must be identical.
ii. The entire assembly process from assembly start such as substrate attachment and MOSFET mounting to package sealing shall be completed within the same 16-week period.

4.3.2 Rework Control

When the rework specified below is performed, the rework results shall be documented in traveler as specified in paragraph 4.3.5. Reworked products shall be clearly identifiable from other products. Once sealed, rework shall be limited to re-cleaning, correction of defective marking and lead straightening (e.g., reshaping of leads such as correction of lead tip shape which does not affect hermeticity of the product.)

a) Class I hybrid IC
Class I hybrid IC shall not be delidded.
b) Class II hybrid IC
Only one-time re-sealing may be allowed for class II hybrid IC. Visual inspection standard of resealed class II hybrid IC shall be identical to that of class II hybrid IC which was not resealed.

4.3.2.1 Re-Bonding and Element Replacement

Unless otherwise specified in the detail specification, re-bonding and replacement of attached elements shall be allowed under the following conditions.

a) Re-bonding shall not be performed on surfaces where the top metallization layer is lifted or peeled, or on bonding pads which are significantly damaged such that the lower metallization layer or substrate is exposed.
b) The total number of re-bonds shall be limited to a maximum of 10% of the total number of bonds in the hybrid IC. Re-bonding of wires to substrate pads or package posts for replacing elements shall not be limited to this maximum number.
c) The total number of interconnection bonding or element replacements shall be limited to three cycles for class I hybrid IC and four cycles for class II hybrid IC.

Element replacements shall only be for the elements which are mounted by adhesive or solder.

4.3.2.2 Rework on Conductors on Substrate

Rework shall be allowed to repair scratches, breaking, discontinuation of conductors on substrates using bonding wires or ribbons which have current capacity of 3.5 times the maximum operating load current (paragraph 3.3.3). Repair shall be limited to one area per substrate area of 323mm^2.

4.3.2.3 Replacement of Substrates or Packages

a) Unless otherwise specified in the detail specification, substrates and packages of class I hybrid IC shall not be replaced.
b) Unless otherwise specified in the detail specification, substrates and packages of class II hybrid IC except for lid shall not be replaced.

4.3.3 Environmental Control

Temperature, relative humidity and dust counts shall be controlled for manufacturing processes such as substrate manufacturing processes and assembly operations which are significantly affected by the environments. The particle counting shall be performed in accordance with ISO 14644-1 and ISO 14644-2.

4.3.4 Water Purity Control

The purity of water shall be controlled with respect to the minimum specific resistively, maximum total solids, maximum organic impurity, maximum bacteria quantity and maximum chlorine contents at room temperature.

4.3.5 Production Records

Production records shall be categorized as either work records for the production processes or control records for the environmental conditions. Production records shall include at least the following items.

a) Work records for the production process
   1) Name of work
   2) Lot identification code of materials and products (including semi-finished products)
   3) Document number and date work order was established.
   4) Quantity of incoming and outgoing products (including semi-finished products) for each work and disposition
   5) Date of work and name or identification code of operator
   6) Identification of equipment used
b) Control records such as for environmental conditions
   1) Document number and date control instruction was established

2) Date of measurement and name or identification code of operator

4.4 Classification of Inspections and Tests

Inspections and tests shall include screening test in addition to three categories specified in paragraph 4.3 of JAXA-QTS-2000.

a) In-process inspection
b) Qualification test
c) Screening test
d) Quality conformance inspection

4.5 In-Process Inspection

The manufacturers shall perform the in-process inspections specified below during the manufacturing process of hybrid IC to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize properties which cannot be measured on the finished products. Test items, test methods, criteria and sample quantity shall be shown in the manufacturing flowchart and shall be specified in detail specification.

a) Internal visual inspection of semi-finished products (100% non-destructive or sampled inspection) Final visual inspection prior to sealing shall be conducted to all sample.
b) Physical or chemical inspection of semi-finished products (sampled destructive or non-destructive inspection)
c) Characterization of semi-finished products (100% non-destructive or sampled inspection)

4.5.1 In-Process Inspection Records

The manufacturer shall specify in-process inspection records in the quality assurance program as specified in paragraph 3.2.1.

4.6 Qualification Test

The qualification test shall be performed on the inspection lot which passed the screening test in accordance with Appendix C using evaluation devices or samples which were produced using the same design, construction, materials and manufacturing line as those to be qualified

4.6.1 Evaluation Circuits or Samples

Evaluation circuits or samples shall be produced using the design, construction, materials and manufacturing line specified in the quality assurance program and shall have sufficient functions and performance to evaluate the construction and design limits of the products. Therefore evaluation circuits or samples shall be identical in critical constructions to the hybrid ICs to be certified. When all critical construction and design

limits cannot be represented by a single evaluation circuit or sample, multiple evaluation circuits or samples may be used.

4.7 Screening

To supply hybrid ICs in compliance with this specification, the manufacturer shall perform screening in accordance with Appendix B. Prior to the screening, production lots shall be re-grouped into inspection lots.
Screenings may be initiated after the final sealing process has been completed. Products shall be serialized within each inspection lot prior to the screening test to provide traceability between each measurement and product.

4.8 Quality Conformance Inspection

The quality conformance inspection is defined as a lot assurance inspection for lot integrity confirmation.
The quality conformance inspection shall be performed in accordance with Appendix C on inspection lots which passed the screening tests. Only those hybrid ICs which have passed the quality conformance inspection can be shipped as products that are in compliance with this specification. The manufacturer is allowed to use the radiation hardness designator only if the products are certified as radiation hardened products.
Products selected as samples shall be handled in accordance with paragraph C.3.5.
When products to be shipped and qualification test sample are within same inspection lot, qualification test results may be used as quality conformance inspection results for the first article.
Product delivery flows are shown in Figure-3 and Figure-4.

4.9 Long-Term Storage

4.9.1 Disposition of Lots Stored for a Long Term at the Manufacturer's Site

When products have been stored at the manufacturer's site for 24 months or longer after the quality conformance inspection, the manufacturer shall repeat the group A quality conformance inspection prior to delivery. Only the products which have passed the tests can be shipped as products. If products fail in any subgroup inspection, 100% inspection shall be performed for items in that subgroup. The hybrid ICs which are judged acceptable can be shipped as products. Failed products shall be removed and shall not be delivered.
Paragraph 4.3.4.1 of JAXA-QTS-2000 shall also be applicable.

4.9.2 Storage by Purchasers

The conditions and period of storage by purchasers shall be specified in the detail specification, if necessary.

4.10 Change of Tests and Inspections

Any change to the in-process inspection, screening test and quality conformance inspection as specified in this specification shall be made in accordance with paragraph 4.3.5 and paragraph A.2.1.3 (appendix A) of JAXA-QTS-2000.

5. PREPARATION FOR DELIVERY

5.1 Packaging

The manufacturer shall package the products individually prior to delivery. The package shall have a construction to hold the products securely and protect the products from mechanical shocks. The package shall protect the products from moisture and be free of sharp edges or burrs on the external surfaces. It is desirable that the package allows visual inspection without opening the package. The packaging materials shall not break, peel off, crumble, loosen, accumulate static electricity or corrode. Tapes or adhesives shall not be used to secure the products.
Proper protection shall be provided to ESD sensitive products. Individual shipping packages shall be placed in a shipping container to protect the products from possible damages during shipment.

5.2 Marking on Package

Each shipping package shall have the markings specified in b) through e) of paragraph 3.4.1. However, when the markings on the products are clearly visible from outside of the shipping package, those markings on the package may be omitted. For packages with ESD protection, a marking “ESD sensitive” shall be added. All markings shall be waterproof.
The marking requirements for each shipping package shall also apply to the shipping container. Paragraph 3.4.1d) shall be omitted. Quantity, applicable specification number, date of packaging and inspection results shall be marked additionally.

6. NOTES

6.1 Definition of Terms

The following definition of terms is used in this specification.

a) Integrated circuit :
Devices which are considered as a single part and composed of high-density, interconnected, small circuit elements that are formed within or on a substrate to perform an electronic circuit function.

b) Hybrid integrated circuit (hybrid IC):
Integrated circuits that contain two or more of the following element types and thin film or thick film substrate.
1) Integrated circuits
2) Semiconductor devices
3) Passive elements such as resistors and capacitors

When quality assurance level of hybrid IC is limited in this specification, hybrid IC is expressed as “Class I hybrid IC” or “Class II hybrid IC”. When both hybrid ICs are included, hybrid IC is expressed as “hybrid IC”.

c) Chip:
Circuit elements used in hybrid IC without a package and leads.

d) Substrate (of hybrid IC):
Supporting base upon or within which elements of integrated circuit are formed or mounted.

e) Device type:
Refers to a specific configuration of integrated circuit. For example, products made by different manufacturers using different mechanical arrangements and materials are referred to as “the same device type” if those devices are functionally and physically interchangeable at the semiconductor chip or substrate level.

f) Package type:
Refers to a specific package configuration. Packages with the same package configuration, materials (including mounting materials such as bonding wires and semiconductor chips), components and assembly processes are of the same package type.

g) Final seal:
A manufacturing process after which access to internal elements of the product is not possible.

h) Delta limit:
The maximum allowable change of parameter value measured before and after test.
Note: If represented in percentage, delta limit shall indicate a percentage with respect to a pre-test value.

i) Wafer lot:
A group of wafers processed together in each process.

j) Substrate lot (of hybrid IC):
A group of substrates formed together in each process.

k) Production lot:
A group of hybrid ICs manufactured (or being manufactured) using the same manufacturing technology, materials, controls, design and production line.
When multiple device types are manufactured in the same processes up to the final seal process, the production lot may include those device types.

l) Inspection lot:
A group of hybrid ICs with the same package type and lead finish. An inspection lot may include multiple device types. Inspection lots are usually divided into inspection sublots.

m) Inspection sublot:
A group of single device type hybrid ICs with the same package type and lead finish. Inspection sublots are processed together in all manufacturing processes.

n) Thin-film:
Film formed on substrate surface by vacuum deposition, ion sputtering or gas phase reaction, among other methods.

o) Thick-film:
Film formed by baking, among other methods, after ink paste is coated, sprayed or printed on substrate surface.

p) Sheet transformer
Transformer composed of multilayer printed wiring board.

q) Flexible printed wiring board
Wiring board which is thin, bendable and composed of copper foil bonded to insulating film.

r) Ferrite core
Ferrite core is produced by forming and baking materials that are made of several layers of various metal oxide films. The primary ingredient of those metal oxide films is iron oxide. The chemical composition of ferrite core is MOFe2O3 (M indicates metals)

s) Single event characteristic
Specific characteristic that causes malfunction or permanent damage in circuit elements by the incidence of a single high-energy particle.

t) Design specification
Document providing qualification coverage for design of hybrid IC.

u) Procurement specification
Document prepared by QML manufacturer and applicable to purchase of materials for hybrid IC manufacturing (refer to paragraph 4.2). This document is included in product assurance documents.

v) First article
Product delivered at first time for detail specification.

w) Class I hybrid IC
Hybrid IC with the highest quality assurance level and at the lowest risk

x) Class II hybrid IC
Hybrid IC with the next-highest quality assurance level after class I hybrid IC and at a lower risk.

6.2 Notes for Manufacturer

6.2.1 Preparation and Registration of Application Data Sheet

The manufacturer shall prepare the application data sheet in accordance with Appendix G of JAXA-QTS-2000 and register it with JAXA.
In the case of products based on purchaser's individual requirements (refer to paragraph 6.3.1), the manufacturer may be exempt from preparing the application data sheet, when the manufacturer takes counsel with the purchaser about necessity of the application data sheet and the exemption is approved by the manufacturer's TRB (refer to paragraph 3.2.2).

6.3 Notes for Acquisition Officers

6.3.1 Procurement Method of Hybrid IC

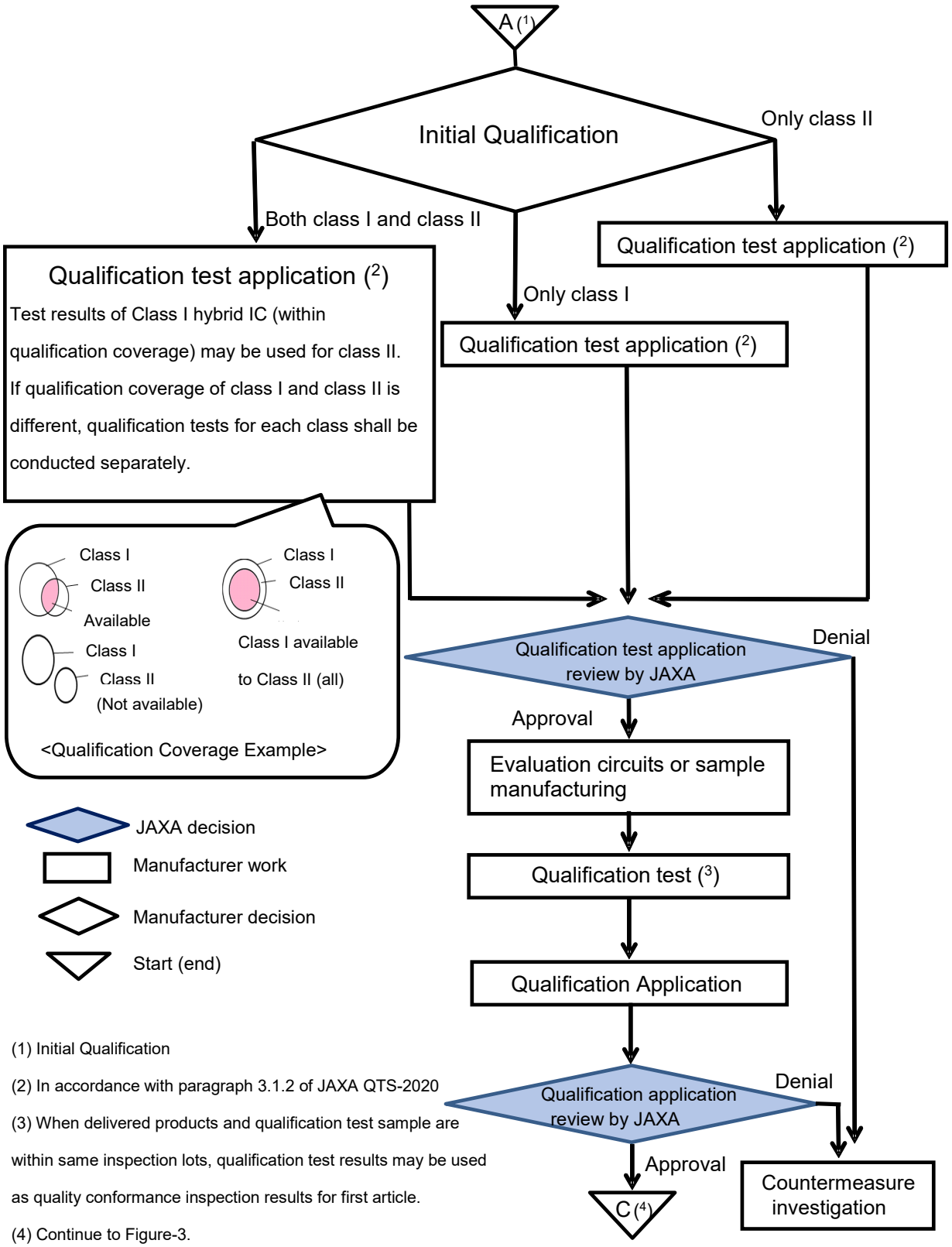
To purchase products in compliance with this specification, procurement methods shall be as specified below:

1) For first article, the purchaser shall provide the manufacturer with technical information (data) including requirements on circuit function, electrical parameters, circuit diagram (if a circuit needs to be specified), and take counsel with manufacturer for procurement. The purchaser shall present technical information needed for preparation of detail specification on the assumption that the manufacturer submits the technical information to JAXA.
2) If a purchaser is procuring previously procured products which previously passed qualification test or quality conformance inspection (level I), the purchaser shall only be required to provide the following items.
   a) Part number
   b) Detail specification number
   c) Necessity of group E of quality conformance inspection
   d) Test data to be submitted for the shipment and whether the source inspection is performed or not performed.
   e) Others

Requirements other than those defined in this specification may be specified for specific applications as item e). However, if the requirements conflict with the existing requirements in this specification, the purchaser shall not request the manufacturer to indicate that the hybrid IC complies with this specification.

6.3.2 Review of Application Data Sheet

The application data sheet contains more detailed product information required for parts selection and designing than is specified in the detail specification such as qualification data. Purchaser must review the application data sheet prior to procurement.



(1) Initial Qualification

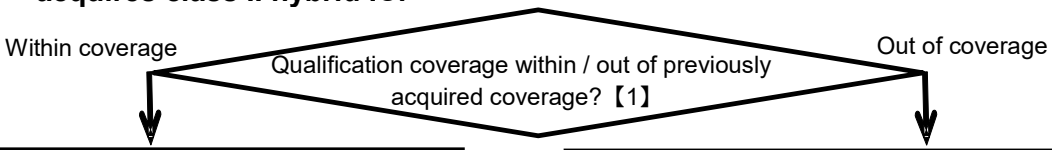
(2) In accordance with paragraph 3.1.2 of JAXA QTS-2020

(3) When delivered products and qualification test sample are within same inspection lots, qualification test results may be used as quality conformance inspection results for first article.

(4) Continue to Figure-3.

Figure-1 Initial Qualification Flow

Case 1: The manufacturer, who previously acquired class I hybrid IC certification, acquires class II hybrid IC.



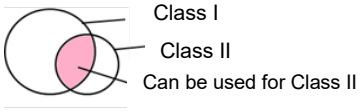
Test results of class I hybrid IC may be used (qualification test is not needed)【1-1】

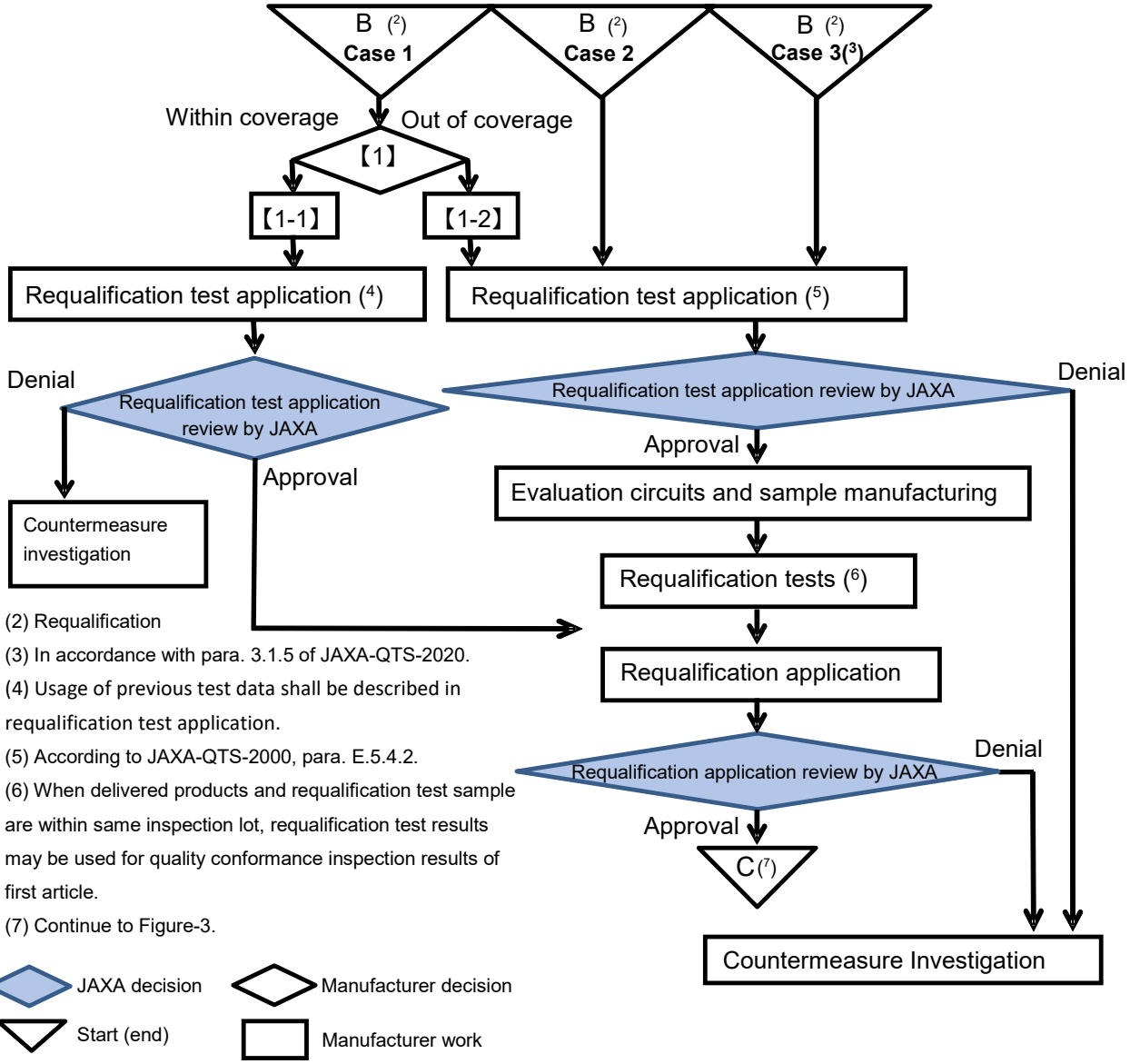
Qualification tests for class II hybrid IC is needed ([1]) 【1-2】

Case 2: The manufacturer, who previously acquired class II hybrid IC certification, acquires class I hybrid IC.

Case 3: Requalification for same class.

([1]) Within qualification coverage of class I hybrid IC, class I test results can be used.





(2) Requalification

(3) In accordance with para. 3.1.5 of JAXA-QTS-2020.

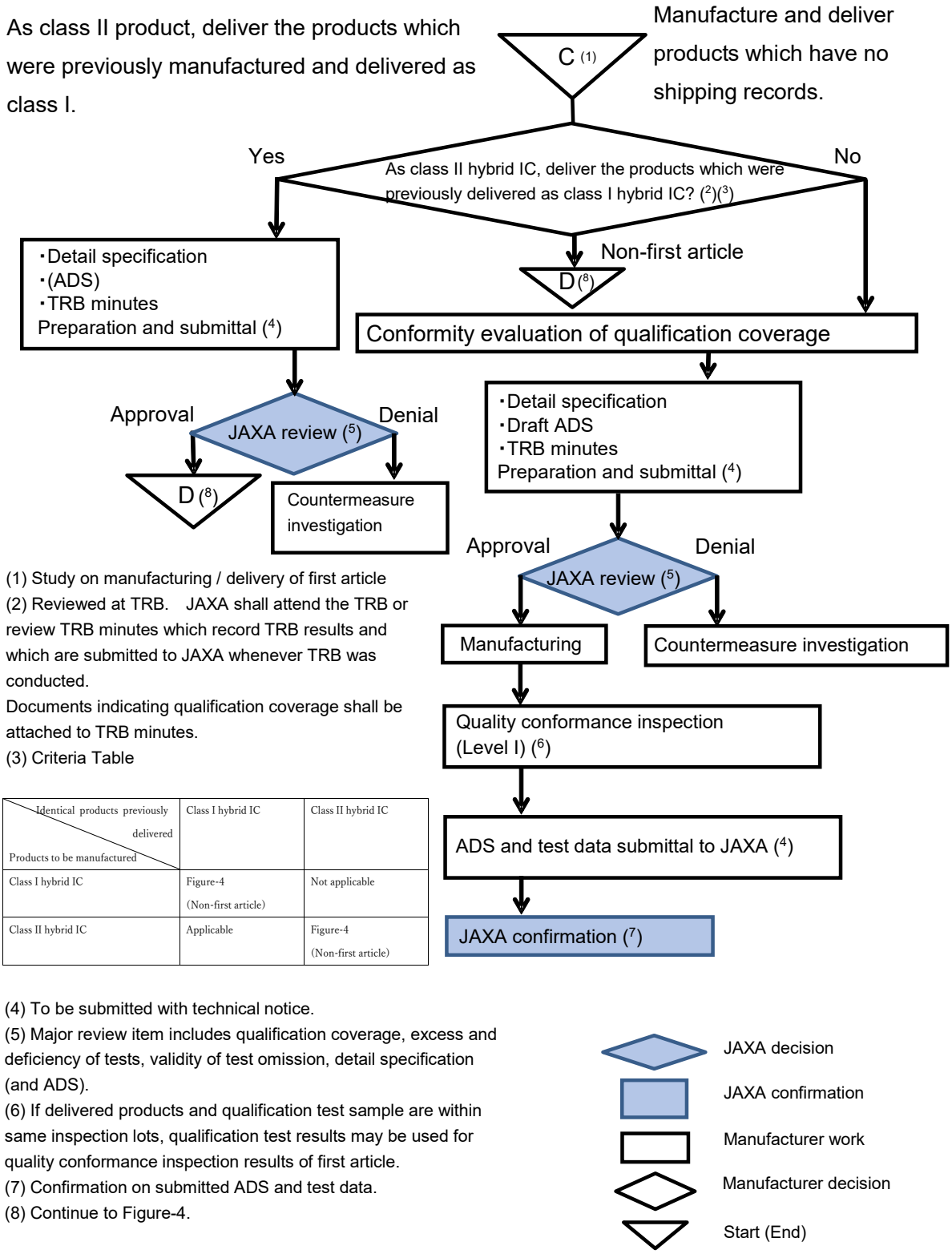
(4) Usage of previous test data shall be described in requalification test application.

(5) According to JAXA-QTS-2000, para. E.5.4.2.

(6) When delivered products and requalification test sample are within same inspection lot, requalification test results may be used for quality conformance inspection results of first article.

(7) Continue to Figure-3.

Figure-2 Requalification Flow



(1) Study on manufacturing / delivery of first article
(2) Reviewed at TRB. JAXA shall attend the TRB or review TRB minutes which record TRB results and which are submitted to JAXA whenever TRB was conducted.
Documents indicating qualification coverage shall be attached to TRB minutes.
(3) Criteria Table

Identical products previously delivered / Products to be manufactured	Class I hybrid IC	Class II hybrid IC
Class I hybrid IC	Figure-4 (Non-first article)	Not applicable
Class II hybrid IC	Applicable	Figure-4 (Non-first article)

(4) To be submitted with technical notice.
(5) Major review item includes qualification coverage, excess and deficiency of tests, validity of test omission, detail specification (and ADS).
(6) If delivered products and qualification test sample are within same inspection lots, qualification test results may be used for quality conformance inspection results of first article.
(7) Confirmation on submitted ADS and test data.
(8) Continue to Figure-4.

Figure-3 First Article Delivery Flow

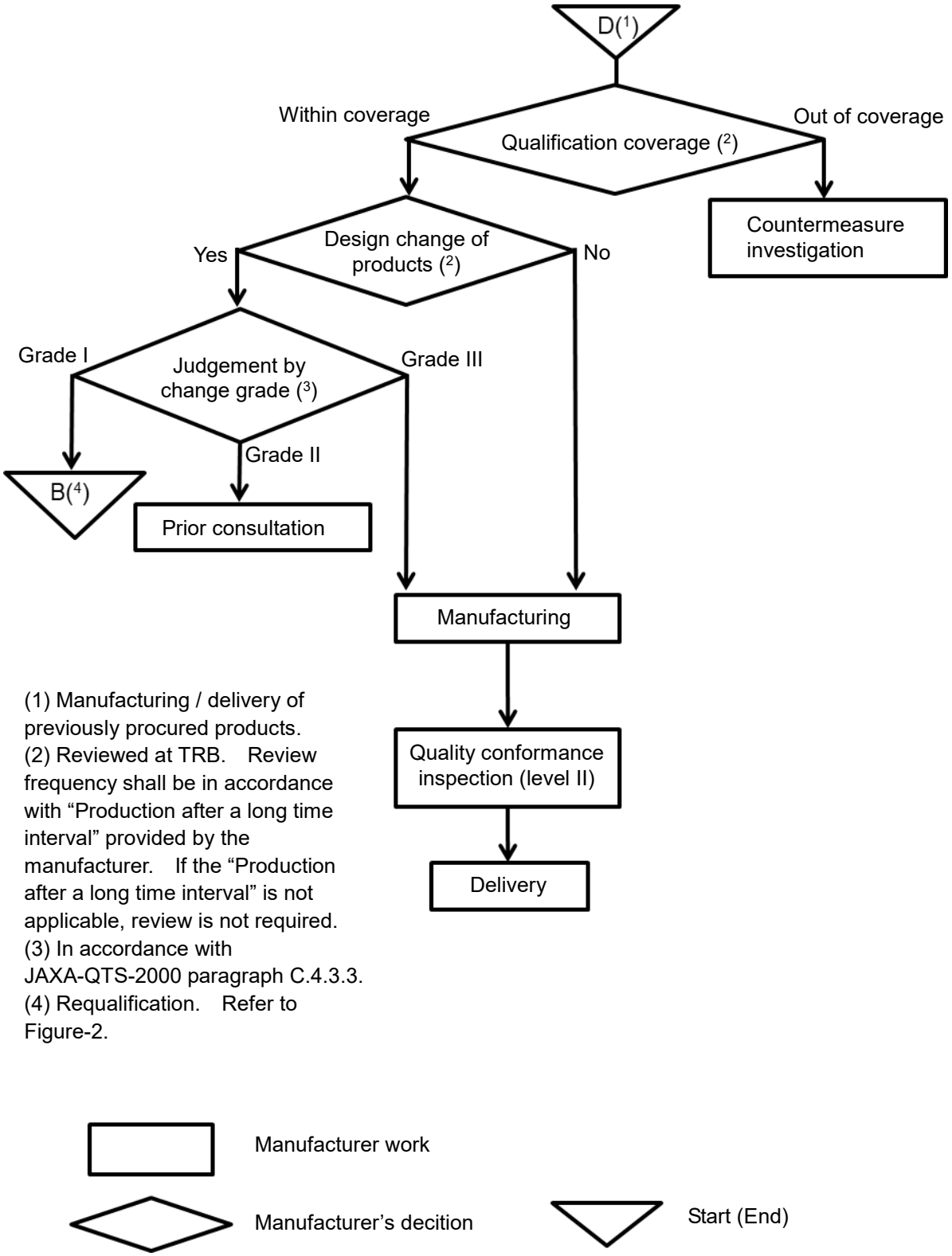


Figure-4. Delivery Flow of Previously Procured Products

APPENDIX A

REQUIREMENTS FOR SEMICONDUCTOR CHIPS, SUBASSEMBLY AND SEMI-ASSEMBLY HYBRID IC

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX A

REQUIREMENTS FOR SEMICONDUCTOR CHIPS, SUBASSEMBLY AND SEMI-ASSEMBLY HYBRID IC

A.1. Scope

This appendix establishes the requirements for semiconductor chips, subassembly used for hybrid ICs and semi-assembly hybrid ICs. From semiconductor chips acceptance to hybrid IC assembly is shown in Figure A-1.

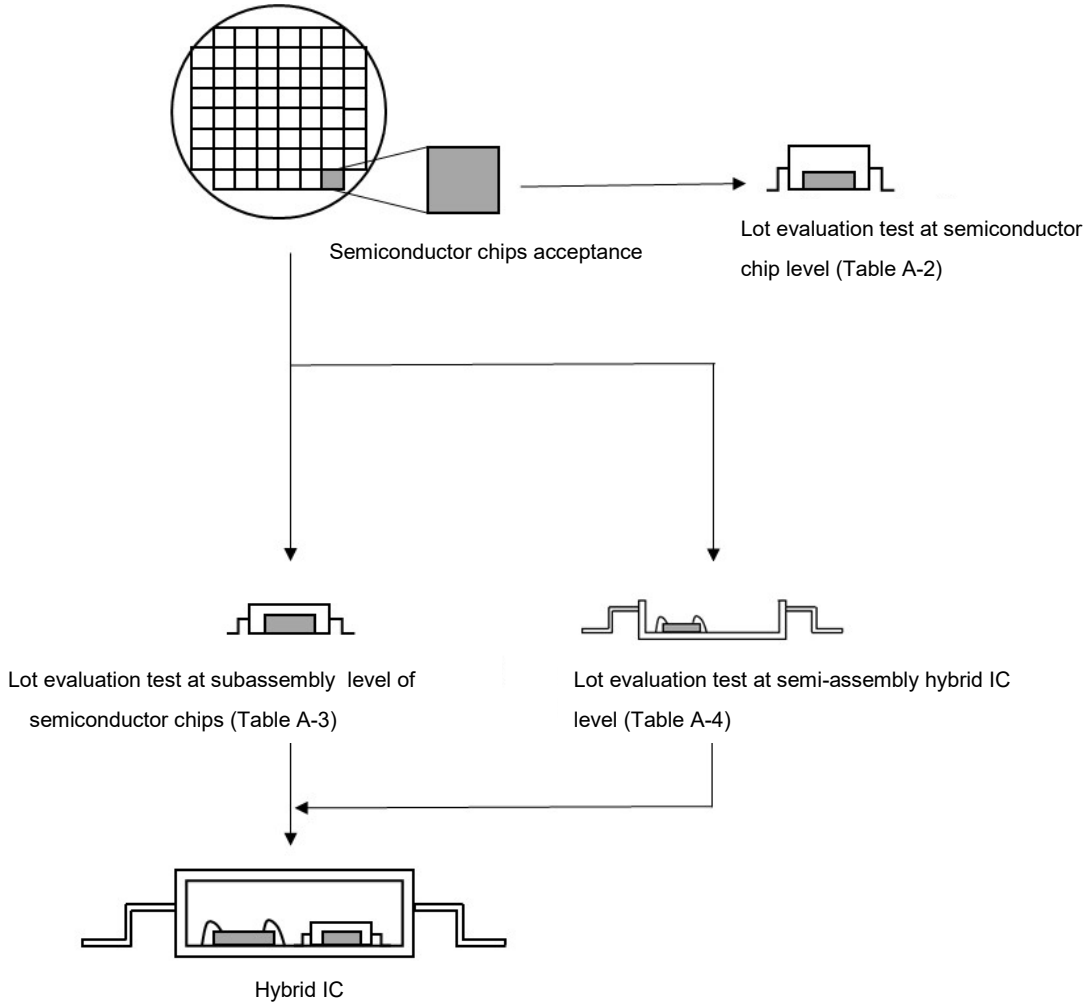


Figure A-1 From semiconductor chips acceptance to hybrid IC assembly

A.2. Requirements

The manufacturer shall verify the quality of semiconductor chips used for hybrid ICs through lot evaluation tests for each lot before the semiconductor chips are used. A specification shall be prepared to establish electrical parameters and test methods, as a minimum.

A.2.1 Design and Construction

The manufacturer shall verify that the design and the construction of semiconductor chips meet the following requirements.

A.2.1.1 Current Density of Metallization

Unless otherwise specified, the metallization shall be designed to ensure that properly produced conductors shall not experience, under the worst case of operating conditions, a current density in excess of the maximum allowable values specified in Table A-1.

Table A-1 Maximum Allowable Current Density of Metallization

Metallization material	Maximum allowable current density (A/cm^2)
Aluminum (99.99%, pure or doped)	5×10^5
High melting point metal (Mo, W, Ti-W, Ti-N)	5×10^5
Gold	6×10^5
All other (unless otherwise specified)	2×10^5

Maximum current densities shall be calculated using current and cross section areas which are determined as follows.

a) Use a current value equal to the maximum continuous current (at full fan-out for digitals or at the maximum load for linears) or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value. Currents shall be calculated on the assumption that currents flow uniformly through the conductor's cross section driven by the maximum recommended operating voltage.
b) Use the minimum allowed metallization thickness within the range specified in the manufacturing specification and controls.
c) Use the minimum actual design metallization widths, not mask widths, including appropriate allowance for narrowing or undercutting experienced in metal etching.
d) Areas of the barrier metals and nonconductive materials shall not be included in the calculation of the metallization cross section.
e) Use the cross section obtained from steps b) through d) multiplied by 0.75 for calculation of the maximum current density to compensate for reduction of the metallization cross section due to thinning, bond or scratches.

A.2.1.2 Glassivation

Unless otherwise specified in detail specification, all semiconductor chips shall be glassivated. The glassivation thickness shall be a minimum of 0.40μm for SiO_2 or a minimum of 0.20μm for Si_3N_4 unless otherwise specified in the detail specification. The glassivation shall cover all conductor surfaces except for bonding pads.

A.2.1.3 Semiconductor Chip Thickness

Unless otherwise specified in detail specification, the minimum semiconductor chip thickness shall be 0.15mm.

A.2.1.4 Plating for Back Surface of Semiconductor Chip

When the back surface of semiconductor chip is plated with gold, the thickness shall be between 0.10μm and 1.00μm. Electrolytic plating shall not be used for back surface of semiconductor chips.

A.2.1.5 Radiation Hardness Assurance

Semiconductor chips used for radiation hardened hybrid ICs shall pass the lot evaluation test of subgroup 4 in Tables A-2 to Table A-4.

A.2.2 Lot Evaluation

The manufacturer shall perform the lot evaluation test specified in Tables A-2 to A-4 for each wafer lot. Unless otherwise specified in the detail specification, Table A-2 shall be applied. Table A-3 or Table A-4, which performs some tests as in-process tests of hybrid ICs, may be applied when semiconductor chips are mounted such that they can be characterized as separate chips. In this case, tests specified in Table A-3 shall be performed for subassembly parts. Tests specified in Table A-4 shall be performed for semi-assembly products of hybrid ICs. Paragraph A.2.3 may apply to MIL, ESA and JAXA qualified semiconductor chips.

A.2.2.1 Samples and Sampling Plan

a) Samples for the lot evaluation test shall be as follows:
   1) Class I hybrid IC
      Samples shall be randomly selected from semiconductor chips produced from the single wafer lot.
   2) Class II hybrid IC
      Samples may be randomly selected from semiconductor chips produced from several wafer lots. When SOI chips are used, single event immunity of each wafer lot shall be evaluated.

b) Samples for the subgroups 2c) and 2d) shall be prepared using the same materials and techniques of semiconductor mounting and wire bonding as those used in the hybrid IC.

c) Unless otherwise specified in detail specification, samples for the subgroups 3, 4a) and 5 of Table A-2, subgroups 3, 4a) and 5 of Table A-3 and subgroups 4a) and 5 of Table A-4 shall be packaged and sealed in compliance with paragraph 3.3.8 except for the requirement specified in paragraph 3.3.8c.

A.2.2.2 Failure and Reevaluation

If the lot evaluation test failed because of an equipment failure or an operator error, the cause and problem shall be documented in detail and the failed chips can be replaced with chips made from the same wafer. The replaced chips must pass all tests conducted previously with the failed chips. The remaining tests shall then be conducted.

A.2.2.3 Evaluation Test Records

Records of lot evaluation tests shall contain a minimum of the following items and be managed in accordance with a quality assurance program specified in paragraph 3.2.1.

a) Test items
b) Document number and established date of test procedures
c) Quantity of passed and failed products
d) Date of test and name or identification code of the operator
e) Miscellaneous test records (e.g., temperature charts)
f) Quantitative data of electrical parameter tests

A.2.3 Lot Evaluation for MIL, ESA and JAXA Qualified Semiconductor Chips

When a manufacturer wishes to procure the semiconductor chips corresponding to a) or b) specified below in accordance with paragraph C.3.3, Appendix C of MIL-PRF-38534 a) or b), ESCC-5000 or ESCC-9000 qualified products c) and JAXA qualified products d) or e), subgroups 2b) Inspection for external dimensions (semiconductor chips), d) Die shear strength test, 4a) Radiation hardness test (1) and 5a) Electrostatic discharge sensitivity test (1) of Table A-2 shall be performed as the lot evaluation.
The test shall be performed as specified in paragraphs A.2.2.1, A.2.2.2 and A.2.2.3.

a) JANKC discrete semiconductor MIL-PRF-19500 qualified chip (listed on QML-19500) or MIL-PRF-38535 Class V qualified chip (listed on QML-38535).
b) MIL-PRF-19500 qualified chip (listed on QML-19500) other than JANKC discrete semiconductor. Or chips other than Class V but qualified under MIL-PRF-38535 (listed on QML-38535) and which has been tested and passed the evaluation test in accordance with Table C-II, Class K, Appendix C of MIL-PRF-38534.
c) ESCC-5000 or ESCC-9000 qualified Level 1 chip
d) JAXA-QTS-2010 qualified chip
e) JAXA-QTS-2030 qualified chip

Note: (1) The radiation hardness test and/or electrostatic discharge sensitivity test may be exempted when the semiconductor chips listed on QML-19500 and QML-38535, ESCC-5000 or ESCC-9000 qualified chips and JAXA-QTS-2010 or JAXA-QTS-2030 qualified chips meet the requirements of hybrid IC.

A.2.3.1 Notice of Acquisition

The following items must be specified in the procurement specification for acquisition of semiconductor chips.

a) Requirements of the radiation hardness test and the electrostatic discharge sensitivity test, if required.
b) Following data records
    1) Certificate of compliance
    2) Test results indicating the conformance to a) to e) of paragraph A.2.3, and/or results of lot evaluation (figures and/or measurements)

Table A-2. Lot Evaluation Test for Semiconductor Chips

Sub-group	Test item	Test method/conditions[1]	Sample size (accept no.)
1	a) DC parameters	As specified in the procurement specification.	100%
	b) Visual inspection	2010[2] 2072[3] and 2073[3]	100%
2	a) SEM inspection	As specified in the procurement specification.	As specified in the procurement specification.
	b) Inspection for external dimensions (semiconductor chip)	As specified in the procurement specification.	3 (0)
	c) Bond strength	2011	3 (0)[4]
	1) Thermocompression	1) Condition C or D	
	2) Ultrasonic	2) Condition C or D	
	3) Flip-chip	3) Condition F	
	4) Beam lead	4) Condition H	
	5) Thermosonic	5) Condition C or D	
	6) Resistance welding	6) Condition C or D	
	d) Die shear strength	2019	3 (0)
3[5]	a) Stabilization bake	1008/Condition C	10 (0)
	b) Temperature cycling	1010/Condition C	
	c) Electrical parameter test	As specified in the procurement specification.	
	d) High temperature reverse bias life test[6]	As specified in the procurement specification (72 hrs. at 150ºC).	
	e) Electrical parameter test[6]	As specified in the procurement specification.	
	f) Steady-state operating life test	As specified in the procurement specification (min. 240 hrs. at 125ºC).	
	g) Electrical parameter test	As specified in the procurement specification.	
4[6]	a) Total dose test	1019, and as specified in the procurement specification.	5 (0)
	b) Single event test (expect for power, discrete semiconductor)	As specified in ASTM F 1192, JESD 57, 1080[3] or procurement specification.	As specified in the procurement specification.
	c) SEB test (power, discrete semiconductor)	1080[3]	As specified in the procurement specification.
	d) SEGR test (power, discrete semiconductor)	1080[3]	As specified in the procurement specification.
5[6] [7]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0)[8]

Notes:

[1] Four-digit number refers to the test method number used in MIL-STD-883.

[2] Condition A shall be applied for class I hybrid IC. Condition B shall be applied for class II hybrid IC.

(3) The number refers to the test method number used in MIL-STD-750.

(4) 15 samples of wire or bonding shall be tested for each semiconductor chip. When sample size is less than 15, all samples shall be tested.

(5) These tests are only performed with the first purchase lot or when a design change has been implemented for class II hybrid IC. When the first lot of purchased parts for other hybrid ICs is already evaluated, these tests are not needed (not considered as first procurement lot).

(6) The tests shall be performed when specified in the procurement specification.

(7) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other hybrid ICs is already evaluated, these tests are not needed (not considered as first procurement lot).

(8) The sample size is applied for identical pin combination.

Table A-3. Lot Evaluation Test for Semiconductor Chips at Subassembly level

Sub-group	Test item	Test method/conditions[1]	Sample size (accept no.)
1	a) DC parameters	As specified in the procurement specification.	100%
	b) Visual inspection	2010[2] 2072[3] and 2073[3]	100%
2	a) SEM inspection	As specified in the procurement specification.	As specified in the procurement specification.
	b) Inspection for external dimensions (semiconductor chip)	As specified in the procurement specification.	3 (0)
	c) Bond strength	2011	3 (0)[4]
	1) Thermocompression	1) Condition C or D	
	2) Ultrasonic	2) Condition C or D	
	3) Flip-chip	3) Condition F	
	4) Beam lead	4) Condition H	
	5) Thermosonic	5) Condition C or D	
	6) Resistance welding	6) Condition C or D	
	d) Die shear strength	2019	3 (0)
3[5][6]	a) Stabilization bake[7]	a) 1008/Condition C (24 hours at 150ºC)	100%
	b) Temperature cycling	b) 1010/Condition C (10 minutes at -65ºC, 10 minutes at +150ºC)	
	c) Sealing test	c) 1014[8]	
	d) Particle Impact Noise Detection Test	d) 2020/Condition A	
	e) Radiograph inspection	e) 2012 only for Y-axis	
	f) Interim electrical parameter test (Ta=25 ºC)	f) As specified in the detail specification[9]	
	g) Burn-in	g) As specified in 1015 and the detail specification. Class I: 240 hours at minimum 125ºC Class II: 168 hours at minimum 125ºC	
	h) Final electrical parameter test (Ta=25 ºC)	h) As specified in the detail specification[9].	
	i) External visual inspection	i) 2009	
4[10]	a) Total dose test	1019, and as specified in the procurement specification.	5 (0)
	b) Single event test (expect for power, discrete semiconductor)	As specified in ASTM F 1192, JESD 57, 1080[3] or procurement specification.	As specified in the procurement specification.
	c) SEB test (power, discrete semiconductor)	1080[3]	As specified in the detail specification.
	d) SEGR test (power, discrete semiconductor)	1080[3]	As specified in the detail specification.
5[10][11]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0)[12]

Notes:

(1) Four-digit number refers to the test method number used in MIL-STD-883.

(2) Condition A shall be applied for class I hybrid IC. Condition B shall applied for class II hybrid IC.

(3) The number refers to the test method number used in MIL-STD-750.

(4) 15 samples of wire or bonding shall be tested for each semiconductor chip. When sample size is less than 15, all samples shall be tested.

(5) Unless otherwise allowed, the test items shall be performed in this order.

(6) Semiconductor chips shall be sealed and package shall be mounted by the manufacturer.

(7) This test may be performed before sealing.

(8) Only the gross leak test shall be performed. Test condition C1 shall apply except for the vacuum/pressurization cycles.

(9) When specified in the detail specification, changes of electrical parameter measurements between pre- and post-burn-in test shall be calculated. If the changes exceed the specified delta limits, the product shall be rejected. For class I subassembly parts, the PDA (percent defective allowable) of the burn-in test shall be 5% for all failures (same failure mode) (a single failure is allowed) and 3% for functional failures (a single failure is allowed). For class II subassembly parts, the PDA of the burn-in test shall be 5% for all failures (same failure mode) (a single failure is allowed). The lots that failed to meet these PDA requirements shall be disposed in accordance with paragraph B.3.2.

(10) The tests shall be performed when specified in the procurement specification.

(11) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other hybrid ICs is already evaluated, these tests are not needed (not considered as first procurement lot).

(12) The sample size is applied for identical pin combination.

Table A-4. Lot Evaluation Test for Semiconductor Chips at Semi- Assembly Hybrid ICs Level

Sub-group	Test item	Test method/conditions[1]	Sample size (accept no.)
1	a) DC parameters	As specified in the procurement specification.	100%
	b) Visual inspection	2010[2] 2072[3] and 2073[3]	100%
2	a) SEM inspection	As specified in the procurement specification.	As specified in the procurement specification.
	b) Inspection for external dimensions (semiconductor chip)	As specified in the procurement specification.	3 (0)
	c) Bond strength	2011	3 (0)[4]
	1) Thermocompression	1) Condition C or D	
	2) Ultrasonic	2) Condition C or D	
	3) Flip-chip	3) Condition F	
	4) Beam lead	4) Condition H	
	5) Thermosonic	5) Condition C or D	
	6) Resistance welding	6) Condition C or D	
	d) Die shear strength	2019	3 (0)
3[5][6][7]	a) Internal visual inspection b) Interim electrical parameter test (Ta=25 ºC) c) Burn-in test	b) Group A Subgroups 1, 4, 7, 9[8] c) As specified in 1015 and the detail specification. Class I: 240 hours at minimum 125ºC Class II: 168 hours at minimum 125ºC.	100%
	d) Final electrical parameter test (Ta=25 ºC) e) Internal visual inspection	d) Group A Subgroups 1, 4, 7, 9[8]	
4[9]	a) Total dose test	1019, and as specified in the procurement specification.	5 (0)
	b) Single event test (expect for power, discrete semiconductor)	As specified in ASTM F 1192, JESD 57, 1080[3] or procurement specification.	As specified in the procurement specification.
	c) SEB test (power, discrete semiconductor)	1080[3]	As specified in the detail specification.
	d) SEGR test (power, discrete semiconductor)	1080[3]	As specified in the detail specification.
5[9] [10]	a) Electrostatic discharge sensitivity test	3015; Pin combination and the electrical parameters before and after testing shall be as specified in the procurement specification.	3 (0)[11]

Notes:

[1] Four-digit number refers to the test method number used in MIL-STD-883.

[2] Condition A shall be applied for class I hybrid IC. Condition B shall applied for class II hybrid IC.

[3] The number refers to the test method number used in MIL-STD-750.

(4) 15 samples of wire or bonding shall be tested for each semiconductor chip. When sample size is less than 15, all samples shall be tested.

(5) Unless otherwise allowed, the test items shall be performed in this order.

(6) Since test sample is unsealed, burn-in test shall be performed in inert gas atmosphere.

(7) Semiconductor chips shall be mounted on the substrate by the QML manufacturer.

(8) When specified in the detail specification, changes of electrical parameter measurements between pre- and post-burn-in test shall be calculated. If the changes exceed the specified delta limits, the product shall be rejected. For class I semi-assembly hybrid IC, the PDA (percent defective allowable) of the burn-in test shall be 5% for all failures (same failure mode) (a single failure is allowed) and 3% for functional failures (a single failure is allowed). For class II semi-assembly hybrid IC, the PDA of the burn-in test shall be 5% for all failures (same failure mode) (a single failure is allowed). The lots that failed to meet these PDA requirements shall be disposed in accordance with paragraph B.3.2.

(9) The tests shall be performed when specified in the procurement specification.

(10) These tests are only performed with the first purchase lot or when a design change has been implemented. When the first lot of purchased parts for other hybrid ICs is already evaluated, these tests are not needed (not considered as first purchase lot).

(11) The sample size is applied for each pin combination.

APPENDIX B

PROCEDURE FOR SCREENING

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APPENDIX B

PROCEDURE FOR SCREENING

B.1. Scope

This appendix establishes the screening test procedure.

B.2. General Test Conditions

The screening test shall be performed under the general test conditions specified herein.

B.2.1 Environmental Conditions

Unless otherwise specified in the detail specification, all inspections shall be performed at ambient temperatures between 20 and 30°C, relative humidity between 20 and 90% and atmospheric pressure between 86.7 and 106.7kPa. Whenever the specified parameters must be closely controlled to obtain reproducible results, the test shall be performed using appropriate control center values and tolerance parameters as established in the detail specification and quality assurance program.

B.2.1.1 Constant Temperature Chamber

The performance of the constant temperature chamber used for the stabilization baking and burn-in tests shall satisfy the following requirements.

a) Temperature distribution in the operating temperature range
Temperature distribution in the operating temperature range shall be 6°C or 6% of the set temperature, whichever is greater.

b) Temperature variation in the operating temperature range
Temperature variation in the operating temperature range shall be ±2°C or ±4% of the set temperature, whichever is greater.

B.2.2 Orientations

The hybrid IC orientation for tests that require application of external mechanical forces shall be as shown in Figure B-1.

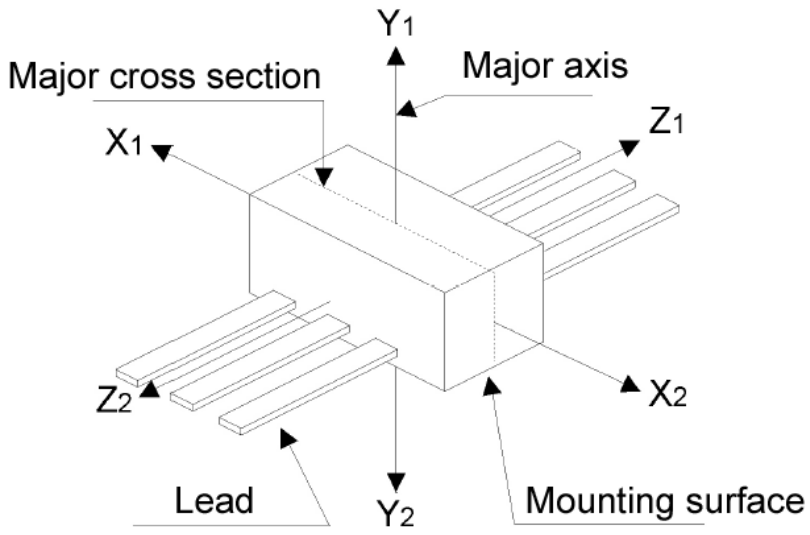


Figure B-1. Orientation

Remark: Y_1 is a force to lift the semiconductor chip off the substrate or the wires off the semiconductor chip.

B.2.3 Test Frequency

Unless otherwise specified in the detail specification, the electrical tests shall be performed at the lowest and highest frequencies of the specified range when the frequency range is specified.

B.2.4 Accuracy

Unless otherwise specified in the detail specification, the specified tolerances are for true values under specified test conditions. The manufacturer shall define appropriate tolerances in the quality assurance program or the detail specification based on the accuracy (for test conditions and measurements) of their test apparatus.

B.3. Procedure for Screening Test

Unless otherwise specified in the detail specification, all hybrid ICs in the inspection lot shall be subject to screening tests under the conditions specified in paragraph B.2 and the screening tests shall be performed in accordance with Table B-1. Additional tests for the particular hybrid ICs that are required to effectively perform screening shall be defined in the detail specification. After completion of the seal test, lead forming that may adversely affect hermeticity shall not be performed except for minor modifications such as correction of lead tips.

B.3.1 Disposition of Rejected Lots

If a product failed any of the screening tests, it shall be identified as a defective product and disposed. A product that failed the electrical tests and is to be used in subgroups of the qualification test or quality conformance inspection in which electrically defective products can be used shall be properly identified and returned to the inspection lot for exposure to the same thermal environments as those applicable to good samples.

B.3.2 Burn-in and Reverse Bias Burn-in Screen Failures and Reselection

The products that failed to satisfy the specified PDA (percent defective allowable) for the burn-in or reverse bias burn-in tests shall be disposed in accordance with paragraph B.3.1. The inspection lot may be used for the remaining screening tests by re-selecting the samples only once per the following procedures.

a) Percent defective does not exceed twice the specified PDA (for all failures).
b) Failure analysis is performed in accordance with the Failure Analysis Program (in paragraph C.4.6.1, Appendix C of JAXA-QTS-2000) and failure causes are specified.
c) Specified failure causes and re-selecting are reviewed at TRB, consulted between JAXA and the purchaser and approved.

The PDA of reselection shall be 3% for all failures (or for one failure, whichever is greater) and 2% for functional failures (or for one failure, whichever is greater).

B.3.3 Failures Due to Test Apparatus Failure or Operator Error

If a product failed the burn-in test due to test apparatus failure or operator error, which resulted in a lot failure, the screening test may be continued. To continue the screening test, the manufacturer shall record the failure with detailed description of reasons and conduct a failure analysis (in accordance with paragraph C.4.6.1 of JAXA-QTS-2000) and the TRB must have determined the remaining products are free from any damage or degradation.

B.3.4 Records of Screening Tests

The screening records shall include a minimum of the following items and shall be controlled in accordance with paragraph 3.2.1.

a) Test item
1) Inspection lot identification code
2) Document number and established date of test instructions
3) Quantity and disposition of passed and failed hybrid ICs
4) Inspection date and operator’s name or identification code
5) Measurements of electrical parameters before and after the burn-in test or reverse bias burn-in when specified in the detail specification. (This data shall be traced to each hybrid IC by serial number.)

Table B-1. Screening Test

Order	Test item[3]	Test method/condition[1] [2]	Class I Hybrid IC	Class II Hybrid IC
1	Stabilization bake[4]	1008/C (24 hours at 150ºC)	X	X
2	Temperature cycling	1010/C	X	X
3	Constant acceleration or mechanical shock	2001/B[5], Y_1 direction only 2002/B, Y_1 direction only[6] or 213/C, Y_1 direction only [7]	X	X
4	Visual inspection	[8]	X	X
5	Particle Impact Noise Detection test	2020/A	X	X
6	(Blank)			
7	Radiographic inspection	2012, Y direction only	X	
8	Interim electrical parameters (subgroups 1, 4, 7 and 9, Group A, pre burn-in Appendix C)	In accordance with the detail specification. [9]	X	X
9	Burn-in test	1015, in accordance with the detail specification.	X (240Hr, Min 125℃)	X (168Hr, Min 125℃)
10	Interim electrical parameters (subgroups 1, 4, 7 and 9, Group A, post burn-in Appendix C)	In accordance with the detail specification. [9]	X	X
11	Reverse bias burn-in test[10] [11]	1015, in accordance with the detail specification.	X (240Hr, Min 125℃)	X (168Hr, Min 125℃)
12	Interim electrical parameters (subgroups 1, 4, 7 and 9, Group A, post reverse bias burn-in, Appendix C)	In accordance with the detail specification. [9]	X	X
13	Seal	1014	X	X
14	Final electrical parameter test a) Static test 1) 25ºC (subgroup 1, Group A, Appendix C) 2) Maximum and minimum operating temperature (subgroups 2 and 3, Group A, Appendix C) b) Dynamic test 1) 25ºC (subgroup 4, Group A, Appendix C) 2) Maximum and minimum operating temperature (subgroups 5 and 6, Group A, Appendix C) c) Functional test 1) 25ºC (subgroup 7, Group A, Appendix C) 2) Maximum and minimum operating temperature (subgroup 8, Group A, Appendix C) d) Switching test 1) 25ºC (subgroup 9, Group A, Appendix C) 2) Maximum and minimum operating temperature (subgroups 10 and 11, Group A, Appendix C)	In accordance with the detail specification [12].	X	X
15	External visual	2009	X	X

Notes:

[1] Four-digit number refers to the test method number specified in MIL-STD-883.

[2] Three-digit number refers to the test method number used in MIL-STD-202.

(3) Unless otherwise allowed, the test items shall be performed in this order.
(4) The test may be performed immediately before sealing.
(5) Use condition A when the internal sealing of the package exceeds 50.8mm.
(6) Applied to hybrid ICs not consisting of sheet transformer.
(7) Applied to hybrid ICs consisting of sheet transformer.
(8) The hybrid ICs are inspected for damages such as any loss of leads, damage to the package and separation of lids.
(9) When specified in the detail specification, the variation of electrical parameter measurements between pre- and post-burn-in test shall be calculated for class I hybrid IC. If a variation exceeds the specified delta limits, the hybrid IC shall be rejected. For class II hybrid IC, calculation of the variation of electrical parameter measurements are not applied. The PDA of the burn-in test of class I hybrid IC shall be 5% on all failures (one failure is allowed) and 3% on functional failures (one failure is allowed). The PDA of the burn-in test of class II hybrid IC shall be 10% on all failures (one failure is allowed) and 3% on functional failures (one failure is allowed). The lots that fail to pass these requirements shall be disposed of in accordance with paragraph B.3.2.
(10) The order of the burn-in and reverse bias burn-in tests may be changed.
(11) This test shall be performed when specified in the detail specification. If not specified, this test and subsequent interim electrical tests (post reverse bias burn-in) may be exempted.
(12) Subgroups, in which electrical parameters of the products are not included, may be exempted.

APPENDIX C

PROCEDURES FOR
QUALIFICATON TEST AND
QUALITY CONFORMANCE INSPECTION

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX C

PROCEDURES FOR QUALIFICATION TEST AND QUALITY CONFORMANCE INSPECTION

C.1. Scope

This appendix establishes the procedures for the qualification test and quality conformance inspection.

C.2. General Test Conditions

The qualification test and quality conformance inspection shall be performed under the following conditions.

C.2.1 Environmental Conditions

Unless otherwise specified in the detail specification, all tests shall be performed at ambient temperatures between 20 and 30°C, relative humidity between 20 and 90% and atmospheric pressure between 86.7 and 106.7kPa. Whenever the parameters specified herein must be closely controlled in order to obtain reproducible results, the test shall be performed using appropriate control center values and tolerance parameters established in the quality assurance program.

C.2.1.1 Constant Temperature Chamber

The performance of the constant temperature chamber used for the steady-state life test shall meet the following requirements.

a) Temperature distribution in the operating temperature range
Temperature distribution in the operating temperature range shall be 6°C or 6% of the set temperature, whichever is greater.

b) Temperature variation in operating temperature range
Temperature variation in the operating temperature range shall be ±2°C or ±4% of the set temperature, whichever is greater.

C.2.2 Orientations

The hybrid IC orientation for tests that require application of external mechanical forces shall be as shown in Figure C-1.

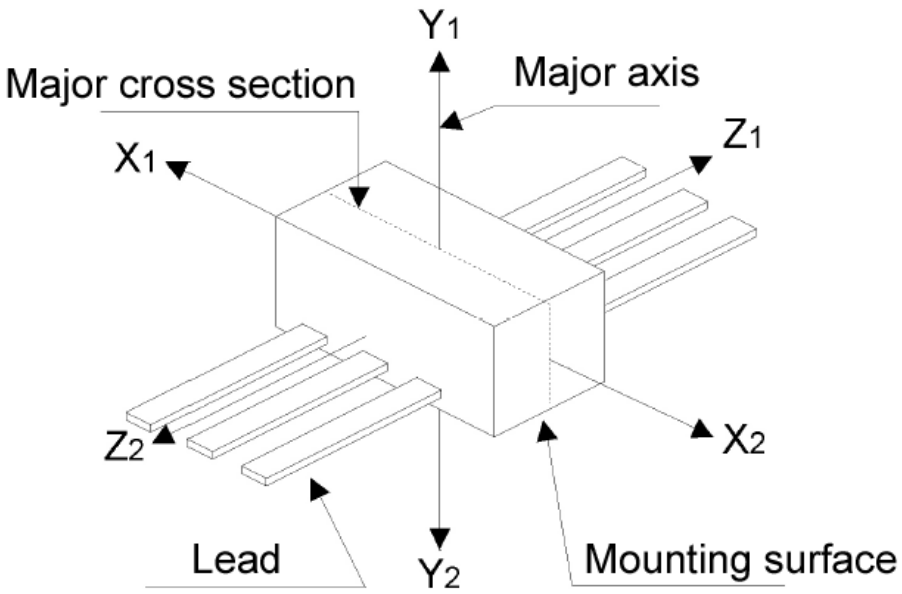


Figure C-1. Orientation

Remark: Y_1 is a force to lift the semiconductor chip off the substrate or the wires off the semiconductor chip.

C.2.3 Test Frequency

Unless otherwise specified in the detail specification, the electrical tests shall be performed at the lowest and highest frequencies of the specified range when a frequency range is specified.

C.2.4 Accuracy

Unless otherwise specified in the detail specification, the specified tolerances are for true values under specified test conditions. The manufacturer shall define appropriate tolerances in the quality assurance program or the detail specification based on the accuracy (for test conditions and measurements) of their test apparatus.

C.3. Procedures for Qualification Test and Quality Conformance Inspection

The qualification test and quality conformance inspection shall be performed under the conditions of paragraph C.2 and in accordance with the procedures specified below.

a) Qualification Test
   Qualification test shall be performed using evaluation circuits or samples manufactured by design, construction, materials and manufacturing line for qualification (refer to paragraph 4.6.1) under the conditions of paragraph C.2 and in accordance with paragraphs C.3.1 and C.3.2. Level I shall be applied.
b) Quality Conformance Inspection

1) For first article, quality conformance inspection shall be performed under the conditions of paragraph C.2 and in accordance with paragraphs C.3.1 and C.3.3. Level I shall be applied.
2) For non-first article, quality conformance inspection shall be performed under the conditions of paragraph C.2 and in accordance with paragraphs C.3.1 and C.3.3. Level II shall be applied.

C.3.1 Sampling

The qualification test and quality conformance inspection are sampling tests or inspections using samples taken from an inspection lot. When the LTPD is specified as the sampling level, the sampling shall be performed as specified in Appendix D. When both the sample size and accept number are specified, sampling shall be performed in accordance with the sampling procedures of Appendix D with the exception of sample size and accept number determination.
If samples are damaged due to test apparatus failure or operator error, the damaged samples may be substituted with spare samples (paragraph C.3.4.2). The order of using these spare samples shall be specified in advance.

C.3.2 Qualification Test Procedures

The qualification test shall be performed in accordance with Tables C-1, C-2, C-3, C-4 and C-5 (the Groups A, B, C, D and E tests) for products of an inspection lot manufactured in accordance with the quality assurance program for hybrid IC and which have passed the screening test. Sampling for the Groups A, B, C, D and E test shall be conducted using Level I in Tables.
Unless otherwise specified in the detail specification, subgroups of the same test group may be performed in any order, but individual tests within a subgroup shall be performed in the order shown in Tables C-2, 3, 4 and 5 except for all subgroups of Group A and subgroup 2 of Group B tests.
Samples subjected to the non-destructive test may be subjected to other subgroups.

C.3.2.1 End-Point Electrical Parameter Test

End-point electrical parameters shall be measured in advance for subgroups that require the end-point electrical parameter test in the qualification test.
If the end-point electrical parameter measurements are not specified in the detail specification, parameters for the final electrical parameter test of the screening test shall be measured.

C.3.2.2 Sample Allocation

When an inspection lot consists of multiple inspection sublots, the number of samples taken from each inspection sublot shall be equal (or as equal as possible) for each subgroup of Group B, C and D tests. However, a minimum of one sample shall be

used for the Group B tests. A minimum of five and two samples shall be used for the subgroups 1 and 2 of Group C tests, respectively.

C.3.3 Procedure for Quality Conformance Inspection

All inspection lots to be delivered in accordance with this specification shall pass the quality conformance inspection in accordance with Tables C-1, C-2, C-3, C-4 and C-5 (Groups A, B, C, D and E tests), except as specified in paragraph C.3.3.2. For first article, level I shall be applied. For non- first article, level II shall be applied. Unless otherwise specified in the detail specification, the subgroups in the same test may be performed in any order, but individual tests within a subgroup shall be performed in the order shown in Tables C-2, C-3, C-4 and C-5, except for all subgroups of Group A and subgroup 2 of Group B tests. Samples subjected to the non-destructive tests may be subjected to other subgroups.

C.3.3.1 End-Point Electrical Parameter Test

The end-point electrical parameter test shall be performed in accordance with paragraph C.3.2.1.

C.3.3.2 Exemption of Groups C, D and E Tests

When one of the following conditions is satisfied, the Group C, D or E test may be exempted by utilizing test data.

a) Exemption of Group C test by utilization of data
Unless otherwise specified in the detail specification, the following cases are allowable.
For class I hybrid IC, when the Group C quality conformance inspection of a hybrid IC of the same type (having the same individual identification of the part number) was initiated within a year from the completion date of the successful screening test or inspection, the test data may be utilized as a valid data for this lot.
For class II hybrid IC, when the Group C quality conformance inspection of a class I or class II hybrid IC of the same type (having the same individual identification of the part number) was initiated within a year from the completion date of the successful screening test or inspection, the test data may be utilized as a valid data for this lot.

b) Exemption of Group D Tests by utilization of data
When the Group D quality conformance inspection of a hybrid IC having a same package type (including lead finish) was initiated within a year from the completion date of the successful screening test or inspection, the test data may be utilized as a valid data for this lot.
Since test items and test conditions of class I hybrid IC Group D tests are identical to those of class II hybrid IC Group D tests, Group D tests for class II

hybrid IC can be considered as Group D tests for class I hybrid IC having a same package type (including lead finish).

c) Exemption of Group E tests by utilization of data
Unless otherwise specified in the detail specification, the Group E tests may be exempted when the hybrid ICs, which were manufactured from the semiconductor chips of the same wafer lot and design, construction and performance are identical to hybrid ICs to be submitted to quality conformance inspection, have passed the Group E tests (If wafer lot of some semiconductor chips composing hybrid IC is different, each semiconductor chip of different wafer lot shall be tested).
When radiation hardness test is performed for each semiconductor chip, and if hybrid ICs manufactured from the semiconductor chips of the same wafer lot have passes the test, the existed data may be utilized as a valid data for this lot.

C.3.3.3 Sample Allocation

Samples shall be allocated to Groups A, B, C, D and E tests in accordance with the following paragraphs.

C.3.3.3.1 Group A Test

When an inspection lot consists of multiple inspection sublots, the number of samples taken from each inspection sublot shall be equal (or as equal as possible) for each subgroup of the Group A test.

C.3.3.3.2 Group B Test

When an inspection lot consists of multiple inspection sublots and if any sublot of an inspection lot has passed a subgroup of the Group B test, other inspection sublots shall be considered to have passed the subgroup. Therefore, samples from any single inspection sublot may be used for each subgroup of the Group B test.

C.3.3.3.3 Group C Test

When an inspection lot consists of multiple inspection sublots and if any sublot of an inspection lot has passed a subgroup of the Group C test, other inspection sublots shall be considered to have passed the subgroup. Therefore, samples from any single inspection sublot may be used for each subgroup of the Group C test.
Unless otherwise specified in the detail specification, the inspection lot for the Group C test shall have passed the Group A test. The result of the Group C test shall remain valid even if the lots fail the Group B, D or E test.

C.3.3.3.4 Group D Test

When an inspection lot consists of multiple inspection sublots and if an inspection sublot of the inspection lot has passed a subgroup of the Group D test, other sublots (all the sublots of the same package type) shall be considered to have passed the subgroup. Therefore, samples from any single inspection sublot may be used for each subgroup of the Group D test.
Unless otherwise specified in the detail specification, electrically defective products in the same inspection lot or empty packages of the same type may be used. The result of the Group D test shall remain valid even if the lots failed the Groups B, C or E test.

C.3.3.3.5 Group E Test

This test shall be performed for each inspection sublot. When an inspection lot consists of hybrid ICs manufactured using semiconductor chips from a single wafer lot and if any sublot of an inspection lot has passed the Group E test, all of the inspection sublots shall be considered to have passed the Group E test.
Unless otherwise specified in the detail specification, inspection lots for the Group E test shall have passed the Group A test prior to the performance of the Group E tests. The results of the Group E test are valid even if the lots fail the Group B, C or D tests.

C.3.4 Criteria for Pass/Fail

When a lot passed all test items, the lot shall pass the qualification test or quality conformance inspection. When any lot has failed during any subgroup tests of the qualification test, the manufacturer shall dispose of the products in the inspection lot in accordance with paragraph C.3.5, cancel the tests, and follow the procedure specified in paragraph 3.4.1.6 of JAXA-QTS-2000.
When any lot has failed during any subgroups of the quality conformance inspection, the manufacturer shall dispose of the products in the inspection lot in accordance with paragraph C.3.5.

C.3.4.1 Reevaluation

When any lot has failed during any subgroups of the quality conformance inspection, the samples reselected from the failed lot may be used for retest unless the lot failed in the subgroups of 2b), 2c), 2d) or the Group C tests. This retest may be done only once and shall be as follows.

a) When any lot has failed in subgroup 1, 2a), or 4 of the Group B test, it may be resubmitted for re-test. The sample size for the failed subgroup shall be doubled. No failure is allowed.
b) When any lot has failed in subgroups of the Group B test other than those specified in a) above or subgroups of Groups A, D and E tests, the lot shall be subjected to a failure analysis specified in paragraph 3.6.1 of JAXA-QTS-2000.

A retest may only continue when the TRB has determined that the failure pertains to one of the following categories.

1) Random failures which are not related to basic design or processes.
2) Failures due to defects that can be effectively removed by re-screening the entire lot.

C.3.4.2 Failure Due to Test Equipment Failure or Operator Error

If a sample failed due to test apparatus failure or operator error, which resulted in lot rejection in the qualification test and quality conformance inspection, a product from the same inspection lot shall be used as a substitute sample. To use a substitute sample, the manufacturer shall perform a failure analysis in accordance with paragraph 3.6.1 of JAXA-QTS-2000 and the TRB must have determined that the failure was caused due to test apparatus failure or operator error. The substitute hybrid IC shall pass all tests that were performed with the failed samples prior to subsequent tests.

C.3.5 Post-Test Disposition of Sample

Products shall be properly identified as defective and disposed of, if used in the destructive tests (paragraph C.3.5.1) of the Group B, C, D or E test, have failed any test, or are in rejected lots.
The samples subjected to qualification tests or quality conformance inspection shall not be delivered. The samples which have only performed and passed Group A test may be delivered.

C.3.5.1 Destructive Test

Unless otherwise specified in the detail specification, the following tests shall be categorized as destructive tests.

a) Solderability
b) Thermal shock test
c) Lead integrity
d) Moisture resistance
e) Electrostatic discharge sensitivity test
f) Radiation hardness test (total dose test)
g) Radiation hardness test (single event test)
h) Radiation hardness test (SEB test)
i) Radiation hardness test (SEGR test)
j) All tests and inspections that require disassembling hybrid IC

All other tests and inspections other than the ones defined as non-destructive (paragraph C.3.5.2) shall initially be treated as destructive. However, if sufficient data is provided, it may be changed and treated as a non-destructive test. A test is considered non-destructive if repeated five times using the same samples and all

samples pass every run of the test without any indication of cumulative degradation or failure.

C.3.5.2 Non-Destructive Test

Unless otherwise specified in the detail specification, the following tests shall be categorized as non-destructive tests.

a) Electrical parameter test
b) Steady-state operating life test
c) Constant acceleration
d) External dimensions
e) Seal test
f) Visual inspection
g) Particle impact noise detection (PIND) test
h) Radiography inspection

C.3.6 Radiation Hardness Test

A minimum of the following requirements shall be specified in the detail specifications for a radiation hardness test (Group E).

C.3.6.1 Total Dose Test

a) Radiation hardness assurance level
The radiation hardness assurance level specified in paragraph 1.3.5 shall be defined.
b) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the irradiation shall be defined.
c) Conditions during irradiation to end-point electrical parameter measurements
The time, including the annealing period, from irradiation to post-irradiation measurements shall be defined.
d) Bias circuit
The manufacturer shall define the bias circuit for the radiation hardness test.

C.3.6.2 Single Event Test

a) Type of single event phenomena and threshold value
Type of single event phenomena and threshold value shall be defined.
b) Sample
Samples (products or evaluation circuits) for single event test shall be defined to associate with types of single event phenomena.
c) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the single event test shall be defined.
d) Bias circuit

The manufacturer shall define the bias circuit for the single event test.

C.3.6.3 SEB Test

a) Threshold value
Threshold values corresponding to SEB tests shall be defined.
b) Sample
Samples (products or evaluation circuits) for SEB test shall be defined.
c) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the SEB test shall be defined.
d) Bias circuit
The manufacturer shall define the bias circuit for the SEB test.

C.3.6.4 SEGR Test

a) Threshold value
Threshold values corresponding to SEGR tests shall be defined.
b) Sample
Samples (products or evaluation circuits) for SEGR test shall be defined.
c) Electrical parameters to be measured and tolerances
The end-point electrical parameters to be measured before and after the SEGR test shall be defined.
d) Bias circuit
The manufacturer shall define the bias circuit for the SEGR test.

C.3.7 Records of Qualification Test and Quality Conformance Inspection

The qualification test and quality conformance inspection records shall include a minimum of the following items and be managed in accordance with the quality assurance program specified in paragraph 3.2.1.

a) Test items
b) Inspection lot identification code
c) Document number and established date of test instructions
d) Quantity and disposition action of passed and failed products
e) Date(s) of test and operator name or identification code
f) Record associated with the tests (including temperature and relative humidity charts, and shock pulse waveforms)

The qualification test records shall also include the following items.

g) Measurement data of the Group A test that satisfies the specified LTPD (not applicable to the subgroups 7 and 8 tests of digital devices)
h) Measurement data of electrical parameters at pre- and post-test required at the end of the steady-state operating life test
i) Measurement data of external dimensions
j) Applied force at failure and failure category in bond strength testing
k) Applied force at failure and failure category in die shear testing

l) Measurement data of electrical parameters at pre- and post-test required at the end of the radiation hardness test
m) Measurements of pre- and post-test electrical parameters required at the end of the electrostatic discharge sensitivity test

Records for inspection lots of a device type initially subjected to the quality conformance inspection should also include the following items.

n) Measurement data of the Group A test that satisfy the specified LTPD (not applicable to the subgroups 7 and 8 tests for digital devices)
o) Measurements of pre- and post-test electrical parameters required at the end of steady-state operating life test

Data g) to o) shall be identified by individual product serial numbers.

Table C-1. Group A Test (1) (2) (3) (4)

(Electrical parameter tests)

Subgroup (4)			Sample size			
			Class I		Class II	
			Level I	Level II	Level I	Level II
1	Static tests	T_C = 25ºC	LTPD 5			
2	Static tests	T_C = maximum operating temperature (5)	LTPD 7			
3	Static tests	T_C = minimum operating temperature(6)	LTPD 7			
4	Dynamic tests	T_C = 25ºC	LTPD 5			
5	Dynamic tests	T_C = maximum operating temperature(5)	LTPD 7			
6	Dynamic tests	T_C = minimum operating temperature(6)	LTPD 7			
7	Functional tests	T_C = 25ºC	LTPD 5			
8	Functional tests	T_C = maximum and minimum operating temperatures(5) (6)	LTPD 10			
9	Switching tests	T_C = 25ºC	LTPD 7			
10	Switching tests	T_C = maximum operating temperature(5)	LTPD 10			
11	Switching tests	T_C = minimum operating temperature(6)	LTPD 10			

Notes:

(1) Electrical parameters, measuring conditions and tolerances shall be as specified in the detail specification.

(2) Provided that when all the electrical parameters of all subgroups of the Group A tests are measured at the final electrical parameter tests of the screening tests (Appendix B), the measurement data of the final electrical parameter test of hybrid ICs which have passed the screening test may also be used as measurement data supplied for the Group A test.

(3) Samples used for the Group A test may also be used for the Group B, C, D and E tests.

(4) The same sample may be used for all subgroups.

(5) Measurements at the maximum operating temperature shall be performed after the temperatures of all internal elements (the junction temperature for semiconductor chips) are in thermal equilibrium and the package temperature has reached at least 80% of the maximum operating temperature.

(6) Measurements at the minimum operating temperature shall be performed after the junction temperature is in the thermal equilibrium and the package temperature has reached within 20% of the minimum operating temperature.

Table C-2. Group B Test

(Product stability evaluation test)

Subgroup	Test method (1)	Test condition or criteria for pass/fail	Sample size (accept no.)			
			Class I		Class II	
			Level I	Level II	Level I	Level II
Subgroup 1(2) (3) a) External physical dimensions b) Internal gas analysis	2016 1018	In accordance with the detail specification	3 (0)			
Subgroup 2(4) a) Resistance to solvents(2) b) Internal visual and mechanical c) Bond strength 1) Thermo compression 2)Ultrasonic 3) Flip-chip 4) Beam lead 5) Thermosonic 6) Resistance welding d) Die shear test	2015 2013 2014 and 2017 (10) 2011 2019	Solvent a (1) Condition C or D (2) Condition C or D (3) Condition F (4) Condition H (5) Condition C or D (6) Condition C or D	1 (0) 2 (0) 3 (0) (5 3 (0)(6)	1 (0) 2 (0) 3 (0) (5) 3 (0) (6)	- 2 (0) 3 (0) (5) 3 (0) (6)	
Subgroup 3(2) (3) Solderability	2003	245ºC ± 5ºC	1 (0) (7)			
Subgroup 4 (2) a) Lead integrity b) Seal 1) Fine 2) Gross	2004 1014	Condition B_2 Condition A_2 Condition C_1	3 (0) (8) 3 (0) (9)			

Notes:

(1) Four-digit number refers to the test method number in MIL-STD-883.

(2) Electrically defective products from the same inspection lot may be used. When a hybrid IC containing sheet transformers is tested, a package containing only the sheet transformers may be used as a sample.

(3) When electrically defective products or a sample which package containing only sheet transformer are used, the samples shall be exposed to the same thermal environments that certified samples experience during the screening test (stabilization bake, temperature cycling and burn-in).

(4) When the Group C test was conducted using a single inspection lot, the samples used for subgroup 2 of the Group C test shall be used except for a) the resistance to solvents test.

(5) The sample size shall be 3 for hybrid IC tests. 15 samples for every type of wire or bonding of sample shall be tested. If sample size is less than 15, all samples shall be tested.

(6) The sample size shall be 3 for hybrid IC tests. All chips for each sample shall be tested. If same type of chips are included, only one chip may be tested.

(7) The sample size shall be a minimum of 1. 15 leads shall be tested. If lead size is less than 15, all samples shall be tested.

(8) For lead integrity, five leads of each sample shall be tested. If sample size is less than 5, all leads shall be tested.

(9) In the case of package of which external lead does not pierce internal cavity, seal test may be exempted.

(10) When internal visual inspection is performed in accordance with MIL-STD-883 Test Method 2017 paragraph 3.1.4 “Element Orientation”, sample categorized as ACCEPT “not preferred” shall be categorized as “Fail”.

Table C-3. Group C Test

(Die related test)

Sub-group	Test method (1)(2)	Test condition or criteria for pass/fail	Sample size (accept no.)			
			Class I		Class II	
			Level I	Level II	Level I	Level II
Subgroup 1 a) Steady-state operating life test b) End-point electrical parameter test	1005	In accordance with the detail specification (1,000 hours at the package temperature of 125ºC). 25ºC, maximum and minimum temperature (including subgroup 1-11). Details as specified in detail specification.	LTPD 10	LTPD 15(8)	12 (0)	5 (0)
Subgroup 2 a) Resistance to soldering heat (12)	2036	In accordance with detail specification.	5 (0)	-	5 (0)	-
b) External visual		In accordance with inspection criteria of method 2009.		-		-
c) Particle impact noise detection test	2020	Condition A				
d) Temperature cycling test	1010	Condition C, 100 cycles (4)				
e) Mechanical shock	2002 or 213	Condition B, Y_1 direction only(6) or condition C, 6 axes (7)				
f) Constant acceleration	2001	Condition B(5), Y_1 direction only				
g) Vibration	2007	Condition A, 3 axes				
h) Seal 1) Fine 2) Gross	1014	 Condition A_2 Condition C_1				
i) External visual		In accordance with inspection criteria of method 1010.				
j) End-point electrical parameter test(3)		25ºC, maximum and minimum temperature (including subgroup 1-11). Details as specified in detail specification.				
Subgroup 3(9) a) Electrostatic discharge sensitivity test b) End-point electrical parameter test	3015	The pin combination shall be as specified in the detail specification. 25ºC (including subgroup 1, 4, 7 and 9). Details as specified in detail specification.	3 (0)(10)	-	3 (0) (10)(11)	-

Notes:

(1) Four-digit number refers to the test method number in MIL-STD-883.

(2) Three-digit number refers to the test method number used in MIL-STD-202.

(3) This test may be performed prior to the seal test.

(4) 20 cycles for Level II.

(5) Use condition A when the internal sealing length of the package exceeds 50.8mm.
(6) Applicable to hybrid ICs not consisting of sheet transformers.
(7) Applicable to hybrid ICs consisting of sheet transformers.
(8) When the inspection lot size is less than 50, the sample size and accept number may be 5 and 0, respectively.
(9) These tests may be replaced with element tests (subgroup 5, lot evaluation test of Appendix A for semiconductor chips).
(10) The sample size shall be applied to identical pin combination.
(11) If specified in detail specification, test items may be exempted.
(12) Test conditions including temperature and time shall be specified in detail specification based on mounting condition.

Table C-4. Group D Test

(Package related tests)

Subgroup	Test method(1)	Test condition or criteria for pass/fail	Sample size (accept no.)			
			Class I		Class II	
			Level I	Level II	Level I	Level II
Subgroup 1						
a) Thermal shock	1011	Condition B, 15 cycles				
b) Moisture resistance	1004					
c) Seal	1014		5 (0)			
1) Fine		Condition A_2				
2) Gross		Condition C_1				

Note:

(1) Four-digit number refers to the test method number in MIL-STD-883.

Table C-5. Group E Test (1)

(Radiation hardness test)

Subgroup	Test method	Test condition or criteria for pass/fail	Sample size (accept no.)			
			Class I		Class II	
			Level I	Level II	Level I	Level II
Subgroup 1 a) Total dose test (2) b) End-point electrical parameter test	1019 (3)	In accordance with the detail specification. In accordance with the detail specification.	5 (0)(4) (5)			
Subgroup 2, except for power, discrete semiconductor(9) a) Single event test (7)(10) b) End-point electrical parameter test	ASTM F 1192, JESD 57 or 1080 (6)	In accordance with the detail specification. In accordance with the detail specification	4 (0) (8)	4 (0)	4 (0) (8)	4 (0) (11)
Subgroup 3, power, discrete semiconductor a) Radiation hardness test (SEB) b) End-point electrical parameter test	1080 (6)	In accordance with the detail specification.	3 (0)	-	3 (0)	-
Subgroup 4, power, discrete semiconductor a) Radiation hardness test (SEGR) b) End-point electrical parameter test	1080 (6)	In accordance with the detail specification.	3 (0)	-	3 (0)	-

Notes:

(1) Test shall be conducted only when specified in the detail specification.

(2) When the radiation hardness test is performed at semiconductor chip level, it shall be performed in accordance with paragraph A.2.1.5.

(3) Four-digit number refers to the test method number in MIL-STD-883.

(4) Sample size and accept number shall be applied to each inspection sublot. When multiple inspection sublots are made from a single wafer lot, a single sublot may represent the inspection lot.

(5) Sample size and accept number shall be applied to each radiation hardness assurance level.

(6) Four-digit number refers to the test method number in MIL-STD-750.
(7) When the single event test is performed at semiconductor chip level, it shall be performed in accordance with paragraph A.2.1.5.
(8) Test shall be conducted in the case of qualification tests, when required by the purchaser or when design or process is changed affecting single event characteristics.
(9) When multiple types of single event test are performed, sample size (accept number) subjected to each type of test shall be specified in the detail specification.
(10) SOI devices of each wafer lot shall be tested.
(11) Only SOI device shall be tested.

APPENDIX D

PROCEDURES FOR SAMPLING TEST AND INSPECTION

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX D

PROCEDURES FOR SAMPLING TEST AND INSPECTION

D.1. Scope

This appendix establishes the procedures for sampling tests and inspections required in this specification.

D.2. Definition of Terms and Symbols

The terms and symbols defined below shall be applied to all sampling tests and inspections in this specification.

a) Lambda (λ)
Value of LTPD (Lot Tolerance Percent Defective) per 1000 hours.

b) LTPD series
The LTPD series is defined as the following series of values (%).
50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15 and 0.1.

c) Tightened inspection
Tightened inspection is defined as the inspection performed using the next LTPD (or λ) value in the LTPD series lower than specified.

d) Acceptance number (c)
The acceptance number is defined as the maximum number of defectives permitted for the selected sample size.

e) Rejection number (r)
Rejection number is defined as the number which is greater than the acceptance number by one.

D.3. Procedures for Sampling Test and Inspection

Unless otherwise specified in the detail specification, the sampling tests and inspections shall be performed in accordance with the LTPD method specified below.

D.3.1 Sample Size

The sample size for the tests and inspections and the acceptance number shall be determined for the specified LTPD series or lambda as specified in Table D-1 or D-2. When Table D-2 is used, a column with the inspection lot size (N column) closest to the actual lot size shall be referenced. If the actual lot size is exactly midway between two lot sizes in the table, the manufacturer may choose either lot size between the two. The sample size shall be determined such that the LTPD or lambda value associated with the sample size in Table D-2 is closest to the specified LTPD value. If the applicable column does not contain a LTPD or lambda value which is equal to or less than the specified value, 100% inspection (paragraph D.3.5) shall be used. The manufacturer may select a sample size greater than that required. However, the acceptance number shall be determined based on the actual sample size.

D.3.2 Selection of Samples

Samples shall be randomly selected from the inspection lot (or inspection sublot).

D.3.3 Failure Count

Failure of a product for one or more test or inspection items (a subgroup of the qualification test or quality conformance inspection is counted as one test) shall be counted as a single failure.

D.3.4 Acceptance Criteria

If the observed number of defectives from the first sample selected in accordance with specified LTPD or lambda is less than or equal to the pre-selected acceptance number, the lot shall be accepted. However if the failure mode of the defect is catastrophic, such as an open- or short-circuit where the function of the product might be lost, the device fails the test or inspection. If the observed number of defects exceeds the pre-selected acceptance number, the lot shall be rejected or the manufacturer may perform a retest using additional samples. A retest is allowed only once. The retest sample size shall be determined by the new acceptance number (which can tolerate the number of defects of the initial sampling) selected based on the sum of the initial and additional sample size using the same table (Table D-1 or Table D-2). If the total number of defects from the first test and re-test is less than or equal to the new acceptance number, the lot shall be accepted.

D.3.5 100% Inspection

If the inspection lot size is smaller than that associated with the specified value of LTPD or lambda (paragraph D.3.1), 100% inspection shall be performed. The certified manufacturer may choose to perform 100% tests and inspections for all tests and inspections. If the observed percent of defects for the inspection lot is less than or equal to the specified value of LTPD or lambda, the lot shall be accepted.

Table D-1. Sampling Plan for Inspection Lot Size Exceeding 200[(1)]

LTPD or λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance Number (c) (r = c + 1)	Minimum Sample Size																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	19 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.8)	31 (3.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.29)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

Note[1] The minimum quality level (approximate AQL) required to accept 19 of 20 lots on average is shown in parenthesis for information only.

Table D-2. Sampling Plans for Inspection Lot Sizes of 200 or Less (1/3)

(N = lot size, n = sample size, c = acceptance number)

C = 0																								
N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD
2	2.2	65	2.5	66	2.5	67	2.5	67	2.5	67	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68
4	1.2	36	1.2	40	1.2	42	1.2	42	1.3	42	1.3	43	1.3	43	1.3	43	1.3	43	1.3	43	1.3	44	1.3	44
5	1.0	29	1.0	33	1.0	34	1.0	35	1.0	35	1.0	35	1.0	36	1.0	36	1.0	37	1.0	37	1.0	37	1.0	37
8	0.5	15	0.6	20	0.6	22	0.6	23	0.6	23	0.6	23	0.6	24	0.7	24	0.7	24	0.7	24	0.7	24	0.7	25
10			0.4	15	0.5	17	0.5	19	0.5	19	0.5	19	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20
16			0.2	6.9	0.25	10	0.25	11	0.3	11	0.3	12	0.3	12	0.3	13	0.3	13	0.3	13	0.3	13	0.3	13
20					0.2	6.8	0.2	8.0	0.25	8.7	0.25	9.0	0.25	9.4	0.25	10	0.25	10	0.25	10	0.25	10	0.25	11
25					0.13	4.3	0.15	5.7	0.2	6.4	0.2	6.9	0.2	7.4	0.2	7.5	0.2	7.6	0.2	7.7	0.2	7.8	0.2	7.9
32							0.1	3.7	0.1	4.4	0.1	5.0	0.1	5.5	0.1	5.9	0.15	6.0	0.15	6.2	0.15	6.3	0.15	6.3
40									0.1	3.0	0.1	3.4	0.1	4.0	0.1	4.5	0.1	4.6	0.1	4.9	0.1	5.0	0.15	5.0
50											0.1	2.3	0.1	2.9	0.1	3.3	0.1	3.5	0.1	3.7	0.1	3.7	0.1	3.9
64													0.08	1.7	0.08	2.2	0.08	2.5	0.08	2.7	0.08	2.8	0.08	2.9
80															0.07	1.5	0.07	1.7	0.07	2.0	0.07	2.1	0.07	2.2
100																	0.05	1.1	0.05	1.5	0.05	1.5	0.05	1.7
125																			0.04	0.8	0.04	0.9	0.04	1.2
128																			0.04	0.8	0.04	0.9	0.04	1.1
160																							0.03	0.7

Table D-2. Sampling Plans for Inspection Lot Sizes of 200 or Less (2/3)

(N = lot size, n = sample size, c = acceptance number)

C = 1																						
N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD
2	27	95	24	95	24	95	23	95	23	95	23	95	23	95	23	95	23	95	22	95	22	95	22	95
4	15	62	12	65	12	66	11	67	11	67	10	67	10	67	10	67	10	67	9.8	67	9.7	67	9.7	68
5	13	51	10	55	8.8	56	8.5	57	8.4	57	8.1	58	7.9	58	7.6	58	7.5	58	7.5	58	7.5	58	7.5	58
8	11	28	7.2	35	6.2	38	5.8	38	5.4	39	5.0	39	4.7	39	4.5	39	4.3	39	4.3	40	4.2	40	4.2	40
10			6.2	30	5.0	30	4.6	31	4.2	32	4.2	32	4.2	32	3.9	33	3.5	33	3.3	33	3.3	33	3.3	33
16			5.6	15	4.2	18	3.8	18	3.4	20	3.0	20	2.9	21	2.6	21	2.5	21	2.3	21	2.3	22	2.2	22
20					4.0	13	3.2	15	2.8	16	2.5	16	2.4	16	2.3	16	2.1	17	2.0	17	2.0	17	2.0	18
25					3.8	9.2	3.1	11	2.5	12	2.2	13	2.0	13	1.8	13	1.7	13	1.6	14	1.6	14	1.6	14
32							3.1	7.4	2.4	8.2	2.1	9.0	1.8	9.9	1.6	10	1.5	10.5	1.4	11	1.3	11	1.3	11
40									2.4	5.9	2.1	6.8	1.6	7.6	1.4	7.8	1.3	8.2	1.2	8.3	1.2	8.4	1.1	8.6
50											1.7	4.6	1.4	5.6	1.2	6.1	1.2	6.4	1.0	6.5	0.9	6.7	0.9	6.7
64													1.3	3.8	1.1	4.4	1.0	4.7	0.8	5.0	0.8	5.0	0.7	5.2
80															1.1	3.0	1.0	3.4	0.8	3.7	0.7	3.8	0.6	4.0
100																	0.9	2.5	0.7	2.8	0.7	2.8	0.6	3.0
125																			0.7	1.9	0.7	2.0	0.5	2.2
128																			0.7	1.7	0.7	1.9	0.5	2.2
160																							0.5	1.5

Table D-2. Sampling Plans for Inspection Lot Sizes of 200 or Less (3/3)

(N = lot size, n = sample size, c = acceptance number)

C = 2																						
N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD	AQL	LTPD
4	33	82	28	83	27	84	27	85	27	85	26	85	26	85	26	86	26	86	25	86	25	86	25	86
5	27	69	23	73	21	74	20	74	20	74	20	75	20	75	19	75	19	75	19	75	19	75	19	75
8	22	42	15	49	14	49	13	52	13	52	13	52	12	53	12	53	12	53	11	53	11	53	11	53
10			13	39	11	42	11	42	10	43	10	43	9.6	43	9.2	44	9.1	44	8.9	44	8.9	44	8.7	44
16			11	22	8.6	25	6.9	27	6.8	27	6.4	27	6.0	28	6.0	29	5.9	29	5.9	29	5.7	29	5.5	30
20					7.7	19	8.2	21	5.9	22	5.6	22	5.1	23	4.8	23	4.8	23	4.8	23	4.5	24	4.5	24
25					7.4	13	6.0	16	4.9	17	4.5	17	4.3	18	4.1	18	3.9	18	3.7	18	3.7	19	3.7	19
32							5.5	11	4.8	12	4.3	13	3.6	14	3.4	14	3.2	14	3.0	14.5	3.0	15	2.9	15
40									4.6	6.9	3.9	9.8	3.1	11	2.8	12	2.5	12	2.4	12	2.4	12	2.3	12
50											3.5	6.9	2.8	8.1	2.4	8.4	2.3	8.6	2.1	9.0	2.1	9.3	2.0	9.5
64													2.6	5.7	2.2	6.2	2.0	6.6	1.3	7.1	1.7	7.1	1.6	7.4
80															2.1	4.5	1.2	4.9	1.5	5.4	1.5	5.4	1.4	5.6
100																	1.6	3.5	1.4	3.9	1.4	4.0	1.2	4.4
125																			1.4	2.8	1.3	2.9	1.1	3.3
128																			1.4	2.6	1.3	2.9	1.1	3.2
180																							1.1	2.3

APPENDIX E

PREPARATION OF DESIGN SPECIFICATION

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX E

PREPARATION OF DESIGN SPECIFICATION

E.1. Scope

This appendix provides formats and contents of design specifications.

E.2. Design Specifications

The design specifications based on paragraph 2.4 a) of this specification shall include at least contents specified in paragraph 3.3 of this specification, shall be in accordance with paragraph 3.1.1 to represent construction and design limit values indicating qualification coverage. Example of design specification is shown in Format E-1 (1).
To supply hybrid ICs based on this specification, the manufacturer shall attach design specification which was prepared in accordance with this Appendix to quality assurance program plan and submit to JAXA at qualification (requalification) test application.

Note (1) Contents of example is exemplification.

Attachment-○

Integrated Circuits, Hybrid, High Reliability, Space Use

Design Specification

Prepared: YYYY/MM/DD

Format E-1 (Cover)

Note (1) Contents are exemplification (the same shall apply hereinafter).

Integrated Circuits, Hybrid, High Reliability, Space Use
Design Specification

1. General

This specification establishes qualification coverage of design on space use, high reliability, hybrid integrated circuits used for electronic equipment installed on space crafts. Other requirements resulting from specific use may be specified in detail specification.

2. Applicable Documents

Unless otherwise specified, the latest issues of documents listed below form a part of this specification to the extent specified herein.
JAXA-QTS-2000 Common Parts/Materials, Space Use, General Specification for
JAXA QTS-2020 Integrated Circuits, Hybrid, High Reliability, Space Use, General Specification For
MIL STD-883 Test Methods standard, Microelectronics

3. Requirements

3.1 Design and Construction

Design and construction of hybrid IC shall be in compliance with the following "Construction and design limit values" and JAXA-QTS-2020 paragraph 3.3 "Design and Construction". In the event of a conflict between this specification and JAXA-QTS-2020, this appendix shall take precedence over JAXA-QTS-2020.

Format E-1 (Text)

Construction and Design Limit Values

1. Part number _____
2. Manufacturer's name _____
2.1 Factory location and manufacturing line

Line (or process) name	Factory name	Location

3. Operating case temperature range : Min. _____ ºC Max. _____ºC
4. Substrate
   a) Material _____
   b) Film formation process ☐Thin-film ☐Thick-film
   c) Membrane composition (Metallization and glassivation)

	Level No. (1)	Material	Forming Method	Thickness	
				Min.	Max.
Metallization material					
Glassivation					

Note (1) When the metallization or glassivation is multi-layered, the layer closest to the substrate shall be numbered level 1, and descriptions shall be made for all levels.

   d) Conductor
      Maximum current density (thin-film): _____ A/cm^2
      Maximum power consumption (thick-film): _____ W/cm^2
   e) Maximum power consumption of resistors
      1) Thin-film resistor: _____W/cm^2
      2) Thick-film resistor: _____ W/cm^2

5. Pattern form
   a) Minimum element spacing
      1) Conductor – Conductor: _____
      2) Conductor – Resistor: _____
      3) Resistor – Resistor: _____
      4) Spacing of element mount: _____

b) Minimum pattern width
1) Conductor: _____
2) Resistor: _____
c) Element dimension
1) Resistors Min. :_____ Max.: _____
2) Chip capacitors Min. :_____ Max. : _____
3) Chip resistors Min. :_____ Max. : _____
4) Semiconductor chips Min. : _____ Max. : _____
d) Trimming ☐Laser ☐Sand-blast ☐Anodic treatment
☐Others
e) Scribing ☐Diamond ☐Laser ☐Saw

6. Mounted element and mounting structure

Element type (mounting structure)	Mounting material	Maximum area (mm^2)	Maximum weight (mg)	Derating	No. of elements used (pcs)
a) Substrate					
b) Chip capacitor					
c) Chip resistor					
d) Semiconductor chips ☐Face-up ☐Eutectic bonding ☐Adhersive ☐Others					
e) Other items					

7. Intra- connection

	Material	Dimensions/ configuration of wire (or ribbon)	Connecting method	Maximum wire length (or bond spacing)	Maximum current
a) Semiconductor chips / substrate					
b) Chip capacitor / substrate					
c) Chip resistor / substrate					
d) Substrate / substrate					
e) Substrate / package leads					
f) Other items					

8. Package and packaging material

a) Package configuration _____

b) Number of pins _____

c) Material _____

Header	Material	Plating material
Post to be bonded		
Cap or lid		
External leads		

9. Final seal

a) Atmosphere at sealing _____

b) Sealing method ☐Welding ☐Brazing ☐Others _____

c) Sealing material (except when welding) _____

Melting point _____

Maximum temperature _____

10. Sheet transformer

a) Material: _____

b) Number of layer: _____

c) Winding pattern

1) Minimum pattern width : _____mm

2) Minimum pattern spacing :_____mm

3) Temperature riseing : _____max.

11. Typical construction illustration

Typical construction illustration of hybrid IC is as follows:

APPENDIX F

PREPARATION OF DETAIL SPECIFICAITON

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX F

PREPARATION OF DETAIL SPECIFICATION

F.1. Scope

This appendix establishes instructions for preparation of detail specifications for hybrid ICs as specified in this specification.

F.2. General

This specification establishes the general requirements for hybrid ICs. To manufacture hybrid ICs using JAXA certified production lines in accordance with this specification, the detail specification which defines individual and specified requirements for the hybrid IC shall be prepared.

F.3. Contents

The detail specification shall contain the following items in accordance with paragraph A.4 of JAXA-QTS-2000. Format of detail specifications shall be as specified in Format F-1.

a) Revision record
b) General
c) Applicable documents
d) Requirements
e) Quality assurance provisions
f) Preparation for delivery
g) Notes

F.3.1 General

General shall specify the following items.

a) Scope
b) Part number
c) Absolute maximum ratings
d) Recommended operating conditions

F.3.1.1 Scope

Scope shall contain applicable general specification and specify the scope of the detail specification.

F.3.1.2 Part Number

The part number shall be specified in accordance with paragraph 1.3.

F.3.1.3 Absolute Maximum Ratings

The absolute maximum ratings applied to hybrid ICs shall be specified in table format.

F.3.1.4 Recommended Operating Conditions

The recommended operating conditions for hybrid ICs shall be specified in table format.

F.3.2 Applicable Documents

Applicable documents shall be in accordance with paragraph A.3.2.1 of JAXA-QTS-2000. Applicable documents shall include at least quality assurance program plan.

F.3.3 Requirements

F.3.3.1 Design and Construction

In addition to paragraph 3.3, design and construction requirements shall specify the following items.

It shall be clarified that product design and construction shall be in compliance with quality assurance program plan.

a) Mounted elements (paragraph 3.3.4)
b) Organic and Polymeric materials (paragraph 3.3.5)
c) Mounting materials for substrate, semiconductor chips and passive elements (paragraph 3.3.6)
d) Package (paragraphs 3.3.8 a), b) and F.3.3.1.1)
e) Lead material and finish (paragraphs 3.3.8 c) and F.3.3.1.2)
f) Electrical characteristics (paragraph F.3.3.1.3)
g) Logic diagram and terminal connections (paragraphs F.3.3.1.4)
h) Truth table and logical expression (paragraph F.3.3.1.5)

F.3.3.1.1 Package Configuration

Package configuration shall be shown with a case outline drawing, dimensions and external lead numbers of hybrid IC.

F.3.3.1.2 Lead Material and Finish

Lead material and finish shall be specified. The lead finish shall be specified including adequate control limits.

F.3.3.1.3 Electrical Characteristics

Requirements for electrical characteristics shall be defined for each circuit function referring to Tables F-1, F-2, F-3 and F-4. Test conditions and limits (maximum, minimum or both) shall be specified for all required electrical parameters to

represent intended function and assure interchangeability. In addition, a table shall be provided to define the relationship between the lead numbers and input/output signals in the Group A tests (electrical parameter tests).

F.3.3.1.4 Logic Diagram and Terminal Connections

Logic diagrams and terminal connections shall be depicted in figures to clearly indicate circuit functions and the relationship between each terminal and external lead numbers. Block diagrams may be used for devices with a large number of logic elements. The same requirement shall apply for analog circuits and the figures shall be labeled "circuit diagram and terminal connections."

F.3.3.1.5 Truth Tables and Logical Expressions

Truth tables and logical expressions, together with the logic diagrams, shall clearly define the circuit functions. For complex sequential circuits and analog circuits, this requirement may be waived.

Table F-1. Electrical Parameters for Digital Integrated Circuit

Parameter	Symbol	Test method number in MIL-STD-883	Remarks
High level output voltage	V_{OH}	3006	
Low level output voltage	V_{OL}	3007	
High level input current	I_{IH}	3010	
Low level input current	I_{IL}	3009	
High level output current	I_{OH}		Measured together with $V_{OH.}$
Low level output current	I_{OL}		Measured together with $V_{OL.}$
Output short-circuit current	I_{OS}	3011	
Collector cutoff current	I_{CEX}		
Noise margin	V_N	3013	When the noise margin is considered important for the application.
Power supply current, low level	I_{CCL}, I_{DDL}, I_{EEL}, etc.	3005	
Power supply current, high level	I_{CCH}, I_{DDH}, I_{EEH}, etc.	3005	
Breakdown voltage	BV	3008	When applicable.
When a node terminal exists:			
a. High level node current	I_{INH}	3010	At specified V_{INH}.
b. Low level node current	I_{INL}	3009	At specified V_{INL}.
Propagation delay time (low-to-high level output)	t_{PLH}	3003	
Propagation delay time (high-to-low level output)	t_{PHL}	3003	
Transition time (high-to-low level output)	t_{THL}	3004	
Transition time (low-to-high level output)	t_{TLH}	3004	
Supply current drain versus frequency			
Output pulse width (for mono-stable circuit only)			
Terminal capacitance		3012	When the terminal capacitance is considered important for the application.
AC noise margin	V_N	3013	When the AC noise margin is considered important for the application.

Table F-2. Electrical Parameters for Analog Integrated Circuit (Amplifier)

Parameter	Symbol	Test method no. in MIL-STD-883	Remarks
AC unbalanced voltage	V_{OU}		
Automatic gain control range	AGC	4007	
Bandwidth (small signal)	BW	4004	
Common mode input voltage range	V_{ICR}	4003	
Common mode output voltage	V_{OC}	4003	
Common mode rejection ratio	CMRR	4003	
Common mode voltage gain	A_{VC}	4003	
Power dissipation	P_D	4005	
Differential input impedance	Z_{id}	4004	
Differential voltage gain	A_{VD} or A_{vd}	4004	
Input bias current	I_{IB}	4001	
Temperature coefficient of input bias current	$\Delta I_{IB}/\Delta T$	4001	
Input offset current	I_{IO}	4001	
Temperature coefficient of input offset current	$\Delta I_{IO}/\Delta T$	4001	
Input offset voltage	V_{IO}	4001	
Temperature coefficient of input offset voltage	$\Delta V_{IO}/\Delta T$	4001	
Maximum output voltage swing	V_{OPP}	4004	
Single ended input voltage range	V_{ISR}		
Noise figure	NF	4006	
Differential output impedance	Z_{od}	4005	
Single ended output impedance	Z_{os}	4005	
Output offset voltage	V_{OO}		
Phase margin	φ_m	4002	
Power gain, or insertion power gain	G_P or G_p	4006	
Power supply rejection ratio	PSRR	4003	
Static input voltage	V_I		
Static output voltage	V_O		
Single ended input impedance	Z_{is}	4004	
Single ended voltage gain	A_{VS} or A_{vs}	4004	
Slew rate	SR	4002	
Total harmonic distortion factor	THD	4004	
Transient response	TR		
Maximum output swing bandwidth	B_{OM}		
Overload recovery time	t_{or}		

Table F-3. Electrical Parameters for Analog Integrated Circuit (Comparators)

Parameter	Symbol	Test method no. in MIL-STD-883	Remarks
Common mode rejection ratio	CMRR	4003	
Input bias current	I_{IB}	4001	
Input offset current	I_{IO}	4001	
Temperature coefficient of input offset current	$\Delta I_{IO}/\Delta T$	4001	
Input offset voltage	V_{IO}	4001	
Temperature coefficient of input offset voltage	$\Delta V_{IO}/\Delta T$	4001	
Single ended voltage gain	A_{VS} or A_{vs}	4004	
High level output voltage	V_{OH}	3006	
Low level output voltage	V_{OL}	3007	
Output voltage (strobed)	$V_{O(STROBED)}$		
Collector cutoff current	I_{CEX}		
Low level output current	I_{OL}		Measured together with V_{OL}.
Output short-circuit current	I_{OS}	3011	
Strobe current	I_{STROBE}		
Input leakage current	I_I		
Power supply current	I_{CC}	3005	
Response time (low-to-high level)	t_{RLH}		
Response time (high-to-low level)	t_{RHL}		

Table F-4. Electrical Parameters for Analog Integrated Circuits (Voltage Regulators)

Parameter	Symbol	Test method no. in MIL-STD-883	Remarks
Output voltage	V_O	3001	
Input voltage stability	V_{RLINE}		
Load current stability	V_{RLOAD}		
Static operating current	I_{SCD}		
Static operating current delta (1)	$\Delta I_{SCD(line)}$		
Static operating current delta (2)	$\Delta I_{SCD(load)}$		
Output short-circuit current	I_{OS}		
Reference voltage	V_{START}		
Ripple rejection	$\Delta V_{IN}/\Delta V_O$		
Output noise voltage	N_O		
Change rate of output voltage (1)	$\Delta V_O/\Delta V_I$		
Change rate of output voltage (2)	$\Delta V_O/\Delta V_L$		
Temperature coefficient of output voltage	$\Delta V_O/\Delta T$		
Zener voltage	V_z		

F.3.3.2 Marking

Marking requirements shall be in accordance with paragraph 3.4. Details for the products that require a radiation hardness designator (total dose radiation hardness) or a beryllium oxide package identifier shall be specified.

F.3.3.3 Certification

Certification requirements shall be in accordance with paragraph 3.1 and specify all electrical parameters to be measured, the steady-state operating life test circuit and conditions for the electrostatic discharge sensitivity test (paragraph F.3.4.6). If the manufacturer chooses to conduct the radiation hardness test, the details for the test shall be specified.

F.3.4 Quality Assurance Provisions

Requirements regarding the quality assurance provisions shall specify the following items.

a) General requirements
b) Incoming materials control
c) Manufacturing process control
d) In-process inspection

e) Screening
f) Qualification test and quality conformance inspection
g) Long-term storage
h) Change of tests and inspections

F.3.4.1 General Requirements

General requirements shall be in accordance with paragraph 4.1.

F.3.4.2 Incoming Materials Control

Incoming materials control shall be in accordance with paragraph 4.2.

F.3.4.3 Manufacturing Process Control

Manufacturing process control shall be in accordance with paragraph 4.3.

F.3.4.4 In-Process Inspection

In-process inspection shall be in accordance with paragraph 4.5.
Items, methods, criteria and sample size of in-process inspection shall be specified.

F.3.4.5 Screening

Screening requirements shall be in accordance with paragraph 4.7 and specify the following items.

a) Electrical parameters to be measured
b) Test circuits and test conditions for burn-in and reverse bias burn-in tests
c) Delta limits

F.3.4.5.1 Electrical Parameters to be Measured

As a minimum, electrical parameters shown below shall be measured during the screening test. If the electrical parameter tests (subgroup) of Group A tests are not specified due to circuit functions, the items may be exempted.

Electrical parameter test	Subgroups of Group A tests
Interim electrical parameter test	1, 4, 7, 9
Final electrical parameter test	1-11

F.3.4.5.2 Burn-in and Reverse Bias Burn-in Test Circuits

Circuits for burn-in and reverse bias burn-in tests shall be designed to operate the product as close as possible to actual operations to induce initial failures caused by embedded defects thus enabling defective products to be removed.

F.3.4.5.3 Delta Limits

Delta limits of class I hybrid IC shall be defined using Table F-5 as a reference.

Table F-5. Delta Limits

CMOS	I_{SS}	± (0.4 × maximum allowable value)
	V_{OH}	± (0.02 × minimum allowable value)
	V_{OL}	± (0.08 × maximum allowable value)
TTL	V_{OH}	± (0.05 × minimum allowable value)
	V_{OL}	± (0.1 × specified value)
	I_{IH}	± (0.1 × maximum allowable value) or ten times the initial value, whichever is greater.
Amplifiers	V_{IO}	± (0.25 × maximum allowable value)
	I_{IB}	± (0.1 × maximum allowable value)
	I_{IO}	± (0.5 × maximum allowable value)

F.3.4.6 Qualification Test and Quality Conformance Inspection

Requirements for the qualification test and quality conformance inspection shall be as specified in paragraphs 4.6 and 4.8 and shall define the external dimensions to be measured, electrical parameters, steady-state operating life test circuit and conditions of the electrostatic discharge sensitivity test. Radiation tests for the products qualified as radiation hardened hybrid ICs shall be specified

F.3.4.6.1 External Dimensions to be Measured

The external dimensions to be measured in the quality conformance inspection shall include the dimensions designated with the following symbols at a minimum as defined in paragraph G.3.2, Appendix G of JAXA-QTS-2020. If any symbol is not specified in the package configuration drawings in Appendix G, the measurements shall not be applied.

Package configuration	Dimension symbol
Flat package	A, D, D_1, E, E_1, e, L
Cylindrical package	A, φb, φD, e, L

F.3.4.6.2 Electrical Parameters to be Measured

Items shown below shall be specified as electrical parameters to be measured in addition to the Group A test as a minimum. If not specified in the Group A tests due to circuit function, the test items may be exempted.

End-point electrical parameter test	Applicable subgroups of the Group A test
Group C test, subgroup 1	1-11
Group C test, subgroup 2	1-11
Group C test, subgroup 3	1, 4, 7, 9
Group E test, subgroup 1	1, 4, 7, 9
Group E test, subgroup 2	1, 4, 7, 9
Group E test, subgroup 3	1, 4, 7, 9
Group E test, subgroup 4	1, 4, 7, 9

F.3.4.6.3 Steady-State Operating Life Test Circuit

Circuits for the steady-state operating life test shall be designed so that the all internal elements in hybrid IC operates as close as possible to actual operations. For this purpose, the test circuits used in the burn-in test may be used in the steady-state operating life test (refer to paragraph F.3.4.5.2).

F.3.4.6.4 Radiation Hardness Test

a) When radiation hardness test (total dose test) is required for hybrid IC, radiation hardness assurance level shall be specified in accordance with paragraph 1.3.5 as well as test conditions. When radiation hardness test (total dose test) is performed at semiconductor chip level, the requirements shall be defined in accordance with Appendix A.
b) When radiation hardness test (single event test) is required for hybrid IC, test conditions shall be defined. When radiation hardness test (single event test) is performed at semiconductor chip level, the requirements shall be defined in accordance with Appendix A.
c) When radiation hardness test (SEB test) is required for hybrid IC, test conditions shall be defined. When radiation hardness test (SEB test) is performed at semiconductor chip level, the requirements shall be defined in accordance with Appendix A.
d) When radiation hardness test (SEGR test) is required for hybrid IC, test conditions shall be defined. When radiation hardness test (SEGR test) is performed at semiconductor chip level, the requirements shall be defined in accordance with Appendix A.

F.3.4.6.5 Electrostatic Discharge Sensitivity Test

The combination of pins for electrostatic discharge sensitivity test shall be specified.

F.3.4.7 Long-Term Storage

Delivery of the products stored at the manufacturer's site for 24 months or longer shall be in accordance with paragraph 4.9.1.

F.3.4.8 Change of Tests and Inspections

If any change was made in the in-process inspection, screening or quality conformance inspection specified in this specification or any test was exempted, it shall be described in the detail specification in accordance with paragraph 4.10.

F.3.5 Preparation for Delivery

Preparation for delivery shall be in accordance with paragraph 5.

F.3.6 Notes

Note shall be specified in accordance with paragraph 6. Handling Instructions shall be shown as needed.

Format F-1 (Cover sheet)

Registration No.xxx

JAXA-QTS-2020/xxxxA
(date)

Superseding
NASDA-QTS-2020/xxxx
Cancelled
(date)

INTEGRATED CIRCUITS, HYBRID, HIGH RELIABILITY, SPACE USE, DETAIL SPECIFICATION FOR xxxxx

Prepared and Established by: ABCD CORPORATION

Issued by: JAPAN AEROSPACE EXPLORATION AGENCY

Format F-1 (Revision record)

Revision Record		
Revision	Date	Description

Format F-1 (Table of contents)

Contents

Format F-1 (Text 1/35)

INTEGRATED CIRCUITS, HYBRID,
POL DC/DC COMVERTER,
HIGH RELIABILITY, SPACE USE,
DETAIL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the detail requirements for the space use, high reliability, hybrid integrated circuits (JAXA-QTS-2020), POL DC/DC converters to be used for electronic or electrical equipment installed in the space crafts. Requirements unique to specific applications may be documented separately (refer to paragraph 6.2).

1.2 Part Number

The part numbers for products covered by this specification are as follows.

Class I

JAXA(1) 2020/0101*1 — 1 (Device type, paragraph 1.2.1) DB (Package configuration, paragraph 1.2.2) C (Lead finish, paragraph 1.2.3) R (Radiation hardness, paragraph 1.2.4)

Class II

JAXA(1) 2025/0101*1 — 1 (Device type, paragraph 1.2.1) DB (Package configuration, paragraph 1.2.2) C (Lead finish, paragraph 1.2.3) R (Radiation hardness, paragraph 1.2.4)

Note (1) "JAXA" indicates the common part is for space use and may be abbreviated to "J".

1.2.1 Device Type

The device type of products covered by this specification is as follows.

Device type	Circuit Function
1*2	POL DC/DC converter, input 5V / output 1.2V-3.3V

Notes:

*1 This number refers to an individual identification.

*2 In principle, the device type number shall be assigned sequentially from 1 to 9.

Format F-1 (Text 2/35)

1.2.2 Package Configuration

The package configuration of products covered by this specification is as follows.

Letter	Package configuration
DB[*1]	26-lead, flat package (Figure-1)

1.2.3 Lead Material and Finish

The lead material and finish of products covered by this specification are as follows.

Finish letter	Lead material and finish
C	Type A, gold plate[*2]

1.2.4 Radiation Hardness

The radiation hardness level of semiconductor chips used in the products covered by this specification is as follows.

Designator	Radiation hardness level
R	1000 Gy(Si) {1 x10^5rad(Si)}[*3]

1.3 Absolute Maximum Ratings

The absolute maximum ratings of products covered by this specification are shown in Table-1. Output current limit characteristics are shown in Figure-8 through Figure-13.

Table-1 Absolute Maximum Ratings [*4]

Item		Absolute Maximum Ratings	
Input voltage range (V_{IN})		0 to +16V	
Output current range (I_{OUT})		0 to 3.5A	
Storage temperature range (T_{STG})		-65 to +150ºC (case temperature)	
SYNC IN input voltage (V_{SYNC})		+5.5V	
ENABLE input terminal (V_{CE})		V_{IN}	
Output overvoltage limit terminal (O_V)		+5.5V	
Terminal temperature (soldering)		+350ºC [*5]	
Thermal resistance (θ_{JC})		15.63ºC/W	

Notes:

[*1] In accordance with paragraph 1.3.3 of JAXA-QTS-2020.

[*2] In accordance with paragraph 3.3.8 c) 2) of JAXA-QTS-2020.

[*3] In accordance with paragraph 1.3.5 of JAXA-QTS-2020.

[*4] Proper items shall be added as needed.

[*5] When the temperature is +300ºC (60 sec) or below, the temperature shall be specified in paragraph 6.2.1 as handling precaution.

Format F-1 (Text 3/35)

1.4 Recommended Operating ConditionsThe recommended operating conditions of the products covered by this specification is shown in Table-2.

Table-2 Recommended Operating Conditions [*1] (Device Type 1)

Items		Recommended operating condition	
Operating temperature range (T_{OP})		-55 to +125ºC (case temperature)	
Input voltage (V_{IN})		+5V	
Output current range (I_{OUT})	V_{OUT}=1.8V	0 to 3A	
SYNC IN input voltage (V_{SYNC})		+5V	
ENABLE input terminal (V_{CE})		V_{IN}	

2. APPLICABLE DOCUMENTS

Unless otherwise specified, the latest issues of the documents listed below form a part of this specification to the extent specified herein.

JAXA-QTS-2020	Integrated Circuits, Hybrid, High Reliability, Space Use, General Specification for
MIL-STD-883	Test Method Standard – Microelectronics
XXXXXX	Quality Assurance Program Plan

3. REQUIREMENTS

3.1 Design and Construction

The design and construction of the products shall be in compliance with the requirements specified in this section and paragraph 3.3 of JAXA-QTS-2020. The products designed and manufactured in accordance with this specification shall satisfy the requirements for design specification specified in paragraph 2 of this specification.

3.1.1 Mounted Elements

Mounted elements of products shall be in accordance with paragraph 3.3.4 of JAXA-QTS-2020 and as follows:

3.1.1.1 Passive Element Chip

As passive element chips, JAXA certified, MIL certified or the parts which passed acceptance inspection specified in paragraph 4.2.1.1 shall be used.

Note:[*1] Requirements shall be added as needed.

Format F-1 (Text 4/35)

3.1.1.2 Semiconductor Chips

Semiconductor chips which satisfy performance requirements specified in Appendix A of JAXA-QTS-2000 shall be used.

3.1.1.3 Printed Wiring Board for Sheet Reactor

For sheet reactor, printed wiring boards which passed incoming inspection specified in paragraph 4.2.1.3 shall be used.

3.1.2 Organic and Polymeric Material

As organic and polymeric material, following materials which satisfy requirements specified in paragraph 3.3.5 of JAXA-QTS-2020 shall be used:
a) Silicone-based adhesive
b) Epoxy adhesive

3.1.3 Mounting Materials for Substrate and Semiconductor Chip

Mounting materials for substrate and semiconductor chips shall be as specified in paragraph 3.3.6 of JAXA-QTS-2020 and as follows:

3.1.3.1 Mounting Materials for Semiconductor Chip

As mounting materials for semiconductor chips, following materials shall be used:
a) AuSn solder (mounting MOSFETs and diodes)
b) Conductive adhesive (mounting control ICs and diodes)

3.1.3.2 Mounting Materials for Passive Element Chip

As mounting materials for passive element chips, following materials shall be used:
a) Sn3Ag0.5Cu solder or Sn37Pb solder (mounting capacitors)
b) Conductive adhesive (mounting resistors)

3.1.4 Package Configuration

The package configuration shall be as specified in Figure-1.

3.1.5 Packaging Materials

The packaging materials shall be as specified in Figure-1. Gold plate shall be used as finish.

Format F-1 (Text 5/35)

3.1.6 Lead Material and Finish

The lead material and finish shall satisfy type “A” and “Gold plating” as specified in paragraph 3.3.8 of JAXA-QTS-2020.

3.1.7 Electrical Characteristics

The electrical characteristics shall be as specified in Table-3.

3.1.8 Circuit Diagrams and Pin Connections

The circuit diagrams and pin connections shall be as specified in Figures 2 and 3.

Format F-1 (Text 6/35)

Table-3 Electrical Characteristics (Device Type 1) ([1])*1

Item	Letter	Condition	Group A subgroup ([2])	Min.	STD	Max.	Units
Output voltage	V_{out}	Vin=5V±5% Iout=2A	1	1.764	1.8	1.836	V
			2, 3	1.728	1.8	1.872	V
Output voltage regulation	VR	Iout=0,1,2,3A Vin=4.5,5,16V	1	-2	—	+2	%
		Iout=0,1,2A Vin=4.5,5,16V	2	-4	—	+4	
		Iout=0,1,2,3A Vin=4.5,5,16V	3	-4	—	+4	
Efficiency	E_{ff}	Vin=5V±5% Iout=2A	1,3	81	—	—	%
			2	78	—	—	
Output voltage ripple	V_{RIP}	Vin=4.5,5,16V Iout=0,1,2,3A Only switching freq. component	1,3	—	—	25	mVpp
		Vin=4.5,5,16V Iout=0,1,2A Only switching freq. component	2	—	—	25	
Output noise	V_{NOISE}	Vin=4.5,5,16V Iout=0,1,2,3A	1,3	—	—	100	mVpp
		Vin=4.5,5,16V Iout=0,1,2A	2	—	—	100	
Switching freq.	f_{SW}	Vin=5V±5% Iout=2A	1	200	250	300	kHz
			2,3	195	250	325	
Soft start time	T_{SS}	Vin=5V±5% Iout=0A	1	9	11	14	ms
			2,3	8	11	15	
UVLO ON	V_{UVON}	Iout=0A	1,2,3	—	4.4	4.5	V
UVLO OFF	V_{UVOFF}		1,2,3	—	4.2	—	V
Output overcurrent limit	$I_{o\ trip}$	Vin=5V±5%	1	—	—	4.5	A
Synchronization signal input	—	Vin=5V±5%, Iout=2A Input signal: 300kHz	1,2,3	To synchronize			
External ON/OFF	—	Iout=0A ENABLE terminal condition Vin=5V , 16V ON :H(3V) , Vin OFF:L(0.4V), OPEN	1,2,3	To be ON To be OFF			
Output overvoltage limit	—	Vin=5V, Iout=0A OVERVOLTAGE terminal condition Shutdown: 1V Return: 0.9V Or power supply again	1,2,3	To shut down To return			

Note([1]) This test shall be performed with installing input / output capacitor shown in Figure-5.

([2]) Subgroup 1 (case temp.: nominal), subgroup 2 (case temp.: +125℃), subgroup 3 (case temp.: -55℃)

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 7/35)

3.2 Marking

The marking shall be as specified in Figure-4 in accordance with paragraph 3.4 of JAXA-QTS-2020.

3.2.1 Radiation Hardness Designator Marking

Any hybrid IC that passed the radiation hardness test (paragraph 4.6.5) shall be assigned a radiation hardness designator as specified in paragraph 1.2.4 which shall be included in the part number.

3.3 Certification

The manufacturer shall have their manufacturing lines of hybrid integrated circuits certified by JAXA in accordance with paragraph 3.1 of JAXA-QTS-2020. Electrical parameters to be measured in the qualification test, the steady-state operating life test circuit, and the radiation hardness test shall be in accordance with the requirements specified in paragraph 4.6 herein.

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The general requirements shall be in accordance with paragraph 4.1 of JAXA-QTS-2020.

4.2 Incoming Materials Control

The incoming materials control shall be in accordance with paragraph 4.2 of JAXA-QTS-2020.

4.2.1 Incoming Inspection

The procurement specification shall require performance verification of at least following mounted elements which have possibility causing functional failures on hybrid integrated circuit after assembly. Performance requirements such as electrical characteristics shall be specified in procurement specification. Receiving inspection of incoming materials except for specified herein shall be in accordance with paragraph 4.2.1 of JAXA-QTS-2020.

4.2.1.1 Passive Element Chip

When passive element chips except for JAXA or MIL certified parts are used, acceptance inspection shall be performed for each lot in accordance with Table-4 and Table-5. Applicable resistor chips are limited to bare chip type resistor chips which thin film resistor is formed on silicon.

4.2.1.2 Semiconductor Chip

When semiconductor chips except for JAXA or MIL certified parts are used, acceptance inspection shall be performed for each lot in accordance with Tabel-6.

4.2.1.3 Printed Wiring Board for Sheet Reactor

Each lot of printed wiring board for sheet reactor shall be inspected for each lot in accordance with Table-7.

Format F-1 (Text 8/35)

Table-4 Incoming Inspection Items for Capacitor Chips [*1]

Group	Test item	Test method / condition ([1])	Sample size (accept no.)
1	Thermal shock	107 Condition A, 20 cycle, Phase 3: +125 $^{+4}_{0}$ ℃	100% (0)
	Voltage aging	+125℃, 200%±5%of rated voltage Min. 168 hrs.	
	Insulation resistance (+125℃)	302 rated voltage, max. charging / discharging current 50mA, charging time 120 $^{+10}_{0}$ sec.	
	Dielectric withstanding voltage	301 250%～400% of DC rated current, 5±1sec, max. charging / discharging current 50mA	
	Insulation resistance (+25℃)	302 rated voltage, max. charging / discharging current 50mA, charging time 120 $^{+10}_{0}$ sec.	
	Capacitance	305 1k±100Hz([2])、1.0±0.2Vrms	
	Dissipation factor	305 1k±100Hz([2])、1.0±0.2Vrms	
2	External inspection, dimension, marking	External and dimension inspection shall be tested. 10x magnifier shall be used for external inspection.	20 (0)
3	Humidity, steady-state, low voltage	103 Condition A, +85℃, 85%RH, DC voltage 1.3V $^{+0.20}_{-0.25}$ V impression	12 (0)
4	DPA	EIA-469	Note ([3])
5	Thermal shock	107 Condition A, 100 cycle, Phase 3: +125 $^{+4}_{0}$ ℃	25 (0)
	Life	108 +125 $^{+4}_{0}$ ℃、max. charging / discharging current 50mA, Voltage application time: 1000 $^{+48}_{0}$ hrs.	
6	Voltage – temperature characteristics	JAXA-QTS-2040 paragraph L.4.4.7.5	12 (0)
	Moisture resistance	106 20 cycle	
7	Terminal strength	211 Condition A	6 (0)
	Solderability	208 +230℃±5℃、5sec±0.5sec	6 (0)
	Resistance to soldering heat	210 Condition B, +260℃±5℃、10sec±1sec	6 (0)

Note ([1]) 3-digit number refers to MIL-STD-202 test method number.

([2]) For X7R characteristic with maximum nominal capacitance 100pF and C0G characteristic with maximum nominal capacitance 1000pF: 1M±100kHz

Format F-1 (Text 9/35)

(^{3}) Sample size is as follows: (lot size: minimum sample size (allowable defect no.))
1-500：5(0)、501-10,000：10(0)、10,001-35,000：25(0)

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 10/35)

Table-5 Acceptance Inspection Item for Resistor Chips [*1]

Group	Test item	Test method / condition ([1]) ([2])	Sample size (accept no.)
1	Electrical test	DC resistor value measurement, +25°C	100%
2	Visual inspection	2032 Condition K	100%
3	Thermal cycle test	1010 Condition C, 10 cycle	10(0)
	Power conditioning	+70°C, rated power, 100 hrs.	
	Visual inspection	2032 Condition K	
	Electrical test	DC resistor value measurement, +25℃	
4	Resistance-temperature characteristic	304 (-55°C,+125°C)	20(0)
	Short-time overload	+25°C, 2.5 times rated voltage, 5 sec	
5	Wire bonding evaluation	2011	10(0) wire Or 20(1) wire

Notes ([1]) 4-digit number refers to test method number of MIL-STD-883.
([2]) 3-digit number refers to test method number of MIL-STD-202.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 11/35)

Table-6 Incoming Inspection Items for Semiconductor Chips[*1]

Group	Test item	Test method / condition ([1])	Sample size (accept no.)
1	DC parameter	In accordance with procurement specification.	100%
	Visual inspection	2010 Condition A 2072 ([2]) 2073 ([2])	
2	SEM inspection	In accordance with procurement specification.	Same as on the left
	External dimension (semiconductor chip)	In accordance with procurement specification.	3 (0)
	Bonding strength test 1) Thermocompression 2) Ultrasonic 3) Thermo-sonic 4) Resistance welding	2011 1) Condition C or D 2) Same as above 3) Same as above 4) Same as above	LTPD15 ([3])
	Die shear strength	2019	3（0）
3	Stabilization bake	1008 Condition C	10（0）
	Thermal cycle test	1010 Condition C	
	Electrical parameter test	In accordance with procurement specification.	
	High temperature reverse bias life test ([4])	In accordance with procurement specification.(150℃, 72 hrs)	
	Electrical parameter test ([4])	In accordance with procurement specification.	
	Steady-state operating life test	In accordance with procurement specification. (125℃ min., 240 hrs.)	
	Electrical parameter test	In accordance with procurement specification.	
4	Radiation hardness test([4])	1019 In accordance with procurement specification.	5（0）
5	Electrostatic discharge destruction test ([4]) ([5])	3015 Pin combination and electrical parameters before and after test shall be in accordance with procurement specification.	3 (0) ([6])

Notes ([1]) 4-digit number refers to test method number of MIL-STD-883.
([2]) This number refers to test method number of MIL-STD-750.
([3]) Applicable to bonding size. Minimum sample size is 3.

Format F-1 (Text 12/35)

([4]) This test shall be performed when specified in procurement specification.
([5]) This test shall performed for first purchase lot and design change.
([6]) Sample size shall be applied to each identical pin combination.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 13/35)

Table-7 Acceptance Inspection Items for Printed Wiring Boards for Sheet Reactor*1

Group	Test item	Test method / condition ([1])	Product	Test pattern
1	External and construction	B.4.4.2.1	All	—
	Workmanship	B.4.4.3	All	—
2	Circuitry	B.4.4.6.2	All	—
3	Through holes	B.4.4.2.2	—	3
4	Solderability	B.4.4.7.2	—	2
5	Hot oil resistance	B.4.4.8.3	—	1
	Connection resistance	B.4.4.6.3	—	1
6	Dielectric withstanding voltage	B.4.4.6.1	—	1
7	Inductance	In accordance with procurement specification.	3	—

Note ([1]) Number shown in above table refers to paragraph number of JAXA-QTS-2140 Appendix B.

4.3 Manufacturing Process Control

Manufacturing process control shall be in accordance with paragraph 4.3 of JAXA-QTS-2020.

4.4 In-Process Inspection

In-process inspection specified in Table-8 for each manufacturing lot shall be performed. The in-process inspection except for that specified in Table-8 may be performed in accordance with paragraph 4.5 of JAXA-QTS-2020.

Table-8 In-process Inspection *1

Test item	Test method / condition ([1])	Sample size
Particle impact noise detection test	2020 Condition A Only A-plane ([2])	100%
Constant acceleration test	2001 Condition A Y1,Y2 directions	100%
Visual inspection	([3])	100%

Notes ([1]) Number refers to test method of MIL-STD-883.

([2]) Marking plane shall be considered as A-plane.

([3]) Defective lead, package damage and lid peeling shall be inspected.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 14/35)

4.5 Screening

Screening shall be in accordance with paragraph 4.7 of JAXA-QTS-2020 and following provisions. Electrical parameters to be measured, burn-in test circuits and delta limits shall be as follows.

4.5.1 Test Items and Conditions

Screening for products specified in this specification shall be performed in accordance with test items and conditions shown in Table-9.

4.5.2 Electrical Parameters to be Measured

All the parameters included in the following subgroups among those shown in Table 3, shall be measured at the interim and final electrical parameters test of the screening test.

	Subgroup
Interim electrical parameter test	1[*1]
Final electrical parameter test	1, 2, 3[*1]

4.5.3 Burn-in Test Circuit

The burn-in test in the screening test shall be performed using the circuit shown on Figure 6.

4.5.4 Delta Limits

The delta limits for the burn-in test shall be as follows[*2].

ΔV_{OUT} ±0.2%

Note: [*1] The subgroups listed on Table 3 among those specified in Appendix C of JAXA-QTS-2020, shall be specified.

[*2] Refer to paragraph F.3.4.5.3.

Format F-1 (Text 15/35)

4.6 Qualification Test and Quality Conformance Inspection

The qualification test and quality conformance inspection shall satisfy the requirements specified in paragraphs 4.6 and 4.8 of JAXA-QTS-2020. Others shall be as specified in the following provisions. External dimensions to be measured, electrical parameters, steady-state operating life test circuit shall satisfy the requirements specified in paragraphs 4.6.2 to 4.6.4. Radiation hardness test and electrostatic discharge sensitivity test shall satisfy the requirements specified in paragraphs 4.6.5 and 4.6.6.

4.6.1 Test Items and Conditions

Qualification test and quality conformance inspection specified in this specification shall be performed in accordance with test items and conditions shown in Tables 10 to Table 14.

4.6.2 External Dimensions to be Measured

The external dimensions shown in Figure-1 to be measured shall include the dimensions designated with the following symbols.

Package configuration symbol	Dimension symbol
DB	A, b, c, D, D_1, D_2, E, E_1, e, L, Q, S

4.6.3 Electrical Parameters to be Measured

All the parameters included in the following subgroups among those shown in Table 3, shall be measured.

	Applicable subgroups
Group A test	1, 2, 3[*1]
Group C test, subgroup 1	1, 2, 3
Group C test, subgroup 2	1, 2, 3
Group E test, subgroup 1	1

4.6.4 Steady-State Operating Life Test Circuit

The steady-state operating life test shall be performed using the circuit shown on Figure 6.

Note:

[*1] Subgroups shall be added as needed.

Format F-1 (Text 16/35)

4.6.5 Radiation Hardness Test

The radiation hardness test shall be performed at product level or element level. Unless otherwise specified, the test shall be performed at element level. When radiation hardness is not required, Group E test may be exempted. When Group E test is exempted, assurance letter of radiation hardness shall not be marked.

a) Product level

The product shall be tested in accordance with Table C-5 of JAXA-QTS-2020 Appendix C. Following conditions shall be applied:

1) Radiation source: ^{60}Co gamma-ray
2) Exposure dose: 1×10^3 Gy(Si)
3) Dose rate: 2×10^3 Gy(Si)/h
4) Bias circuit: In accordance with Figure-7.
5) Electrical characteristics allowance after irradiation is shown in Table-3. Considering degradation characteristic of control IC, output voltage and output voltage regulation shall be 2% and -4%, respectively.
6) Electrical characteristics shall be measured within 24 hours after irradiation. Bias application during transfer is not required.

b) Element level

Semiconductor chips composing products shall be tested in accordance with Appendix A of JAXA-QTS-2020. Absorbed dose shall satisfy assurance level of radiation hardness.

4.6.6 Electrostatic Discharge Sensitivity Test

The electrostatic discharge sensitivity test shall be performed on semiconductor chips composing products such as IC manufactured in CMOS process and MOSFET which are susceptible to static electricity at element level.

4.7 Long-Term Storage

Products stored for 24 months or more shall be delivered in accordance with paragraph 4.9.1 of JAXA-QTS-2020.

4.8 Change of Tests and Inspections

Changed Group B test items and inspections specified in Table C-2 of JAXA-QTS-2020 Appendix C are as follows:

a) Internal water-vapor content

Since semiconductor chips of which reliability are affected by internal water-vapor are not mounted (only sheet reactor and capacitor) on sheet reactor mounted plane (B-plane: opposite side of marking), internal water-vapor content is not required.

Format F-1 (Text 17/35)

5. PREPARATION FOR DELIVERY

The hybrid ICs shall be prepared for delivery in accordance with paragraph 5 of JAXA-QTS-2020.

6. NOTES

Notes shall be as specified in paragraph 6 of JAXA-QTS-2020.

6.1 Definition of Terms

The definition of terms specified in paragraph 1.2 of JAXA-QTS-2020 shall be used.

6.2 Notice for Acquisition Officers

The precautions taken by the acquisition officers shall be as follows and as specified in paragraph 6.3 of JAXA-QTS-2020.

6.2.1 Handling Instructions[*1]

a) It is known that if gold plated leads, which products have lead finish letter "C" (gold plating), are soldered, the gold diffuses into the solder and the joint strength is greatly reduced. When soldering of leads with gold plating cannot be avoided, the gold plating on the surface of the leads shall be removed by appropriate means such as dipping to molten solder and mechanical methods.

b) In handling, static electricity countermeasures such as wrist strap (earth band) and grounded electrostatic conductive mat shall be taken.

c) At lead forming, stress shall not be loaded to lead brazing

d) Reflow shall not be allowed.

e) Recommended soldering condition is as follows. Soldering iron shall be grounded.
Iron tip temperature : 270 to 350 ℃
Heating time : 2 to 5 sec

Format F-1 (Text 18/35)

Table-9 Screening*1

Order	Test items	Test methods / conditions ([1])
1	Stabilization bake ([2])	1008 Condition C (150°C, 48 hours)
2	Thermal cycle test	1010 Condition C
3	Constant acceleration test ([3])	2001 Condition A Y1,Y2-direction
4	Visual inspection([3])	([4])
5	Particle Impact Noise Detection test	2020 Condition A ([5]) Only B-plane([6])
6	Serialization ([7])	
7	Radiograph inspection	2012 Only Y-direction
8	Interim electrical parameter test (Group A subgroup 1)	([8]) In accordance with Table-3.
9	Burn-in test	1015 min. 240 hrs., min. Tc=125°C, Figure-6
10	Seal	1014.13 ([9])
11	Final electrical parameter test a) Static characteristic 1) 25°C (Group A subgroup 1) 2) Max. and Min. operating temperature (Group A subgroups 2 and 3)	In accordance with Table-3.
12	External visual inspection	2009

Notes

([1]) 4-digit number refers to test method number of MIL-STD-883.

([2]) This test shall be performed just before sealing.

([3]) This inspection may be exempted if this inspection is performed during in-process inspection.

([4]) Defective lead, damaged package and lid peeling shall be inspected.

([5]) Acceptance criteria of Part Impact Noise Detection test shall be as follows:
Percent Defective Allowable (PDA) of each inspection lot shall be maximum 1%. The manufacturer shall not perform additional Part Impact Noise Detection test prior to screening in order to exclude devices which have possibility of including particle. Unless otherwise specified, single lot may be subject to additional Part Impact Noise Detection test four times (after excluding devices which have possibility of including particle). Resubmitted lot, of which PDA (parts applied to retest) does not satisfy 1%, shall be considered as fail.

([6]) Opposite side of marking shall be B-plane.

([7]) This inspection may be performed prior to thermal cycle test.

([8]) Electrical parameter variation before and after burn-in test shall be estimated and the products, whose variation exceeds specified delta limit value, shall be considered as fail.

Format F-1 (Text 19/35)

PDA of burn-in test shall be 3% for functional failure (single failure is allowed) and 10% for all failure (same failure mode) (single failure is allowed). The lot which failed burn-in test shall be disposed in accordance with paragraph B.3.2.

(^{9}) When helium mixed gas is used as internal filler gas of hybrid IC, test condition A1 shall be applied to fine leak test. Specified helium pressurization shall not be performed. When helium mixed gas is not used as internal filler gas, test condition A2 shall be applied to fine leak test. Applied pressure of tracer gas (He) shall be 105.9kPa abs {30psi}. Test condition C1 shall be applied to gross leak test. Vacuum and pressurization cycle shall not be performed.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 20/35)

Table-10 Group A Test ([1]) ([2]) ([3])*1

Subgroup	Measurement condition and allowance	LTPD
Subgroup 1 Static characteristic test (Tc=25℃)	In accordance with Table-3.	5
Subgroup 2 Static characteristic test (Tc=Max. operating temp.) ([4])		7
Subgroup 3 Static characteristic test (Tc=Min. operating temp.) ([5])		7

Notes

([1]) When all electrical parameters specified in subgroups of Group A test are obtained at final electrical parameter test, obtained final electrical parameter test of hybrid IC which passes screening test may be used as sample data for Group A test.

([2]) Test samples subjected to Group A test may be subject to Group tests B, C, D and E.

([3]) Single sample may be used for all subgroups.

([4]) Static characteristics at maximum operating temperature shall be measured after all internal element temperature (junction temperature for semiconductor chips) has reached at thermal equilibrium state and case temperature is minimum 80% of maximum operating temperature.

([5]) Static characteristics at minimum operating temperature shall be measured after junction temperature has reached at thermal equilibrium state and case temperature is maximum 20% of minimum operating temperature.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 21/35)

Table-11 Group B Test *1

Subgroup	(1) Test method	Test condition or criteria	Sample size (accept no.)
Subgroup 1 (2)(8)			
a) External dimension inspection	2016	In accordance with paragraph 4.6.2.	3 (0)
b) Internal gas analysis (9)	1018	100℃, with max. 5000ppm moisture contents, Only A-plane (3)	3 (0)
Subgroup 2 (4)			
a) Resistance to solvent (2)	2015	Solvent a	1 (0)
b) Internal visual and mechanical	2013 and 2014		2 (0)
c) Bonding strength test	2011		LTPD15 (5)
1) Thermocompression 2) ultrasonic 3) Thermo-sonic 4) Resistance welding		Condition D	
d) Die shear test	2019		3(0) (6)
Subgroup 3 (2) (8) Solderability test	2003	245℃±5℃	LTPD15 (7)
Subgroup 4 (2)			
a) Lead integrity	2004	Condition B_2	LTPD15 (10)
b) Seal	1014.13		3 (0)
1) Fine		Condition A_2 (105.9kPa abs {30psia})	
2) Gross		Condition C_1 (105.9kPa abs {30psia}, 23.5 hrs.)	

Notes(1) Number refers to test method number of MIL-STD-883.
(2) Electrical defective parts in identical inspection lot may be used.
(3) Marking side shall be considered as A-plane.
(4) Except for a), when Group C test is performed using identical inspection lot, samples subjected to subgroup 2 of Group C test shall be used.
(5) Sample size of hybrid IC shall be 3 and LTPD shall be applicable to type and number of each sample's wire and bonding.
(6) Sample size of hybrid IC shall be 3 and all chips of each sample shall be tested. When same type of chips is included, single chip may be tested.

Format F-1 (Text 22/35)

([7]) Sample size is minimum 1. LTPD shall be applied to number of leads.

([8]) When electrical defective parts are applied, the parts shall be exposed to thermal condition identical to thermal test at screening (stabilization bake, thermal cycle test and burn-in test) for conforming parts.

([9]) This test shall be performed using 1 sample within 1 year or 1 sample every 500 sample.

([10]) Sample size of hybrid IC shall be 3. LTPD shall be applied to number of leads, and 5 leads for 1 sample shall be tested.

Note: [*1] The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 23/35)

Table-12 Group C Test *1

Subgroup	Test method (1)	Test condition or criteria	Sample size (accept no.)	
			Level Ⅰ	Level Ⅱ
Subgroup 1 a) Steady-state operating life test b) End point electrical parameter test	1005	Tc=minimum 125℃, minimum 1000 hours. Figure-6 In accordance with Table-3 of Group A subgroups 1, 2 and 3	LTPD10	(4) LTPD15
Subgroup 2 a) External visual inspection b) Particle Impact Noise Detection Test c) Thermal cycle test d) Shock test e) Vibration test f) Seal 1) Fine 2) Gross g) Particle Impact Noise Detection Test h) External visual inspection i) End point electrical parameter test (2)	 2020 1010 2002 2007 1014.13 2020 	In accordance with method 2009 inspection criteria. Condition A Condition C, 100 cycle (3) Condition B, 6-axis Condition A, 3-axis Condition A_2 (105.9kPa abs) Condition C_1 (105.9kPa abs, 23.5 hours.) Condition A In accordance with method 1010 inspection criteria. In accordance with Table-3 of Group A subgroups 1, 2 and 3.	5 (0)	5 (0)
Subgroup 3(5) a) Electrostatic discharge destruction test b) End point electrical parameter test	3015	All combination of pins shall be tested. Group A, subgroup 1	3(0) (6)	—

Notes (1) The number refers to test method number of MIL-STD-883.
(2) This test may be performed prior to sealing test.

Format F-1 (Text 24/35)

(3) Test cycle shall be 20 at level Ⅱ.

(4) When size of inspection lot is less than 50, sample size and accept number may be 5 and 0, respectively.

(5) Element-level test (for semiconductor chips, subgroup 5 of lot evaluation test in Appendix A) may be substituted for this test.

(6) Sample size is applicable to every combination of identical pin.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 25/35)

Table-13 Group D Test *1

Subgroup	(1) Test method	Test condition or criteria	Sample size (accept no.)
Subgroup 1 a) Thermal shock b) Moisture resistance c) Seal 1) Fine 2) Gross d) Visual inspection	 1011 1004 1014.13	 Condition B, 15 cycle Condition A_2（105.9kPa abs） Condition C_1（105.9kPa abs, 23.5 hours.） In accordance with inspection criteria of method 1010 or 1011.	5 (0)
Subgroup 2 (2) a) Mechanical shock b) Vibration test c) Seal 1) Fine 2) gross d) Visual inspection	 2002 2007 1014.13	 Condition B, 6-axis Condition A, 3-axis Condition A_2（105.9kPa abs） Condition C_1（105.9kPa abs, 23.5 hours.） In accordance with inspection criteria of method 2002 or 2007.	5 (0)
Subgroup 3(3) a) Salt atmosphere test	1009	Condition A	5 (0)

Notes (1) The number refers to test method number of MIL-STD-883.
(2) Samples subjected to subgroup 1 may be used.
(3) Electrical defective parts of identical inspection lot or identical type of sealed package may be used.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 26/35)

Table-14 Group E test ([1])*1

Subgroup	([2]) Test method	Test condition or criteria	Sample size (accept no.)
Subgroup 1 a) Radiation hardness test (total dose test) b) End point electrical parameter test	1019	In accordance with paragraph 4.6.5 and Figure-7. Group A subgroup 1 In accordance with paragraph 4.6.5.	5 (0) ([3]) ([4])

Note ([1]) When radiation hardness test at semiconductor chip level is performed instead of Group E test, the test shall be performed in accordance with JAXA-QTS-2020 paragraph 1.3.5 and Appendix A.

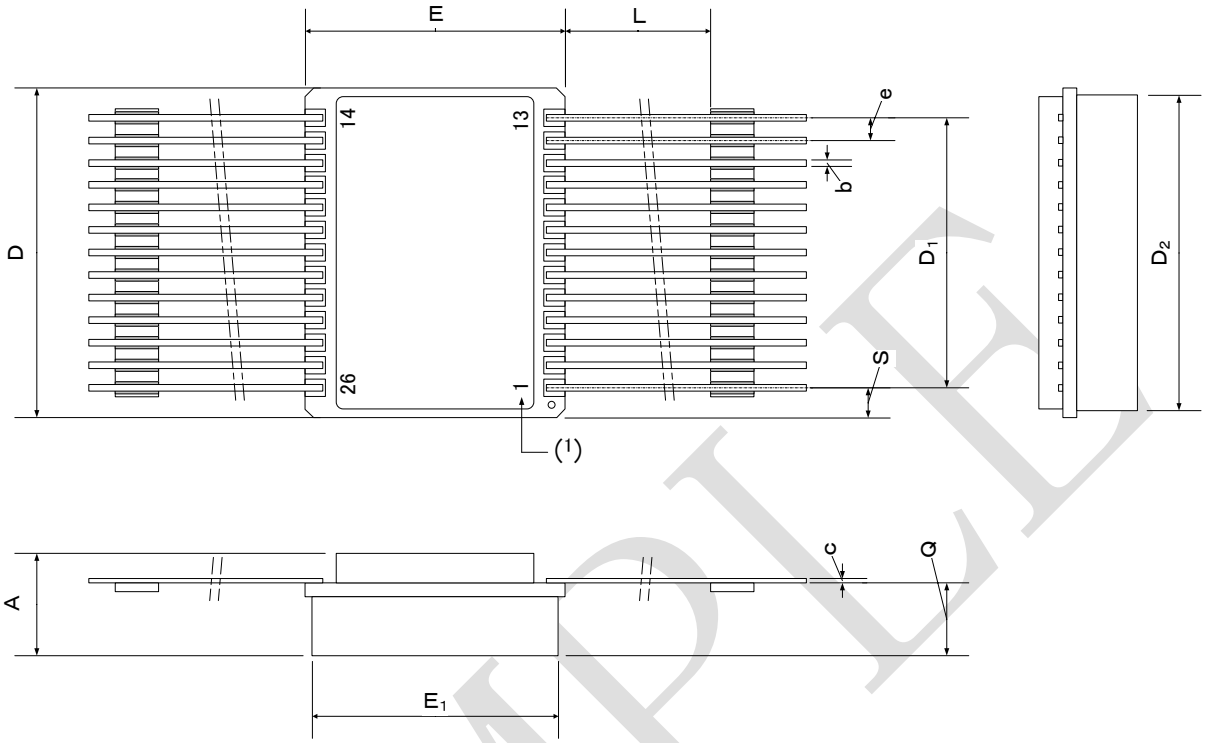
([2]) This number refers to test method number of MIL-STD-883.

([3]) This test shall be performed at each inspection sub-lot. When single wafer lot composes multiple inspection sub-lots, single inspection sub-lot may be represented.

([4]) This sample size shall be applied to each radiation hardness assurance level.

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 27/35)



(Note) Package material: Ceramic, Fe-Ni-Co alloy

Unit: mm

Letter	Dimension		Note
	Minimum	Maximum	
A	5.35	6.05	
b	0.30	0.46	(2)
c	0.20	0.30	(2)
D	18.70	19.30	(3)
D_1	14.80	15.70	
D_2	17.90	18.50	
E	14.80	15.20	(3)
E_1	13.90	14.50	
e	1.27STD		(4)
L	15.00	—	
Q	3.85	4.75	
S	1.50	2.20	(5)

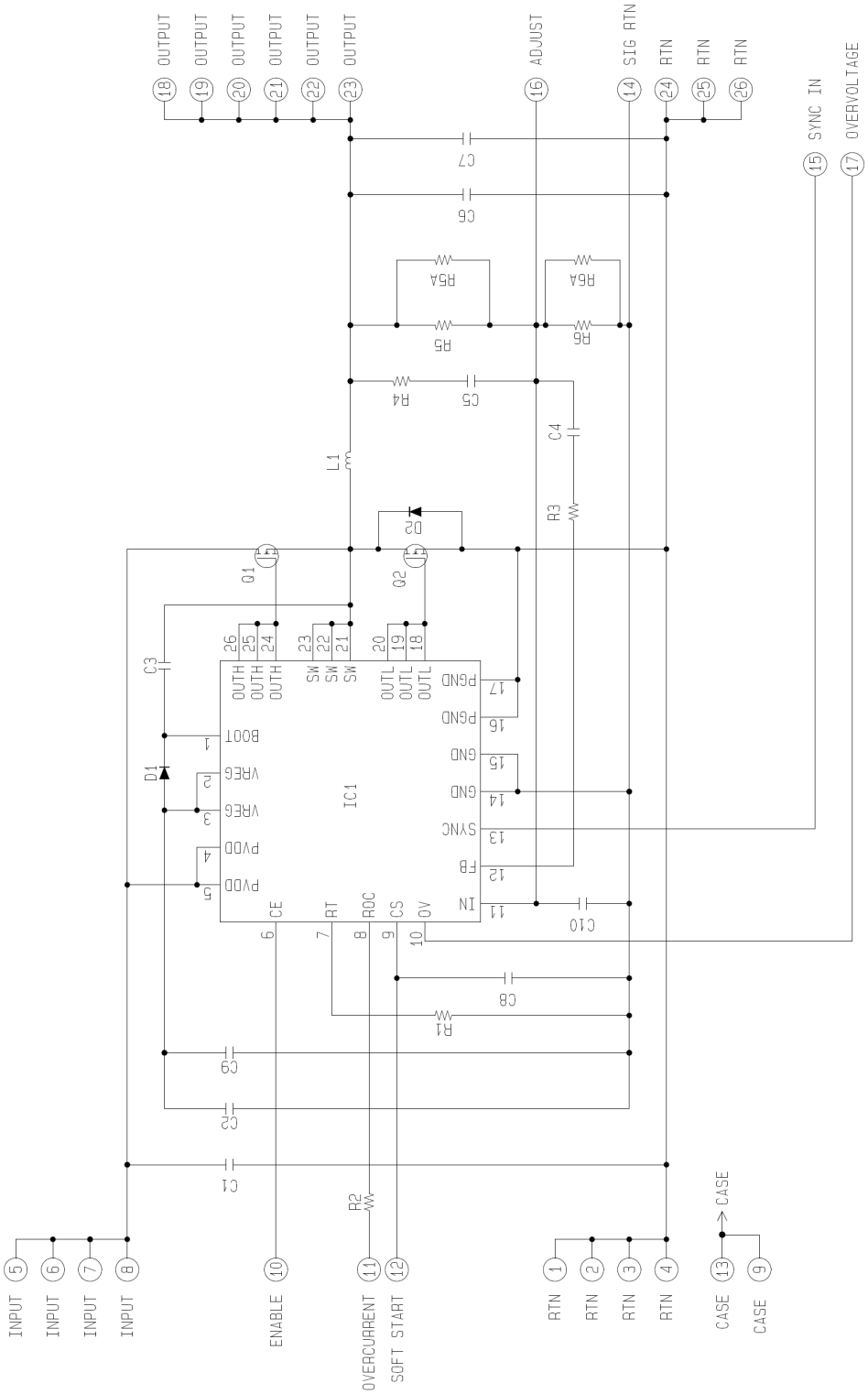
Notes:
(1) Index location
(2) Applicable to all leads.
(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.
(5) Applicable to no. pin number 1, 13, 14 and 26.

* Weight: 7.2g (maximum value)

Figure-1 Package Configuration DB (26 lead) *1

Note: *1 The table shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 28/35)

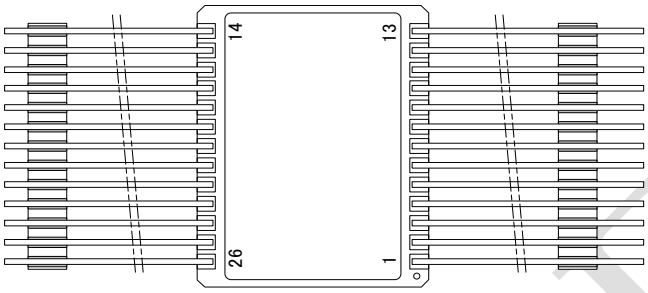


(Note) Pin No. 9 and 13 which are the common terminal and shall be connected to the GND of the board so that every conductors will be connected.

Figure-2 Circuit Diagram (Identification Number 00) *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 29/35)



Pin No.	Letter	Function
1	RTN	Input / output GND terminal
2	RTN	
3	RTN	
4	RTN	
5	INPUT	+Input terminal
6	INPUT	
7	INPUT	
8	INPUT	
9	CASE	Case GND terminal
10	ENABLE	External ON/OFF control terminal
11	OVERCURRENT	Output overcurrent limit adjustable terminal
12	SOFT START	Soft-start time adjustable terminal
13	CASE	Case GND terminal
14	SIG-RTN	Signal GND terminal
15	SYNC IN	Synchronized signal input terminal
16	ADJUST	Output voltage adjustable terminal
17	OVERVOLTAGE	Output overvoltage limit setting terminal
18	OUTPUT	+Output terminal
19	OUTPUT	
20	OUTPUT	
21	OUTPUT	
22	OUTPUT	
23	OUTPUT	
24	RTN	Input / output GND terminal
25	RTN	
26	RTN	

(Note) Pin No. 9 and No.13 are connected with seal ring and lid.

Figure-3 Pinout *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 30/35)

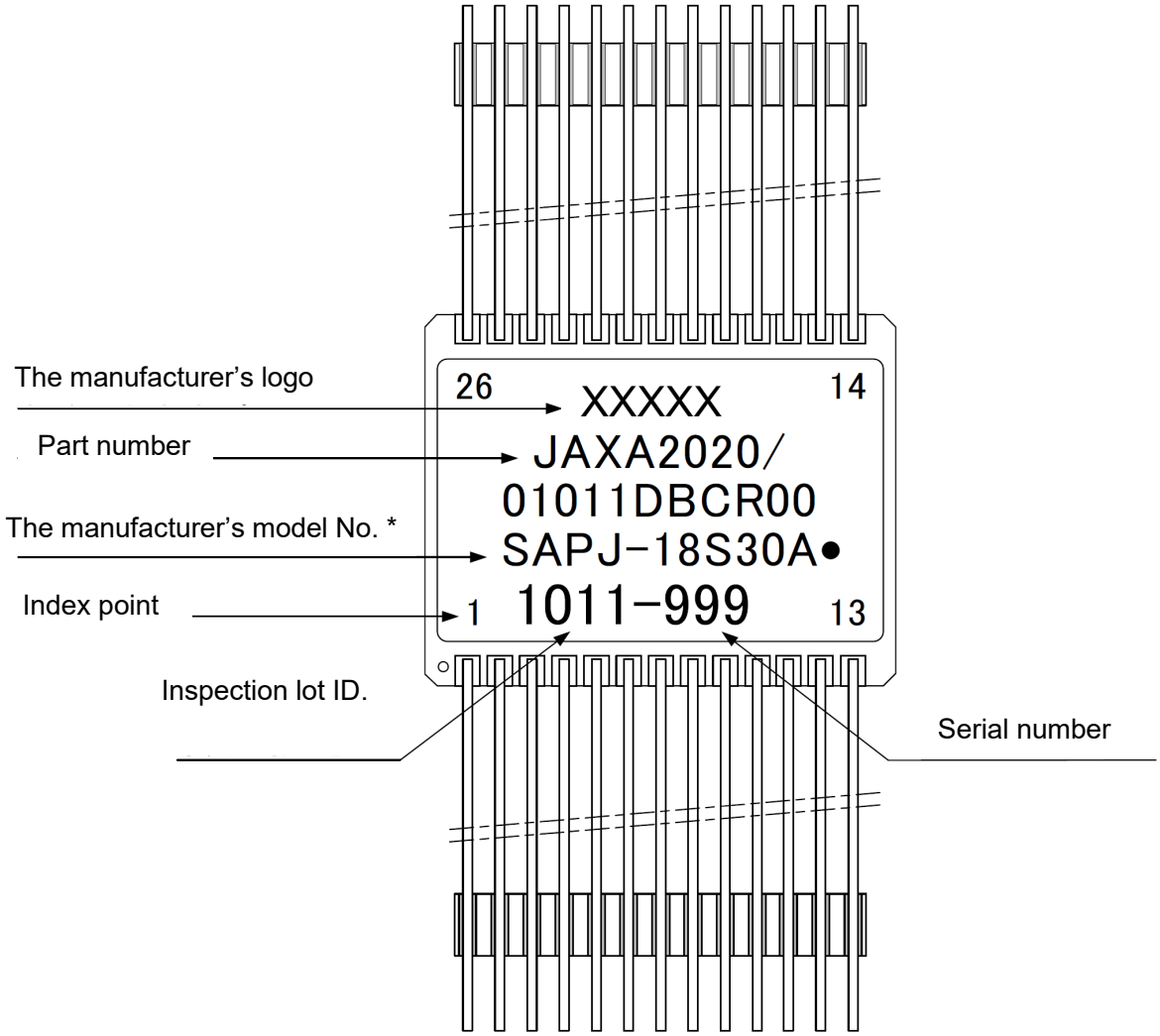


Figure-4 Marking *1

＊: When ● is not shown, this part's orbital life may be within 10 years.

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 31/35)

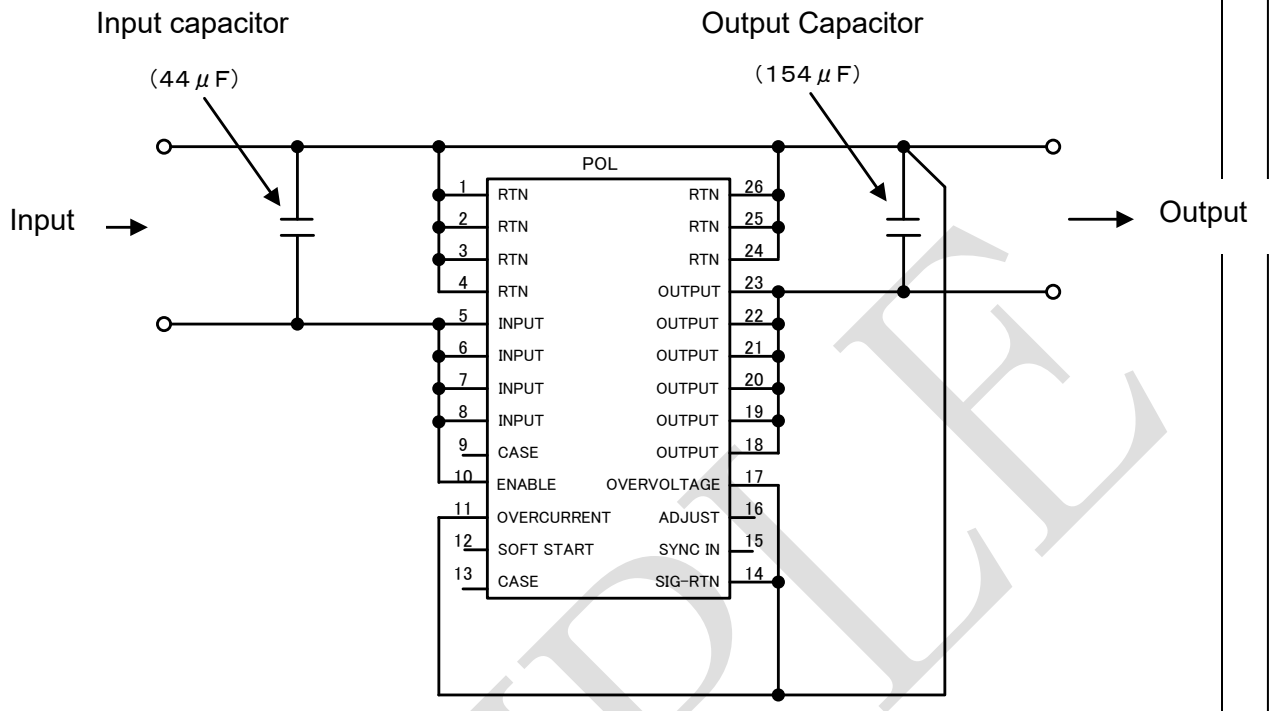


Figure-5 Basic Connection*1

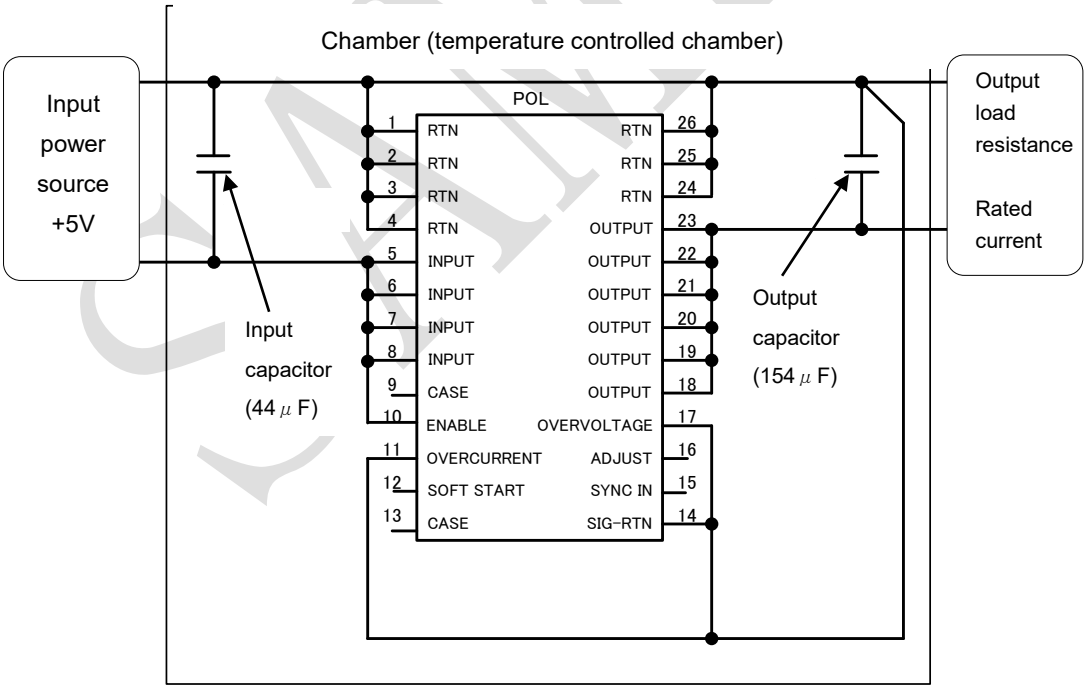


Figure-6 Test Circuit for Burn-in and Steady-state Operating Life *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 32/35)

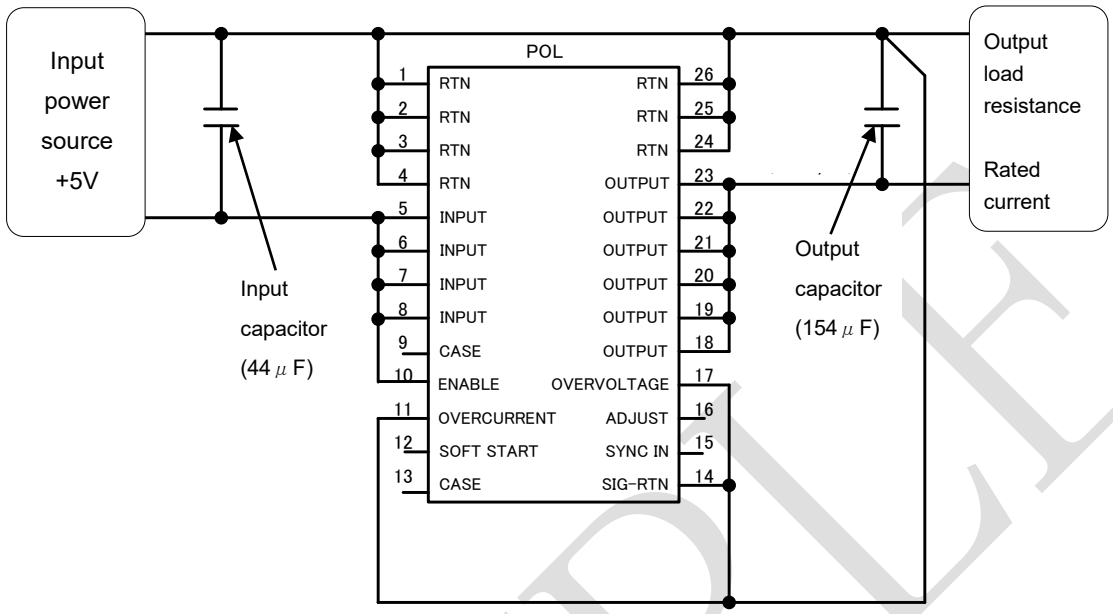


Figure-7 Radiation Hardness Test - Bias Circuit *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 33/35)

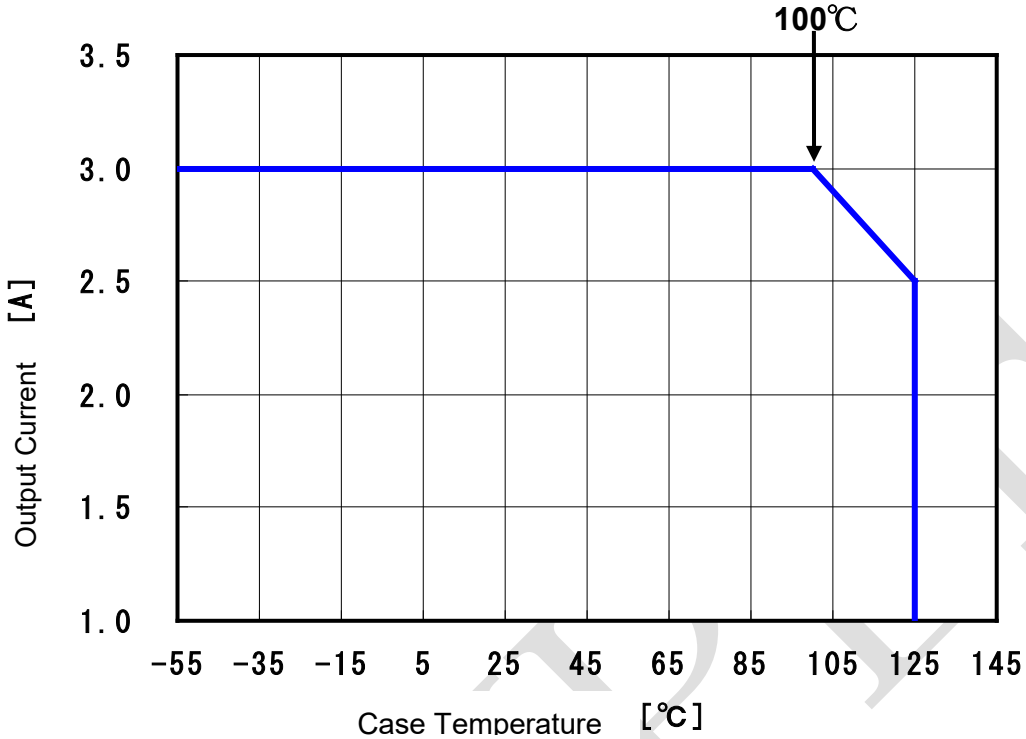


Figure-8 Output Current Limit (Vin=16V, 1.2V, 1.5V, 1.8V output)*1

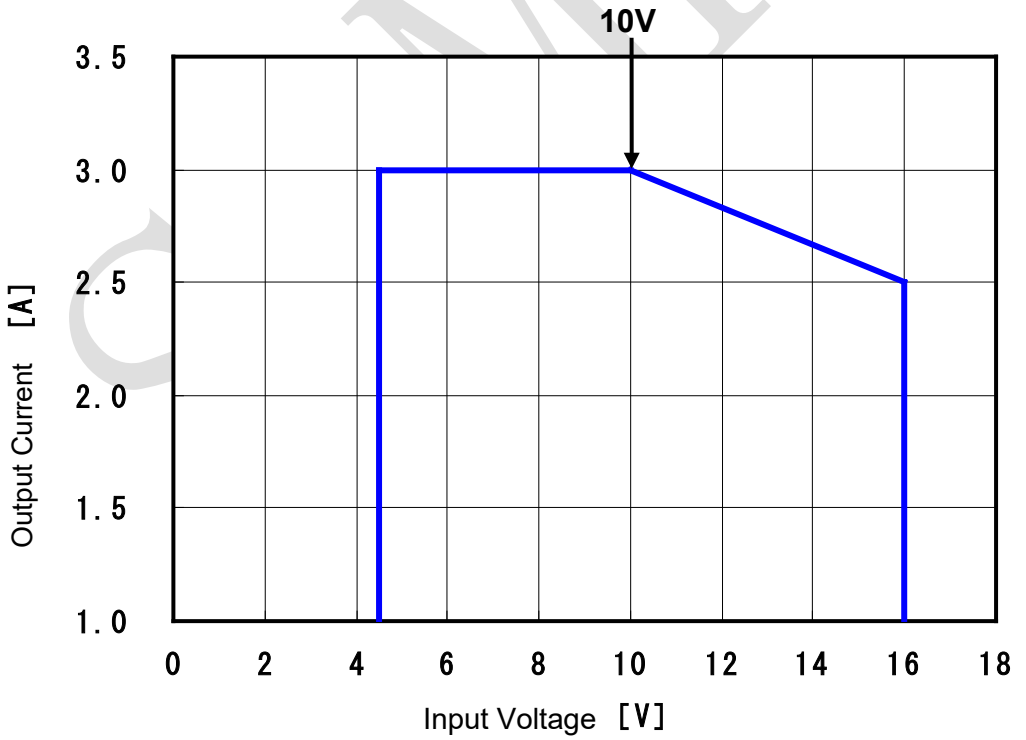


Figure-9 Output Current Limit (Tc=+125℃, 1.2V, 1.5V, 1.8V output) *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 34/35)

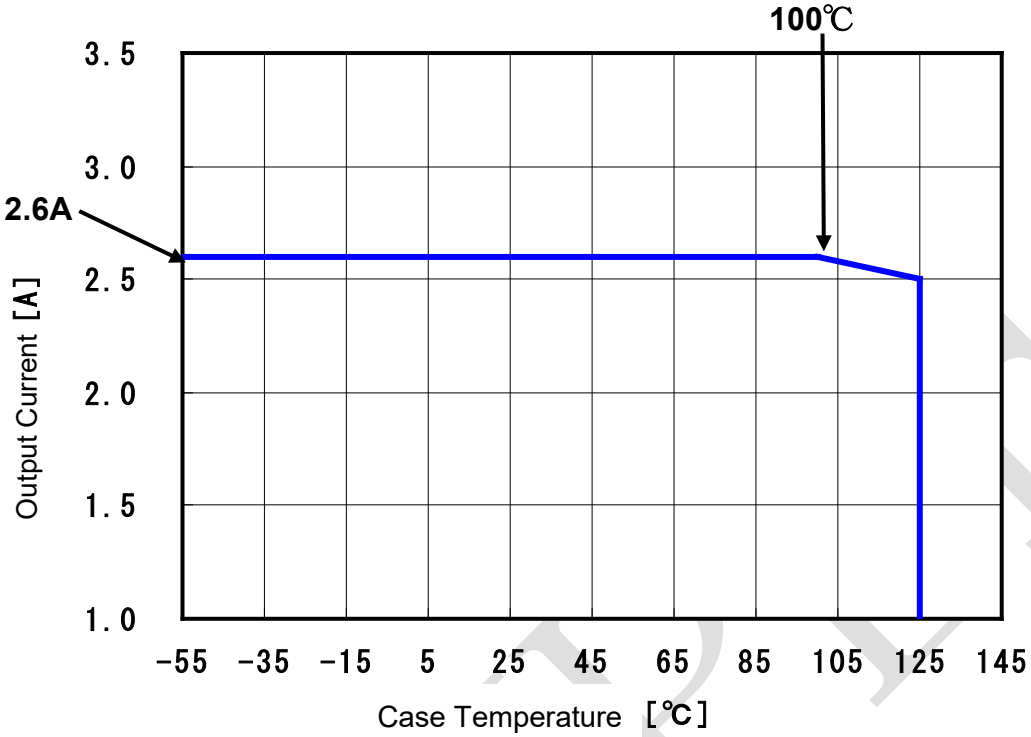


Figure-10 Output Current Limit (Vin=16V, 2.5V output)*1

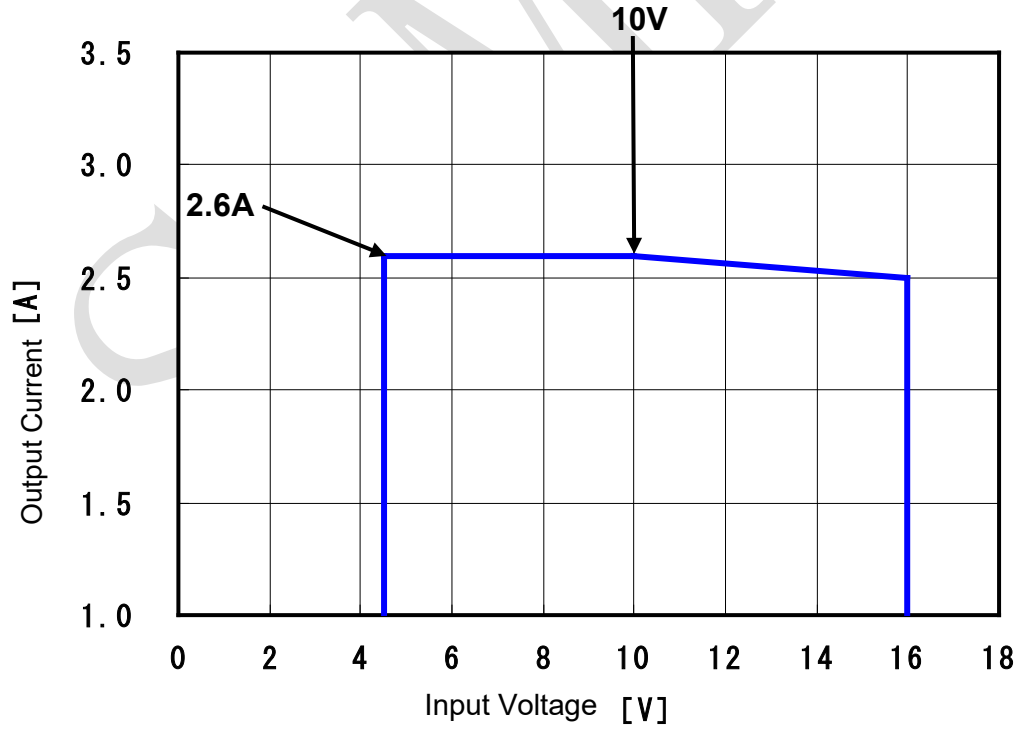


Figure-11 Output Current Limit (Tc=+125℃, 2.5V output) *1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

Format F-1 (Text 35/35)

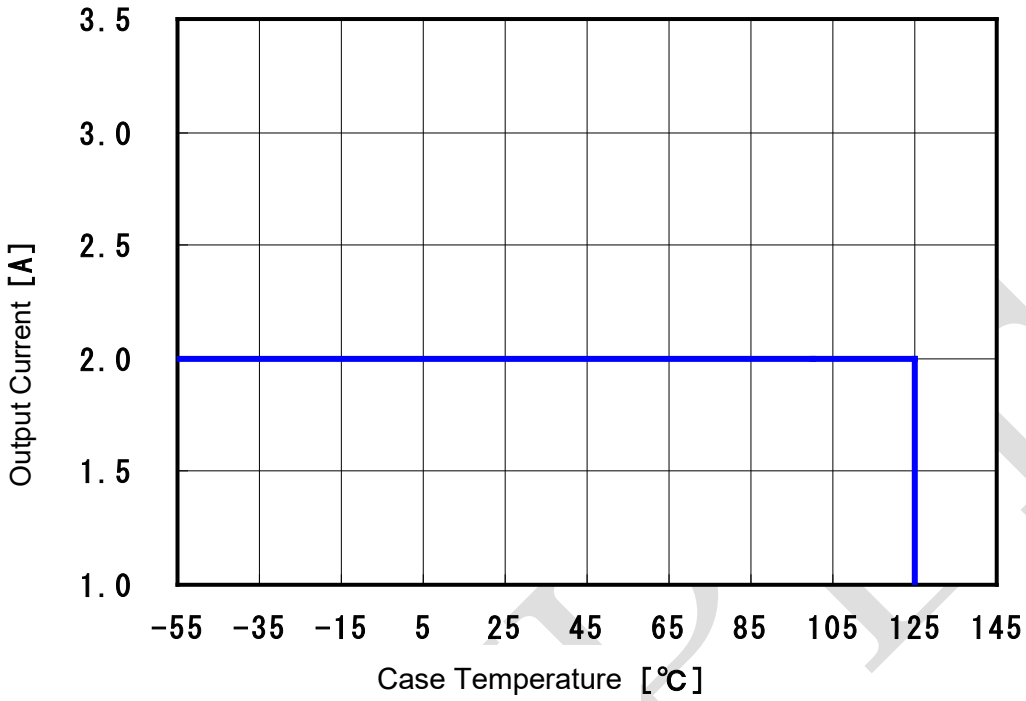


Figure-12 Output Current Limit (Vin=16V, 3.3V output)*1

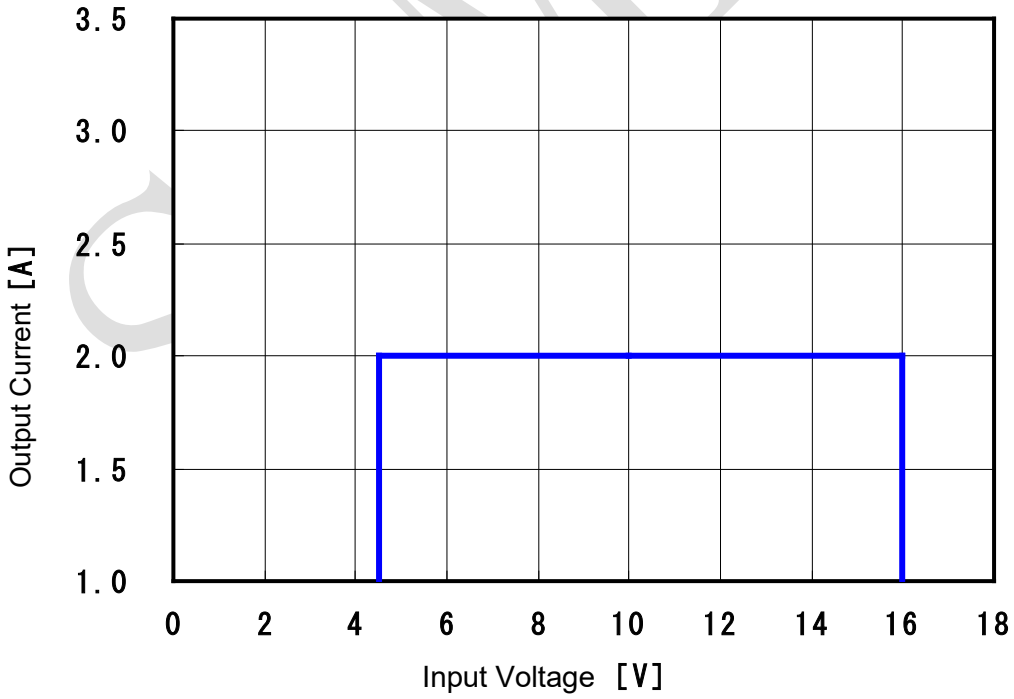


Figure-13 Output Current Limit (Tc=+125℃, 3.3V output)*1

Note: *1 The figure shown above is an example and the details may not be consistent with the contents of other pages.

APPENDIX G

PACKAGE CONFIGURATION

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX G

PACKAGE CONFIGURATION

G.1. Scope

This appendix establishes the requirements for package configuration of hybrid ICs.

G.2. Definition of Terms

The definition of terms used in this appendix shall be as follows.

a) Shape
The physical form of a package excluding dimensions.

b) Package configuration
The physical form of a package including dimensions.

c) Base plane
The reference plane, parallel to the nominal seating plane, containing the lowest point of the package body.

d) Seating plane
The reference plane which designates the interface of the case outline with the mounting surface.

e) Flat package
A package in which the base and top planes are flat and parallel and leads are parallel to the base plane (refer to Figure G-1).

f) Cylindrical package
A tubular package with external leads perpendicular to the seating plane that is attached to the circumference of the body (refer to Figure G-2).

g) Index
A reference mark such as a tab and notch that identifies the location of the first external lead position.

h) Index area
The area in which all or a portion of the index must be located.

i) Dual in-line package
A square package with leads arranged in two rows and leads are vertical to the side plane (refer to Figure G-3).

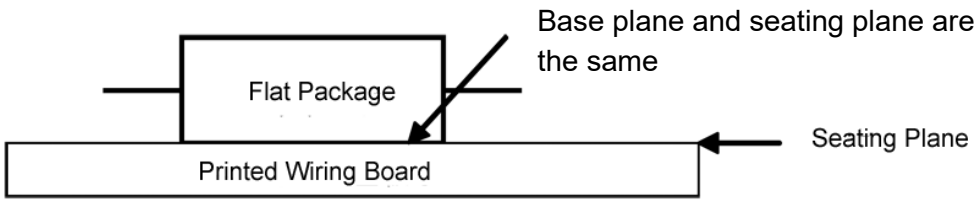


Figure G-1. Flat package

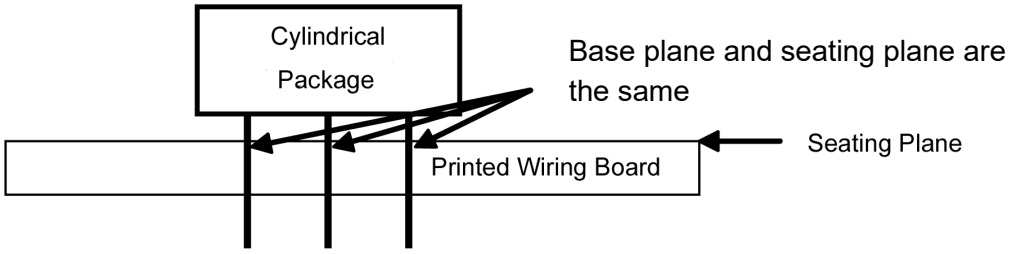


Figure G-2. Cylindrical package

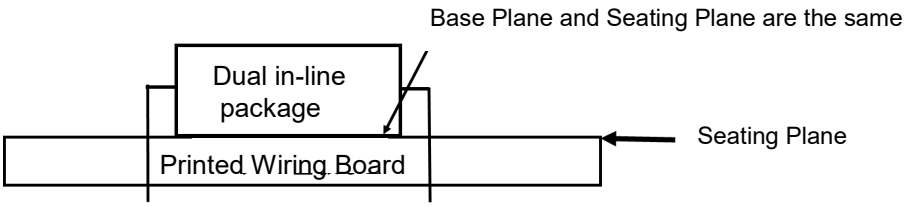


Figure G-3. Dual In-Line Package

G.3. Definition of Package Configuration

Package configuration shall be specified to meet the following requirements.

G.3.1 External Leads Numbering

For flat packages and dual in-line packages, external lead 1 shall be on the closest point to the index when viewed from the top. If the index is between two leads at equal distances, external lead 1 is located immediately adjacent to and counterclockwise from the index. The lead numbers shall increase in a counterclockwise direction. For cylindrical packages, the external lead 1 shall be at the external lead 2 location determined as specified above, and the lead numbers shall increase in a counterclockwise direction.

G.3.2 Dimensions

A minimum value, maximum value or both shall be specified for the dimensions identified with one of the symbols defined below.

A	Body height
Φb	External lead diameter
b	External lead width
c	External lead thickness
ΦD	Body diameter
D	Body length
D_1	Spacing of external lead row in the length direction
E	Body width
E_1	Spacing of external lead row in the width direction
e	External lead spacing
F	Flange dimension

k Index dimension
L External lead length
Q Standoff height (the height from the seating plane to the base plane)
S Distance between external leads and body edge
α Angle of external leads spread

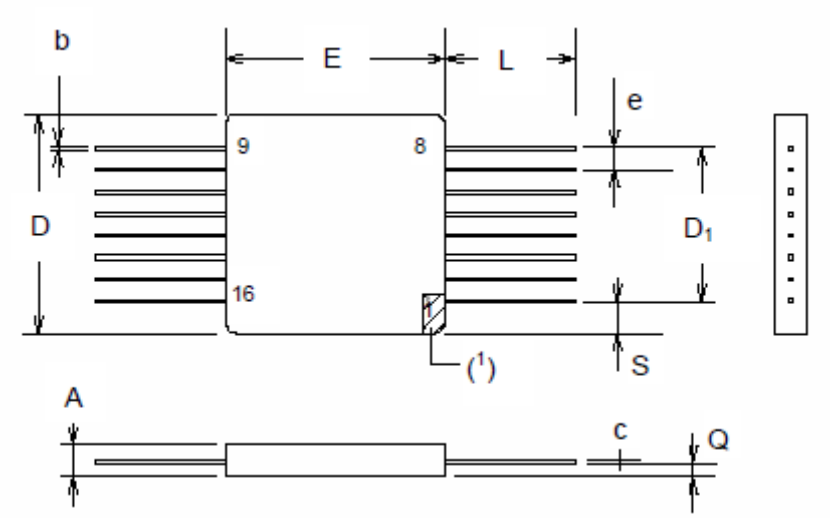
G.3.3 Drawing Requirements for Package Configuration

For flat packages, front, top, and side views shall be provided in orthogonal projections. For cylindrical packages, front and bottom views shall be provided in orthogonal projections. For dual in-line packages, front, bottom and side views shall be provided in orthogonal projections. Dimension symbols (paragraph G.3.2) shall be shown in the drawings and actual dimensions (minimum, maximum or both) with corresponding symbols shall be provided in table format.

G.3.4 Package Configuration Drawings

This section provides drawings of the typical package configurations as follows.

	Package configuration	Number of leads	Figure no.
Flat packages	HA	16	Figure G-4.
	HB	32	Figure G-5.
	HC	34	Figure G-6.
	HD	68	Figure G-7.
	HE	40	Figure G-8.
	HF	80	Figure G-9.
	HG	120	Figure G-10.
	HH	68	Figure G-11.
	HI	34	Figure G-12.
	HJ	52	Figure G-13.
Cylindrical packages	HM	12	Figure G-14.
Flat packages	DA	8	Figure G-15
	DB	26	Figure G-16
Dual in-line packages	CA	14	Figure G-17
Flat packages	CB	20	Figure G-18

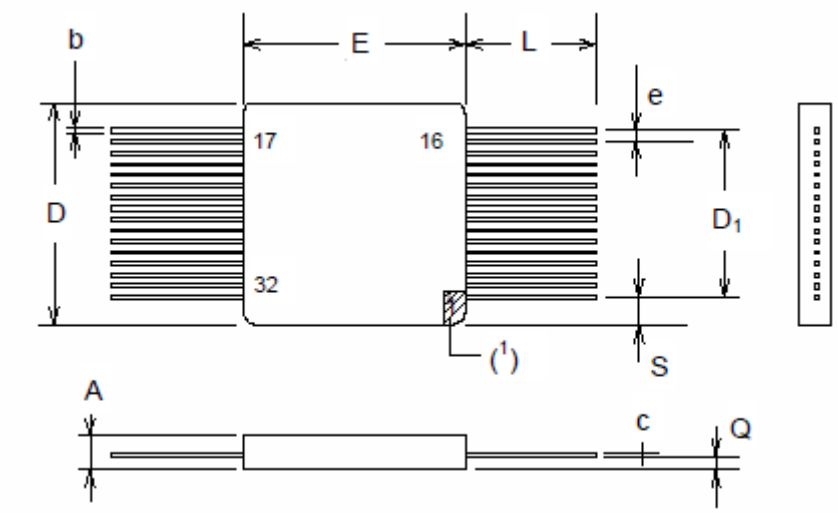


Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.31	3.91	
b	0.33	0.44	(2)
c	0.22	0.28	(2)
D	25.25	25.55	(3)
D_1	17.53	18.03	
E	25.25	25.55	(3)
e	2.54 STD		(4)
L	15.00	-	
Q	1.37	1.68	
S	3.66	3.96	(5)

Notes:
(1) Index location
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.
(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 2.54±0.25mm.
(5) Applicable to lead numbers 1, 8, 9 and 16.

Figure G-4. Package Configuration HA (16 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.31	3.91	
B	0.33	0.44	(2)
C	0.22	0.28	(2)
D	25.25	25.55	(3)
D_1	18.80	19.30	
E	25.25	25.55	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.37	1.68	
S	3.02	3.32	(5)

Notes:

(1) Index location

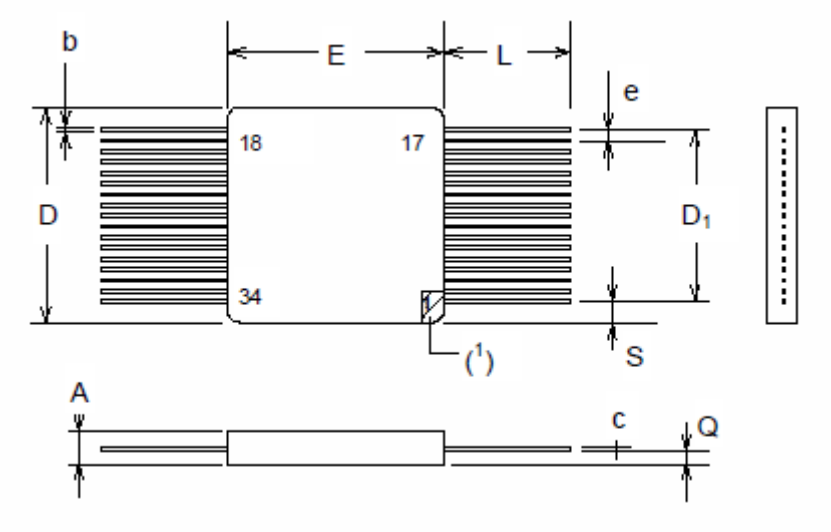
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 16, 17 and 32.

Figure G-5. Package Configuration HB (32 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.13	3.73	
b	0.33	0.44	(2)
c	0.22	0.28	(2)
D	25.25	25.55	(3)
D_1	20.07	20.57	
E	25.25	25.55	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.54	1.86	
S	2.39	2.69	(5)

Notes:

(1) Index location

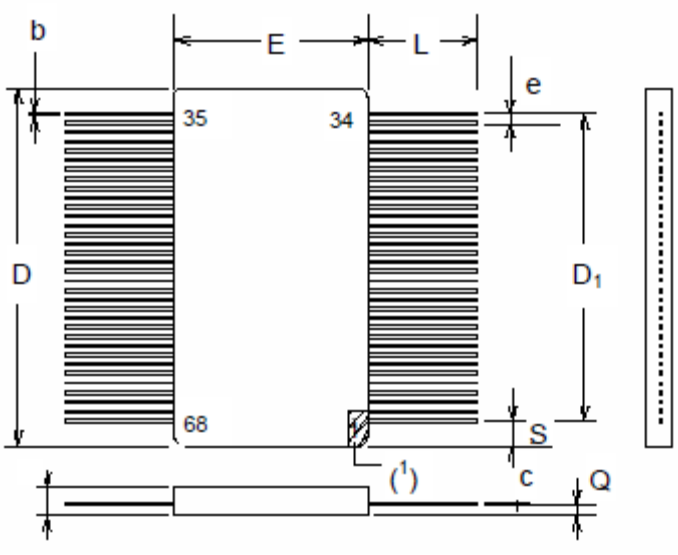
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 17, 18 and 34.

Figure G-6. Package Configuration HC (34 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.44	4.04	
b	0.33	0.44	(2)
c	0.22	0.28	(2)
D	48.75	49.05	(3)
D_1	41.66	42.16	
E	26.16	26.46	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.37	1.68	
S	3.35	3.65	(5)

Notes:

(1) Index location

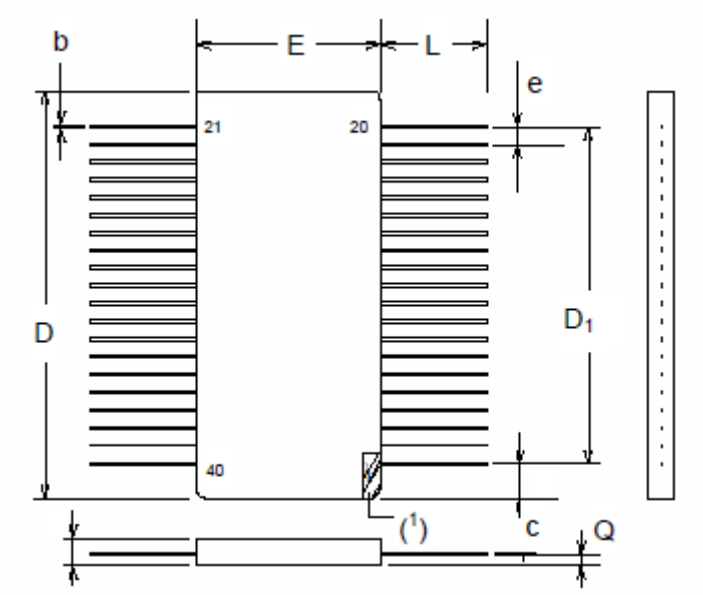
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 34, 35 and 68.

Figure G-7. Package Configuration HD (68 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.44	4.04	
b	0.33	0.44	(2)
c	0.22	0.28	(2)
D	58.27	58.57	(3)
D_1	48.01	48.51	
E	25.25	25.55	(3)
e	2.54 STD		(4)
L	15.00	-	
Q	1.49	1.81	
S	4.93	5.23	(5)

Notes:

(1) Index location

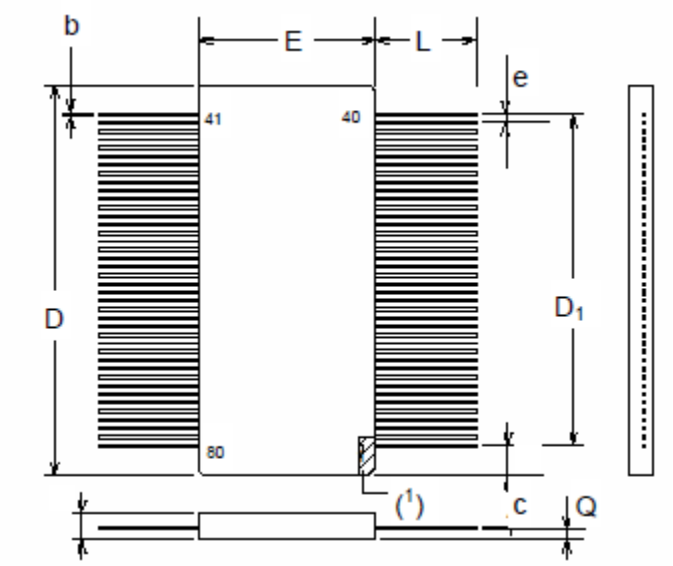
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 2.54±0.25mm.

(5) Applicable to lead numbers 1, 20, 21 and 40.

Figure G-8. Package Configuration HE (40 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.44	4.04	
b	0.33	0.44	(2)
c	0.22	0.28	(2)
D	58.27	58.57	(3)
D_1	49.28	49.78	
E	25.25	25.55	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.49	1.81	
S	4.29	4.59	(5)

Notes:

(1) Index location

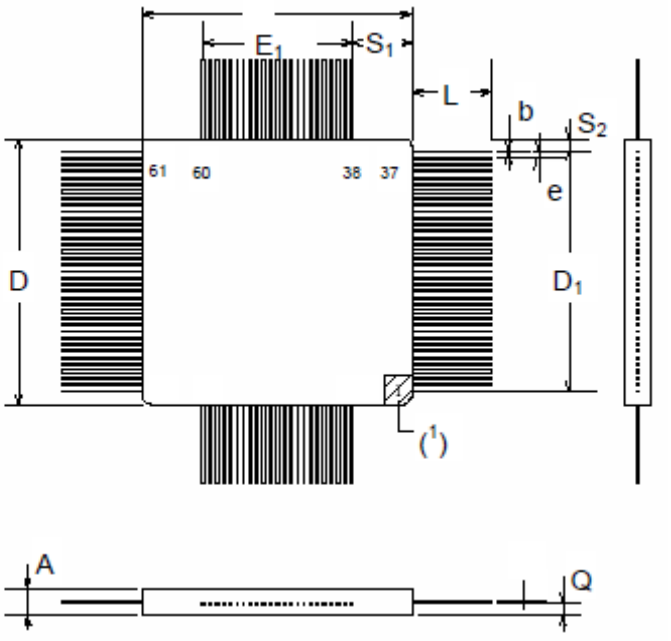
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 40, 41 and 80.

Figure G-9. Package Configuration HF (80 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	4.80	5.30	
b	0.30	0.46	(2)
c	0.20	0.31	(2)
D	50.60	51.00	(3)
D_1	45.54	45.90	
E	50.60	51.00	(3)
E_1	27.78	28.10	
e	1.27 STD		(4)
L	15.00	-	
Q	1.92	2.40	
S_1	11.26	11.60	(5)
S_2	2.38	2.70	(6)

Notes:

(1) Index location

(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

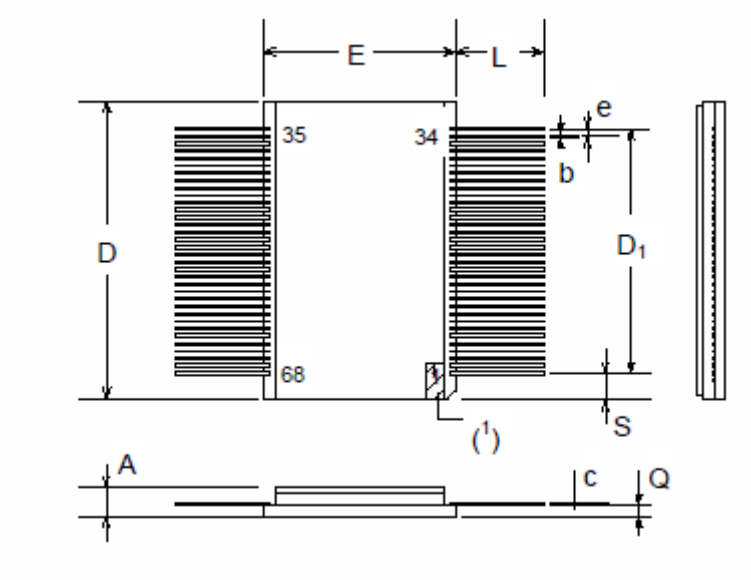
(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 38, 60, 98 and 120.

(6) Applicable to lead numbers 1, 37, 61 and 97.

Figure G-10. Package Configuration HG (120 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	4.50	5.80	
b	0.30	0.46	(2)
c	0.20	0.30	(2)
D	50.30	51.90	(3)
D_1	41.66	42.16	
E	31.80	33.00	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.45	2.05	
S	4.09	5.10	(5)

Notes:

(1) Index location

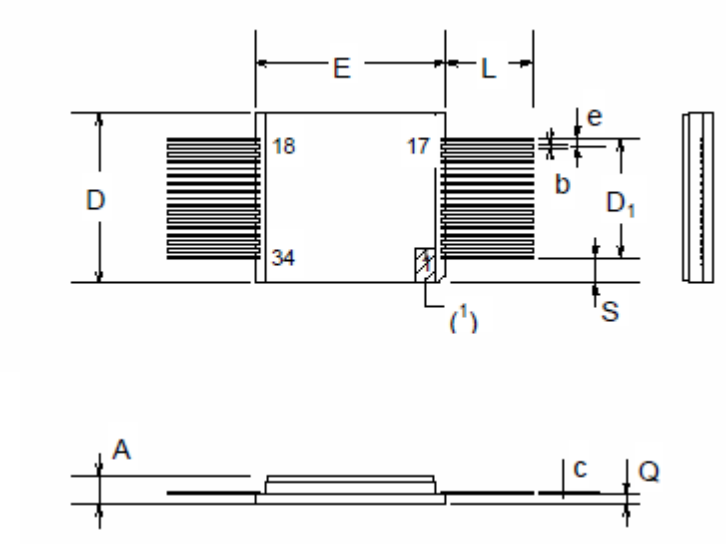
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 34, 35 and 68.

Figure G-11. Package Configuration HH (68 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	4.50	5.80	
b	0.30	0.46	(2)
c	0.20	0.30	(2)
D	26.90	28.10	(3)
D_1	20.07	20.57	
E	31.80	33.00	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.45	2.05	
S	3.08	4.10	(5)

Notes:

(1) Index location

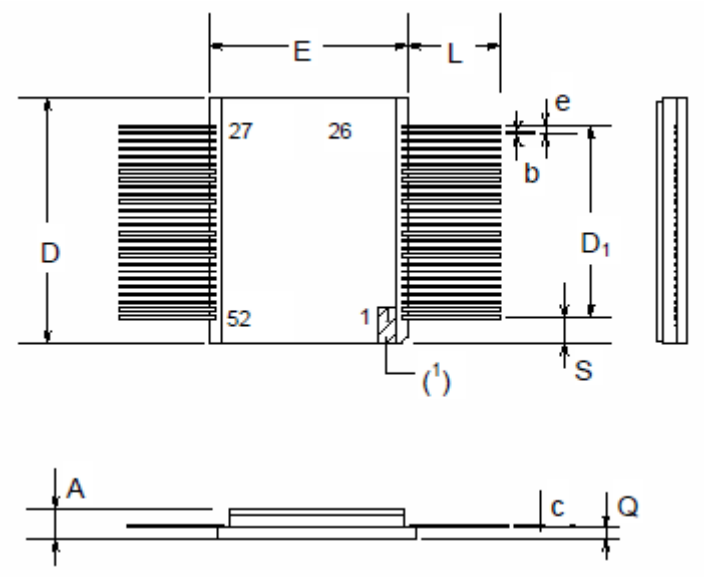
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 17, 18 and 34.

Figure G-12. Package Configuration HI (34 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	4.50	5.80	
b	0.30	0.46	(2)
c	0.20	0.30	(2)
D	38.65	40.05	(3)
D_1	31.50	32.00	
E	31.80	33.00	(3)
e	1.27 STD		(4)
L	15.00	-	
Q	1.45	2.05	
S	3.29	4.31	(5)

Notes:

(1) Index location

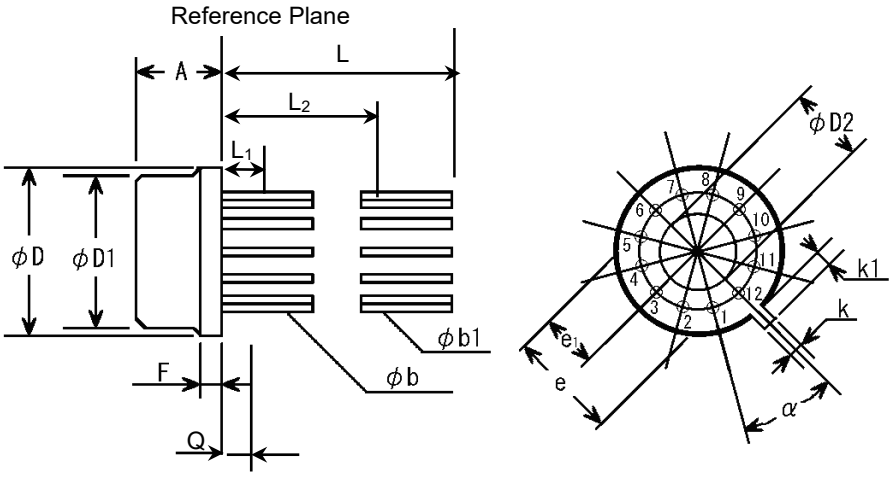
(2) Applicable to all leads. The maximum limit may be increased by 0.08mm when lead finish is a solder dip.

(3) Dimension of the off-center lid and any metal overflow at sealing shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead numbers 1, 26, 27 and 52.

Figure G-13. Package Configuration HJ (52 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	4.19	4.70	
Φb	0.41	0.48	(1), (2)
$Φb_1$	0.41	0.53	(1), (2)
ΦD	8.51	9.40	
$ΦD_1$	7.75	8.51	
$ΦD_2$	2.79	4.06	
e	5.84 STD		(3)
e_1	2.92 STD		(3)
F	-	1.02	
k	0.69	0.86	
k_1	0.69	1.14	(4)
L	12.70	19.05	(1)
L_1	-	1.27	(1)
L_2	6.35	-	(1)
Q	0.25	1.14	
α	30º STD		(3)

Notes:

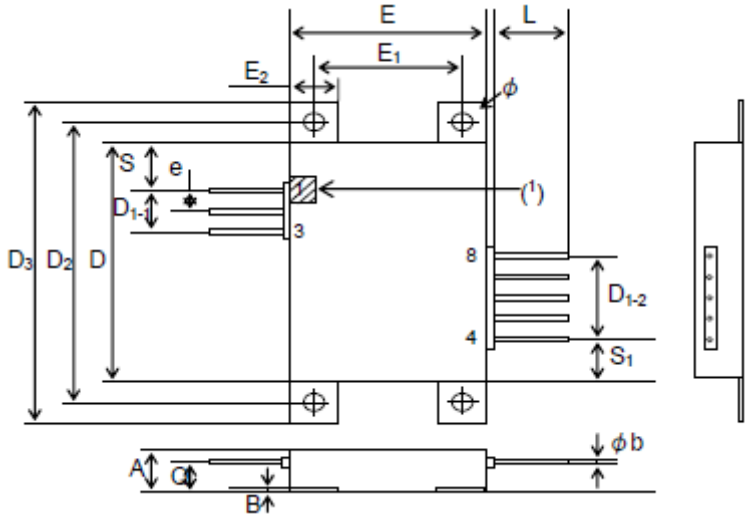
(1) Applicable to all leads.

(2) Φb applies between L_1 or L_2 from the reference plane. $Φb_1$ applies between L_2 and 12.70mm from the reference plane. The maximum limit may be increased by 0.08mm when lead finish is a solder dip. If not specified as above, the control of lead diameter is not necessary.

(3) All leads shall be positioned within 0.84mm in diameter from the center of the geometric arrangement shown in the drawings on the gauge plane, $1.37^{+0.03}_{0.00}$ mm below the base plane of the package.

(4) K_1 is obtained by measuring the value of ΦD + K_1 and arithmetically subtracting the maximum value of ΦD.

Figure G-14. Package Configuration HM (12 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	-	17.00	
B	0.90	1.10	
Φb	0.90	1.10	(2)
D	57.80	58.20	(3)
D_{1-1}	10.06	10.26	
D1-2	20.22	20.42	
D2	67.90	68.10	
D3	-	78.20	
E	39.80	40.20	(3)
E1	29.90	30.10	
E2	9.90	10.10	
e	5.08 STD		(4)
L	14.50	-	
Q	13.05	13.45	
S	10.70	11.30	(5)
S1	11.70	12.30	(6)
Φ	3.50	3.70	

Notes:

(1) Index location

(2) Applicable to all leads.

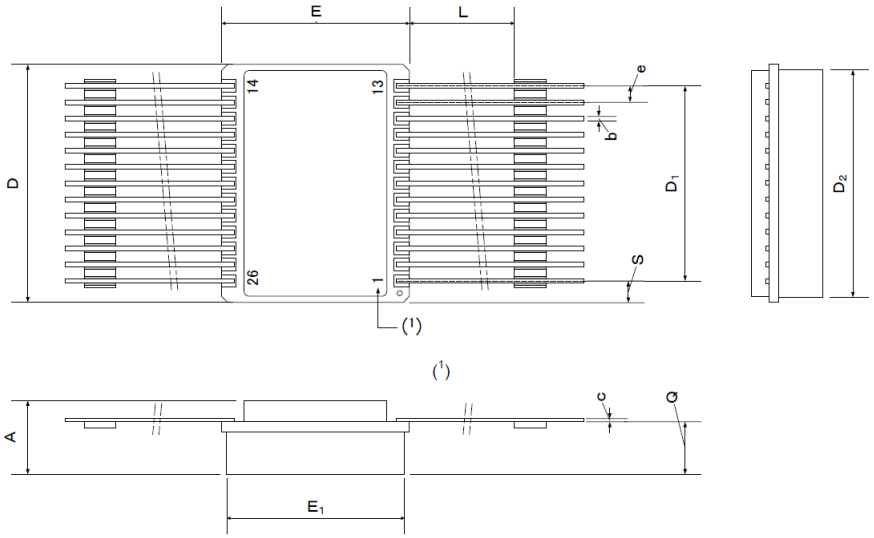
(3) Dimension of the off-center lid and any metal overflow produced during the sealing process shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 5.08±0.1mm.

(5) Applicable to lead number 1.

(6) Applicable to lead number 4.

Figure G-15. Package Configuration DA (8 leads)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	5.35	6.05	
b	0.30	0.46	(2)
c	0.20	0.30	(2)
D	18.70	19.30	(3)
D_1	14.80	15.70	
D_2	17.90	18.50	
E	14.80	15.20	(3)
E_1	13.90	14.50	
e	1.27 STD		(4)
L	15.00	-	
Q	3.85	4.75	
S	1.50	2.20	(5)

*** Weight: 7.2g (Max.)**

Notes:

(1) Index location

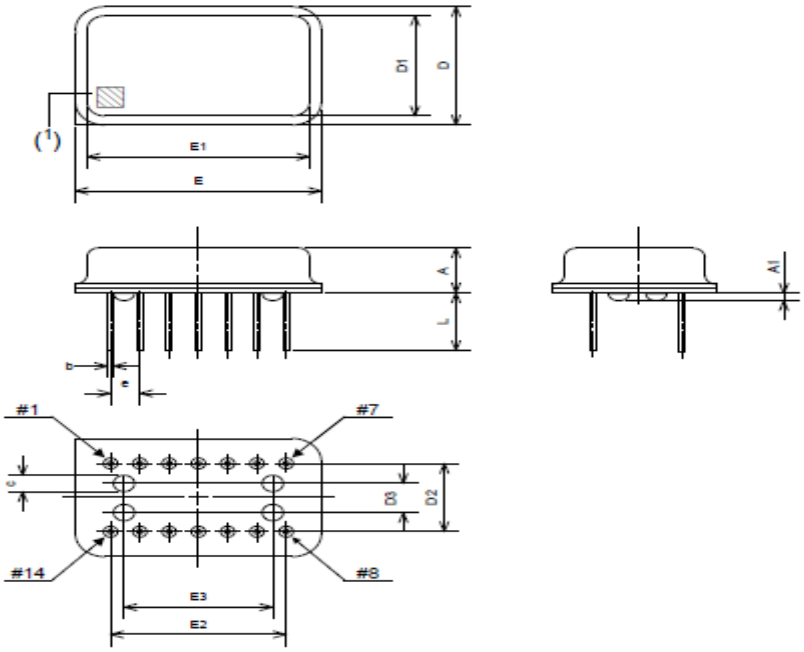
(2) Applicable to all leads.

(3) Dimension of the off-center lid and any metal overflow produced during the sealing process shall be included in the measurement.

(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

(5) Applicable to lead number 1, 13, 14 and 26.

Figure G-16. Package Configuration DB (26 leads)

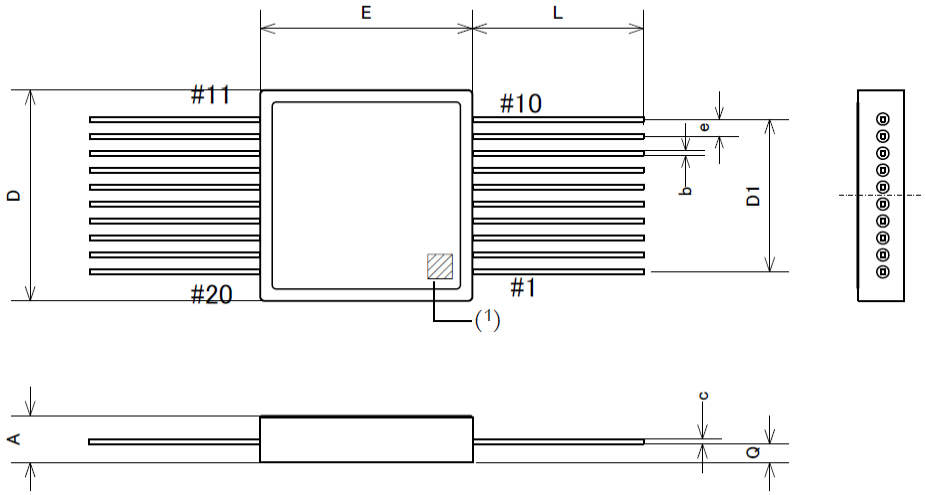


Unit: mm

Symbol	Dimensions(5)		Notes
	Min.	Max.	
A	4.5	5.1	
A1	(0.8)		(5)
b	0.35	0.55	(3)
c	(1.8)		(5)
D	12.0	13.0	(4)
D1	10.4	11.0	
D2	7.32	7.92	
D3	(3.2)		
E	19.6	20.6	(4)
E1	18.1	18.7	
E2	14.94	15.54	
E3	(12.7)		
e	2.54 STD		
L	5.85	6.85	

Notes:
(1) Index location
(2) Applicable to all leads.
(3) Dimension of the off-center lid and any metal overflow produced during the sealing process shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 2.54±0.25mm.
(5) Applicable to all standoffs.

Figure G-17. Package Configuration CA (14 pin DIP)



Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.2	3.8	
b	0.35	0.55	(2)
c	0.2	0.3	(2)
D	15.6	16.0	(3)
D1	11.13	11.73	
E	15.6	16.0	(3)
e	1.27 STD		(4)
L	12.7	-	

Notes:
(1) Index location
(2) Applicable to all leads.
(3) Dimension of the off-center lid and any metal overflow produced during the sealing process shall be included in the measurement.
(4) The relative centerline spacing of all adjacent leads shall be within 1.27±0.13mm.

Figure G-18. Package Configuration CB (20 lead flat package)

APPENDIX Z

PROCEDURE AFTER REVISION OF JAXA-QTS-2020

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

APPENDIX Z

PROCEDURE AFTER REVISION OF JAXA-QTS-2020

The transition period from JAXA-QTS-2020B and JAXA-QTS-2025 shall be one year from the established date of JAXA-QTS-2020C.
QML manufacturer and user shall coordinate with JAXA about transitional procedure.