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INTEGRATED CIRCUITS,
Multi-Core Processor, SOI-SOC, CMOS, MONOLITHIC SILICON,
HIGH RELIABILITY,
SPACE USE,

DETAIL SPECIFICATION FOR

Prepared and Established by
Mitsubishi Heavy Industries, Ltd.

Issued by Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

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Record of Revisions

Revision	Date	Description
NC	28 July 2025	Original issued in accordance with VET25310 Revision NC issued by Mitsubishi Heavy Industries, Ltd.
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Revision History

Revision	Date	Description
NC	28 July 2025	Original
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DETAIL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the detail requirements for the monolithic silicon, CMOS, SOI-SOC, Multi-Core Processor (hereinafter referred to as "IC") to be used for electronic equipment installed on spacecrafts such as satellites. Additional requirements specific to a given application may be documented separately (refer to paragraph 6).
The ICs shall be manufactured using the COT method (refer to paragraph 6.1 of JAXA-QTS-2010 Revision D for definition of terms).

1.2 Part Number

The part numbers for the IC covered by this specification are assigned as follows:

JAXA([1]) 2010/	201	01	X	Z	R
	Individual identification (paragraph 1.2.1)	Device type (paragraph 1.2.2)	Package configuration (paragraph 1.2.3)	Lead material and finish (paragraph 1.2.4)	Radiation hardness (paragraph 1.2.5)

Notes:
([1]) “JAXA” indicates that the part is for space use and may be abbreviated “J.”

1.2.1 Individual Identification

The individual identification for the IC shall be the document number of this detail specification.

1.2.2 Device Type

The device type defined in this specification shall be as follows:

Device type	Circuit
01	Multi-Core Processor

1.2.3 Package Configuration

Package configuration of the ICs defined in this specification shall be as follows:

Package configuration symbol	Package configuration
X	572 pins, CBGA

1.2.4 Pin Material

The pin material of the ICs defined in this specification shall be as shown below. The details shall be as specified in paragraph 3.1.3.

Finish letter	Pin material
Z	Sn10/Pb90 (center 8x8 terminal, solder balls), Sn63/Pb37 (all terminals except center 8x8 terminal, solder balls)

1.2.5 Radiation Hardness

1.2.5.1 TID Hardness

The radiation hardness (TID hardness) defined in this specification shall be as follows.

Letter	Radiation hardness assurance level
R	1000 Gy(Si) {1 x 10^5rad(Si)}

1.3 Absolute Maximum Ratings

The absolute maximum ratings common to the ICs defined in this specification shall be as follows.

Table 1. Absolute Maximum Ratings

Item		Symbol	Min.	Max.	Unit
Power supply voltage		V_{CCQ}	-0.3	4.6	V
		V_{DD}	-0.3	1.4	V
Input voltage (1)		V_{in}	-0.3	V_{CCQ} + 0.3	V
Output voltage (1)		V_O	-0.3	V_{CCQ} + 0.3	V
Output current	8mA buffer	$I_{O(8mA)}$	-90	86	mA
	24mA buffer	$I_{O(24mA)}$	-266	267	mA
Storage temperature		T_{stg}	-55	+150	°C
Junction temperature		T_j	-40	+125	°C

Note: (1) Shall not exceed +4.6V.

1.4 Recommended Operating Conditions

The recommended operating conditions common to the ICs defined in this specification shall be as shown in Table 2.

Table 2. Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage range		V_{CCQ}	3.0	3.3	3.6	V
		V_{DD}	1.11	1.2	1.29	V
High level input voltage		V_{IH}	0.7 x V_{CCQ}	-	V_{CCQ} + 0.3	V
Low level input voltage		V_{IL}	-0.3	-	0.2 x V_{CCQ}	V
Operating board surface temperature		T_b (1)	-37 (5)	-	+120	°C
Operating junction temperature		T_j (2)	-40 (6)	-	+125	°C
External clock frequency	When the PLL on the chip is used	f_{extclk}	-	20	-	MHz
	When the PLL on the chip is not used		-	100	-	MHz

Notes:

(1) Defined as the temperature at the board surface (directly beneath the chip edge).

(2) T_J is calculated as follows.

$T_J = T_b + \theta_{j\text{-}b} \times P_D$

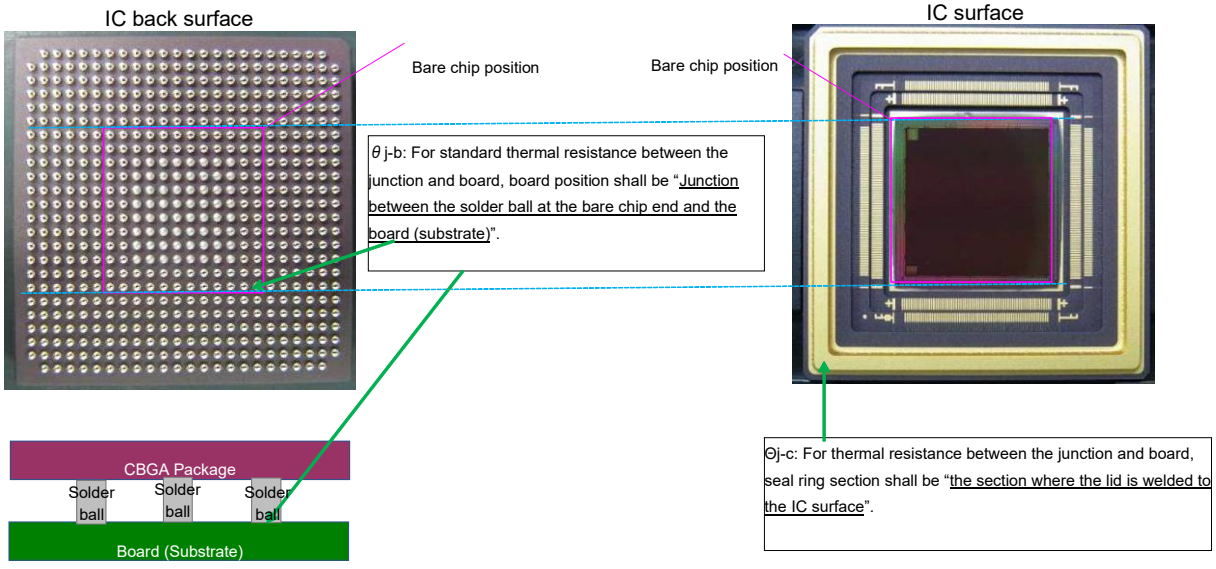
Where,

T_b: Operating board surface temperature (°C)

$\theta_{j\text{-}b}$: Standard thermal resistance between the junction and board (1.8°C/W) (3)

P_D: Power dissipation (1.8W) (4)

(3) Defined as the thermal resistance calculated in the simulation between "the junction and board surface (directly beneath the chip edge)". For reference, the thermal resistance $\Theta_{j\text{-}c}$ calculated in the simulation between "the junction and case (seal ring section)" is 7.1°C/W. Thermal design shall be performed to ensure that the absolute maximum rating T_{jmax} is not exceeded.
The locations of $\theta_{j\text{-}b}$ and $\Theta_{j\text{-}c}$ are shown below.



(4) Simulation results under the worst-case power consumption conditions (manufacturing process: fast corner, temperature: 125°C, V_{DD}: 1.29V, V_{CCQ}: 3.6V, toggle rate: 10%, operation frequency: 160MHz, including I/O power consumption).

(5) Specified as the upper limit value for the test conditions of the package.

(6) Specified as the upper limit value for the test conditions of the wafer.

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1.5 Function and Performance

The function and performance of the ICs defined in this specification shall be as shown in Table 3.

Table 3. Function and Performance (1/4)

Item	Specification	Construction	Overview
Processor core	Renesas RXv3	2 cores	- Operation frequency: 160MHz (Temperature: +125°C, operation voltage: 1.11V, worst path) - Operation frequency: 190MHz (Temperature:+25°C, operation voltage: 1.2V, worst path) - Double-precision FPU support (customized for Multi-Core Processor)
Core peripheral functions	DMAC (DMA controller)	CPU0: 4ch CPU1: 4ch	- Equivalent to RX64M product (DMACAa) by Renesas
	DTC (Data transfer controller)	CPU0: 1ch CPU1: 1ch	- Equivalent to RX64M product (DTCa) by Renesas
	EXDMAC (EXDMA controller)	CPU0: 2ch CPU1: -	- Equivalent to RX64M product (EXDMACa) by Renesas - External bus transfer only - However, the following functions are excluded: (1) Transfer to SDRAM (2) Control via external pins (EDREQ and EDACK)
	BSC (Bus controller)	CPU0: 1ch CPU1: -	- Equivalent to RX64M product (BSC) by Renesas
	ICU (Interrupt controller)	CPU0: 1ch CPU1: -	- Equivalent to RX64M product (ICUA) by Renesas
High-speed communication I/F	SpaceWire (SpaceWire communication function)	CPU0/1 shared: 6ch	- Refer to Table 4. - Support for SpaceWire/RAMP, SpaceWire-PTP and RAW packet
	Ethernet (EthernetAVB communication function)	CPU0/1 shared: 2ch	- Refer to Table 4.

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Table 3. Function and Performance (2/4)

Item	Specification	Construction	Overview
Low-speed communication I/F	MIL-STD-1553B (MIL-STD-1553B communication function)	CPU0/1 shared: 2ch	- Refer to Table 4.
	CAN (CAN communication function)	CPU0: 1ch CPU1: 1ch	- Refer to Table 4.
	Multifunction serial (SCI)	CPU0: Max. 2ch CPU1: Max. 2ch	- Refer to Table 4. - Shared pins with GPIO
	SPI (SPI communication function)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 4. - Shared pins with GPIO
	I2C (I2C communication function)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 4. - Shared pins with GPIO
Universal I/O	GPIO (Universal input and output)	CPU0/1 shared: Max. 76ch	- Refer to Table 4. - Shared pins with PWM, SPI, I2C, SCI, TMR and CMTW
	PWM (GPT) (Universal PWM timer)	CPU0: Max. 4ch CPU1: Max. 4ch	- Refer to Table 4. - Shared pins with GPIO
Timer	TMR (8-bit timer)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 4. - Shared pins with GPIO
	WDTA (Watchdog timer)	CPU0: 1ch CPU1: 1ch	- Refer to Table 4.
Processing support	CRC (CRC processing circuit)	CPU0: 1ch CPU1: 1ch	- Refer to Table 4.
	DOC (Data processing circuit)	CPU0: 1ch CPU1: 1ch	- Refer to Table 4.
Internal memory (1)	Code RAM	CPU0/1 shared: 4MByte	- Implemented accelerator and memory scrubber
	Shared memory	CPU0/1 shared: 2MByte	- Implemented accelerator and memory scrubber
	Local RAM	CPU0: 64kByte CPU1: 64kByte	- Implemented memory scrubber (option)

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Table 3. Function and Performance (3/4)

Item	Specification	Construction	Overview
External memory (1)	Universal external bus controller	CPU0: 1ch CPU1: -	- Equivalent to RX64M product (CSC) by Renesas
	SDRAM controller	CPU0: 1ch CPU1: -	- RX64M product (SDRAMC) by Renesas with the following modifications. (1) Added error correction functions (capable of correcting multi-bit errors using Reed-Solomon codes). Note that the function may be enabled or disabled. (2) Expanded the address space to a maximum of 512MB. - Throughput between external SDRAM and internal memory: Minimum 100Mbps
Debug I/F			- Compatible with Renesas original emulators (E1 emulator).
Boot function			- After reset, CPU0 acquires the fixed address of the CS1 area as a vector and executes the program. - The following addresses may be switched by configuring the MODE pin (external terminal). (1) CS1 base address (2) 2Mbyte offset (3) 4Mbyte offset
Security		CPU0: 1ch CPU1: 1ch	- Implemented the functions shown in Table 5. - Supports the equivalent of TSL 1.3 authentication methods.

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Table 3. Function and Performance (4/4)

Item	Specification	Construction	Overview
Power consumption	Maximum 1W	-	- Temperature: +25°C, operation voltage: 1.2V, except for external I/O power consumption. - Total power consumption of Multi-Core Processor (when using 2 cores).
	1.8W (Worst case) (For reference)	-	- Simulation results under worst-case power consumption conditions (manufacturing process: fast corner, temperature: +125°C, VDD: 1.29V, VCCQ: 3.6V, toggle rate: 10%, operating frequency: 160MHz, including I/O power consumption). - Total power consumption of Multi-Core Processor (when using 2 cores).
Radiation hardness	TID hardness	-	- 100krad(Si)
	SEL hardness	-	- Minimum threshold LET: 75 MeV/(mg/cm^2) (Tj = +125°C)
	SEU hardness	Logic cell (Flip-Flop)	- Minimum threshold LET: 40 MeV/(mg/cm^2) - Maximum saturated cross section (Flip-Flop): 2 x 10^{-9} (cm^2/cell)
		Local RAM	- Minimum threshold LET: 40 MeV/(mg/cm^2) (2) (3) - Maximum saturated cross section: 2 x 10^{-9} (cm^2/bit)
		Code RAM and shared memory	- Based on the saturated cross section (9.96x10^{-10}(cm^2/bit)), the Scrubbing Period (4) was calculated from the target threshold LET for each orbit. - The target threshold LET for each orbit and Scrubbing Period are shown in (5).

Notes:

(1) This area may be used for program storage. However, an accelerator for external memory access has not been implemented.

(2) The LET value when the saturated cross section is 1/100th of the saturated cross section without SEU countermeasure.

(3) The LET value without scrubbing. The ICs have EDAC and scrubbing functions.

(4) The Scrubbing Period is defined as the amount of time required to read, modify and write all memory within the specified range.

(5) Refer to the following table.

No.	Target LET Threshold (6) for Each Orbit	Scrubbing Period
1	Equivalent to a threshold LET ≥ 25 MeV/(mg/cm^2) in the ISS orbit	327680 (seconds)
2	Equivalent to a threshold LET ≥ 40 MeV/(mg/cm^2) in the GEO orbit	1310 (seconds)

(6) Defined as the results of calculating the threshold LET (the LET value when the saturated cross section is 1/100th of the saturated cross section without SEU countermeasure) using the saturated cross section.

(7) The calculation conditions for orbital flux when calculating the Scrubbing Period are shown below.
- Aluminum shielding thickness: 2.54mm
- Solar activity: Solar min.

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Table 4. List of Peripheral IP Addresses (1/2)

IP name	Overview	CPU0		CPU1		IP Specification
		unit	ch	unit	ch	
SpW Engine	SpaceWire communication function	6	6	Shared with CPU0		
SpW Router	SpaceWire Router	2	6	Shared with CPU0		
Mil-STD-1553B	MIL-STD-1553B communication function	2	2	Shared with CPU0		
GPIO	Universal input and output	1	76	Shared with CPU0		
Ethernet (for DualUse)	EthernetAVB communication function	2	2	Shared with CPU0		- Equivalent to RZA1H (EthernetAVB) by Renesas
PWM (GPT)	Universal PWM timer	1	4	1	4	- Equivalent to RX64M product (GPTa) by Renesas
SPI	SPI communication function	1	1	1	1	- Eqivalent to RX64M product (RSPIa) by Renesas
Multifunction serial (SCI)	Serial communication function	2	2	2	2	- Equivalent to RX64M product (SCIg) by Renesas
CRC	CRC processing unit	1	1	1	1	- Equivalent to RX64M product (CRC) by Renesas
DOC	Data processing unit	1	1	1	1	- Eqivalent to RX64M product (DOC) by Renesas
WDTA	Watchdog timer	1	1	1	1	- Eqivalent to RX64M product (WDTA) by Renesas
OS timer	16/32 bit compare match timer	5(1)	5(1)	5(1)	5(1)	- Equivalent to RX64M product (CMTW) by Renesas Note (1): Two of the five channels share CPU0/CPU1.
CMTW	16/32 bit compare match timer	2	2	2	2	- Equivalent to RX64M product (CMTW) by Renesas
TMR	8bit timer	1	1	1	1	- Equivalent to RX64M product (TMR) by Renesas

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Table 4. List of Peripheral IP Addresses (2/2)

IP name	Overview	CPU0		CPU1		IP Specification
		unit	ch	unit	ch	
CAN	CAN communication function	1	1	1	1	- Equivalent to RX64M product (CAN) by Renesas
I2C(RIIC)	I2C communication function	1	1	1	1	- Equivalent to RX64M product (RIICa) by Renesas
CPG	Clock generation circuit	1	1	-	-	

Table 5. Security Function and Cryptographic Performance

Major Function Item	Minor Function Item	Function Summary
Encryption and decryption function	Data encryption function	Function for encrypting data and generating signature and authentication codes
	Encrypted communication function	Function for keeping the contents of communication data confidential from third parties
	Classified information management function	Function for restricting access to confidential information
Falsification prevention and detection function	Destination authentication function	Function for inhibiting communication with unknown parties
	Software authentication function	Function for inhibiting the operation of unauthorized software
	Countermeasures for flaw exploitation attacks	Function for preventing leakage of confidential information due to out of specification operation
Cryptographic Performance		
Security level indicator: 128-bit security		

2. RELATED DOCUMENTS

2.1 Applicable Documents

The documents listed below shall form a part of this specification to the extent specified herein.

a)	JAXA-QTS-2010D	Integrated Circuits, High Reliability, Space Use, General Specification for
b)	MIL-STD-883L	Test Methods Standards – Microcircuits
c)	JAXA-QTS-2000F	Common Parts/Materials, Space Use, General Specification for
d)	JESD22-B115A	SOLDER BALL PULL
e)	CCA-115025A	Proceedings of lot certification
f)	JERG-0-043E	Standard for Surface Mount Soldering Process for Space Use
g)	JERG-0-054A	Standard for BGA/CGA Mounting Process for Space Use
h)	J-STD-002E	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

2.2 Order of Precedence

Order of precedence shall be as specified in paragraph G.2.3, Appendix G of JAXA-QTS-2010.

3. REQUIREMENTS

To supply the ICs under this specification, certified manufacturers shall comply with all requirements specified in this section and paragraph G.3, Appendix G of JAXA-QTS-2010.

3.1 Design and Construction

Design and construction of the ICs shall be in accordance with the requirements specified in this section and paragraph G.3.3, Appendix G of JAXA-QTS-2010.

3.1.1 Operating Temperature

The operation temperature range of the ICs shall be defined as the board surface (directly beneath the chip edge) temperature. The minimum and maximum operating temperatures shall be -37°C and +120°C, respectively.

3.1.2 Package Configuration

The package configuration (including mass) shall meet the requirements specified in Figure 1.

3.1.3 Pin Material

The pin material for center 8x8 terminal shall be the solder ball content of high-temperature solder (Sn10/Pb90). The pin material for all terminals except center 8x8 terminal shall be the solder ball content of eutectic solder (Sn63/Pb37).

3.1.4 Block Diagram and Pin-Outs

The block diagram of ICs shall be in accordance with Figure 2 and the pin-outs shall be as specified in Table 6 and Figure 3.

3.1.5 Electrical Characteristics

The electrical characteristics shall be in accordance with Tables 7 and 8.

3.2 Marking

Marking on the products shall be as specified in paragraph G.3.4, Appendix G of JAXA-QTS-2010. An example is shown in Figure 4.

3.3 Certification

The manufacturer shall acquire certification in accordance with paragraph G.3.1, Appendix G of JAXA-QTS-2010 and paragraph 3.4.1.10 of JAXA-QTS-2000.

3.4 Quality Assurance Program

Quality assurance program shall be in accordance with paragraph G.3.2, Appendix G of JAXA-QTS-2010.

4. QUALITY ASSURANCE PROVISIONS

The quality assurance shall meet the requirements of this section and paragraph G.4, Appendix G of JAXA-QTS-2010.

4.1 General Requirements

The general requirements shall be in accordance with paragraph 4.1 of JAXA-QTS-2010.

4.2 Functional Drawing Control

The functional drawing control shall be in accordance with paragraph G.4.1, Appendix G of JAXA-QTS-2010.

4.3 Incoming Materials Control

The incoming materials control shall be in accordance with paragraph G.4.2, Appendix G of JAXA-QTS-2010.

4.4 Manufacturing Process Control

Manufacturing process control shall be in accordance with paragraph G.4.3, Appendix G of JAXA-QTS-2010.
However, since the wafer is a catalog item, the requirements specified in items a) through g) of paragraph G.4.3.1, Appendix G of JAXA-QTS-2010 shall not be applied.

4.5 In-Process Inspection

The in-process inspection shall be in accordance with paragraph G.4.4, Appendix G of JAXA-QTS-2010.

4.6 Screening

The screening shall meet the requirements specified in this section and paragraph G.4.6, Appendix G of JAXA-QTS-2010.

4.6.1 Screening Items and Conditions

Screening items and conditions for the ICs defined in this specification shall be as specified in Table 9.

4.6.2 Electrical Parameters to be Measured

At the pre burn-in and final electrical parameters test of the screening test, all parameters included in the following subgroups, among those shown in Table 10 shall be measured.

Pre burn-in electrical parameter test	Subgroups 1 and 7
Post burn-in electrical parameter test	Subgroups 1 and 7
Final electrical parameter test	Subgroups 1, 2, 3, 7, 8, 9 10, and 11
Electrical parameter test after eutectic solder ball attach	Subgroups 1,7, and 11

4.6.3 Burn-In Test Circuit

The burn-in test in the screening test shall be performed using the circuits shown in Figure 44.

4.6.4 Delta Limits

The delta limits for the burn-in test shall be as shown in Table 19.

4.7 Qualification Test for JAXA-developed Parts and Quality Conformance Inspection

The qualification test for JAXA-developed parts and quality conformance inspection shall meet the requirements specified in paragraphs G.4.5 and G.4.7, Appendix G of JAXA-QTS-2010, respectively.
However, when lot certification for wafer (specified in CCA-115025A) is applied to quality conformance inspection, other requirements specified in this section shall also apply.

4.7.1 Test/Inspection Items and Conditions

Test/inspection items and conditions for the ICs defined in this specification shall be as specified in Tables 10 through 14.

4.7.2 Electrical Parameters to be Measured

In the qualification test for JAXA-developed parts and quality conformance inspection, all electrical parameters included in the following subgroups specified in Tables 10 through 14 shall be measured.

Group A test	Subgroups 1, 2, 3, 7, 8, 9, 10, and 11
Group C test, subgroup 1(c)	Subgroups 1, 2, 3, 7, 8, 9, 10, and 11
Group C test, subgroup 2(d)	Subgroups 1, 2, and 3
Group C test, subgroup 3(b)	Subgroup 1
Group D test, subgroup 1(f)	Subgroup 1
Group D test, subgroup 2(e)	Subgroup 1
Group E test, subgroup 1(b)	Subgroups 1, 7, and 9

Group E test, subgroup 2(b) Subgroups 1, 7, and 9

4.7.3 Exemption of Tests and Inspections

The tests or inspections may be exempted as specified in paragraph G.4.7.1.1, Appendix G of JAXA-QTS-2010 or when one of the following conditions is met.

a) Exemption of group A test
When the test items of the final electrical parameters of the screening test is the same as those of the group A test, the group A test may be exempted for the inspection lot if the lot passed the final electrical parameter test and if failed products were removed.

b) Exemption of group E tests
Group E tests may be exempted when the radiation hardness is not required for the ICs in the same inspection lot. In this case, the radiation hardness designator "R" shall not be marked on the ICs.

4.8 Long-Term Storage

4.8.1 Disposition of Products Stored for a Long-Term at the Manufacturer's Site

Disposition of products stored for a long-term at the manufacturer's site shall be in accordance with paragraph G.4.8, Appendix G of JAXA-QTS-2010.

4.8.2 Storage by Purchasers

The storage conditions at purchaser's sites shall be as follows.

a) Ambient temperature: +15°C to +35°C
b) Relative humidity: No more than 35% (The ICs shall be stored in a desiccator to prevent the formation of oxide on the surface of the solder balls).
c) Pressure: 86kPa to 106kPa
d) Others: Vibration and shock shall not be applied.

4.9 Change of Tests and Inspections

4.9.1 Inspection of Wafer Lot

The manufacturer shall purchase wafers in conformance with the manufacturer's specifications (catalog) and shall verify that the wafers are in accordance with the specifications at item a) "Incoming inspection". Upon confirmation of wafer compliance with the specifications, those wafers that have passed the evaluation outlined in item b) "Post-Incoming Inspection Evaluation" shall be forwarded to the backside grinding process.

a) Incoming inspection
   1) Part number
   2) Number of wafers
   3) WAT (Wafer Acceptance Test) measurement results
   4) Visual inspection results

b) Post-incoming inspection evaluation
1) WAT measurement at power supply voltage (V_{DD}) = 1.2V
2) Characteristics evaluation of the elements of resistors, capacitors and transistors
3) Function evaluation of high density SRAM
4) Function and performance evaluation of Multi-Core Processor

4.9.2 Screening

The following changes have been made to the screening test specified in Table B-1 of JAXA-QTS-

.

a) Stabilization bake
This test has been substituted with the pre-sealing stabilization bake, since it is a seam weld, no high temperatures are applied to the ICs during sealing and since eutectic solder ball attach is performed after sealing but at a temperature equivalent to the soldering temperature.

b) Radiographic inspection
1) Screening before qualification test for JAXA-developed parts
While JAXA-QTS-2010 specifies that radiographic inspection shall be performed from two views, the inspection have been changed to a total of three views: one upward view and two lateral views, taking into account the internal structure of the package.
2) Screening before quality conformance inspection
While JAXA-QTS-2010 specifies that radiographic inspection shall be performed from two views, screening results prior to the qualification test for JAXA-developed parts indicate that wire bending and foreign materials can be inspected from the one upward view alone. Therefore, radiographic inspection in the lateral views (X1 and Z1 directions) is omitted, and the inspection has perform the one upward view (Y2 direction) only.

c) Reverse bias burn-in test and interim (post reverse bias burn-in) electrical parameter test
Reverse bias burn-in test and interim (post reverse bias burn-in) electrical parameter test shall not be performed because the I/O terminals have protective diodes.

d) Final electrical parameter test
In order to prevent IC socket contact marks from adhering to the solder balls of the package, final electrical parameter tests (at room temperature, high temperature and low temperature) shall be performed prior to the eutectic solder ball attach.
For the electrical parameter test at room temperature, since the test conditions are identical to those for the post burn-in electrical parameter test (at room temperature), so the results from that test may be applied.

e) Seal
Eutectic solder balls shall be attached to the package between the final electrical parameter test and seal. Therefore, seal shall be performed after applying thermal conditions at the eutectic solder ball attach.

f) Electrical parameter test after eutectic solder ball attach
With the change in the sequence of final electrical parameter tests to precede seal,

an additional electrical parameter test at “room temperature only” shall be performed after seal.

4.9.3 Qualification Test for JAXA-developed Parts

4.9.3.1 Group A Test

The following changes have been made to the group A test specified in Table C-1 of JAXA-QTS-2010.

a) Subgroups 1 to 11
Since subgroups 1 to 11 tests are conducted in conjunction with the final electrical parameter screening test, the tests shall not be performed repeatedly.

4.9.3.2 Group B Test

The following changes have been made to the group B test specified in Table C-2 of JAXA-QTS-2010.

a) Subgroup 2
1) Resistance to solvents
Hand pressure measurement shall not be performed during brushing. For paragraph 3.1, “Optional procedure for the fourth group”, test method 2015 of MIL-STD-883, immersion shall be used, and chemical application by spray shall not be performed.
2) Verification of glassivation layer integrity
If there are any doubts with regard to the glassivation layer on the chip surface during the “Internal Visual and Mechanical” in Subgroup 2, verification of glassivation layer integrity shall be performed.

b) Subgroup 3
1) Radiographic inspection
Radiographic inspection shall be added to inspect void(s) at the joint area between the solder ball and the package electrode.
2) Solderability
Since the requirements for solderability of BGAs are not specified in JAXA-QTS-2010, the requirements for solderability shall be changed as follows.
The preconditioning condition shall be “155°C, Dry Bake for 4 hours,” based on the long-term storage environment (Section 4.8) as a desiccator, applying Table 3-3 "Condition Category E" of item h), paragraph 2.1 of J-STD-002E.
- Evaluation item: Wettability of solder balls.
- Test method: MIL-STD-883L TM2003.10 BGA

c) Subgroup 4
1) Lead integrity
While requirements for leads are specified in JAXA-QTS-2010, the requirements for BGA are not specified. For BGA, the lead integrity is substituted by the solder ball pull test in accordance with JESD22-B115A. Since acceptance criteria for solder ball pull test strength are not specified in

JESD22-B115A, the following values, which were defined based on the results of the development of small packages for space use, shall be specified as the requirement for acceptance criteria.
- Eutectic solder balls: Minimum 40.0MPa
- High temperature solder balls: Minimum 19.7MPa

2) Seal
Seal shall not be performed because the external leads do not penetrate through the package.

4.9.3.3 Group C Test

The following changes have been made to the group C tests specified in Table C-3 of JAXA-QTS-2010.

a) Subgroup 1

1) Steady state life test
When steady state life test conditions are set to +125°C for 2000 hours (double the standard 1000 hours), based on the LTPD concept, the sample size for the qualification test for JAXA-developed parts may be half of the LTPD5 requirement. If the sample size includes a decimal fraction, the sample size shall be rounded up.

b) Subgroup 2

1) Constant acceleration
Test conditions shall apply condition A (5000G), test method 2001 of MIL-STD-883L.

4.9.3.4 Group D Test

The following change has been made to the group D tests specified in Table C-4 of JAXA-QTS-2010.

a) Subgroup 4

1) Short circuit verification test
Since it was verified that wire short circuits did not occur based on evaluation results using an engineering model with the same wire bonding conditions as the product, this test shall be exempted.

4.9.3.5 Group E Test

For the same wafer lot, if Group E tests have been performed on one inspection lot, the remaining inspection lots may be exempted from all Group E tests.

4.9.4 Quality Conformance Inspection

For the inspections specified in Appendixes C and D of JAXA-QTS-2010, the changes specified in paragraph 4.9.3 shall also apply to this section. Other change items except those specified in paragraph 4.9.3 are as follows.

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4.9.4.1 Group B Test

a) Subgroup 1

1) Internal gas analysis
When quality conformance inspection data from the same wafer lot as the inspection lot ICs are not applicable, the sample size shall be determined according to Level I in the table of Appendix C of JAXA-QTS-2010. (For reference, JAXA-QTS-2010 specifies that Level II in the table of Appendix shall be applied.)

b) Subgroup 2

1) From Internal visual and mechanical inspection to Die shear test
When quality conformance inspection data from the same wafer lot as the inspection lot ICs are not applicable, the sample size shall be determined according to Level I in the table of Appendix C of JAXA-QTS-2010. (For reference, JAXA-QTS-2010 specifies that Level II in the table of Appendix shall be applied.)

c) Subgroup 4

Subgroup 4 tests shall be performed regardless the test status of the ICs in the inspection lot. The sample size shall be determined according to Level II in the table of Appendix C of JAXA-QTS-2010. (For reference, Appendix G of JAXA-QTS-2010 specifies that subgroup 4 tests may be exempted.)

5. PREPARATION FOR DELIVERY

Preparation for delivery shall be in accordance with paragraph G.5, Appendix G of JAXA-QTS-2010.

6. NOTES

Refer to the paragraph G.6, Appendix G of JAXA-QTS-2010.

6.1 Definition of Terms

Definitions of terms shall be applied in accordance with paragraph 6.1 of JAXA-QTS-2010 and the following.

a) Wafer lot
The definition of term specified in item k), paragraph 6.1 of JAXA QTS-2010 shall be applied.

b) Production lot
Same as the inspection lot.

c) Inspection lot
The inspection lot consists of a single wafer lot.

6.2 Application Datasheet

The manufacturer shall prepare the application data sheet in accordance with Appendix G of JAXA-QTS-2000 and register it with JAXA.

6.3 Notes for Purchasers

Notes for purchasers shall be applied in accordance with paragraph 6.3 of JAXA-QTS-2010 and the following.

a) The ICs shall be handled carefully to avoid damaging the solder balls.
During temporary storage while handling, place the package with the LID side facing down to protect the solder balls.

b) The cap on the package surface is connected to GND.

c) The solder ball attachment areas of IC package feature a dimple structure.
Therefore, since the solder balls are not able to be removed completely, it is impossible to perform rework on the solder balls.

d) Maximum number of reflow cycles shall be two.

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Table 6. Pin-Outs and Functions (1/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
A2	GND	-	-	-		As noted	VSS, VSSQ
A3	GND	-	-	-		As noted	VSS, VSSQ
A4	3.3V	-	-	-		As noted	VCCQ
A5	1.2V	-	-	-		As noted	VDD
A6	1.2V	-	-	-		As noted	VDD
A7	GND	-	-	-		As noted	VSS, VSSQ
A8	3.3V	-	-	-		As noted	VCCQ
A9	1.2V	-	-	-		As noted	VDD
A10	1.2V	-	-	-		As noted	VDD
A11	3.3V	-	-	-		As noted	VCCQ
A12	GND	-	-	-		As noted	VSS, VSSQ
A13	1.2V	-	-	-		As noted	VDD
A14	1.2V	-	-	-		As noted	VDD
A15	GND	-	-	-		As noted	VSS, VSSQ
A16	3.3V	-	-	-		As noted	VCCQ
A17	1.2V	-	-	-		As noted	VDD
A18	GND	-	-	-		As noted	VSS, VSSQ
A19	1.2V	-	-	-		As noted	VDD
A20	3.3V	-	-	-		As noted	VCCQ
A21	1.2V	-	-	-		As noted	VDD
A22	GND	-	-	-		As noted	VSS, VSSQ
A23	GND	-	-	-		As noted	VSS, VSSQ
B1	GND	-	-	-		As noted	VSS, VSSQ
B2	GND	-	-	-		As noted	VSS, VSSQ
B3	GND	-	-	-		As noted	VSS, VSSQ
B4	D40	External bus	CPU0	inout	24mA	Pulldown	
B5	D36	External bus	CPU0	inout	24mA	Pulldown	
B6	D32	External bus	CPU0	inout	24mA	Pulldown	
B7	D28	External bus	CPU0	inout	24mA	Pulldown	
B8	D22	External bus	CPU0	inout	24mA	Pulldown	
B9	D17	External bus	CPU0	inout	24mA	Pulldown	
B10	D13	External bus	CPU0	inout	24mA	Pulldown	
B11	D9	External bus	CPU0	inout	24mA	Pulldown	
B12	D5	External bus	CPU0	inout	24mA	Pulldown	
B13	A23	External bus	CPU0	out	24mA	Open	

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Table 6. Pin-Outs and Functions (2/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
B14	A17	External bus	CPU0	out	24mA	Open	
B15	A11	External bus	CPU0	out	24mA	Open	
B16	A5	External bus	CPU0	out	24mA	Open	
B17	MIL 1553B_TX_DATA_B_2	MIL-1553B	Common	out	8mA	Open	
B18	MIL 1553B_TX_DATA_BAR_B_2	MIL-1553B	Common	in	-	Pulldown	
B19	MIL 1553B_TX_DATA_BAR_A_2	MIL-1553B	Common	out	8mA	Open	
B20	MIL 1553B_SUBSYSTEM_2	MIL-1553B	Common	in	-	Pulldown	
B21	MIL 1553B_TX_DATA_B_1	MIL-1553B	Common	out	8mA	Open	
B22	GND	-	-	-		As noted	VSS, VSSQ
B23	GND	-	-	-		As noted	VSS, VSSQ
B24	GND	-	-	-		As noted	VSS, VSSQ
C1	GND	-	-	-		As noted	VSS, VSSQ
C2	GND	-	-	-		As noted	VSS, VSSQ
C3	GND	-	-	-		As noted	VSS, VSSQ
C4	D42	External bus	CPU0	inout	24mA	Pulldown	
C5	D38	External bus	CPU0	inout	24mA	Pulldown	
C6	D34	External bus	CPU0	inout	24mA	Pulldown	
C7	D30	External bus	CPU0	inout	24mA	Pulldown	
C8	D24	External bus	CPU0	inout	24mA	Pulldown	
C9	D19	External bus	CPU0	inout	24mA	Pulldown	
C10	D15	External bus	CPU0	inout	24mA	Pulldown	
C11	D11	External bus	CPU0	inout	24mA	Pulldown	
C12	D7	External bus	CPU0	inout	24mA	Pulldown	
C13	D1	External bus	CPU0	inout	24mA	Pulldown	
C14	A19	External bus	CPU0	out	24mA	Open	
C15	A13	External bus	CPU0	out	24mA	Open	
C16	A7	External bus	CPU0	out	24mA	Open	

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Table 6. Pin-Outs and Functions (3/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
C17	A1	External bus	CPU0	out	24mA	Open	
C18	MIL 1553B_RX_STROBE_B_2	MIL-1553B	Common	out	8mA	Open	
C19	MIL 1553B_TX_TX_INHIBIT_A_2	MIL-1553B	Common	out	8mA	Open	
C20	MIL 1553B_TX_DATA_BAR_A_2	MIL-1553B	Common	in	-	Pulldown	
C21	MIL 1553B_TX_DATA_BAR_B_1	MIL-1553B	Common	out	8mA	Open	
C22	GND	-	-	-		As noted	VSS, VSSQ
C23	GND	-	-	-		As noted	VSS, VSSQ
C24	GND	-	-	-		As noted	VSS, VSSQ
D1	1.2V	-	-	-		As noted	VDD
D2	D47	External bus	CPU0	inout	24mA	Pulldown	
D3	D45	External bus	CPU0	inout	24mA	Pulldown	
D4	D44	External bus	CPU0	inout	24mA	Pulldown	
D5	D41	External bus	CPU0	inout	24mA	Pulldown	
D6	D37	External bus	CPU0	inout	24mA	Pulldown	
D7	D31	External bus	CPU0	inout	24mA	Pulldown	
D8	D26	External bus	CPU0	inout	24mA	Pulldown	
D9	D20	External bus	CPU0	inout	24mA	Pulldown	
D10	GND	-	-	-		As noted	VSS, VSSQ
D11	3.3V	-	-	-		As noted	VCCQ
D12	D2	External bus	CPU0	inout	24mA	Pulldown	
D13	D3	External bus	CPU0	inout	24mA	Pulldown	
D14	GND	-	-	-		As noted	VSS, VSSQ
D15	3.3V	-	-	-		As noted	VCCQ
D16	A9	External bus	CPU0	out	24mA	Open	
D17	A2	External bus	CPU0	out	24mA	Open	
D18	GND	-	-	-		As noted	VSS, VCCQ
D19	3.3V	-	-	-		As noted	VCCQ

Table 6. Pin-Outs and Functions (4/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
D20	MIL 1553B_RX_DATA_A_2	MIL-1553B	Common	in	-	Pulldown	
D21	MIL 1553B_EX_SYNC_2	MIL-1553B	Common	in	-	Pulldown	
D22	MIL 1553B_RX_STROBE_B_1	MIL-1553B	Common	out	8mA	Open	
D23	MIL 1553B_TX_INHIBIT_B_1	MIL-1553B	Common	out	8mA	Open	
D24	3.3V	-	-	-		As noted	VCCQ
E1	3.3V	-	-	-		As noted	VCCQ
E2	ALE	External bus	CPU0	out	24mA	Open	
E3	D46	External bus	CPU0	inout	24mA	Pulldown	
E4	BC0	External bus	CPU0	out	24mA	Open	
E5	D43	External bus	CPU0	inout	24mA	Pulldown	
E6	D39	External bus	CPU0	inout	24mA	Pulldown	
E7	D33	External bus	CPU0	inout	24mA	Pulldown	
E8	D27	External bus	CPU0	inout	24mA	Pulldown	
E9	D21	External bus	CPU0	inout	24mA	Pulldown	
E10	D16	External bus	CPU0	inout	24mA	Pulldown	
E11	D8	External bus	CPU0	inout	24mA	Pulldown	
E12	D4	External bus	CPU0	inout	24mA	Pulldown	
E13	A22	External bus	CPU0	out	24mA	Open	
E14	A21	External bus	CPU0	out	24mA	Open	
E15	A15	External bus	CPU0	out	24mA	Open	
E16	A8	External bus	CPU0	out	24mA	Open	
E17	A3	External bus	CPU0	out	24mA	Open	
E18	MIL 1553B_TX_INHIBIT_B_2	MIL-1553B	Common	out	8mA	Open	
E19	MIL 1553B_RX_STROBE_A_2	MIL-1553B	Common	out	8mA	Open	
E20	MIL 1553B_TX_DATA_A_2	MIL-1553B	Common	out	8mA	Open	

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Table 6. Pin-Outs and Functions (5/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
E21	MIL 1553B_RX_DATA__BAR_B_1	MIL-1553B	Common	in	-	Pulldown	
E22	MIL 1553B_TX_INHIBIT_A_1	MIL-1553B	Common	out	8mA	Open	
E23	MIL 1553B_RX_DATA_B_1	MIL-1553B	Common	in	-	Pulldown	
E24	1.2V	-	-	-		As noted	VDD
F1	1.2V	-	-	-		As noted	VDD
F2	BC1	External bus	CPU0	out	24mA	Open	
F3	BC3	External bus	CPU0	out	24mA	Open	
F4	3.3V	-	-	-		As noted	VCCQ
F5	BC2	External bus	CPU0	out	24mA	Open	
F6	CAS#	External bus	CPU0	out	24mA	Open	
F7	D35	External bus	CPU0	inout	24mA	Pulldown	
F8	GND	-	-	-		As noted	VSS,VSSQ
F9	3.3V	-	-	-		As noted	VCCQ
F10	D14	External bus	CPU0	inout	24mA	Pulldown	
F11	D10	External bus	CPU0	inout	24mA	Pulldown	
F12	GND	-	-	-		As noted	VSS,VSSQ
F13	3.3V	-	-	-		As noted	VCCQ
F14	A18	External bus	CPU0	out	24mA	Open	
F15	A14	External bus	CPU0	out	24mA	Open	
F16	GND	-	-	-			VSS,VSSQ
F17	3.3V	-	-	-			VCCQ
F18	MIL 1553B_TX_DATA_BAR_B_2	MIL-1553B	Common	out	8mA	Open	
F19	MIL 1553B_RX_DATA_B_2	MIL-1553B	Common	in	-	Pulldown	
F20	MIL 1553B_TX_DATA_BAR_A_1	MIL-1553B	Common	out	8mA	Open	

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Table 6. Pin-Outs and Functions (6/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
F21	MIL 1553B_RX_DATA__BAR_A_1	MIL-1553B	Common	in	-	Pulldown	
F22	MIL 1553B_RX_STROBE_A_1	MIL-1553B	Common	out	8mA	Open	
F23	MIL 1553B_TX_DATA_A_1	MIL-1553B	Common	out	8mA	Open	
F24	1.2V	-	-	-		As noted	VDD
G1	GND	-	-	-		As noted	VSS,VSSQ
G2	CKE	External bus	CPU0	out	24mA	Open	
G3	CS2#	External bus	CPU0	out	24mA	Open	
G4	GND	-	-	-		As noted	VSS,VSSQ
G5	CS4#	External bus	CPU0	out	24mA	Open	
G6	CS1#	External bus	CPU0	out	24mA	Open	
G7	CS3#	External bus	CPU0	out	24mA	Open	
G8	D29	External bus	CPU0	inout	24mA	Pulldown	
G9	D23	External bus	CPU0	inout	24mA	Pulldown	
G10	D18	External bus	CPU0	inout	24mA	Pulldown	
G11	D12	External bus	CPU0	inout	24mA	Pulldown	
G12	D6	External bus	CPU0	inout	24mA	Pulldown	
G13	D0	External bus	CPU0	inout	24mA	Pulldown	
G14	A20	External bus	CPU0	out	24mA	Open	
G15	A16	External bus	CPU0	out	24mA	Open	
G16	A10	External bus	CPU0	out	24mA	Open	
G17	A4	External bus	CPU0	out	24mA	Open	
G18	A0	External bus	CPU0	out	24mA	Open	
G19	MIL 1553B_SUBSYSYTEM_1	MIL-1553B	Common	in	-	Pulldown	
G20	GPIO _2_11	SpaceWire	Common	in	-	Pulldown	channels 4 to 6 (common)
G21	MIL 1553B_RX_DATA_A_1	MIL-1553B	Common	in	-	Pulldown	
G22	MIL 1553B_EX_SYNC_1	MIL-1553B	Common	in	-	Pulldown	

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Table 6. Pin-Outs and Functions (7/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
G23	GPIO _2_10	SpaceWire	Common	in	-	Pulldown	channels 4 to 6 (common)
G24	GND	-	-	-		As noted	VSS,VSSQ
H1	1.2V	-	-	-		As noted	VDD
H2	DQM0	External bus	CPU0	out	24mA	Open	
H3	DQM2	External bus	CPU0	out	24mA	Open	
H4	CS5#	External bus	CPU0	out	24mA	Open	
H5	CS6#	External bus	CPU0	out	24mA	Open	
H6	3.3V	-	-	-			VCCQ
H7	CS7#	External bus	CPU0	out	24mA	Open	
H8	DQM1	External bus	CPU0	out	24mA	Open	
H9	D25	External bus	CPU0	inout	24mA	Pulldown	
H10	GND	-	-	-		As noted	VSS,VSSQ, VBN
H11	1.2V	-	-	-		As noted	VDD
H12	1.2V	-	-	-		As noted	VDD
H13	1.2V	-	-	-		As noted	VDD
H14	1.2V	-	-	-		As noted	VDD, VBP
H15	1.2V	-	-	-		As noted	VDD
H16	A12	External bus	CPU0	out	24mA	Open	
H17	A6	External bus	CPU0	out	24mA	Open	
H18	GPIO _2_01	SpaceWire	Common	in	-	Pulldown	channels 4 to 6 (common)
H19	3.3V	-	-	-		As noted	VCCQ
H20	D_OUT(5)	SpaceWire	Common	out	8mA	Open	
H21	GPIO _2_00	SpaceWire	Common	in	-	Pulldown	channels 4 to 6 (common)
H22	D_IN(5)	SpaceWire	Common	in	-	Pulldown	
H23	S_IN(5)	SpaceWire	Common	in	-	Pulldown	
H24	3.3V	-	-	-		As noted	VCCQ

Table 6. Pin-Outs and Functions (8/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
J1	3.3V	-	-	-		As noted	VCCQ
J2	DQM5	External bus	CPU0	out	24mA	Open	
J3	RD#	External bus	CPU0	out	24mA	Open	
J4	DQM3	External bus	CPU0	out	24mA	Open	
J5	DQM4	External bus	CPU0	out	24mA	Open	
J6	GND	-	-	-		As noted	VSS,VSSQ
J7	RAS#	External bus	CPU0	out	24mA	Open	
J8	1.2V	-	-	-		As noted	VDD
J9	GND	-	-	-		As noted	VSS,VSSQ
J10	1.2V	-	-	-		As noted	VDD
J11	GND	-	-	-		As noted	VSS,VSSQ
J12	1.2V	-	-	-		As noted	VDD
J13	GND	-	-	-		As noted	VSS,VSSQ
J14	1.2V	-	-	-		As noted	VDD
J15	GND	-	-	-		As noted	VSS,VSSQ
J16	1.2V	-	-	-		As noted	VDD
J17	GND	-	-	-		As noted	VSS,VSSQ
J18	S_OUT(5)	SpaceWire	Common	out	8mA	Open	
J19	GND	-	-	-		As noted	VSS,VSSQ
J20	D_OUT(4)	SpaceWire	Common	out	8mA	Open	
J21	D_IN(4)	SpaceWire	Common	in	-	Pulldown	
J22	S_IN(4)	SpaceWire	Common	in	-	Pulldown	
J23	D_IN(3)	SpaceWire	Common	in	-	Pulldown	
J24	1.2V	-	-	-		As noted	VDD
K1	GND	-	-	-		As noted	VSS,VSSQ
K2	SDCS#	External bus	CPU0	out	24mA	Open	
K3	3.3V	-	-	-		As noted	VCCQ
K4	SDCS2#	External bus	CPU0	out	24mA	Open	
K5	SDCS1#	External bus	CPU0	out	24mA	Open	
K6	SDCS3#	External bus	CPU0	out	24mA	Open	
K7	WE#	External bus	CPU0	out	24mA	Open	
K8	WR1#	External bus	CPU0	out	24mA	Open	
K9	1.2V	-	-	-		As noted	VDD
K10	GND	-	-	-		As noted	VSS,VSSQ

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Table 6. Pin-Outs and Functions (9/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
K11	1.2V	-	-	-		As noted	VDD
K12	GND	-	-	-		As noted	VSS,VSSQ
K13	1.2V	-	-	-		As noted	VDD
K14	GND	-	-	-		As noted	VSS,VSSQ
K15	1.2V	-	-	-		As noted	VDD
K16	GND	-	-	-		As noted	VSS,VSSQ
K17	1.2V	-	-	-		As noted	VDD
K18	S_OUT(4)	SpaceWire	Common	out	8mA	Open	
K19	D_OUT(3)	SpaceWire	Common	out	8mA	Open	
K20	S_OUT(3)	SpaceWire	Common	out	8mA	Open	
K21	S_IN(3)	SpaceWire	Common	in	-	Pulldown	
K22	3.3V	-	-	-		As noted	VCCQ
K23	GPIO _1_10	SpaceWire	Common	in	-	Pulldown	channels 1 to 3 (common)
K24	1.2V	-	-	-		As noted	VDD
L1	1.2V	-	-	-		As noted	VDD
L2	SDCLK	External bus	CPU0	out	24mA	Open	
L3	GND	-	-	-		As noted	VSS,VSSQ
L4	WAIT#	External bus	CPU0	in	-	Pulldown	
L5	WR3#	External bus	CPU0	out	24mA	Open	
L6	CS_BSW[1]	External bus	CPU0	in	-	Pulldown	Initial bus width setting for external bus area 1
L7	PLL_SEL[0]	CPG	Common	in	-	Pulldown	
L8	1.2V	-	-	-	-	As noted	VDD
L9	GND	-	-	-		As noted	VSS,VSSQ
L10	1.2V	-	-	-		As noted	VDD
L11	GND	-	-	-		As noted	VSS,VSSQ
L12	1.2V	-	-	-		As noted	VDD
L13	GND	-	-	-		As noted	VSS,VSSQ
L14	1.2V	-	-	-		As noted	VDD
L15	GND	-	-	-		As noted	VSS,VSSQ
L16	1.2V	-	-	-		As noted	VDD
L17	GND	-	-	-		As noted	VSS,VSSQ,VBN

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Table 6. Pin-Outs and Functions (10/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
L18	GPIO _1_11	SpaceWire	Common	in	-	Pulldown	channels 1 to 3 (common)
L19	GPIO _1_01	SpaceWire	Common	in	-	Pulldown	channels 1 to 3 (common)
L20	D_OUT(2)	SpaceWire	Common	out	8mA	Open	
L21	GPIO_1_00	SpaceWire	Common	in	-	Pulldown	channels 1 to 3 (common)
L22	GND	-	-	-		As noted	VSS,VSSQ
L23	D_IN(2)	SpaceWire	Common	in	-	Pulldown	
L24	3.3V	-	-	-		As noted	VCCQ
M1	1.2V	-	-	-		As noted	VDD
M2	WR0#	External bus	CPU0	out	24mA	Open	
M3	WR2#	External bus	CPU0	out	24mA	Open	
M4	CS_BSW[0]	External bus	CPU0	in	-	Pulldown	Initial bus width setting for external bus area 1
M5	PLL_SEL[2]	CPG	Common	in	-	Pulldown	
M6	3.3V	-	-	-	-	As noted	VCCQ
M7	PLL_SEL[4]	CPG	Common	in	-	Pulldown	
M8	GND	-	-	-	-	As noted	VSS,VSSQ
M9	1.2V	-	-	-	-	As noted	VDD
M10	GND	-	-	-	-	As noted	VSS,VSSQ
M11	1.2V	-	-	-	-	As noted	VDD
M12	GND	-	-	-	-	As noted	VSS,VSSQ
M13	1.2V	-	-	-	-	As noted	VDD
M14	GND	-	-	-	-	As noted	VSS,VSSQ
M15	1.2V	-	-	-	-	As noted	VDD
M16	GND	-	-	-	-	As noted	VSS,VSSQ
M17	1.2V	-	-	-	-	As noted	VDD
M18	S_OUT(2)	SpaceWire	Common	out	8mA	Open	
M19	3.3V	-	-	-	-	As noted	VCCQ
M20	D_OUT(1)	SpaceWire	Common	out	8mA	Open	
M21	D_IN(1)	SpaceWire	Common	in	-	Pulldown	
M22	S_IN(2)	SpaceWire	Common	in	-	Pulldown	

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Table 6. Pin-Outs and Functions (11/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
M23	S_IN(0)	SpaceWire	Common	in	-	Pulldown	
M24	GND	-	-	-	-	As noted	VSS,VSSQ
N1	GND	-	-	-	-	As noted	VSS,VSSQ
N2	EXT_CLK	CPG	Common	in	-	Pulldown	
N3	PLL_SEL[1]	CPG	Common	in	-	Pulldown	
N4	PLL_SEL[3]	CPG	Common	in	-	Pulldown	
N5	JTAG_CLK	CPG	Common	in	-	Pulldown	TCK
N6	GND	-	-	-	-	As noted	VSS,VSSQ
N7	IRQ1	External interrupt	Common	in	-	Pulldown	
N8	1.2V	-	-	-	-	As noted	VDD
N9	GND	-	-	-	-	As noted	VSS,VSSQ
N10	1.2V	-	-	-	-	As noted	VDD
N11	GND	-	-	-	-	As noted	VSS,VSSQ
N12	1.2V	-	-	-	-	As noted	VDD
N13	GND	-	-	-	-	As noted	VSS,VSSQ
N14	1.2V	-	-	-	-	As noted	VDD
N15	GND	-	-	-	-	As noted	VSS,VSSQ
N16	1.2V	-	-	-	-	As noted	VDD
N17	1.2V	-	-	-		As noted	VDD
N18	S_OUT(1)	SpaceWire	Common	out	8mA	Open	
N19	GND	-	-	-	-	As noted	VSS,VSSQ
N20	D_OUT(0)	SpaceWire	Common	out	8mA	Open	
N21	S_IN(1)	SpaceWire	Common	In	-	Pulldown	
N22	D_IN(0)	SpaceWire	Common	In	-	Pulldown	
N23	clk_gptp_extern_1	Ethernet	Common	In	-	Pulldown	gPTP function
N24	1.2V	-	-	-	-	As noted	VDD
P1	3.3V	-	-	-	-	As noted	VCCQ
P2	NMI	External interrupt	CPU0	In	-	Pulldown	
P3	GND	-	-	-	-	As noted	VSS,VSSQ
P4	IRQ2	External interrupt	Common	In	-	Pulldown	
P5	MD[0]	System	Common	In	-	Pulldown	

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Table 6. Pin-Outs and Functions (12/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
P6	IRQ3	External interrupt	Common	In	-	Pulldown	
P7	MD[1]	System	Common	In	-	Pulldown	
P8	1.2V	-	-	-		As noted	VDD
P9	1.2V	-	-	-	-	As noted	VDD
P10	GND	-	-	-	-	As noted	VSS,VSSQ
P11	1.2V	-	-	-	-	As noted	VDD
P12	GND	-	-	-	-	As noted	VSS,VSSQ
P13	1.2V	-	-	-	-	As noted	VDD
P14	GND	-	-	-	-	As noted	VSS,VSSQ
P15	1.2V	-	-	-	-	As noted	VDD
P16	GND	-	-	-	-	As noted	VSS,VSSQ
P17	1.2V	-	-	-	-	As noted	VDD
P18	S_OUT(0)	SpaceWire	Common	out	8mA	Open	
P19	avb_pt_capture_1	Ethernet	Common	in	-	Pulldown	gPTP function
P20	clk_miitx_clk_1	Ethernet	Common	in	-	Pulldown	
P21	3.3V	-	-	-	-	As noted	VCCQ
P22	clk_miirx_clk_1	Ethernet	Common	in	-	Pulldown	
P23	avd_miirx_err_1	Ethernet	Common	in	-	Pulldown	
P24	1.2V	-	-	-	-	As noted	VDD
R1	1.2V	-	-	-	-	As noted	VDD
R2	USER_CLK	CPG	Common	out	-	Open	
R3	3.3V	-	-	-	-	As noted	VCCQ
R4	RES#	System	Common	in	-	Pulldown	
R5	TRST#	_JTAG for CPU	Common	in	-	Pulldown	
R6	TDI	_JTAG for CPU	Common	in	-	Pulldown	
R7	TDO	_JTAG for CPU	Common	out	8mA	Open	
R8	1.2V	-	-	-	-	As noted	VDD
R9	GND	-	-	-	-	As noted	VSS,VSSQ
R10	1.2V	-	-	-	-	As noted	VDD

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Table 6. Pin-Outs and Functions (13/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
R11	GND	-	-	-	-	As noted	VSS,VSSQ
R12	1.2V	-	-	-	-	As noted	VDD
R13	GND	-	-	-	-	As noted	VSS,VSSQ
R14	1.2V	-	-	-	-	As noted	VDD
R15	GND	-	-	-	-	As noted	VSS,VSSQ
R16	1.2V	-	-	-	-	As noted	VDD
R17	1.2V	-	-	-		As noted	VDD, VBP
R18	avd_miirx_rxd0_1	Ethernet	Common	in	-	Pulldown	
R19	avd_miitx_crs_1	Ethernet	Common	in	-	Pulldown	
R20	fet_miitx_err_1	Ethernet	Common	out	8mA	Open	
R21	GND	-	-	-	-	As noted	VSS,VSSQ
R22	avd_miirx_dv_1	Ethernet	Common	in	-	Pulldown	
R23	avd_miitx_col_1	Ethernet	Common	in	-	Pulldown	
R24	GND	-	-	-	-	As noted	VSS,VSSQ
T1	1.2V	-	-	-	-	As noted	VDD
T2	EMLE	_JTAG for CPU	Common	in	-	Pulldown	
T3	TMS	_JTAG for CPU	Common	in	-	Pulldown	
T4	Reserved	-	-	-	-	Pulldown	
T5	Reserved	-	-	-	-	Pulldown	
T6	3.3V	-	-	-	-	As noted	VCCQ
T7	Reserved	-	-	-	-	Pulldown	
T8	Reserved	-	-	-	-	Pulldown	
T9	1.2V	-	-	-	-	As noted	VDD
T10	GND	-	-	-	-	As noted	VSS,VSSQ
T11	1.2V	-	-	-	-	As noted	VDD
T12	GND	-	-	-	-	As noted	VSS,VSSQ
T13	1.2V	-	-	-	-	As noted	VDD
T14	GND	-	-	-	-	As noted	VSS,VSSQ
T15	1.2V	-	-	-	-	As noted	VDD
T16	GND	-	-	-	-	As noted	VSS,VSSQ

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Table 6. Pin-Outs and Functions (14/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
T17	fet_miitx_txd2_1	Ethernet	Common	out	8mA	Open	
T18	avd_miirx_rxd1_1	Ethernet	Common	in	-	Pulldown	
T19	3.3V	-	-	-	-	As noted	VCCQ
T20	avd_miirx_rxd2_1	Ethernet	Common	in	-	Pulldown	
T21	clk_miirx_clk_0	Ethernet	Common	in	-	Pulldown	
T22	fet_miitx_txd0_1	Ethernet	Common	out	8mA	Open	
T23	avd_miirx_rxd3_1	Ethernet	Common	in	-	Pulldown	
T24	3.3V	-	-	-	-	As noted	VCCQ
U1	3.3V	-	-	-	-	As noted	VCCQ
U2	Reserved	-	-	-	-	Pulldown	
U3	Reserved	-	-	-	-	Pulldown	
U4	Reserved	-	-	-	-	Pulldown	
U5	Reserved	-	-	-	-	Pulldown	
U6	GND	-	-	-	-	As noted	VSS,VSSQ
U7	Reserved	-	-	-	-	Pulldown	
U8	TIC0_CPU0_2/PORT_K(4)	CMTW	CPU0	inout	8mA	Pulldown	
U9	TOC0_CPU1_1/PORT_L(1)	CMTW	CPU1	inout	8mA	Pulldown	
U10	1.2V	-	-	-	-	As noted	VDD
U11	GND	-	-	-	-	As noted	VSS,VSSQ
U12	1.2V	-	-	-	-	As noted	VDD
U13	1.2V	-	-	-		As noted	VDD
U14	1.2V	-	-	-	-	As noted	VDD
U15	GND	-	-	-	-	As noted	VSS,VSSQ
U16	1.2V	-	-	-	-	As noted	VDD
U17	fet_miitx_txd1_1	Ethernet	Common	out	8mA	Open	
U18	fec_miimg_crxmdc_1	Ethernet	Common	out	8mA	Open	
U19	GND	-	-	-	-	As noted	VSS,VSSQ

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Table 6. Pin-Outs and Functions (15/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
U20	fet_miitx_txd3_1	Ethernet	Common	out	8mA	Open	
U21	fet_miitx_en_1	Ethernet	Common	out	8mA	Open	
U22	3.3V	-	-	-	-	As noted	VCCQ
U23	clk_gptp_extern_0	Ethernet	Common	in	-	Pulldown	gPTP function
U24	1.2V	-	-	-	-	As noted	VDD
V1	GND	-	-	-	-	As noted	VSS,VSSQ
V2	Reserved	-	-	-	-	Pulldown	
V3	Reserved	-	-	-	-	Pulldown	
V4	Reserved	-	-	-	-	Pulldown	
V5	Reserved	-	-	-	-	Pulldown	
V6	Reserved	-	-	-	-	Pulldown	
V7	TMRI0_CPU1/PORT_J(2)	TMR	CPU1	inout	8mA	Pulldown	Shared pins with TMRI1_CPU1
V8	TIC1_CPU0_1/PORT_K(2)	CMTW	CPU0	inout	8mA	Pulldown	
V9	TOC1_CPU0_2/PORT_K(7)	CMTW	CPU0	inout	8mA	Pulldown	
V10	TOC1_CPU1_2/PORT_L(7)	CMTW	CPU1	inout	8mA	Pulldown	
V11	SS1_0#/CTS1_0#/RTS1_0#/PORT_H(1)	SCI	CPU1	inout	8mA	Pulldown	
V12	TXD0_CPU1/PORT_H(3)	SCI	CPU1	inout	8mA	Pulldown	TXD0_1/SDA0_1/MOSI0_1
V13	TXD1_CPU1/PORT_H(7)	SCIF	CPU1	inout	8mA	Pulldown	TXD1_1/SDA1_1/MOSI1_1
V14	RSPCK/PORT_C(5)	SPI	CPU0	inout	8mA	Pulldown	
V15	SSL1/PORT_D(2)	SPI	CPU1	inout	8mA	Pulldown	
V16	GTIOC2A/PORT_A(5)	GPT	CPU0	inout	8mA	Pulldown	
V17	GTIOC3A/PORT_A(7)	GPT	CPU0	inout	8mA	Pulldown	

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Table 6. Pin-Outs and Functions (16/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
V18	fec_miimg_cxrmdo/mdi_1	Ethernet	Common	inout	8mA	Pulldown	
V19	avd_miirx_err_0	Ethernet	Common	in	-	Pulldown	
V20	fet_miitx_err_0	Ethernet	Common	out	8mA	Open	
V21	avb_pt_capture_0	Ethernet	Common	in	-	Pulldown	gPTP function
V22	GND	-	-	-	-	As noted	VSS,VSSQ
V23	avd_miirx_rxd0_0	Ethernet	Common	in	-	Pulldown	
V24	GND	-	-	-	-	As noted	VSS,VSSQ
W1	1.2V	-	-	-	-	As noted	VDD
W2	Reserved	-	-	-	-	Pulldown	
W3	Reserved	-	-	-	-	Pulldown	
W4	Reserved	-	-	-	-	Pulldown	
W5	Reserved	-	-	-	-	Pulldown	
W6	TMRI0_CPU0/PORT_I(2)	TMR	CPU0	inout	8mA	Pulldown	Shared pins with TMRI1_CPU0
W7	TMO0_CPU1/PORT_J(0)	TMR	CPU1	inout	8mA	Pulldown	
W8	3.3V	-	-	-	-	As noted	VCCQ
W9	GND	-	-	-	-	As noted	VSS,VSSQ
W10	TOC0_CPU1_2/PORT_L(5)	CMTW	CPU1	inout	8mA	Pulldown	
W11	TXD0_CPU0/PORT_G(3)	SCI	CPU0	inout	8mA	Pulldown	TXD0_0/SDA0_0/MOSI0_0
W12	3.3V	-	-	-	-	As noted	VCCQ
W13	GND	-	-	-	-	As noted	VSS,VSSQ
W14	MOSI/PORT_C(3)	SPI	CPU0	inout	8mA	Pulldown	
W15	SSL3/PORT_D(0)	SPI	CPU1	inout	8mA	Pulldown	
W16	3.3V	-	-	-	-	As noted	VCCQ
W17	GND	-	-	-	-	As noted	VSS,VSSQ
W18	GTIOC0B/PORT_B(2)	GPT	CPU1	inout	8mA	Pulldown	

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Table 6. Pin-Outs and Functions (17/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
W19	avd_miirx_dv_0	Ethernet	Common	in	-	Pulldown	
W20	avd_miitx_col_0	Ethernet	Common	in	-	Pulldown	
W21	clk_miitx_clk_0	Ethernet	Common	in	-	Pulldown	
W22	avd_miitx_crs_0	Ethernet	Common	in	-	Pulldown	
W23	fet_miitx_txd2_0	Ethernet	Common	out	8mA	Open	
W24	1.2V	-	-	-	-	As noted	VDD
Y1	1.2V	-	-	-	-	As noted	VDD
Y2	Reserved	-	-	-	-	Pulldown	
Y3	Reserved	-	-	-	-	Pulldown	
Y4	Reserved	-	-	-	-	Pulldown	
Y5	SCL1（FM+)/PORT_F(0)	I2C	CPU1	inout	8mA	Pulldown	For the I2C function, output is LOW/High-Z.
Y6	TMO0_CPU0/PORT_I(0)	TMR	CPU0	inout	8mA	Pulldown	
Y7	TMO1_CPU1/PORT_J(3)	TMR	CPU1	inout	8mA	Pulldown	
Y8	TOC0_CPU0_1/PORT_K(1)	CMTW	CPU0	inout	8mA	Pulldown	
Y9	TOC0_CPU0_2/PORT_K(5)	CMTW	CPU0	inout	8mA	Pulldown	
Y10	TOC1_CPU1_1/PORT_L(3)	CMTW	CPU1	inout	8mA	Pulldown	
Y11	SS0_0#/CTS0_0#/RTS0_0#/PORT_G(1)	SCI	CPU0	inout	8mA	Pulldown	
Y12	SS0_1#/CTS0_1#/RTS0_1#/PORT_G(5)	SCIF	CPU0	inout	8mA	Pulldown	
Y13	SS1_1#/CTS1_1#/RTS1_1#/PORT_H(5)	SCIF	CPU1	inout	8mA	Pulldown	

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Table 6. Pin-Outs and Functions (18/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
Y14	SSL2/PORT_C(1)	SPI	CPU0	inout	8mA	Pulldown	
Y15	SSL2/PORT_D(1)	SPI	CPU1	inout	8mA	Pulldown	
Y16	SSL0/PORT_D(6)	SPI	CPU1	inout	8mA	Pulldown	
Y17	GTIOC1A/PORT_A(3)	GPT	CPU0	inout	8mA	Pulldown	
Y18	GTETRG/PORT_B(0)	GPT	CPU1	inout	8mA	Pulldown	channels 1 to 4 (common)
Y19	GTIOC2B/PORT_B(6)	GPT	CPU1	inout	8mA	Pulldown	
Y20	fet_miitx_en_0	Ethernet	Common	out	8mA	Open	
Y21	fet_miitx_txd0_0	Ethernet	Common	out	8mA	Open	
Y22	avd_miirx_rxd1_0	Ethernet	Common	in	-	Pulldown	
Y23	avd_miirx_rxd2_0	Ethernet	Common	in	-	Pulldown	
Y24	3.3V	-	-	-	-	As noted	VCCQ
AA1	3.3V	-	-	-	-	As noted	VCCQ
AA2	Reserved	-	-	-	-	Pulldown	
AA3	Reserved	-	-	-	-	Pulldown	
AA4	CTX1	CAN	CPU1	out	8mA	Open	
AA5	SCL0（FM+)/PORT_E(0)	I2C	CPU0	inout	8mA	Pulldown	For the I2C function, output is LOW/High-Z.
AA6	3.3V	-	-	-	-	As noted	VCCQ
AA7	GND	-	-	-	-	As noted	VSS,VSSQ
AA8	TIC1_CPU0_2/PORT_K(6)	CMTW	CPU0	inout	8mA	Pulldown	
AA9	TIC0_CPU1_2/PORT_L(4)	CMTW	CPU1	inout	8mA	Pulldown	
AA10	3.3V	-	-	-	-	As noted	VCCQ
AA11	GND	-	-	-	-	As noted	VSS,VSSQ
AA12	RXD1_CPU0/PORT_G(6)	SCIF	CPU0	inout	8mA	Pulldown	RXD1_0/SCL1_0/MISO1_0
AA13	TXD1_CPU0/PORT_G(7)	SCIF	CPU0	inout	8mA	Pulldown	TXD1_0/SDA1_0/MOSI1_0

Table 6. Pin-Outs and Functions (19/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
AA14	3.3V	-	-	-	-	As noted	VCCQ
AA15	GND	-	-	-	-	As noted	VSS,VSSQ
AA16	MISO/PORT_D(4)	SPI	CPU1	inout	8mA	Pulldown	
AA17	GTIOC0A/PORT_A(1)	GPT	CPU0	inout	8mA	Pulldown	
AA18	GTIOC3B/PORT_A(8)	GPT	CPU0	inout	8mA	Pulldown	
AA19	GTIOC1B/PORT_B(4)	GPT	CPU1	inout	8mA	Pulldown	
AA20	fec_miimg_crxmdc_0	Ethernet	Common	out	8mA	Open	
AA21	avd_miirx_rxd3_0	Ethernet	Common	in	-	Pulldown	
AA22	fet_miitx_txd1_0	Ethernet	Common	out	8mA	Open	
AA23	fet_miitx_txd3_0	Ethernet	Common	out	8mA	Open	
AA24	1.2V	-	-	-	-	As noted	VDD
AB1	GND	-	-	-	-	As noted	VSS,VSSQ
AB2	GND	-	-	-	-	As noted	VSS,VSSQ
AB3	GND	-	-	-	-	As noted	VSS,VSSQ
AB4	CTX0	CAN	CPU0	out	8mA	Open	
AB5	SDA0（FM+)/PORT_E(1)	I2C	CPU0	inout	8mA	Pulldown	For the I2C function, output is LOW/High-Z.
AB6	TMCI0_CPU0/PORT_I(1)	TMR	CPU0	inout	8mA	Pulldown	Shared pins with TMCI1_CPU0
AB7	TMCI0_CPU1/PORT_J(1)	TMR	CPU1	inout	8mA	Pulldown	Shared pins with TMCI1_CPU1
AB8	TOC1_CPU0_1/PORT_K(3)	CMTW	CPU0	inout	8mA	Pulldown	
AB9	TIC1_CPU1_1/PORT_L(2)	CMTW	CPU1	inout	8mA	Pulldown	
AB10	SCK0_CPU0/PORT_G(0)	SCI	CPU0	inout	8mA	Pulldown	
AB11	SCK0_CPU1/PORT_H(0)	SCI	CPU1	inout	8mA	Pulldown	

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Table 6. Pin-Outs and Functions (20/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
AB12	SCK1_CPU0/ PORT_G(4)	SCIF	CPU0	inout	8mA	Pulldown	
AB13	RXD1_CPU1/ PORT_H(6)	SCIF	CPU1	inout	8mA	Pulldown	RXD1_1/SCL 1_1/MISO1_1
AB14	SSL1/PORT_ C(2)	SPI	CPU0	inout	8mA	Pulldown	
AB15	SSL0/PORT_ C(6)	SPI	CPU0	inout	8mA	Pulldown	
AB16	RSPCK/POR T_D(5)	SPI	CPU1	inout	8mA	Pulldown	
AB17	GTIOC0B/PO RT_A(2)	GPT	CPU0	inout	8mA	Pulldown	
AB18	GTIOC2B/PO RT_A(6)	GPT	CPU0	inout	8mA	Pulldown	
AB19	GTIOC1A/PO RT_B(3)	GPT	CPU1	inout	8mA	Pulldown	
AB20	GTIOC3B/PO RT_B(8)	GPT	CPU1	inout	8mA	Pulldown	
AB21	fec_miimg_cx rmdo/mdi_0	Ethernet	Common	inout	8mA	Pulldown	
AB22	GND	-	-	-	-	As noted	VSS,VSSQ
AB23	GND	-	-	-	-	As noted	VSS,VSSQ
AB24	GND	-	-	-	-	As noted	VSS,VSSQ
AC1	GND	-	-	-	-	As noted	VSS,VSSQ
AC2	GND	-	-	-	-	As noted	VSS,VSSQ
AC3	GND	-	-	-	-	As noted	VSS,VSSQ
AC4	CRX0	CAN	CPU0	in	-	Pulldown	
AC5	CRX1	CAN	CPU1	in	-	Pulldown	
AC6	SDA1 （FM+)/POR T_F(1)	I2C	CPU1	inout	8mA	Pulldown	For the I2C function, output is LOW/High-Z.
AC7	TMO1_CPU0 /PORT_I(3)	TMR	CPU0	inout	8mA	Pulldown	
AC8	TIC0_CPU0_ 1/PORT_K(0)	CMTW	CPU0	inout	8mA	Pulldown	
AC9	TIC0_CPU1_ 1/PORT_L(0)	CMTW	CPU1	inout	8mA	Pulldown	
AC10	TIC1_CPU1_ 2/PORT_L(6)	CMTW	CPU1	inout	8mA	Pulldown	

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Table 6. Pin-Outs and Functions (21/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
AC11	RXD0_CPU0/ PORT_G(2)	SCI	CPU0	inout	8mA	Pulldown	RXD0_0/SCL 0_0/MISO0_0
AC12	RXD0_CPU1/ PORT_H(2)	SCI	CPU1	inout	8mA	Pulldown	RXD0_1/SCL 0_1/MISO0_1
AC13	SCK1_CPU1/ PORT_H(4)	SCIF	CPU1	inout	8mA	Pulldown	
AC14	SSL3/PORT_ C(0)	SPI	CPU0	inout	8mA	Pulldown	
AC15	MISO/PORT_ C(4)	SPI	CPU0	inout	8mA	Pulldown	
AC16	MOSI/PORT_ D(3)	SPI	CPU1	inout	8mA	Pulldown	
AC17	GTETRG/PO RT_A(0)	GPT	CPU0	inout	8mA	Pulldown	channels 1 to 4 (common)
AC18	GTIOC1B/PO RT_A(4)	GPT	CPU0	inout	8mA	Pulldown	
AC19	GTIOC0A/PO RT_B(1)	GPT	CPU1	inout	8mA	Pulldown	
AC20	GTIOC2A/PO RT_B(5)	GPT	CPU1	inout	8mA	Pulldown	
AC21	GTIOC3A/PO RT_B(7)	GPT	CPU1	inout	8mA	Pulldown	
AC22	GND	-	-	-	-	As noted	VSS,VSSQ
AC23	GND	-	-	-	-	As noted	VSS,VSSQ
AC24	GND	-	-	-	-	As noted	VSS,VSSQ
AD2	GND	-	-	-	-	As noted	VSS,VSSQ
AD3	GND	-	-	-	-	As noted	VSS,VSSQ
AD4	1.2V	-	-	-	-	As noted	VDD
AD5	3.3V	-	-	-	-	As noted	VCCQ
AD6	1.2V	-	-	-	-	As noted	VDD
AD7	GND	-	-	-	-	As noted	VSS,VSSQ
AD8	1.2V	-	-	-	-	As noted	VDD
AD9	3.3V	-	-	-	-	As noted	VCCQ
AD10	GND	-	-	-	-	As noted	VSS,VSSQ
AD11	1.2V	-	-	-	-	As noted	VDD
AD12	1.2V	-	-	-	-	As noted	VDD
AD13	GND	-	-	-	-	As noted	VSS,VSSQ
AD14	3.3V	-	-	-	-	As noted	VCCQ

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Table 6. Pin-Outs and Functions (22/22)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Group E, Subgroup 1, pin treatment	Remarks
AD15	1.2V	-	-	-	-	As noted	VDD
AD16	1.2V	-	-	-	-	As noted	VDD
AD17	3.3V	-	-	-	-	As noted	VCCQ
AD18	GND	-	-	-	-	As noted	VSS,VSSQ
AD19	1.2V	-	-	-	-	As noted	VDD
AD20	1.2V	-	-	-	-	As noted	VDD
AD21	3.3V	-	-	-	-	As noted	VCCQ
AD22	GND	-	-	-	-	As noted	VSS,VSSQ
AD23	GND	-	-	-	-	As noted	VSS,VSSQ

Table 7. Electrical Characteristics (DC Characteristics)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C)

Item		Symbol	Min.	Max.	Unit	Condition
Input voltage		V_{IL}	-	0.2 x V_{CCQ}	V	-
		V_{IH}	0.7 x V_{CCQ}	-	V	-
Input leakage current		I_{IL}	-0.6	0.6	µA	-
		I_{IH}	-0.6	0.6	µA	-
Low level output voltage	8mA buffer	$V_{OL(8mA)}$	-	0.4	V	I_{OL}=8mA
	24mA buffer	$V_{OL(24mA)}$	-	0.4	V	I_{OL}=24mA
	8mA buffer	$V_{OH(8MA)}$	0.8 x V_{CCQ}	-	V	I_{OL}=8mA
	24mA buffer	$V_{OH(24MA)}$	0.8 x V_{CCQ}	-	V	I_{OL}=24mA

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Table 8. Electrical Characteristics (AC Characteristics) (1/13) (Power-on Sequence)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C)

Item	Symbol	Min.	typ.	Max.	Unit	Timing chart (3)
External signal (EXT_CLK) clock cycle	t_{cyc}	-	50 (1) 10 (2)	-	ns ns	Figures 5 and 6
Reset release time (Time from power supply voltage stabilization to reset release)	t_{PLL_RST}	1	-	-	ms	
External signal (PLL_SEL) hold time	t_{PLL_SEL}	3	-	-	t_{cyc}	
PLL lock up time	t_{PLL_LUP}	-	-	50	us	
Internal reset release time	t_{RST}	-	1024	-	t_{cyc}	

Notes: (1) When the internal PLL is used.
(2) When the internal PLL is not used.
(3) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 8. Electrical Characteristics (AC Characteristics) (2/13) (CS function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C)
(Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (1)
Address delay time	t_{AD}	2.8	15.4	ns	Figures 7 to 12
Byte control delay time	t_{BCD}	2.8	15.4	ns	
CS# delay time	t_{CSD}	2.8	15.4	ns	
ALE delay time	t_{ALED}	2.8	15.4	ns	
RD# delay time	t_{RSD}	2.8	15.4	ns	
Read-data setup time	t_{RDS}	12.78	-	ns	
Read-data hold time	t_{RDH}	3	-	ns	
WR# delay time	t_{WRD}	2.8	15.4	ns	
Write-data delay time	t_{WDD}	1.7	15.4	ns	
Write-data hold time	t_{WDH}	2.8	-	ns	
WAIT# setup time	t_{WTS}	12.78	-	ns	Figure 13
WAIT# hold time	t_{WTH}	3	-	ns	
Address delay time 2 (SDRAM)	t_{AD2}	2.8	15.4	ns	Figures 14 to 16
CS# delay time 2 (SDRAM)	t_{CSD2}	2.8	15.4	ns	
DQM delay time (SDRAM)	t_{DQMD}	2.8	15.4	ns	
CKE delay time (SDRAM)	t_{CKED}	2.8	15.4	ns	
Read-data setup time 2 (SDRAM)	t_{RDS2}	12.78	-	ns	
Read-data hold time 2 (SDRAM)	t_{RDH2}	3	-	ns	
Write-data delay time 2 (SDRAM)	t_{WDH2}	1.7	15.4	ns	
Write-data hold time 2 (SDRAM)	t_{WDH2}	2.8	-	ns	
WE# delay time (SDRAM)	t_{WED}	2.8	15.4	ns	
RAS# delay time (SDRAM)	t_{RASD}	2.8	15.4	ns	
CAS# delay time (SDRAM)	t_{CASD}	2.8	15.4	ns	

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 8. Electrical Characteristics (AC Characteristics) (3/13) (SYSTEM function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C)

Item	Symbol	Min.	Max.	Unit	Timing chart (1)
NMI pulse width	t_{NMIOUT}	200	-	ns	Figure 17
IRQ pulse width	t_{IRQOUT}	200	-	ns	Figure 18

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Table 8. Electrical Characteristics (AC Characteristics) (4/13) (JTAG function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (1)
TCK clock high-level pulse width	t_{TCKH}	45	-	ns	Figure 19
TCK clock low-level pulse width	t_{TCKL}	45	-	ns	
TCK clock rise time	t_{TCKr}	-	5	ns	
TCK clock fall time	t_{TCKf}	-	5	ns	
TRST# pulse width	(t_{TRSTW})	20	-	ns	Figure 20
TMS setup time	t_{TMSS}	20	-	ns	Figure 21
TMS hold time	t_{TMSH}	20	-	ns	
TDI setup time	t_{TDIS}	20	-	ns	
TDI hold time	t_{TDIH}	20	-	ns	
TDO data delay time	t_{TDOD}	0	40	ns	

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 8. Electrical Characteristics (AC Characteristics) (5/13) (Ethernet function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (1)
ET_TXCLK cycle time	t_{Tcyc}	40	-	ns	Figures 22 to 26
ET_TXCLK high level width	t_{TCKWH}	0.35X t_{Tcyc}	-	ns	
ET_TXCLK low level width	t_{TCKWL}	0.35X t_{Tcyc}	-	ns	
EX_TXEN output delay time	t_{TEND}	0	25	ns	
ET_TXD[3:0] output delay time	t_{TOD}	0	25	ns	
ET_RXCLC cycle time	t_{Rcyc}	40	-	ns	
ET_RXCLK high level width	t_{RCKWH}	0.35X t_{Rcyc}	-	ns	
ET_RXCLK low level width	t_{RCKWL}	0.35X t_{Rcyc}	-	ns	
ET_RXDV setup time	t_{RDVS}	10	-	ns	
ET_RXDV hold time	t_{RDVH}	10	-	ns	
ET_RXD[3:0] setup time	t_{RDDS}	10	-	ns	
ET_RXD[3:0] hold time	t_{RDDH}	10	-	ns	
ET_RXER setup time	t_{RERS}	10	-	ns	
ET_RXER hold time	t_{RERH}	10	-	ns	
AVB_GPTP_EXTERN cycle time	t_{Gcyc}	40	-	ns	
AVB_GPTP_EXTERN high level width	t_{GCKWH}	0.35X t_{Gcyc}	-	ns	
AVB_GPTP_EXTERN low level width	t_{GCKWL}	0.35X t_{Gcyc}	-	ns	
AVB_CAPTURE high level width	t_{CAPWH}	2X t_{Ccyc}		ns	
ET_CRS setup time	t_{CRSs}	10	-	ns	Figure 27
ET_CRS hold time	t_{CRSh}	10	-	ns	
ET_COL setup time	t_{COLs}	10	-	ns	Figure 28
ET_COL hold time	t_{COLh}	10	-	ns	

Note: (1) The timing voltage threshold of t_{Tcyc}, t_{Rcyc} and t_{Gcyc} shall be set to "V_{CCQ} × 0.5". Other timing voltage thresholds shall be "V_{OH}=0.7xV_{CCQ}, V_{OL}=0.3xV_{CCQ}, V_{IH}=0.7xV_{CCQ} and V_{IL}=0.3xV_{CCQ}".

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Table 8. Electrical Characteristics (AC Characteristics) (6/13) (GPT function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input capture input pulse width (single edge designation)	t_{GTICW1}	3	-	t_{PAcyc} (1)	Figure 29
Input capture input pulse width (both edges designation)	t_{GTICW2}	5	-	t_{PAcyc} (1)	
External trigger input pulse width (single edge designation)	t_{OTETW1}	1.5	-	t_{PAcyc} (1)	Figure 30
External trigger input pulse width (both edges designation)	t_{TCKf}	2.5	-	t_{PAcyc} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle
Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Table 8. Electrical Characteristics (AC Characteristics) (7/13) (TMR function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Timer clock input pulse width (single edge designation)	t_{TMCWH}	1.5	-	t_{PBcyc} (1)	Figure 31
Timer clock input pulse width (both edges designation)	t_{TMCWL}	2.5	-	t_{PBcyc} (1)	

Note: (1) t_{PBcyc}: PCLKB cycle
Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 8. Electrical Characteristics (AC Characteristics) (8/13) (RSPI function (1/2))

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
RSPCK clock cycle (master)	t_{SPcyc1}	2	4096	t_{PAcyc} (1)	Figure 32
RSPCK clock cycle (slave)	t_{SPcyc2}	8	4096	t_{PAcyc} (1)	
RSPCK clock high level pulse width (master)	t_{SPCKWH}	(t_{SPcyc1}-t_{SPCKr}-t_{SPCKf})/2-3	-	ns	
RSPCK clock high level pulse width (slave)	t_{SPCKWH}	(t_{SPcyc2}-t_{SPCKr}-t_{SPCKf})/2	-	ns	
RSPCK clock low level pulse width (master)	t_{SPCKWL}	(t_{SPcyc1}-t_{SPCKr}-t_{SPCKf})/2-3	-	ns	
RSPCK clock low level pulse width (slave)	t_{SPCKWL}	(t_{SPcyc2}-t_{SPCKr}-t_{SPCKf})/2	-	ns	
RSPCK clock rise / fall time (output) (3)	t_{SPCKr}, t_{SPCKf}	-	5	ns	
RSPCK clock rise / fall time (input)	t_{SPCKr}, t_{SPCKf}	-	1	μs	
Data input setup time (master)	t_{su}	6	-	ns	Figures 33 to 38
Data input setup time (slave)	t_{su}	8.3-t_{PAcyc} (1)	-	ns	
Data Input Hold Time (Master, PCLKA set to divide-by-2)	t_{HF}	0	-	ns	
Data Input Hold Time (Master, PCLKA set to a value other than divide-by-2)	t_{H}	t_{PAcyc}	-	ns	
Data input hold time (slave)	t_{H}	8.3+2 x t_{PAcyc} (1)	-	ns	
SS input setup time (master)	t_{LEAD}	1	8	t_{SPcyc1}	
SS input setup time (slave)	t_{LEAD}	4	-	t_{PAcyc1} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (8/13) (RSPI function (2/2))

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SS input hold time (master)	t_{LAG}	1	8	t_{SPcyc1}	Figures 33 to 38
SS input hold time (slave)	t_{LAG}	4	-	t_{PAcyc} (1)	
Data output delay time (master)	t_{OD}	-	6.3	ns	
Data output delay time (slave)	t_{OD}	-	3 x t_{PAcyc} +20	ns	
Data output hold time (master)	t_{OH}	0	-	ns	
Data output hold time (slave)	t_{OH}	0	-	ns	
Continuous transmission delay time (master)	t_{TD}	t_{SPcyc1} + 2 x t_{PAcyc}	8 x t_{SPcyc1} +2 x t_{PAcyc}	ns	
Continuous transmission delay time (slave)	t_{TD}	4 x t_{PAcyc}	-	ns	
MOSI rise / fall time (master) (3)	t_{Dr}, t_{Df}	-	5	ns	
MISO rise / fall time (slave)	t_{Dr}, t_{Df}	-	1	µs	
SS input rise / fall time (output) (3)	t_{SSLr}, t_{SSLf}	-	5	ns	
SS input rise / fall time (input)	t_{SSLr}, t_{SSLf}	-	1	µs	
Slave access time	t_{SA}	-	4	t_{PAcyc} (1)	Figure 37 Figure 38
Slave output release time	t_{REL}	-	3	t_{PAcyc} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (9/13) (Simple SPI function (SCIF))

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SCK clock cycle output (master)	t_{SPcyc1}	4	65536	t_{PAcyc} (1)	Figure 32
SCK clock cycle input (slave)	t_{SPcyc2}	6	65536	t_{PAcyc} (1)	
SCK clock high level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock high level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock rise time (3)	t_{SPCKr}	-	5	ns	
SCK clock fall time (3)	t_{SPCKf}	-	5	ns	
Data input setup time (master)	t_{SU}	15	-	ns	Figures 33 to 36
Data input setup time (slave)	t_{SU}	5	-	ns	
Data input hold time	t_H	5	-	ns	
SS input setup time	t_{LEAD}	1	-	t_{SPcyc1} t_{SPcyc2}	
SS input hold time	t_{LAG}	1	-	t_{SPcyc1} t_{SPcyc2}	
Data output delay time (master)	t_{OD}	-	5	ns	
Data output delay time (slave)	t_{OD}	-	25	ns	
Data output hold time	t_{OH}	-5	-	ns	
Data rise time (3)	t_{Dr}	-	5	ns	
Data fall time (3)	t_{Df}	-	5	ns	
SS input rise time (3)	t_{SSLr}	-	5	ns	
SS input fall time (3)	t_{SSLf}	-	5	ns	
Slave access time	t_{SA}	-	3 x t_{Pcyc} +25	t_{PAcyc} (1)	Figure 37 Figure 38
Slave output release time	t_{REL}	-	3 x t_{Pcyc} +25	t_{PAcyc} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (10/13)

(Simple SPI Function (SCI))

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SCK clock cycle output (master)	t_{SPcyc1}	4	65536	t_{PBcyc} (1)	Figure 32
SCK clock cycle input (slave)	t_{SPcyc2}	8	65536	t_{PBcyc} (1)	
SCK clock high level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock low level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock rise time (3)	t_{SPCKr}	-	20	ns	
SCK clock fall time (3)	t_{SPCKf}	-	20	ns	
Data input setup time (master)	t_{SU}	33.3	-	ns	Figures 33 to 36
Data input setup time (slave)	t_{SU}	33.3	-	ns	
Data input hold time	t_H	33.3	-	ns	
SS input setup time	t_{LEAD}	1	-	t_{SPcyc1} t_{SPcyc2}	
SS input hold time	t_{LAG}	1	-	t_{SPcyc1} t_{SPcyc2}	
Data output delay time	t_{OD}	-	33.3	ns	
Data output hold time	t_{OH}	-10	-	ns	
Data rise time (3)	t_{Dr}	-	16.6	ns	
Data fall time (3)	t_{Df}	-	16.6	ns	
SS input rise time (3)	t_{SSLr}	-	16.6	ns	
SS input fall time (3)	t_{SSLf}	-	16.6	ns	
Slave access time	t_{SA}	-	5	t_{PBcyc} (1)	Figure 37 Figure 38
Slave output release time	t_{REL}	-	5	t_{PBcyc} (1)	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (11/13) (SCIF Function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input clock cycle phase-locked synchronization	t_{Scyc1}	4	-	t_{PAcyc} (1)	Figure 39
Input clock cycle clock synchronization	t_{Scyc2}	6	-	t_{PAcyc} (1)	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Input clock rise time	t_{SCKr}	-	5	ns	
Input clock fall time	t_{SCKf}	-	5	ns	
Output clock cycle phase-locked synchronization	t_{Scyc1}	8	-	t_{PAcyc} (1)	
Output clock cycle clock synchronization	t_{Scyc2}	4	-	t_{PAcyc} (1)	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Output clock rise time(3)	t_{SCKr}	-	5	ns	
Output clock fall time(3)	t_{SCKf}	-	5	ns	
Transmission data delay time master	t_{TXD1}	-	5	ns	Figure 40
Transmission data delay time slave	t_{TXD2}	-	25	ns	
Received data setup time master	t_{rxs1}	15	-	ns	
Received data setup time slave	t_{rxs2}	5	-	ns	
Received data hold time master	t_{RXH1}	5	-	ns	
Received data hold time slave	t_{RXH2}	5	-	ns	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (12/13) (SCI Function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input clock cycle phase-locked synchronization	t_{Scyc1}	4	-	t_{PBcyc} (1)	Figure 41
Input clock cycle clock synchronization	t_{Scyc2}	6	-	t_{PBcyc} (1)	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Input clock rise time	t_{SCKr}	-	5	ns	
Input clock fall time	t_{SCKf}	-	5	ns	
Output clock cycle phase-locked synchronization	t_{Scyc1}	8	-	t_{PBcyc} (1)	
Output clock cycle clock synchronization	t_{Scyc2}	4	-	t_{PBcyc} (1)	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Output clock rise time(3)	t_{SCKr}	-	5	ns	
Output clock fall time(3)	t_{SCKf}	-	5	ns	
Transmission data delay time clock synchronization	t_{TXD}	-	28	ns	Figure 42
Received data setup time clock synchronization	t_{rxs}	15	-	ns	
Received data hold time clock synchronization	t_{RXH}	5	-	ns	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

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Table 8. Electrical Characteristics (AC Characteristics) (13/13) (CMTW Function)

(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacity=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input capture input pulse width single edge designation	$t_{CMTWTICW1}$	1.5	-	t_{PBcyc} (1)	Figure 43
Input capture input pulse width both edges designation	$t_{CMTWTICW2}$	2.5	-	t_{PBcyc} (1)	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 9. Screening Tests (1/2)

Test item (1)	Test method (2)
Stabilization bake (3)	[1008] Condition C (Min. 24 hours at min. 150°C) Stabilization bake shall be performed at pre-sealing process.
Temperature cycling	[1010] Condition C (10 minutes each at -65ºC and +150ºC), with 10-cycles. End-point electrical parameter measurements and inspections are not applicable.
Visual inspection	(4)
Particle Impact Noise Detection Test	[2020] Condition A
Radiographic inspection (5)	[2012] 1 direction (upper: Y2) (8)
Pre-burn-in electrical parameters (subgroups 1 and 7, Group A)	(6) In accordance with Table 15.
Burn-in test	[1015] Min. 240 hours at min. 125°C. Test circuits shall be in accordance with Figure 44.
Post-burn-in electrical parameters (subgroups 1 and 7, Group A)	(6) In accordance with Table 15.
Final electrical parameter test (7) a) Static test 1) 25°C (subgroup 1, group A) 2) Maximum and minimum operating temperature (subgroups 2 and 3, group A) b) Switching test 1) 25°C (subgroup 9, group A) 2) Maximum and minimum operating temperature (subgroups 10 and 11, group A) c) Functional test 1) 25°C (subgroup 7, group A) 2) Maximum and minimum operating temperature (subgroup 8, group A)	In accordance with Table 15.
Reverse bias burn-in test	(Exempted)

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Table 9. Screening Tests (2/2)

Test item (1)	Test method (2)
Seal	[1014]
Electrical parameter test after eutectic solder ball attach a) Static test 1) 25°C (subgroup 1, group A) b) Switching test 1) 25°C (subgroup 9, group A) c) Functional test 1) 25°C (subgroup 7, group A)	In accordance with Table 15.
External visual	[2009]

Notes:

(1) Unless otherwise specified, the tests shall be performed in the order shown above.

(2) Four-digit number in square brackets refers to the test method number specified in MIL-STD-883.

(3) The sum of the stabilization baking hours performed immediately before sealing and the baking duration specified herein may be negotiated to be 24 hours minimum.

(4) Defects such as damage to the package and separation of lids shall be inspected. Since the type of the package is leadless, “defects such as loss of leads” specified in Note (3) of Table B-1 of JAXA-QTS-2010 was removed.

(5) Following this inspection, appropriate stabilization baking may be performed.

(6) Products shall fail if deviations of electrical parameters calculated pre- and post-burn-in test in accordance with Note (6) of Table B-1 of JAXA-QTS-2010 exceed the specified delta limits. The failed lots shall be disposed of in accordance with paragraph B.3.2, Appendix B of JAXA-QTS-2010.

(7) For test items common to the final and post-burn-in electrical parameter tests, the final electrical parameter test for the test items may be substituted with the post-burn-in electrical parameter test at 25°C.

(8) The definition of direction shall apply paragraph B.2.2, Appendix B of JAXA-QTS-2010.

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Table 10. Group A Test [1]

(Electrical parameter tests)

Subgroup	Test [2] and [3]	Measurement conditions and tolerance
1	Static test (Tb = +25°C)	The measurement conditions and tolerances shall satisfy the electrical characteristics specified in Table 15. These tests shall be combined as the final electrical parameter test for screening tests and shall not be performed separately.
2	Static test (Tb = +120°C as a minimum)	
3	Static test (Tb = -37°C as a maximum)	
7	Static test (Tb = +25°C)	
8	Functional test (Tb = +120°C as a minimum) Functional test (Tb = -37°C as a maximum)	
9 [4]	Switching tests (Tb = +25°C)	
10 [5]	Switching tests (Tb = +120°C as a minimum)	
11 [6]	Switching test (Tb = -37°C as a maximum)	

Notes:

[1] The samples subjected to the group A test may also be used for the groups B, C, D and E tests.

[2] A single sample may be used for all subgroups.

[3] All measurements shall be performed while the junction temperature is in the thermal equilibrium state and the ambient temperature is at least 110% of the specified temperature.

[4] Dynamic tests (Tb = +25°C) specified in subgroup 4 of Table C-1 of JAXA-QTS-2010 shall be included in this test.

[5] Dynamic tests (Tb = +120°C) specified in subgroup 5 of Table C-1 of JAXA-QTS-2010 shall be included in this test.

[6] Dynamic tests (Tb = -37°C) specified in subgroup 6 of Table C-1 of JAXA-QTS-2010 shall be included in this test.

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Table 11. Group B Test

Subgroup	Test method (1)	Test condition	Sample size (accept no.)	
			Qualification test for JAXA-developed parts	Quality conformance inspection
1 (2)				
a) External physical dimensions	2016	Test requirements shall be in accordance with Table 18.	3 (0)	3 (0)
b) Internal gas analysis	2018	Water vapor concentration shall be 5000ppm as a maximum at +100°C.	3 (0)	3 (0)
2 (3)				
a) Resistance to solvents	2015	Condition C or D	3 (0)	-
b) Internal visual and mechanical	2013 and 2014		2 (0)	2 (0)
c) Bond strength (4)	2011		2 (0)	2 (0)
d) Die shear test	2019		3 (0)	3 (0)
e) Verification of glassivation layer integrity	abbreviated		-	-
3 (2) and (7)				
Radiographic inspection	(10)	Void ratio at junction shall be 25% maximum.	3 (0) (10)	3 (0) (10)
Solderability	(5)		3 (0) (8)	3 (0) (8)
4 (2)				
a) Lead integrity	(6)		2 (0) (9)	2 (0) (9)
b) Hermeticity test (seal) 1) Fine leak 2) Gross leak	exempted			

Notes:

(1) Four-digit number refers to the test method number defined in MIL-STD-883.

(2) Electrically defective products in the same inspection lot may be used.

(3) When subgroup 2 tests of the group test are performed, the samples used for subgroup 2 of the Group C test shall be used, except for the resistance to solvents.

(4) All bonding shall be tested.

(5) This test shall be performed using a ceramic substrate, and a solder wettability test under reflow heating conditions shall be performed. Pre-conditioning conditions for the solderability test shall be “+155°C, DRY Bake 4H” specified in Condition Category E of Table 3-3 of J-STD-002E.

(6) Since MIL-STD-883L 2004 is not applicable to BGAs, tests shall be conducted using the following alternative methods.

Solder ball pull test: In accordance with JESD22-B115A

Pull strength requirements for eutectic solder ball: 40.0MPa as a minimum

Pull strength requirements for high-temperature solder ball: 19.7MPa as a minimum

(7) When electrically defective samples are used, the samples shall be exposed to the same thermal environments as qualified samples experience during the screening test (such as stabilization bake, temperature cycling and burn-in) prior to the tests.

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(8) The sample size shall be three and the number of solder ball shall be LTPD15 (15(0)).
(9) The total number of solder ball shall be LTPD5 (45(0)). Equivalent number of solder balls from each sample shall be selected.
(10) The Voids at solder ball junction shall be inspected. All solder balls shall be inspected. Criteria for pass / fail of void ratio shall be 25% maximum (in accordance with JERG-0-054).

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Table 12. Group C Test

(Die related tests)

Subgroup	Test method (1)	Test condition	Sample size (accept no.)		
			Qualification test for JAXA-developed parts	Quality conformance inspection (5)	
				Cond. 1	Cond.2
Subgroup 1					
a) Preconditioning	-	Samples shall be heated under conditions shown in Figure 5-4 and Table 5-3 of JERG-0-043. The number of heating cycles shall be two.	LTPD5	LTPD10	-
b) Steady state life test	1005	1,000 hours at +125°C. Test circuit shall be in accordance with Figure 44.	LTPD5	LTPD10	-
c) End-point electrical parameter test		Group A, subgroups 1, 2, 3, 7, 8, 9, 10 and 11	LTPD5	LTPD10	-
d) Bond strength (4)	2011	Condition C or D	2(0)	2(0)	-
Subgroup 2					
a) Temperature cycling test	1010	Condition C (10 minutes each at -65ºC and +150ºC), with 100-cycles.			
b) Constant acceleration	2001	Condition A, Y1 direction (3)			
c) Hermeticity test (seal): 1) Fine 2) Gross	1014		12(0)	5(0)	-
d) End-point electrical parameter test		Group A, subgroups 1, 2 and 3			
Subgroup 3					
a) Electrostatic discharge sensitivity test	3015	The pin combination shall be as specified in Table 16.	3(0) (2)	-	-
b) End-point electrical parameter test		Group A, subgroup 1			

Notes:

(1) Four-digit number refers to the test method number defined in MIL-STD-883.

(2) The sample size shall apply to each pin combination.

(3) The definition of direction shall be in accordance with paragraph C.2.2, Appendix C of JAXA-QTS-2010.

(4) All bonding shall be tested.

(5) The sample size requirements for quality conformance inspection are as follows.

Condition 1: Except for Condition 2, Paragraph G.4.7.1 (Table G-1), Appendix G of JAXA-QTS-2010 shall be applied.

Condition 2: For ICs manufactured from the same wafer lot as the inspection lot ICs, when qualification test for JAXA-developed parts or quality conformance inspection has

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been performed and the ICs have passed, item b), paragraph G.4.7.1.1, Appendix G of JAXA-QTS-2010 shall apply and the ICs shall be exempted.

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Table 13. Group D Test (1/2)

(Package related tests)

Subgroup	Test method (1)	Test condition	Sample size (accept no.)		
			Qualification test for JAXA-developed parts	Quality conformance inspection	
				Cond.1	Cond.2
Subgroup 1					
a) Thermal shock	1011	Condition B (5 minutes each at -55ºC and +125ºC), 15 cycles			
b) Temperature cycling test	1010	Condition C (10 minutes each at -65ºC and +150ºC), 100 cycles			
c) Moisture resistance	1004	10 cycles			
d) Hermeticity test (seal)	1014		LPTD15	5(0)	-
1) Fine					
2) Gross					
e) Visual inspection		In accordance with test methods 1004, 1010 and 1011.			
f) End-point electrical parameter test		Group A, subgroup 1			
Subgroup 2 (2)					
a) Mechanical shock	2002	Condition B (1,500g, 0.5ms, five times), six directions (X1, X2, Y1, Y2, Z1 and Z2) (5)			
b) Vibration test	2007	Condition A (20g, four minutes/times, four times/direction, three directions (X, Y and Z) (5)			
c) Hermeticity test (seal):	1014		LPTD15	5(0)	-
1) Fine					
2) Gross					
d) Visual inspection		In accordance with test methods 2002 and 2007.			
e) End-point electrical parameter test (3)		Group A, subgroup 1			
f) Internal visual inspection (7) (8) or radiographic inspection (7)	2013 2012	Only wire appearance shall be inspected for anomaly. When wire appearance can be inspected by radiographic inspection, radiographic inspection may be used as a substitute for visual inspection.	2(0)	-	-
Subgroup 3			-	-	-
(Deleted)	-	-			

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Table 13. Group D Test (2/2)

(Package related tests)

Subgroup	Test method (1)	Test condition	Sample size (accept no.)		
			Qualification test for JAXA-developed parts	Quality conformance inspection	
				Cond.1	Cond.2
Subgroup 3 (Deleted)	-	-	-	-	-
Subgroup 4 (10) a) Short-circuit verification test (7) (9)					
1) Short-circuit during shock test	2002	Condition B	1(0)	-	-
2) Short-circuit during vibration test	2007	Condition A	1(0)	-	-

Notes:

(1) Four-digit number refers to the test method number defined in MIL-STD-883.

(2) Samples used for subgroup 1 tests may also be used.

(3) This test may be performed following b) vibration test.

(5) The definition of direction shall be in accordance with paragraph C.2.2, Appendix C of JAXA-QTS-2010.

(6) The sample size requirements for quality conformance inspection are as follows.

Condition 1: Except for Condition 2, paragraph G.4.7.1 (Table G-1), Appendix G of JAXA-QTS-2010 shall be applied.

Condition 2: When Group D testing for the same integrated circuit group has started and the ICs have passed within one year prior to the completion date of screening for the current inspection lot, item c), paragraph G.4.7.1.1, Appendix G of JAXA-QTS-2010 shall apply and the ICs shall be exempted.

(7) This test shall be conducted when internal wire is gold.

(8) Prior to the tests, sample shall be opened in a manner to avoid damage and contamination.

(9) If it is verified that different internal lead wire do not contact with each other and possibility of the electrical short-circuit due to shock and vibration is eliminated by design and structure of internal lead wire as shown in paragraph 3.3.6 of JAXA-QTS-2010, this test may be exempted.

(10) Samples subjected to subgroup 2 tests may be used. Electrically defective products or newly sampled devices in the same inspection lot may be used. However, electrically defective products, which do not interfere with this test, shall be used. When electrically defective products are used, the samples shall be exposed to the same thermal environments as qualified samples experience during the screening test (such as stabilization bake, temperature cycling and burn-in) prior to the tests.

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Table 14. Group E Test

(Radiation Test)

Subgroup	Test method (1)	Test condition	Sample size (accept no.)		
			Qualification test for JAXA-developed parts	Quality conformance inspection (7)	
				Cond.1	Cond.2
1 a) Steady state total ionizing dose test	1019	Radiation source (^{60}Co gamma ray, uniformity±10%, accuracy±5%) Test circuit shown in Figure 45 shall be used. The terminal treatment during ionizing dose test shall be in accordance with Table 6, "Group E Subgroup 1 Terminal Treatment".	5 (0) (2) (3)	5 (0) (2) (3)	-
b) End-point electrical parameter test		Group A ,subgroups 1, 7 and 9 (4) (5)			
2 a) Single-event effects tests		Test condition shall be in accordance Table 17. Test circuit of Figure 46 shall be used.	4(0) (6)	4(0) (6)	-
b) End-point electrical parameter test		Group A, subgroups 1, 7 and 9 (5)			

Notes:

(1) Four-digit number refers to the test method number defined in MIL-STD-883.

(2) Sample size and acceptance number shall be applied to each inspection sublot. When multiple inspection sublots are made from a single wafer lot, a single sublot may represent the inspection lot.

(3) Sample size and acceptance number shall be applied to each radiation assurance level.

(4) The post-irradiation electrical parameter measurements at the irradiation site and application of bias voltage during transportation are not required. The post-irradiation electrical parameter measurements shall be performed within 48 hours after irradiation.

Post-annealing electrical parameter tests shall be conducted within 168 ± 12 hours from the completion of irradiation. During the storage period between the completion of irradiation and the post-annealing electrical parameter tests, bias shall be applied (terminal treatment shall be the same as during irradiation), and the temperature shall be maintained at +24 ± 6°C.".

(5) Test items of pre-irradiation electrical parameter tests shall be identical to those of end-point electrical parameter tests.

(6) If there are more than one type of single event effect tests, the sample size (acceptance number) for each type of test shall be 4(0).

(7) The sample size requirements for quality conformance inspection are as follows.

Condition 1: Except for Condition 2, Table C-5 of JAXA-QTS-2010 shall be applied.

Condition 2: For ICs manufactured from the same wafer lot as the inspection lot ICs, when qualification test for JAXA-developed parts or quality conformance inspection has been performed and the ICs have passed, item b), paragraph G.4.7.1.1, Appendix G of JAXA-QTS-2010 shall apply and the ICs shall be exempted.

Table 15. Group A Tests (1/4)

Symbol	Test condition										Tolerance						Unit
	VDD	VDDPLL	VCCQ	VBP	VBN	VSSPLL	VSS/VSSQ	Input pin	Output pin	Test pin	Subgroup 1 (Tb=+25℃)		Subgroup 2 (Tb=+120℃)		Subgroup 3 (Tb=-37℃)		
											Min.	Max.	Min.	Max.	Min.	Max.	
OPEN	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	-600μA 600μA	-1 0.4	-0.4 1	-1 0.4	-0.4 1	-1 0.4	-0.4 1	V
	Contact check (Set all pins other than the measurement target to Low)																
SHORT	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	0.0V	Hi-Z	Hi-Z	-600μA 600μA	-1 0.4	-0.4 1	-1 0.4	-0.4 1	-1 0.4	-0.4 1	V
	Contact check (Set all pins other than the measurement target to Open)																
VBP Bias	1.2V	1.2V	0.0V	0.6V	0.0V	0.0V	0.0V	0.0V	0.0V	0.6V	-100	100	-100	100	-100	100	μA
	The current consumption between VDD and VBP shall be measured.																
VBN Bias	1.2V	1.2V	0.0V	VDD	0.6V	0.0V	0.0V	0.0V	0.0V	0.6V	-100	100	-100	100	-100	100	μA
	The current consumption between VSS and VBN shall be measured.																
IDDcore _NOP	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- -	828 991	- -	828 991	- -	828 991	mA
	The current consumption of the core while the CPU is continuously executing NOP commands shall be measured.																
IDDcore _Function	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- -	859 1030	- -	859 1030	- -	859 1030	mA
	The current consumption of the core while the CPU is operating at an external clock frequency shall be measured.																
IDDcore _PLL(1CPU)	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- - -	1003 937 1141	- - -	1003 937 1141	- - -	1003 937 1141	mA
	The current consumption of the core while the CPU is operating at an PLL clock frequency shall be measured.																
IDDcore _PLL(2CPU)	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- - -	1094 994 1213	- - -	1094 994 1213	- - -	1094 994 1213	mA
	The current consumption of the core while the CPU is operating at an PLL clock frequency shall be measured.																
IDDIO	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- -	71 96	- -	71 96	- -	71 96	mA
	The current consumption of the core while the CPU is operating at an external clock frequency shall be measured.																
IDDIO_PLL	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	- -	51 69	- -	51 69	- -	51 69	mA
	The current consumption of the I/O while the CPU is operating at an PLL clock frequency shall be measured.																

Table 15. Group A Tests (2/4)

Symbol	Test condition										Tolerance						Unit
	VDD	VDDPLL	VCCQ	VBP	VBN	VSSPLL	VSS/VSSQ	Input pin	Output pin	Test pin	Subgroup 1 (Tb=+25℃)		Subgroup 2 (Tb=+120℃)		Subgroup 3 (Tb=-37℃)		
											Min.	Max.	Min.	Max.	Min.	Max.	
IIL	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	1.0V/VCCQ	open	0.0V	-0.6	0.6	-0.6	0.6	-0.6	0.6	μA
	Voltage shall be applied to the input terminal to verify the gate leakage of Tr.																
IIH	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/1.0V	open	3.3V 2.97V 3.6V	-0.6	0.6	-0.6	0.6	-0.6	0.6	μA
	Voltage shall be applied to the input terminal to verify the gate leakage of Tr.																
IOZL	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V			0.0V	-0.6	0.6	-0.6	0.6	-0.6	0.6	μA
	Voltage shall be applied to the input terminal to verify the gate leakage of Tr.																
VIL	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.2×VCCQ /VCCQ	0～VCCQ	0.2×VCCQ	-	-	-	-	-	-	-
	Voltage shall be applied to the input terminal to verify the threshold.																
VIH	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V /0.7×VCCQ	0～VCCQ	0.7×VCCQ	-	-	-	-	-	-	-
	Voltage shall be applied to the input terminal to verify the threshold.																
VOL	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	4mA/8mA	-	0.4	-	0.4	-	0.4	V
	Current shall be applied to the output terminal to verify the terminal voltage.																
VOH	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	4mA/8mA	VCCQ×0.8	-	VCCQ×0.8	-	VCCQ×0.8	-	V
	Current shall be applied to the output terminal to verify the terminal voltage.																

Table 15. Group A Tests (3/4)

Symbol	Test condition										Tolerance						Unit
	VDD	VDDPLL	VCCQ	VBP	VBN	VSSPLL	VSS/VSSQ	Input pin	Output pin	Test pin	Subgroup 1 (Tb=+25℃)		Subgroup 2 (Tb=+120℃)		Subgroup 3 (Tb=-37℃)		
											Min.	Max.	Min.	Max.	Min.	Max.	
TIS	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	Each AC characteristics shall be satisfied.						-
	AC characteristics (input setup) shall be measured.																
TIH	- 1.11V 1.29V	VDD	- 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	Each AC characteristics shall be satisfied.						-
	AC characteristics (input hold) shall be measured.																
TO	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	-	-	Each AC characteristics shall be satisfied.						-
	AC characteristics (output delay) shall be measured.																
PLL_TMR	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	The frequency shall be as specified by the terminal settings.						-
	PLL clock frequency (TMR mode) shall be measured.																
PLL_DMR	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	The frequency shall be as specified by the terminal settings.						-
	PLL clock frequency (DMR mode) shall be measured.																
PLL_SINGLE	1.2V	VDD	3.3V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	The clock waveform shall not be output and shall remain fixed at L.						-
	PLL clock frequency (SINGLE mode) shall be measured.																
OCVTEG	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be oscillation waveform.						-
	Ring oscillator output shall be verified.																
Function	1.2V	VDD	3.3V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be consistent with the test pattern (expected value).						-
	Function tests shall be performed (external clock operation).																
Function _PLL	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be consistent with the test pattern (expected value).						-
	Function tests shall be performed (PLL clock operation).																

Table 15. Group A Tests (4/4)

Symbol	Test condition										Tolerance						Unit
	VDD	VDDPLL	VCCQ	VBP	VBN	VSSPLL	VSS/VSSQ	Input pin	Output pin	Test pin	Subgroup 1 (Tb=+25℃)		Subgroup 2 (Tb=+120℃)		Subgroup 3 (Tb=-37℃)		
											Min.	Max.	Min.	Max.	Min.	Max.	
MEMORY _BIST _FUNCTION	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be consistent with the test pattern (expected value).						-
	SRAM BIST test shall be performed at finction tests.																
MEMORY _BIST _VDR	1.2V	VDD	3.3V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	-	0.81	-	0.81	-	0.81	V
	VDR shall be measured.																
SCAN	1.11V 1.29V	VDD	3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be consistent with the test pattern (expected value).						-
	Scan test shall be performed (Stuck-at test (Rate=10MHz)).																
SCAN _POWER	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	- - -	417 888 1044	- - -	972 888 1190	- - -	972 888 1044	mA
	Current consumption at scan test shall be measured (Stuck-at test (Rate=10MHz)).																
SCAN _OCC	1.2V 1.11V	VDD	3.3V 3.0V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	190 ([1]) -	- -	- 160 ([2])	- -	- -	- -	MHz MHz
	Scan test shall be performed (At-speed test (Rate=190MHz)).																
IDDq	1.2V 1.11V 1.29V	VDD	3.3V 3.0V 3.6V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	- - -	758 698 10	- - -	758 698 -	- - -	758 698 10	mA
	The quiescent current consumption shall be measured. However, under the 1.29V/3.6V condition, pass/fail shall be determined based on the difference between the maximum and minimum values obtained from 90 measurements.																
SRAM_Vmin	Search	VDD	1.7V	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	1.054	-	1.054	-	1.054	-	V
	The minimum VDD voltage required for SRAM operation shall be determined.										Samples tested in Subgroup 3 of Group C are permitted to reach 1.11V.						
Level Shifter	Search	VDD	3.6	VDD	0.0V	0.0V	0.0V	0.0V/VCCQ	0～VCCQ	-	Shall be consistent with the test pattern (expected value).						-
	The minimum VDD required for the level shifter within the IO cell to operate when VCCQ is 3.6V shall be determined.																

Notes [(1)]: The pass/fail threshold for the SCAN_OCC test to guarantee 190MHz (1.20V/25°C) shall be 228.1MHz (if the worst-case path operates at 190MHz, the SCAN_OCC test path shall operate at 228.1MHz).

[(2)] The pass/fail threshold for the SCAN_OCC test to guarantee 160MHz (1.11V/125℃) shall be 185.4MHz (if the worst-case path operates at 160MHz, the SCAN_OCC test path shall operate at 185.4MHz).

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Table 16. Pin Combination for Electrostatic Discharge Sensitivity Test in Subgroup 3 of Group C Tests

No.	Reference pin ([1])	Applied voltage	Number of applying cycles
1	A5,A6,A9,A10,A13,A14,A17,A19,A21,D1, E24,F1,H1,H11,H13,H15,J8,J10,J12,J14, J16,J24,K9,K17,K24,L1,L16,M1,M9,M17, N8,N16,N24,P9,P17,P24,R1,R8,R16,T1, T9,T11,T13,T15,U12,U14,U16,U24,W1, W24,Y1,AA24,AD4,AD6,AD8,AD11,AD12, AD15,AD16,AD19,AD20	±2000V	(3 times for positive voltage and 3times for negative voltage) / Pin
2	A4,A8,A11,A16,A20,D11,D15,D19,D24,E1, F4,F9,F13,F17,H6,H19,H24,J1,K3,K22,L8, L24,M6,M19,P1,P21,R3,T6,T19,T24,U1, U10,U22,W8,W12,W16,Y24,AA1,AA6,AA10, AA14,AD5,AD9,AD14,AD17,AD21		
3	H10,H12,H14,L17,N17,P8,R17,U13		
4	A7,A12,A15,A18,C3,C22,D10,D14,D18,F8,F12, F16,G1,G4,G24,J6,J9,J11,J13,J15,J17,J19,K1, K16,L3,L9,L22,M8,M16,M24,N1,N6,N9,N19,P3, P16,R9,R21,R24,T10,T12,T14,T16,U6,U11,U15, U19,V1,V22,V24,W9,W13,W17,AA7,AA11,AA15, AB3,AB22,AD7,AD10,AD13,AD18		
5	Pin to Pin method		

Note [(1)]: Pin information are shown in the column of CBGA Pin No. of Table 6.

Table 17. Test Condition for Single-Event Test in Subgroup 2 of Group E Tests

No.	Item	Sample conditions				Irradiation conditions				Number of LET condition		Remarks
		Operating condition	Power supply voltage	Board surface temp.	Number of samples(*1)	LET value(*2)	Irradiation angle(*3)	Flu [ions/cm^2/s](*4)	Fluence [ions/cm^2]	Qualification test for JAXA-developed parts	Quality conformance inspection	
1	SEU(1) (without error correcting)	The operation for local RAM, code RAM and shared memory shall not use the scrubbing function.	VCCQ= 3.3 V(*6) VDD= 1.2 V(*6)	Room temp.	4	4~68	0°	1×10^4	Min. 1×10^6	5	1	
						Max. 1	0°	2×10^5	Min. 2×10^7	1	1	
2	SEU(2) (with error correcting)	The operation for local RAM, code RAM and shared memory shall use the scrubbing function.	VCCQ= 3.3 V(*6) VDD = 1.2 V(*6)	Room temp.	4	4~68	0°	1×10^4	Min. 1×10^6	1	1	
3	SEU(3) (Logic section)	The operation shall perform a sort calculation on the logic section.	VCCQ= 3.3 V(*6) VDD = 1.2 V(*6)	Room temp.	4	4~68	0°	1×10^5	Min. 1×10^7	5	1	(*5)
4	SEL	Same operational state as SEU (1) (without error correcting)	VCCQ= 3.6 V(*6) VDD = 1.3 V(*6)	+120 ^{o}C	4	Min. 75	0°	1×10^6	Min. 1×10^8	1	1	

Notes (*1): Samples for SEU(1), SEU(2), SEU(3) and SEL may be shared among each other.

(*2): The unit for LET value is MeV/(mg/cm^2) and this applies hereinafter in this specification.

(*3): The irradiation angle of 0° is defined as the case where the beam is parallel to the direction perpendicular to the semiconductor chip surface of the sample and the beam is injected into the sample from the semiconductor chip surface side.

(*4): The flux values listed here are reference values. In actual tests, the flux shall be adjusted appropriately based on the beam conditions provided by the test facility.

(*5): If an error occurs during irradiation, the test shall be repeated until the specified fluence is reached.

(*6): Power supply voltage set value during tests.

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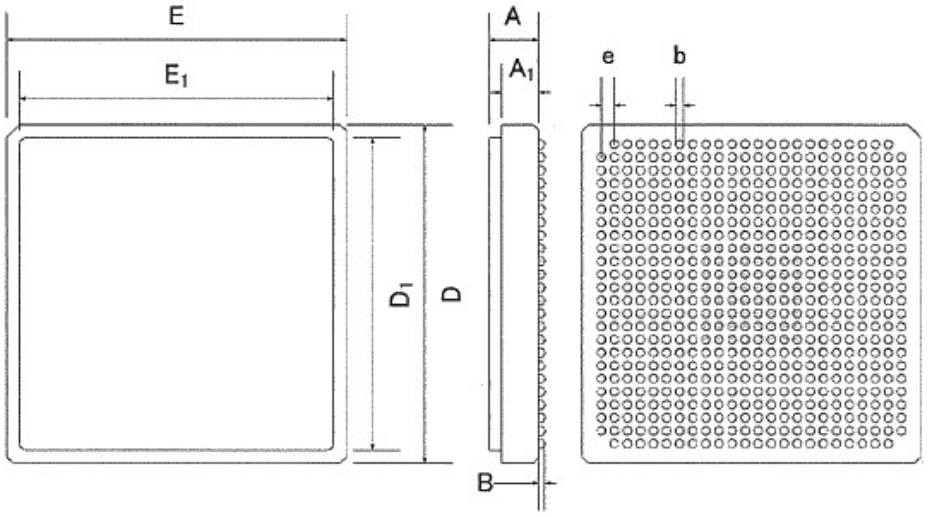
Table 18. Inspection Requirements for External Physical Dimensions of Subgroup 1 of Group B Tests

(1) Large chamfered edge



Notes:
(*1) Package material: Ceramic, Fe-Ni-Co alloy
(*2) Solder pin material: Sn10/Pb90 (central 8x8 terminals), Sn63/Pb37 (perimeter terminals)
(*3) Shall not perform stamping.

(Unit: mm)

Symbol	Dimensions		Remarks
	Min.	Max.	
A	3.45	4.15	
A1	2.55	3.15	
B	0.40	0.60	
b	0.60	0.80	(2)
D	25.80	26.20	
D1	24.00	24.40	(3)
E	25.80	26.20	
E1	24.00	24.40	(3)
e	1.00 standard		(2)

(1) Indicator
(2) Shall be applied to all pins.
(3) Includes lid misalignment and seam ring brazing.

Requirements for measurement count are as follows.
B: Eutectic solder balls at 3 locations, high-temperature solder balls at 3 locations, for a total of 6 locations.
b: Eutectic solder balls at 3 locations, high-temperature solder balls at 3 locations, for a total of 6 locations.
e: Eutectic solder balls at 3 locations, high-temperature solder balls at 3 locations, for a total of 6 locations.

Table 19. Delta Judgement Items for Screening Test (1/2)

No.	Test Item		Subject for judgement (1)	Judgement value	Test content
	Medium category	Minor category			
1	Continuity test	OPEN	-	-	To verify that the protection diodes for the IO cell relative to VDD and VSS are connected.
2		OPEN	-	-	To verify that there is no short circuit between adjacent IO cells.
3		VBP Bias	-	-	To verify that the source, drain, and NWELL of Tr are not shorted.
4		VBN Bias	-	-	To verify that the source, drain, and NWELL of Tr are not shorted.
5	DC test	IDDcore	O	(2)	To measure the VDDcore current consumption with the input terminals fixed (PLL stopped at EXT_CLK=100MHz).
6		IDDcore (PLL)	O	(2)	To measure the VDDcore current consumption with the input terminals fixed (PLL operating at 160MHz with EXT_CLK=20MHz).
7		IDDIO	O	(2)	To measure the VDDIO current consumption with the input terminals fixed (PLL stopped at EXT_CLK=100MHz).
8		IDDIO (PLL)	O	(2)	To measure the VDDIO current consumption with the input terminals fixed (PLL operating at 160MHz with EXT_CLK=20MHz).
9	DC test	IIL	O	(2)	To verify the gate leakage of core Tr when 0V is applied to the input terminal.
10		IIH	O	(2)	To verify the gate leakage of core Tr when VDDIO V is applied to the input terminal.
11		IOZL	O	(2)	To set the output terminal to Hi-Z output state and verify the gate leakage of the output stage Tr when 0V is applied.
12	DC test	VIL	O	(2)	To verify functional operation by inputting a pattern at Lo=0.8V from the input terminal. (TTL)
13		VIH	O	(2)	To verify that the device functions correctly by inputting a pattern with Hi=2.0V to the input terminal. (TTL)
14	DC test	VOL	O	(2)	To verify that the output terminal voltage is 0.4V or less when 0V is output to the output terminal and an IO current is applied. (TTL)
15		VOH	O	(2)	To verify that the output terminal voltage is 2.4V or less when VODDIO V is output to the output terminal and an IO current is applied. (TTL)

Table 19. Delta Judgement Items for Screening Test (2/2)

No.	Test Item		Subject for judgement (1)	Judgement value	Test content
	Medium category	Minor category			
16	AC test	TIS	O	(2)	To verify setup time of input terminals.
17		TIH	O	(2)	To verify hold time of input terminals.
18	AC test	TO	O	(2)	To verify output delay time of output terminals.
19		PLL output (TMR)	O	(2)	To verify that the PLL operates in TMR mode and outputs a stable frequency. (80MHz)
20		PLL output (DMR)	O	(2)	To verify that the PLL operates in DMR mode and outputs a stable frequency. (80MHz)
21		PLL output (SINGLE)	-	-	To verify that the PLL is in SINGLE mode and that there is no output.
22	Function test	Loose Function Test	-	-	Verify ASIC operation at low frequencies using representative operation patterns.
23	Structural test	MEMORY BIST	-	-	To verify operation in march patterns for high-density SRAM and logic rule SRAM.
24	Structural test	MEMORY BIST	-	-	To perform VDR measurements on high-density SRAM and logic rule SRAM.
25		SCAN	O (3)	(2)	To perform structural tests using the SCAN pattern. The expected failure modes are stuck-at failure, short/bridge failure, and open failure.
26		SCAN (OCC)	-	-	To perform speed tests using SCAN patterns, for FFs with low setup/hold margins.
27		IDDq	O	(2)	To perform currents tests using the SCAN pattern. The expected failure modes is short/bridge failure between wires.

Notes:
(1) The legend is as follows. O: Judge, -: Do not judge.
(2) Shall be 0.4 times the maximum allowable value.
(3) The subject of judgment shall be only the current consumption.

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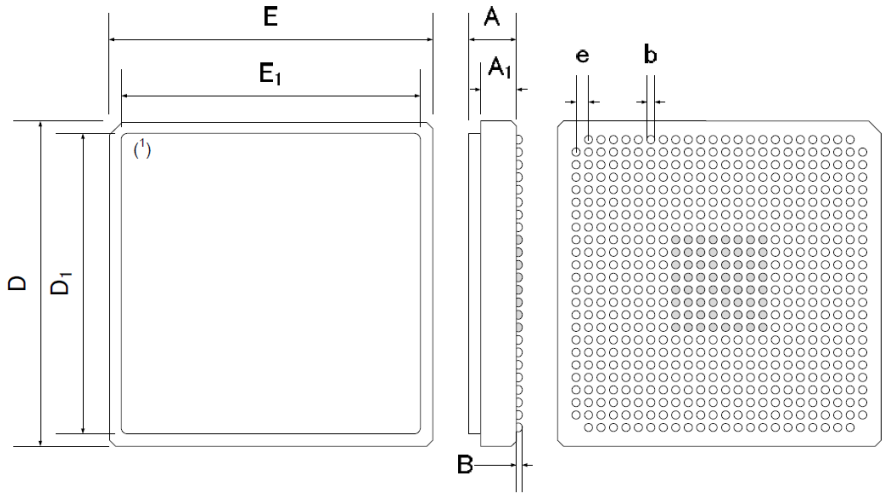
[Package Configuration]



Package material: Ceramic, Fe-Ni-Co alloy
Solder pin material: Sn10/Pb90 (central 8x8x solder balls), Sn63/Pb37 (perimeter solder balls)

(Unit: mm)

Symbol	Dimension		Remarks
	Min.	Max.	
A	3.45	4.15	
A_1	2.55	3.15	
B	0.40	0.60	
b	0.60	0.80	(2)
D	25.80	26.20	
D_1	24.00	24.40	(3)
E	25.80	26.20	
E_1	24.00	24.40	(3)
e	1.00 standard		(2)

Notes:
(1) Indicator area
(2) Shall be applied to all terminals.
(3) lid misalignment and brazing material overflow during sealing shall be included.

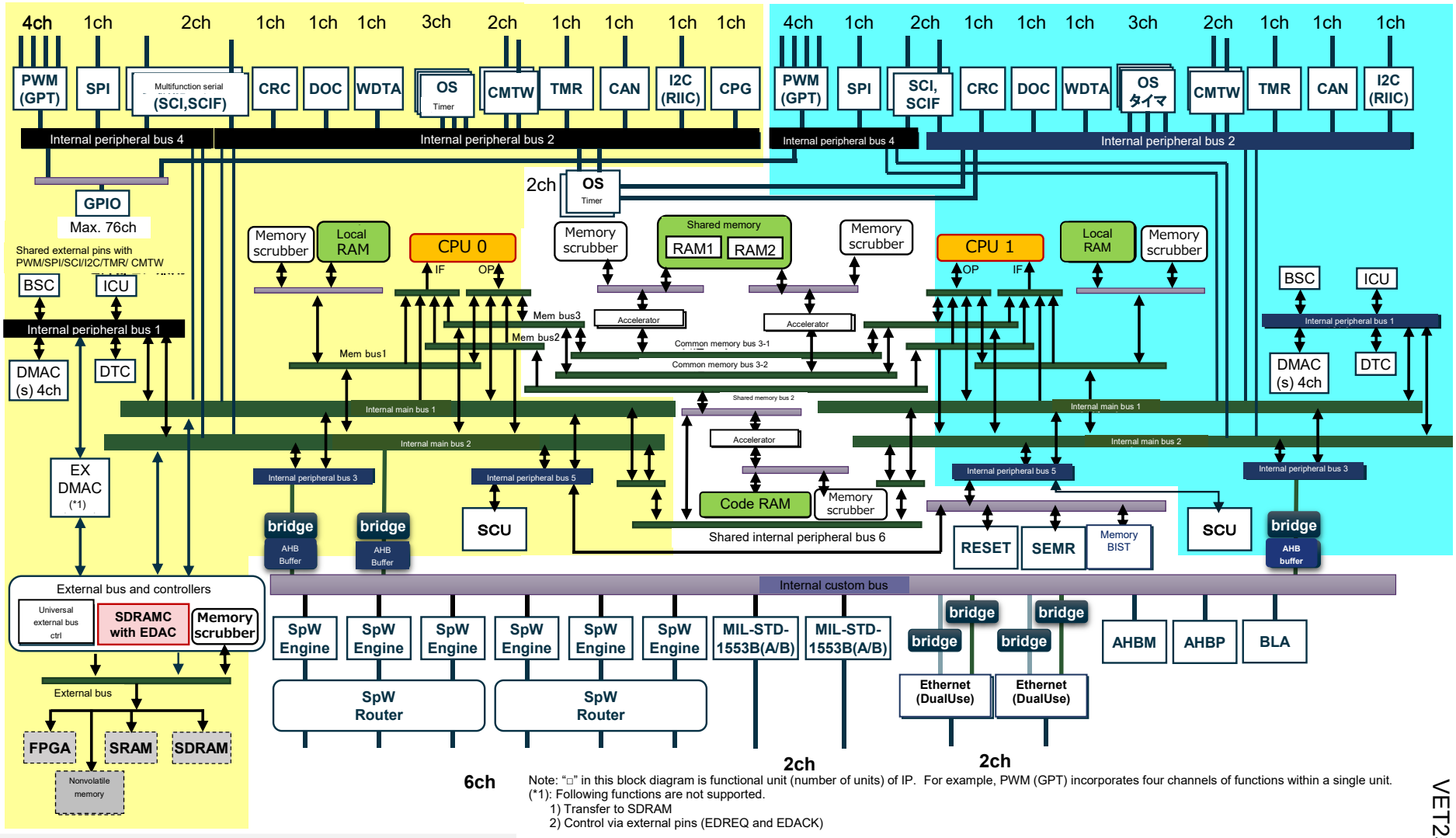
[Mass]

Mass (reference value): 7.6g to 12.0g (Typ. 9.7g) (1)
Note: (1) Design values calculated based on mass variations in ceramic packages and other components. The mass variation (actual results) for assembly lot 3 is 9.5g to 9.8g.

[Substrate pad size] (Reference value)

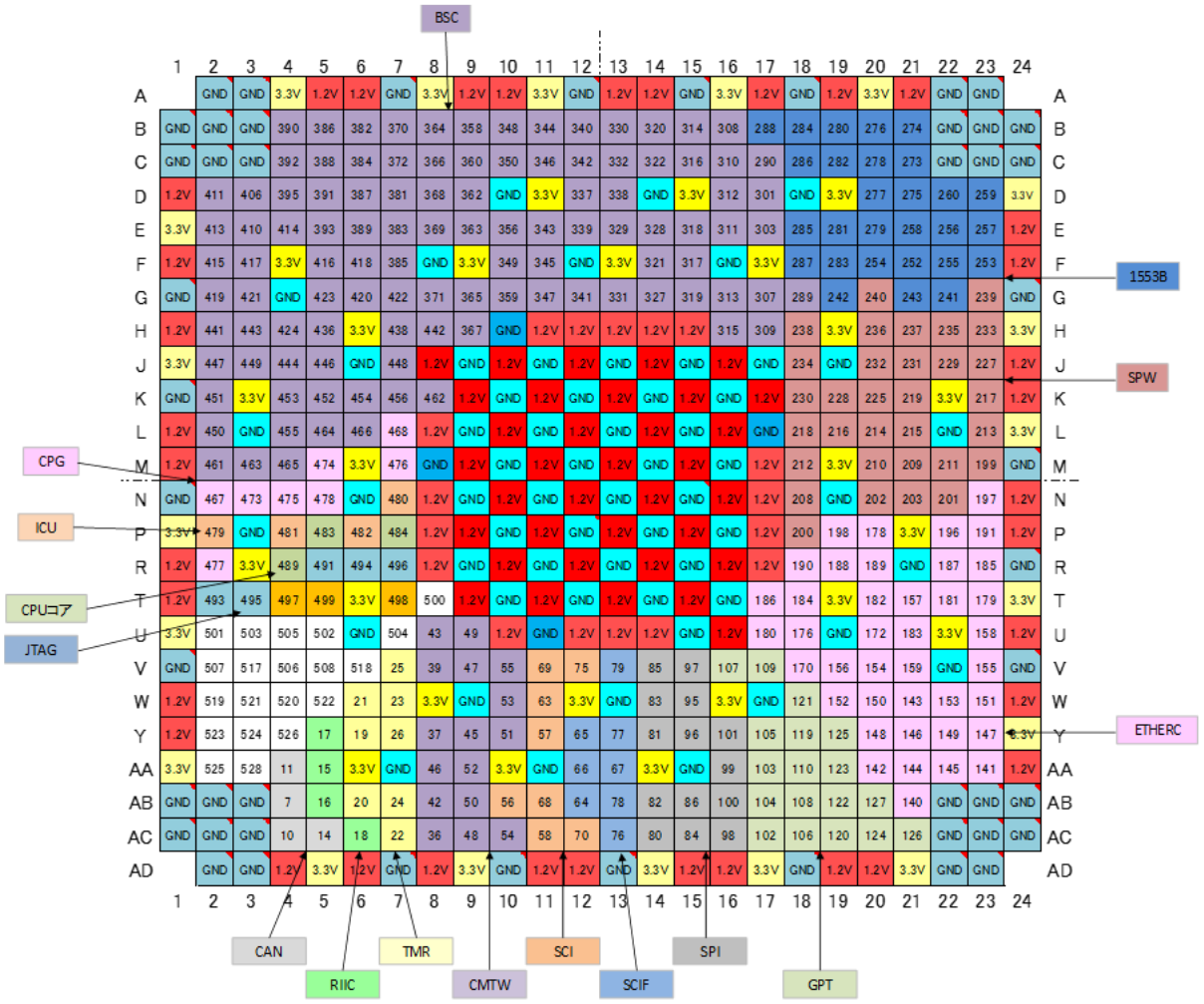
0.7mm diameter regardless of solder pin materials.

Figure 1. Package Drawing and Mass



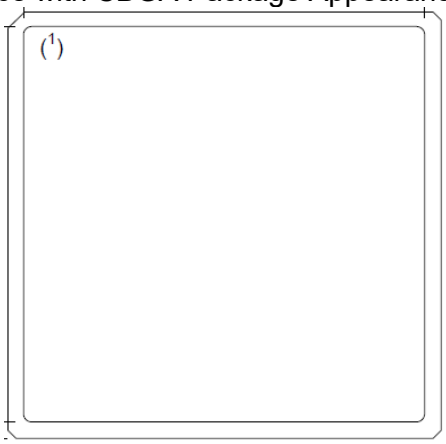
Note: "□" in this block diagram is functional unit (number of units) of IP. For example, PWM (GPT) incorporates four channels of functions within a single unit.
(*1): Following functions are not supported.
1) Transfer to SDRAM
2) Control via external pins (EDREQ and EDACK)

Figure 2. System Block Diagram



<TOP VIEW>

[Correspondence with CBGA Package Appearance<TOP VIEW>]



Note: (1) The notch position is at the top left of the drawing.

Figure 3. Pin Configuration Drawing (CBGA Package)

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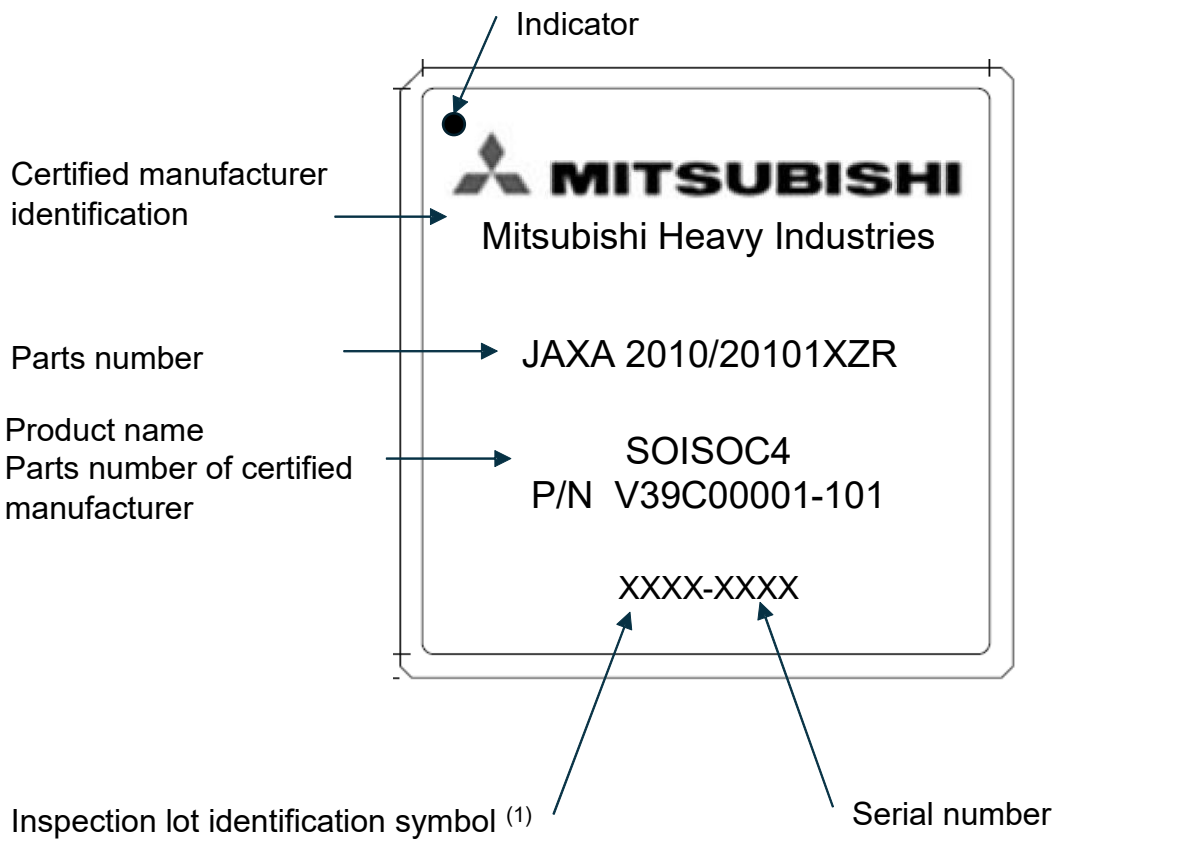

Note: (1) Four-digit numbers consisting of the last two digits of the year and two digits for the month in which assembly began shall be printed. For example, for assembly in June 2023, “2306” shall be printed.

Figure 4. Marking

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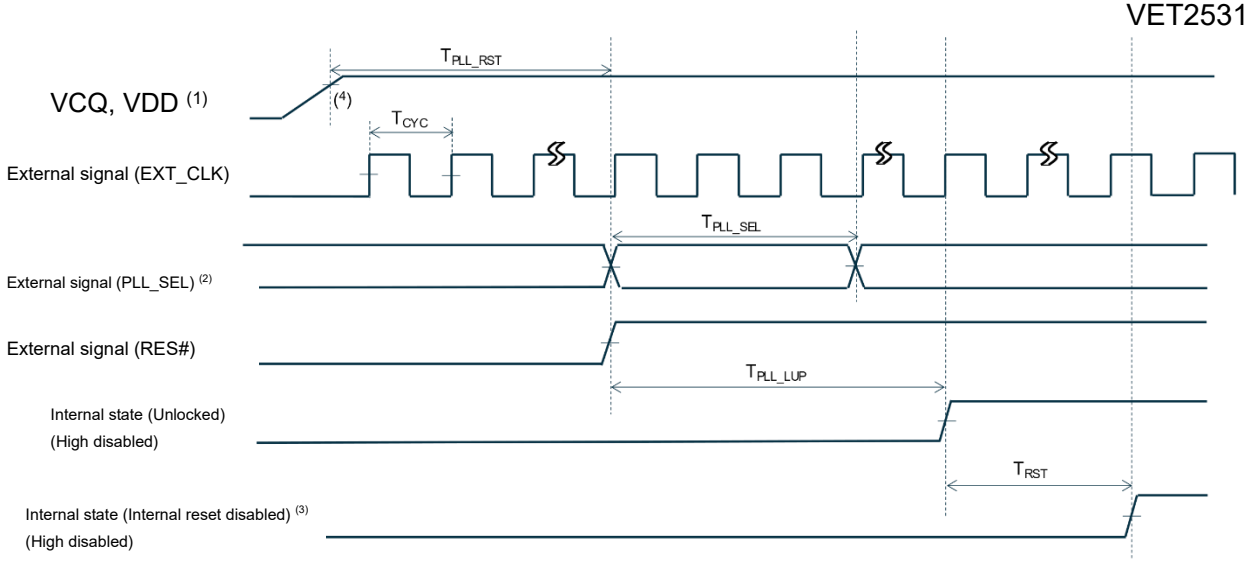


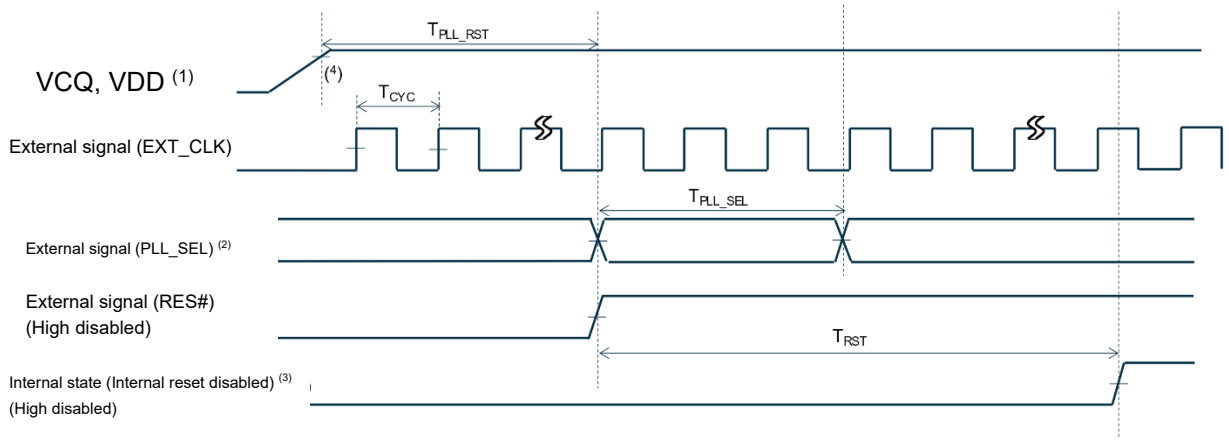
Notes (1): The recommended power-on sequence is to activate the internal logic power supply VDD (1.2V) first, followed by the I/O power supply VCCQ (3.3V), or to activate them simultaneously.

(2): The value shall be maintained for at least T_{PLL_SEL} periods after the rise of the external signal (RES#). Setting the value before the rise of the external signal (RES#) is acceptable.

(3): After internal reset is disabled, access to the CS area shall start approximately 25 internal clock cycles later.

(4): T_{PLL_RST} shall be based on the time when the power supply voltage stabilizes within the recommended operating conditions power supply voltage range specified in Table 2.

Figure 5. Power-On Sequence Timing (using internal PLL)



Notes (1): The recommended power-on sequence is to activate the internal logic power supply VDD (1.2V) first, followed by the I/O power supply VCCQ (3.3V), or to activate them simultaneously.

(2): The value shall be maintained for at least T_{PLL_SEL} periods after the rise of the external signal (RES#). Setting the value before the rise of the external signal (RES#) is acceptable.

(3): After internal reset is disabled, access to the CS area shall start approximately 25 internal clock cycles later.

(4): T_{PLL_SEL} shall be based on the time when the power supply voltage stabilizes within the recommended operating conditions power supply voltage range specified in Table 2.

Figure 6. Power-On Sequence Timing (not using internal PLL)

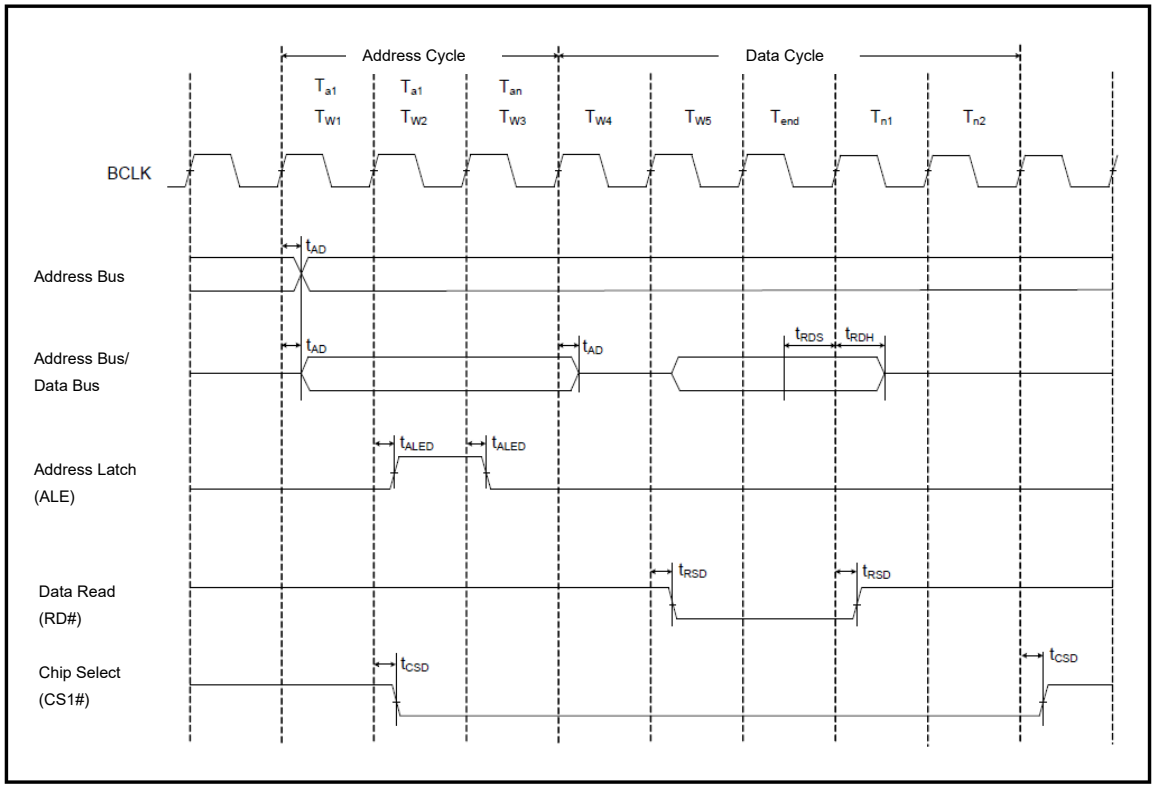


Figure 7. Read Access Timing for Address/Data Multiplex Bus

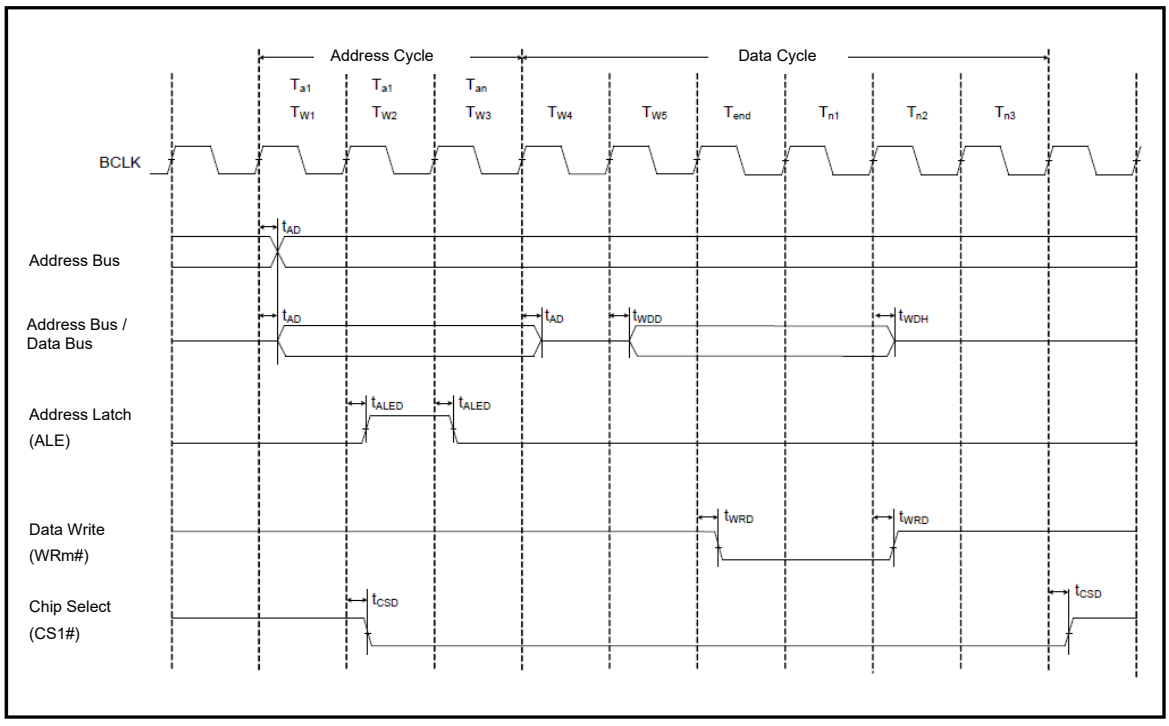


Figure 8. Write Access Timing for Address/Data Multiplex Bus

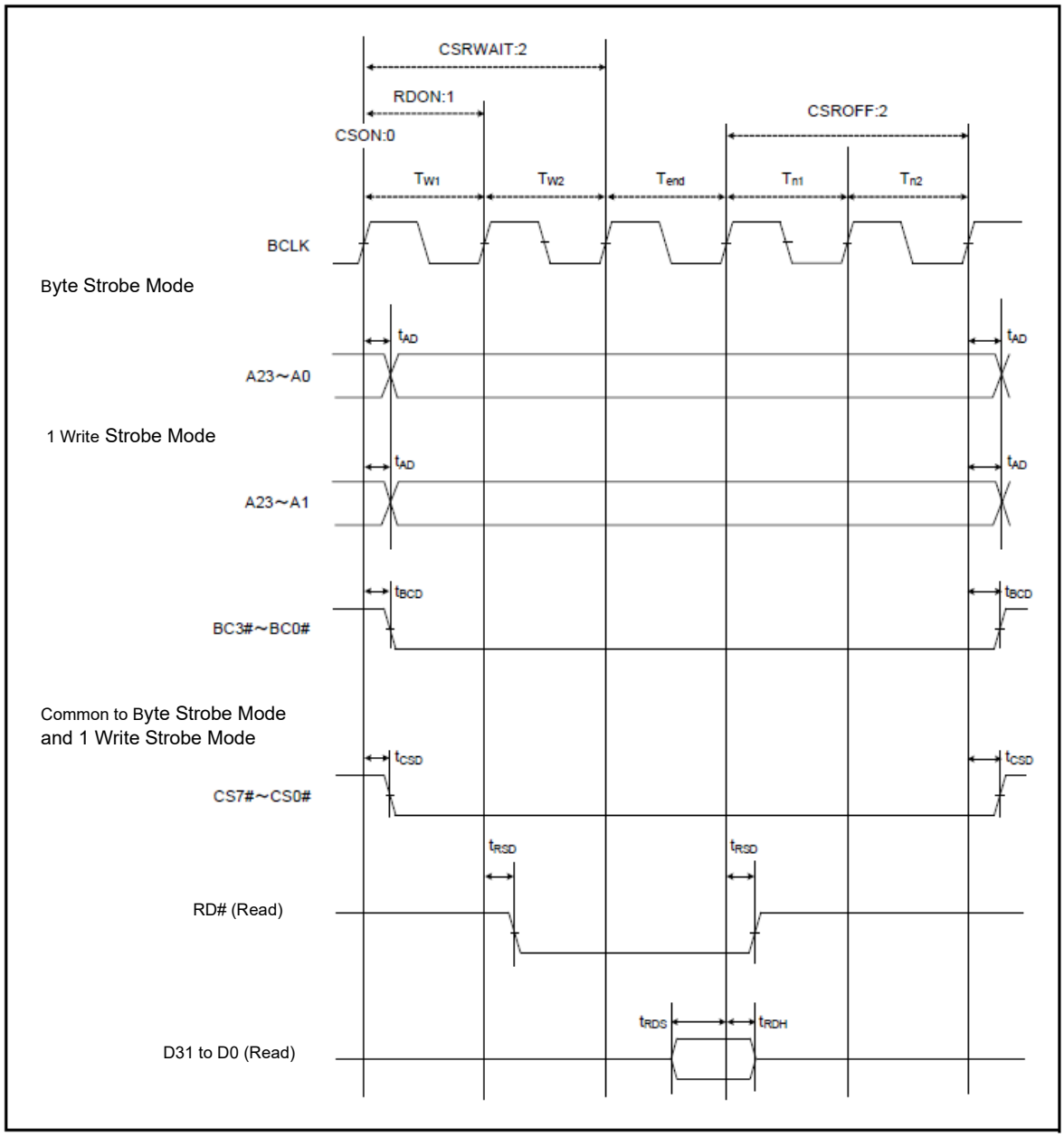
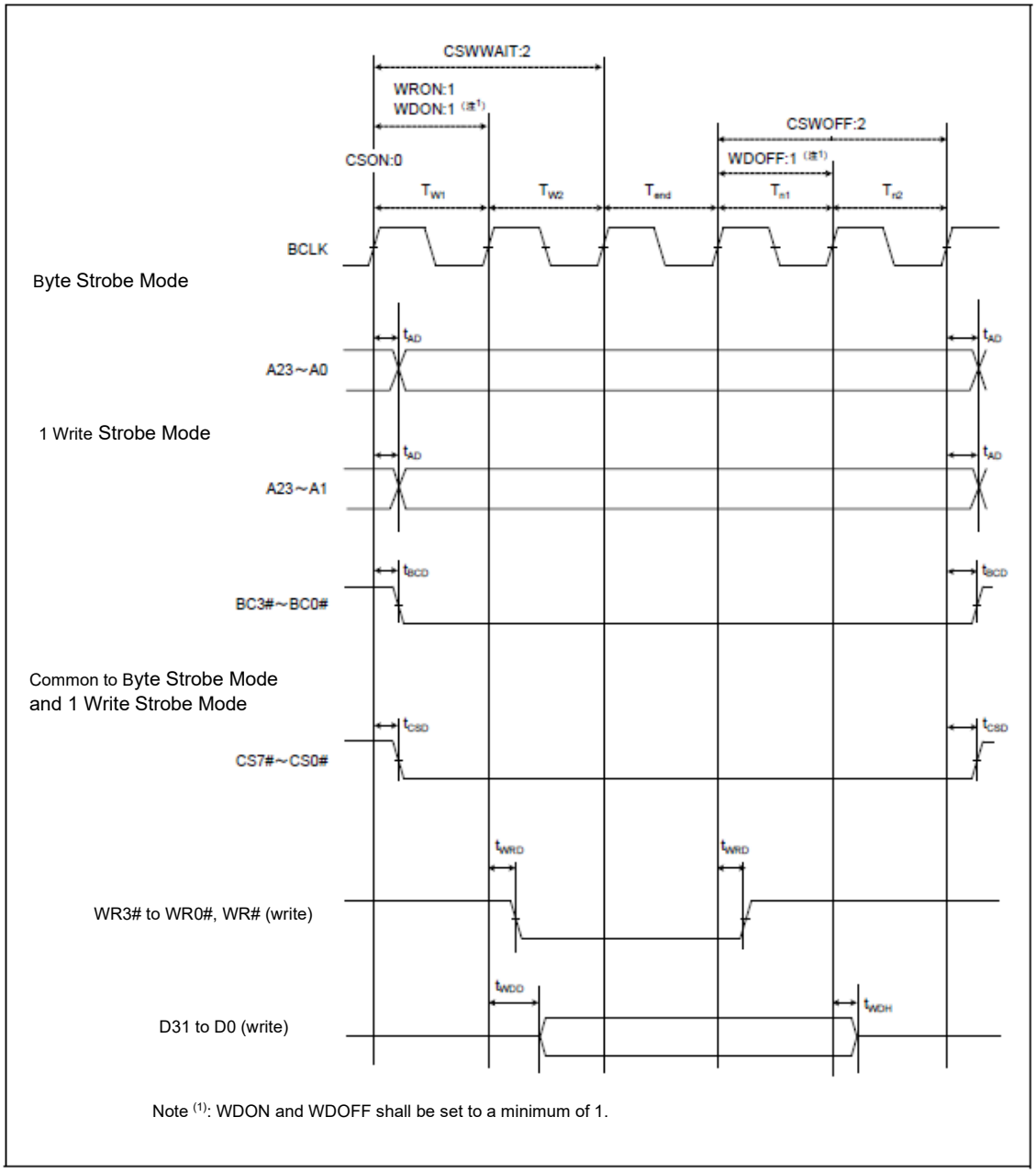


Figure 9. External Bus Timing / Normal Read Cycle (Bus Clock Synchronization)



Note (1): WDON and WDOFF shall be set to a minimum of 1.

Figure 10. External Bus Timing / Normal Write Cycle (Bus Clock Synchronization)

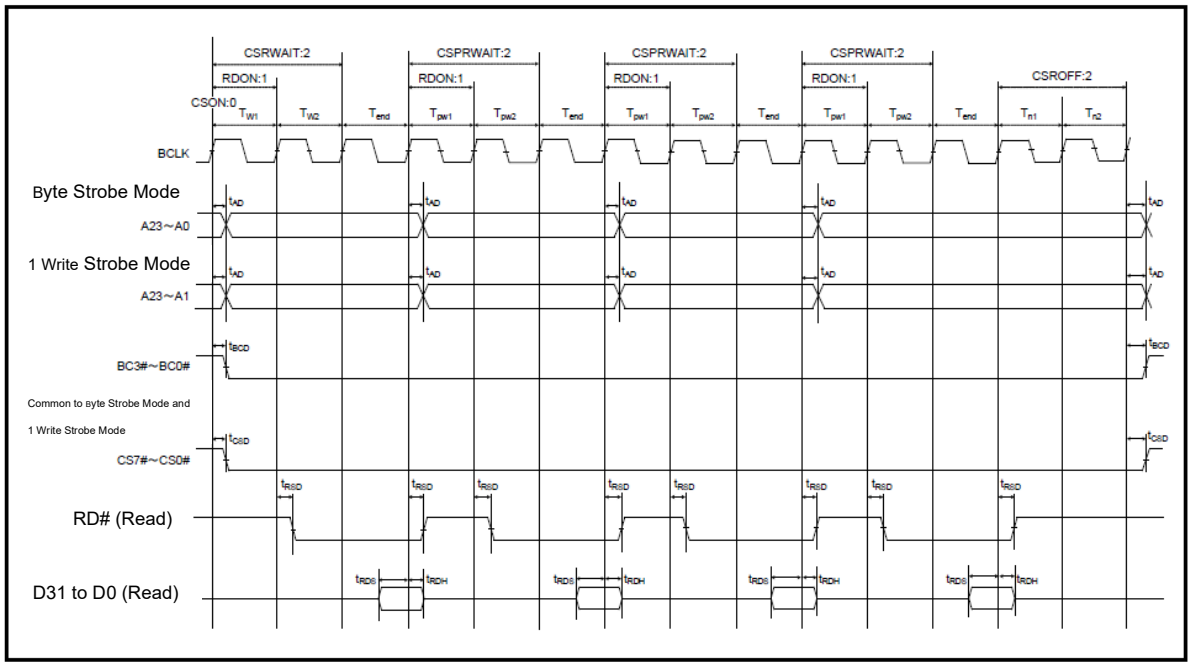
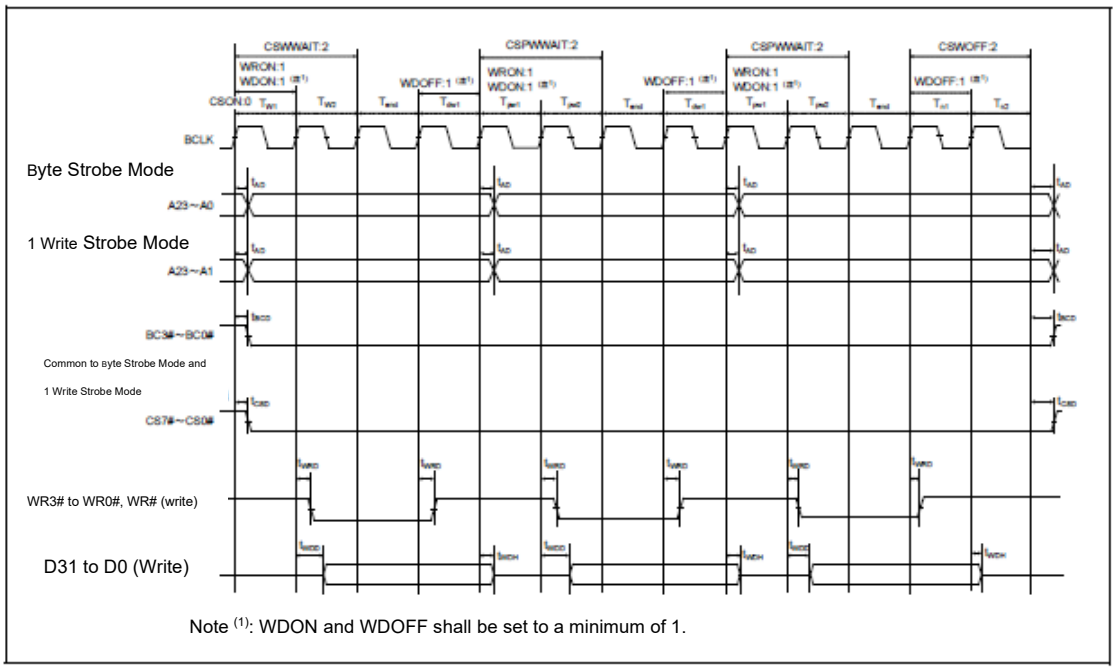


Figure 11. External Bus Timing / Page Read Cycle (Bus Clock Synchronization)



Note (1): WDON and WDOFF shall be set to a minimum of 1.

Figure 12. External Bus Timing / Page Write Cycle (Bus Clock Synchronization)

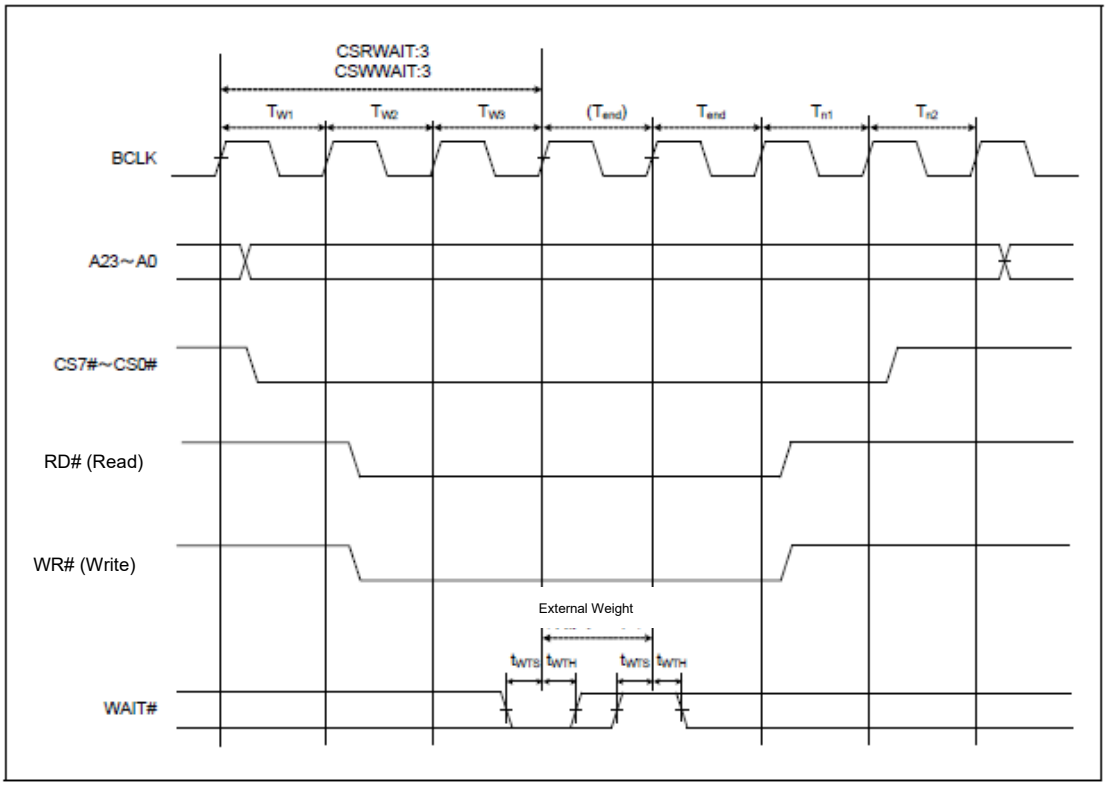
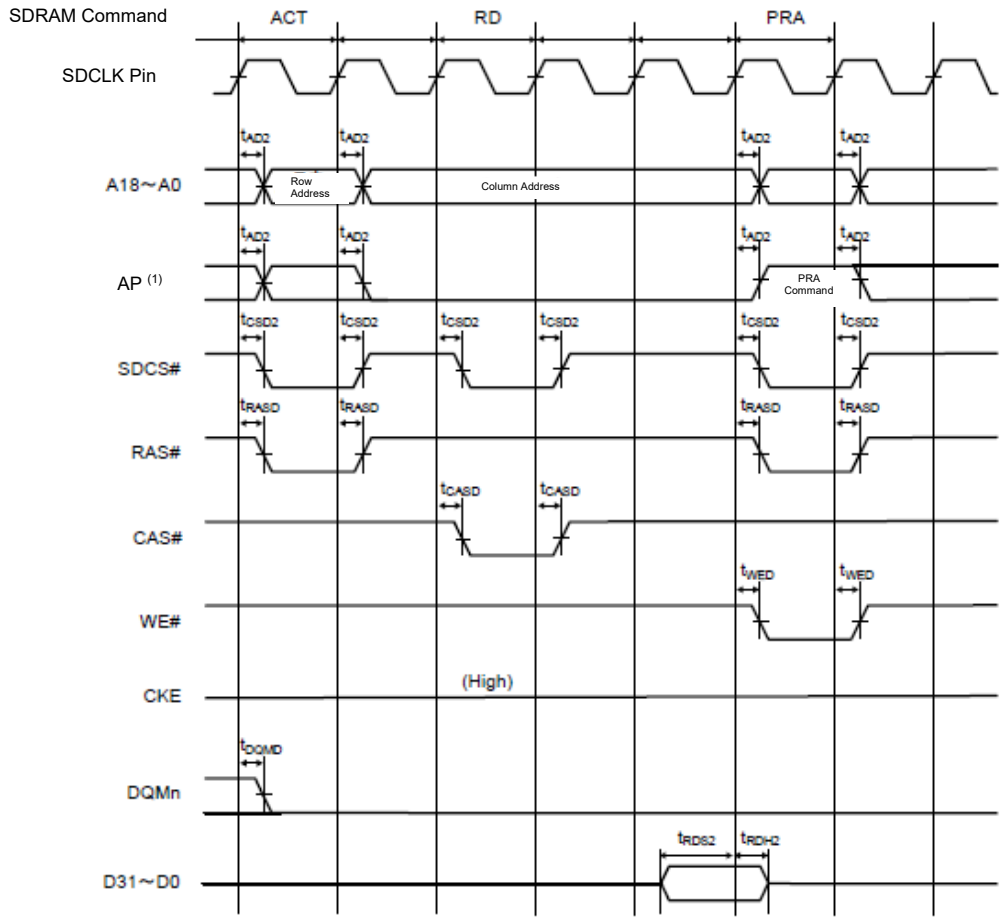
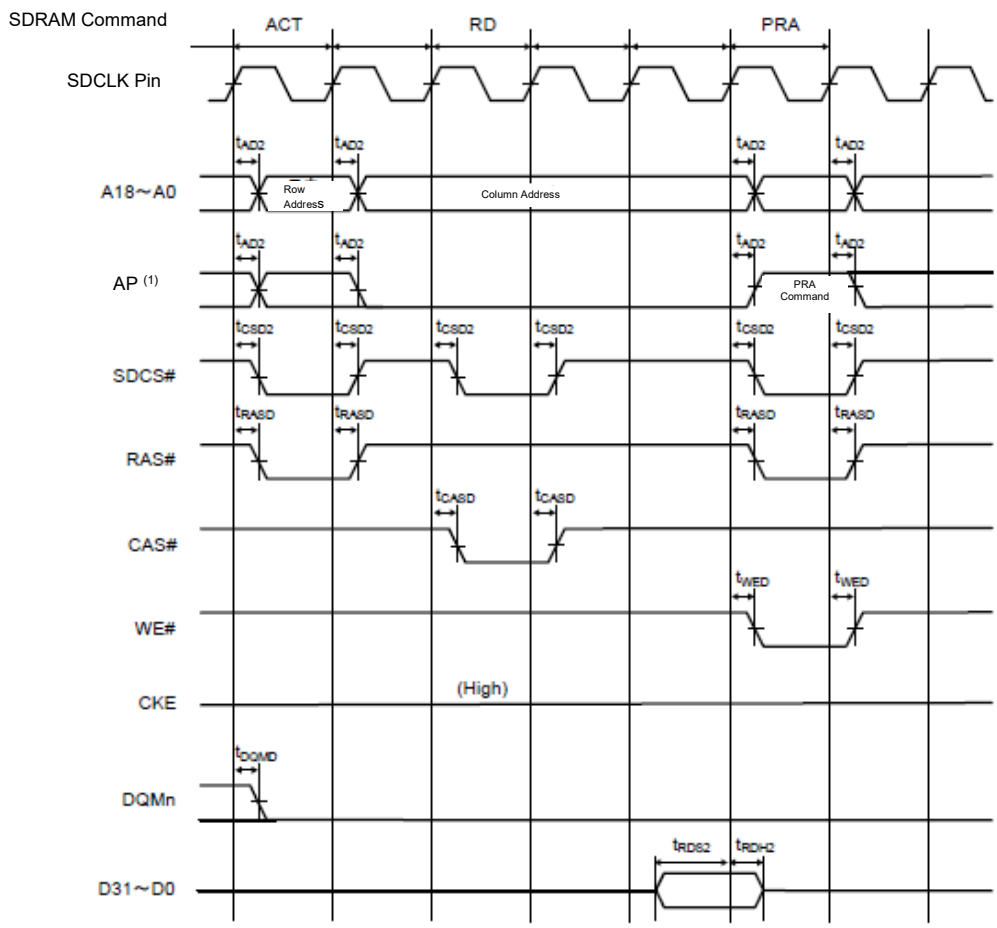


Figure 13. External Bus Timing / External Weight Control



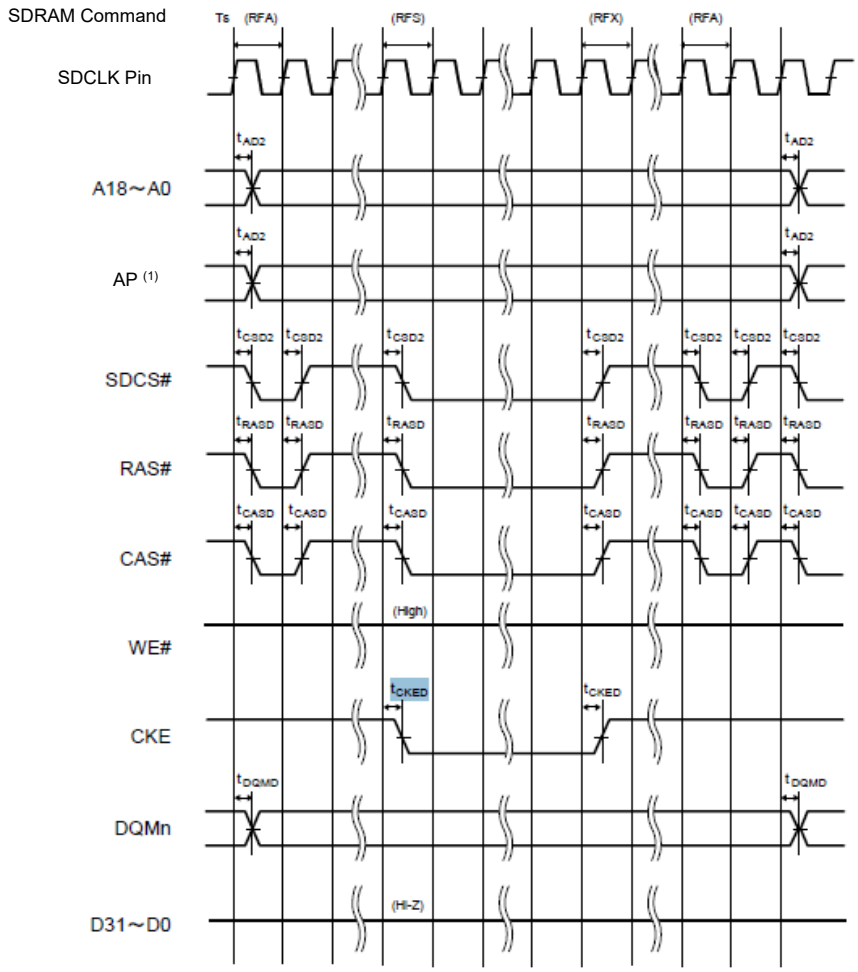
Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 14. SDRAM Space Single Read Bus Timing



Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 15. SDRAM Space Single Write Bus Timing



Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 16. SDRAM Space Self Refresh Bus Timing

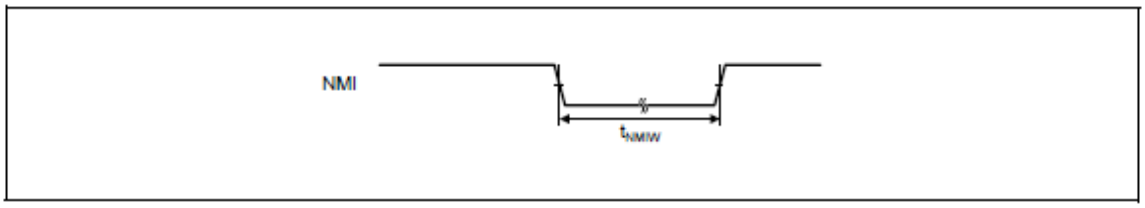


Figure 17. NMI Interrupt Input Timing

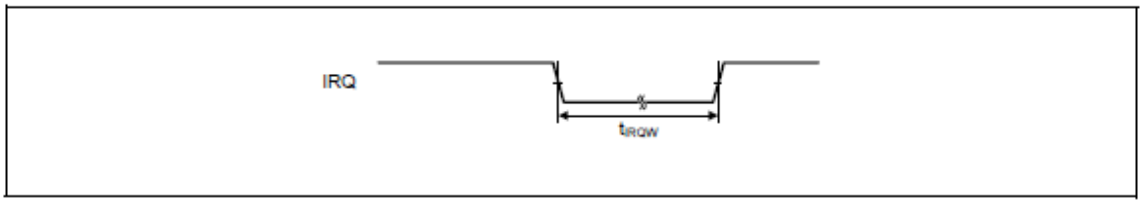


Figure 18. IRQ Interrupt Input Timing

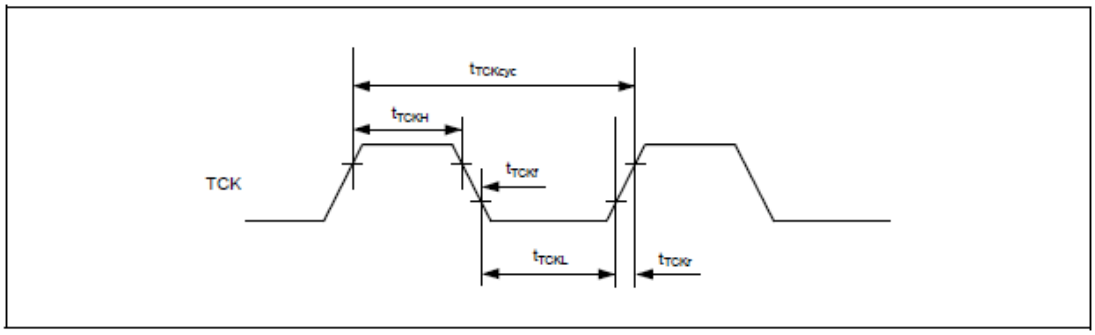


Figure 19. Boundary Scan TCK Timing

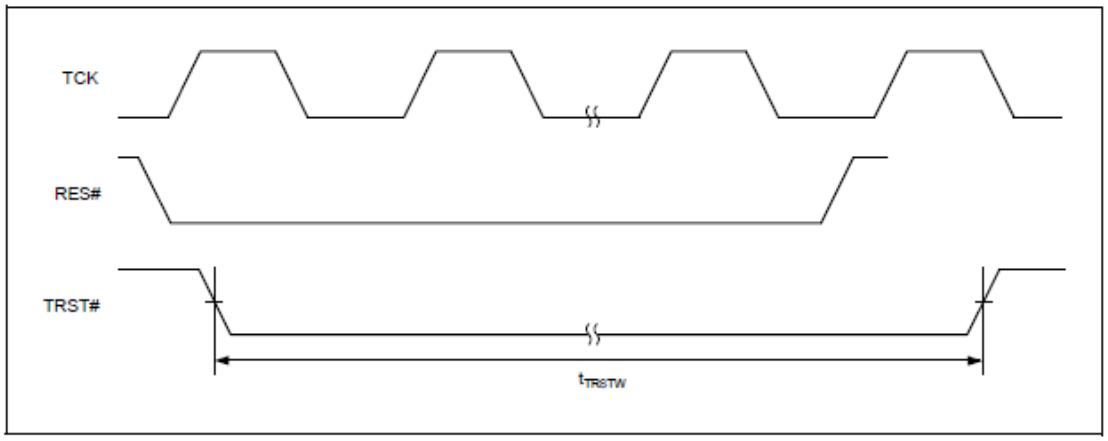


Figure 20. Boundary Scan TRST Timing

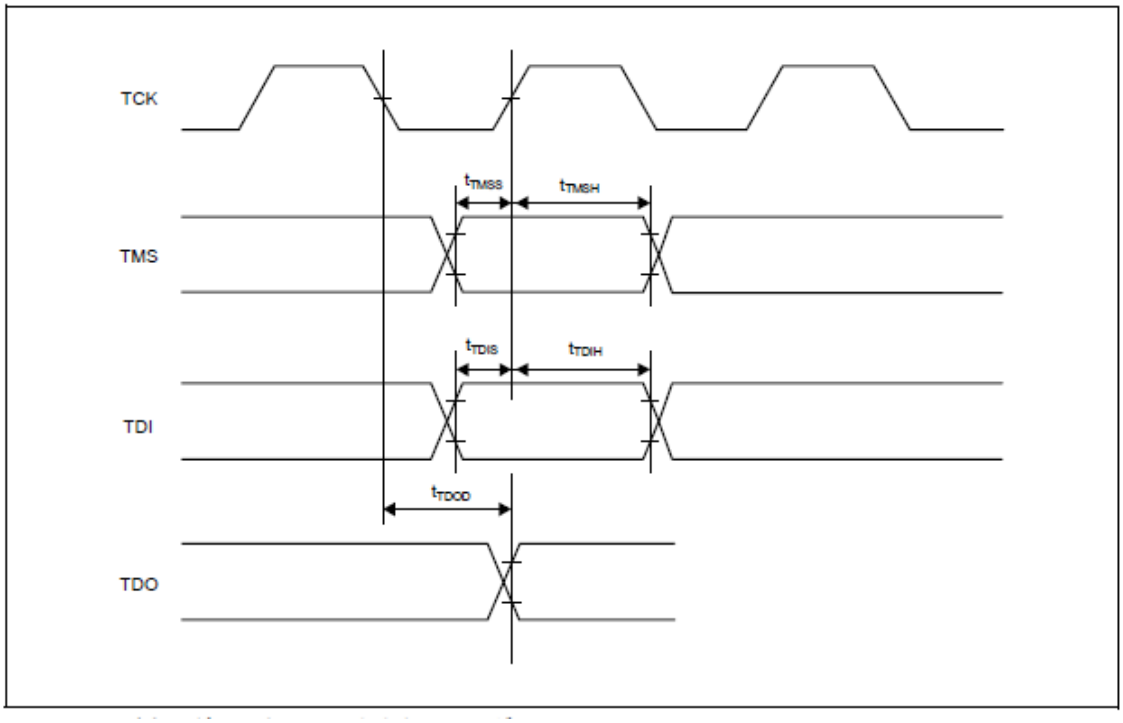


Figure 21. Boundary Scan Input and Output Timing

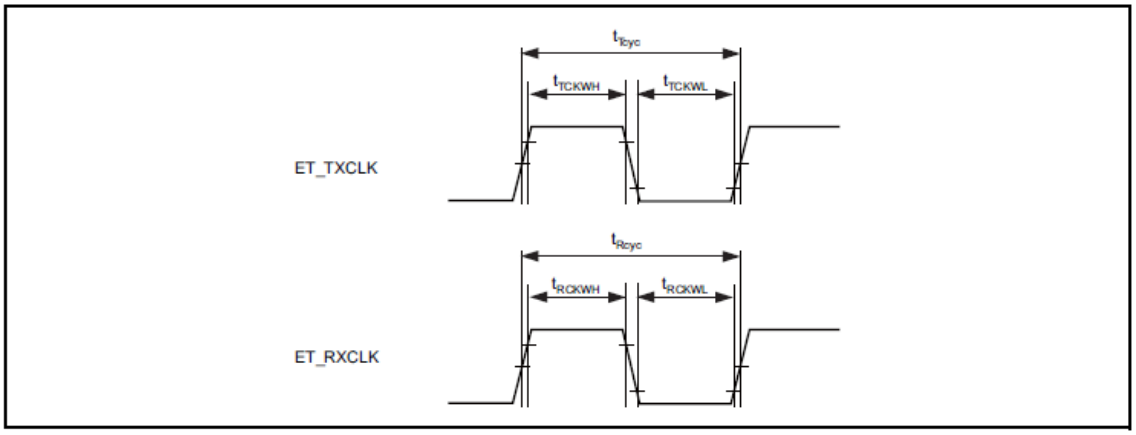


Figure 22. MII Clock Timing

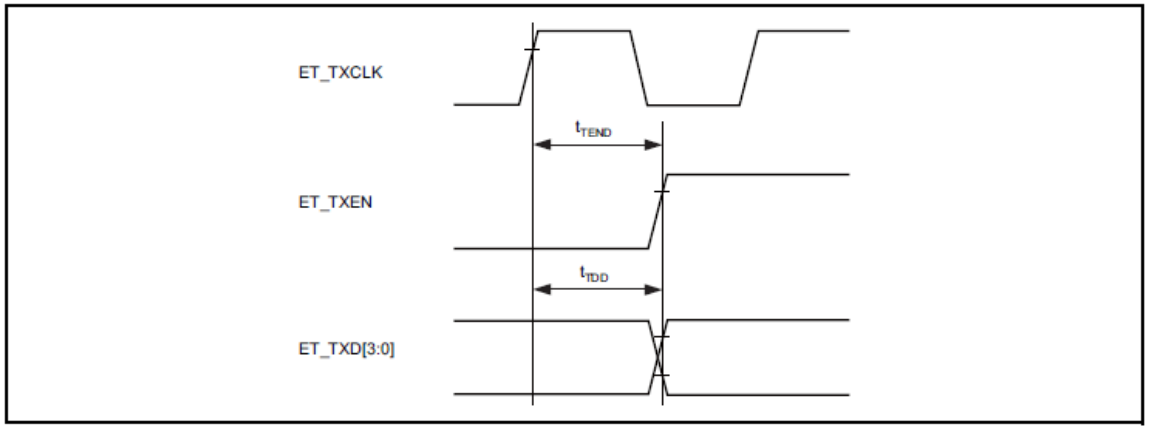


Figure 23. MII Transmission Data Timing

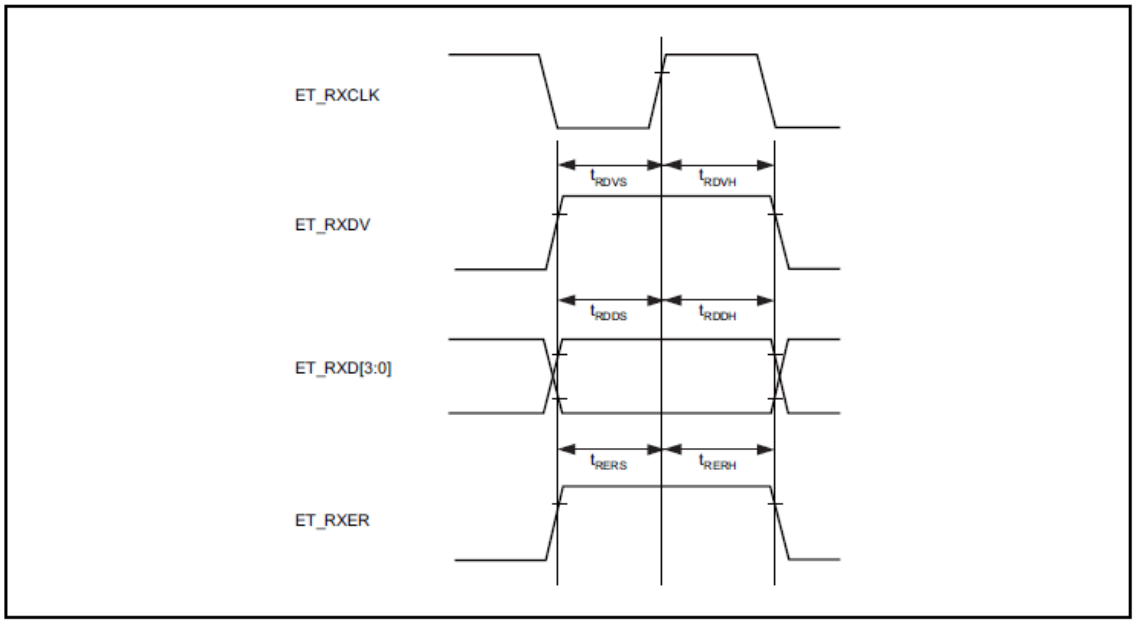


Figure 24. MII Receive Data Timing

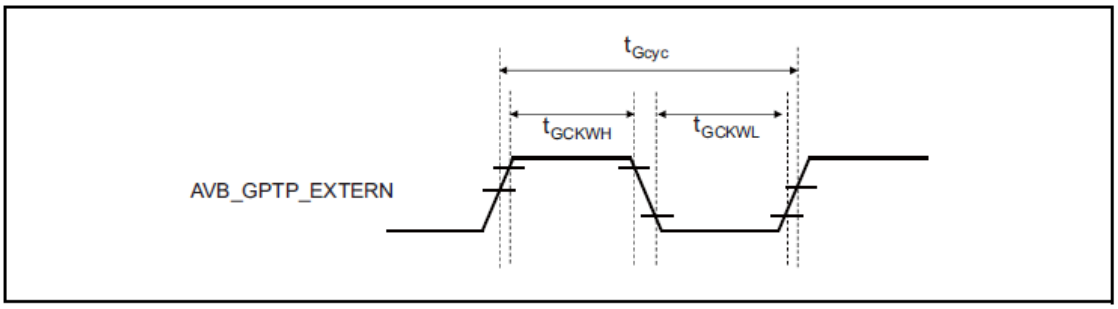


Figure 25. gPTP Timer External Clock Timing

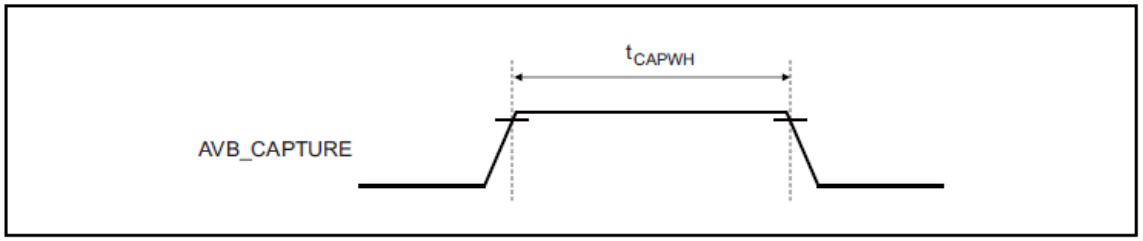


Figure 26. Timer Capture Signal Timing

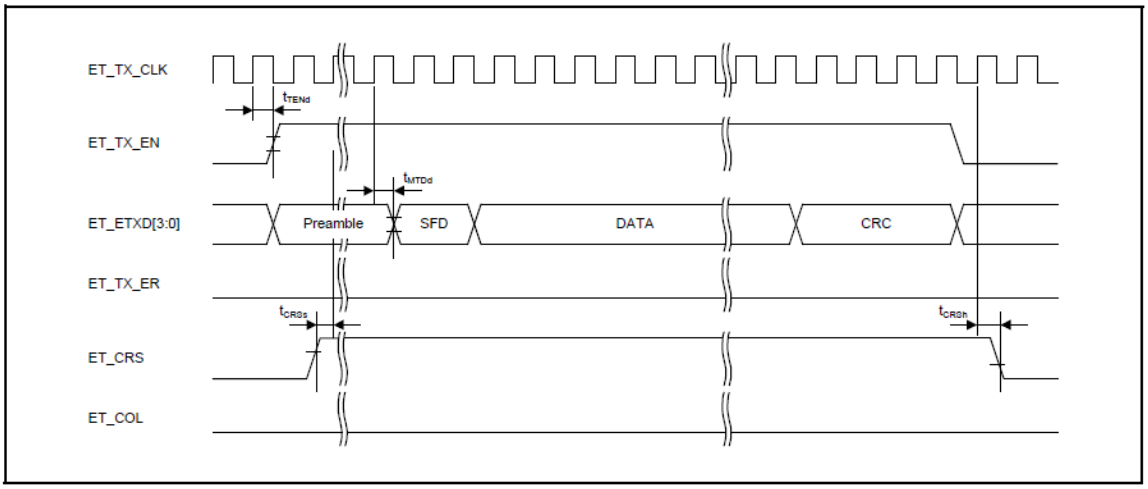


Figure 27. MII Transmission Timing (Normal Operation)

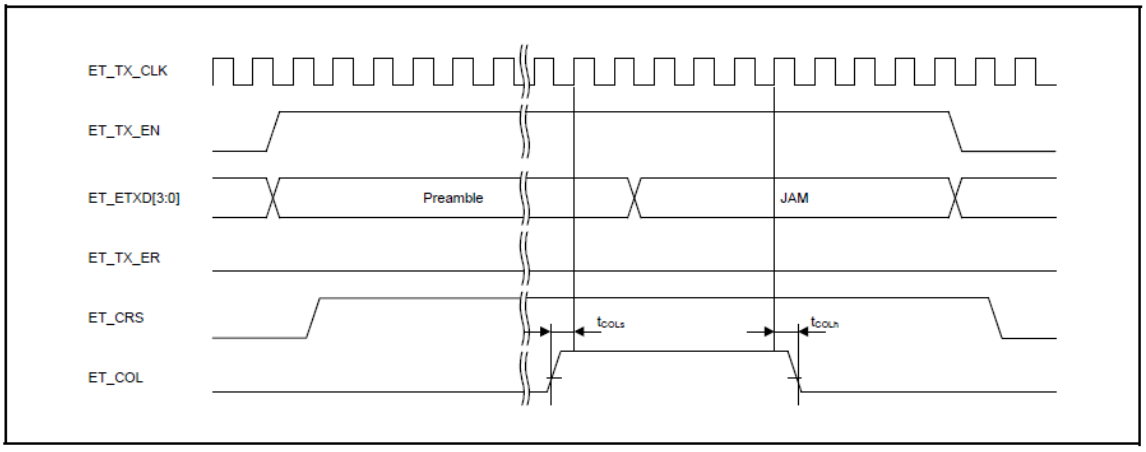


Figure 28. MII Transmission Timing (Collision Occurrence Case)

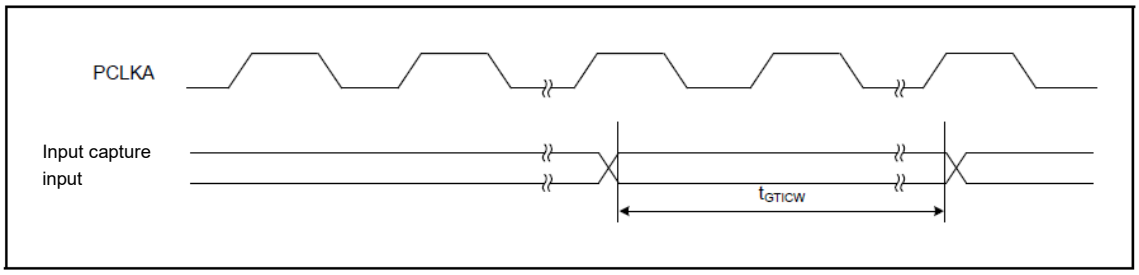


Figure 29. GPT Input Capture Input Timing

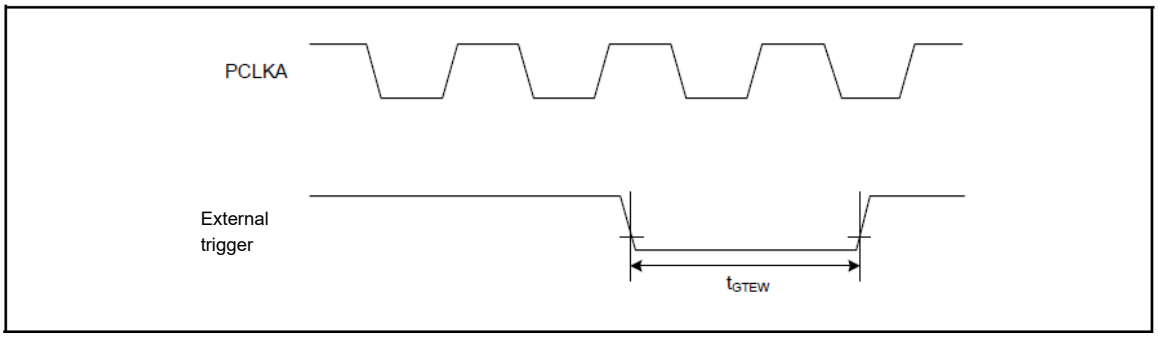


Figure 30. GPT External Trigger Input Timing

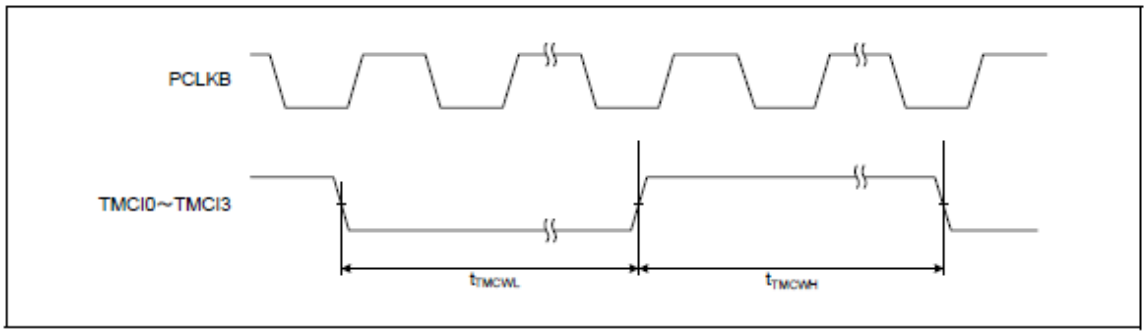


Figure 31. TMR Clock Input Timing

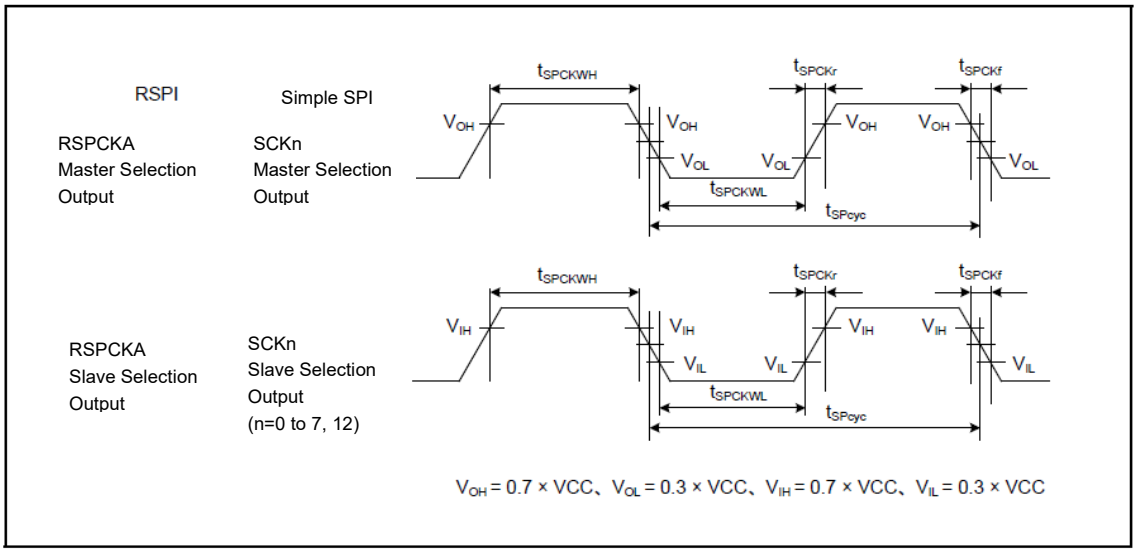


Figure 32. RSPI Clock Timing / Simple SPI Clock Timing

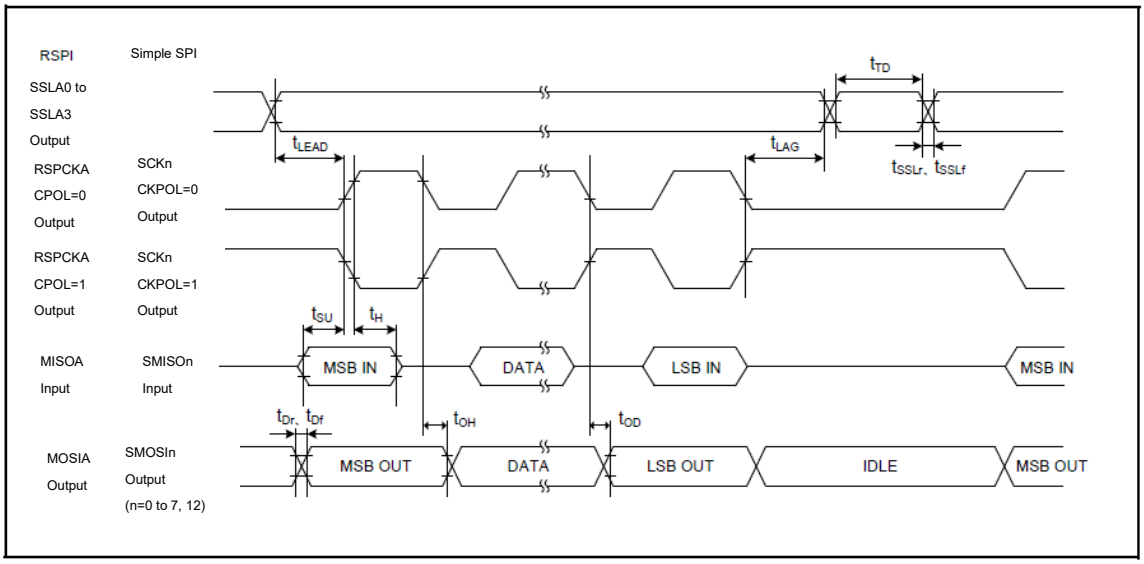


Figure 33. RSPI Timing (Master, CPHA=0)

(Bit rate: Set PCLK to a division factor other than 2) / Simple SPI Timing (Master, CKPH=1)

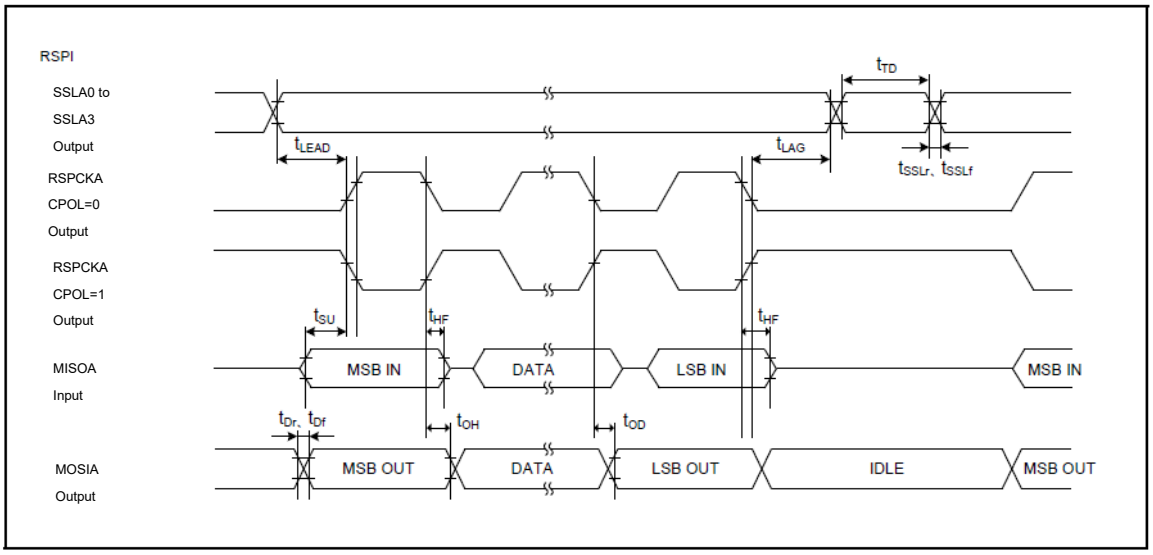


Figure 34. RSPI Timing (Master, CPHA=0)

(Bit rate: Set PCLK to a division factor 2)

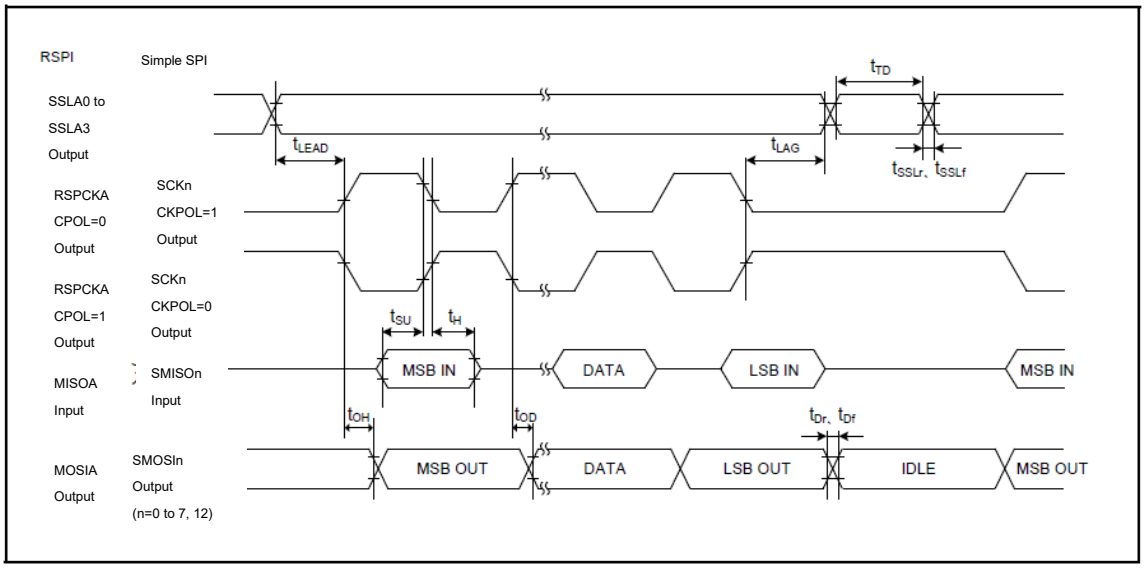


Figure 35. RSPI Timing (Master, CPHA=1)

(Bit rate: Set PCLK to a division factor other than 2) / Simple SPI Timing (Master, CKPH=1)

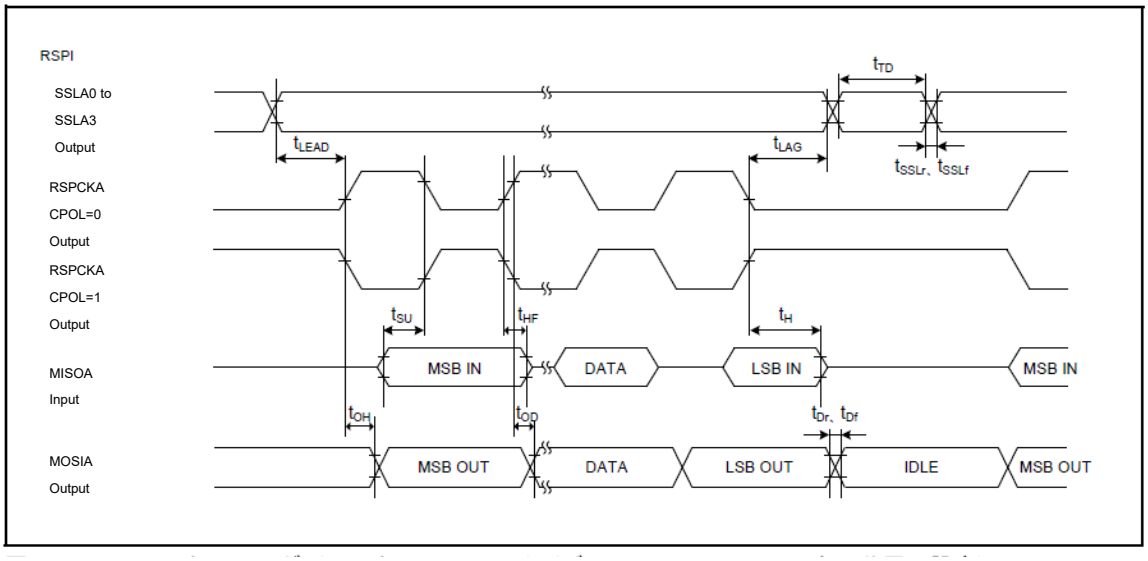


Figure 36. RSPI Timing (Master, CPHA=1)

(Bit rate: Set PCLK to a division factor 2)

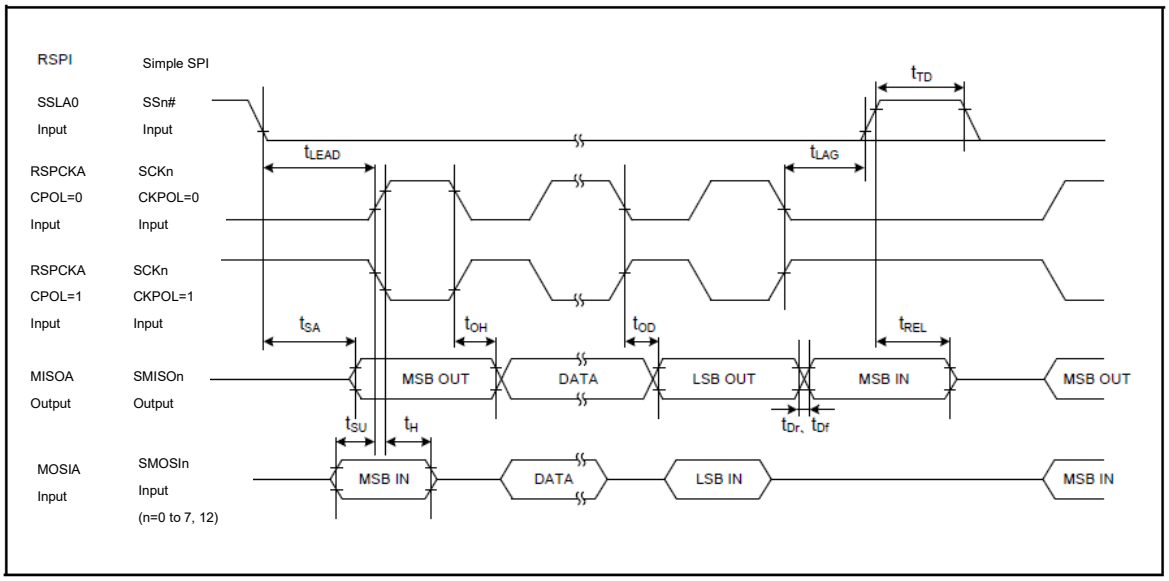


Figure 37. RSPI Timing (Slave, CPHA=0) / Simple SPI Timing (Slave, CKPH=1)

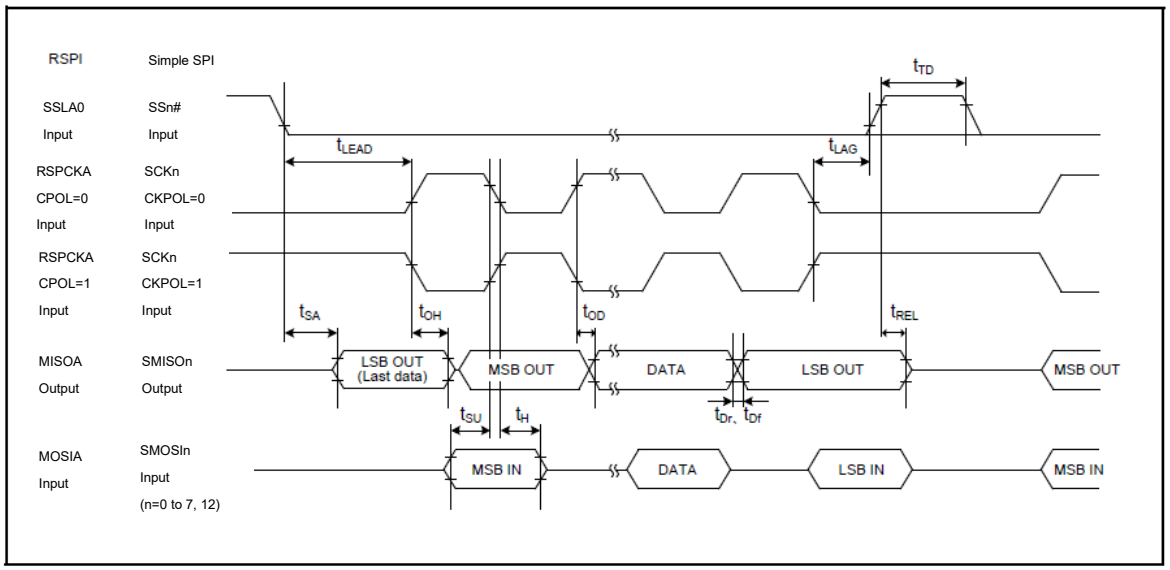


Figure 38. RSPI Timing (Slave, CPHA=1) / Simple SPI Timing (Slave, CKPH=0)

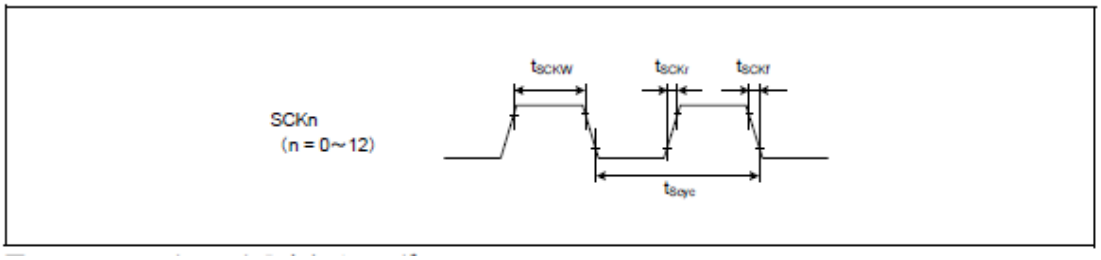


Figure 39. SCK Clock Input Timing

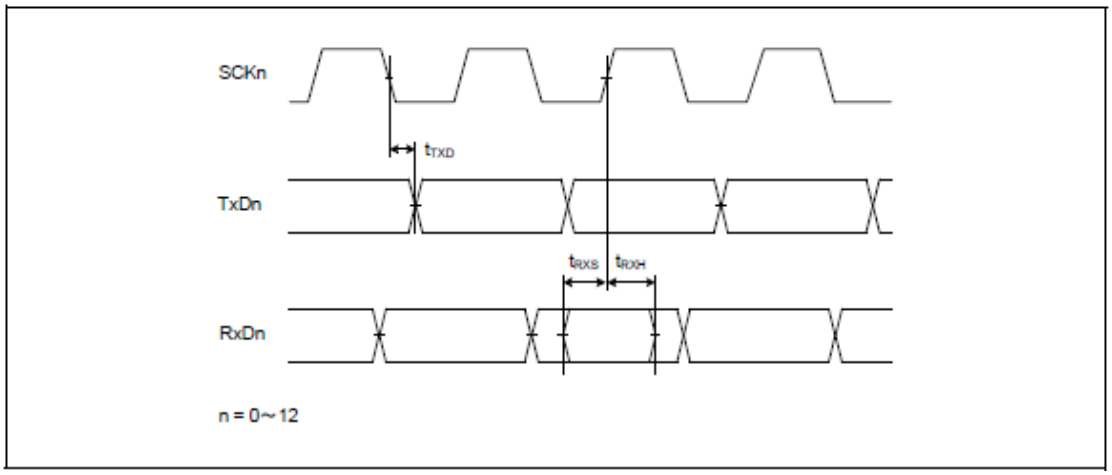


Figure 40. SCI Input and Output Timing / Clock-Synchronous Mode

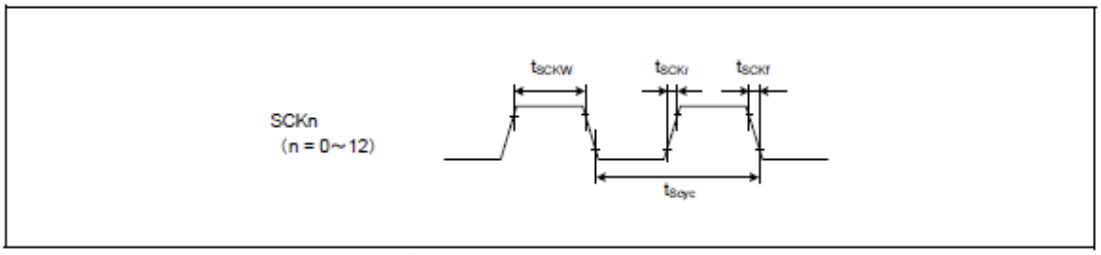


Figure 41. SCK Clock Input Timing

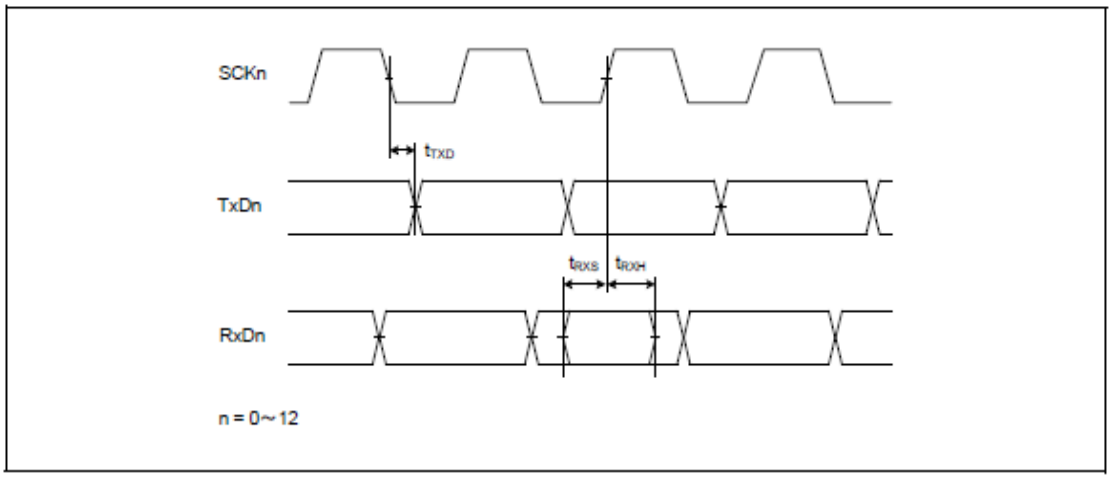


Figure 42. SCI Input and Output Timing / Clock-Synchronous Mode

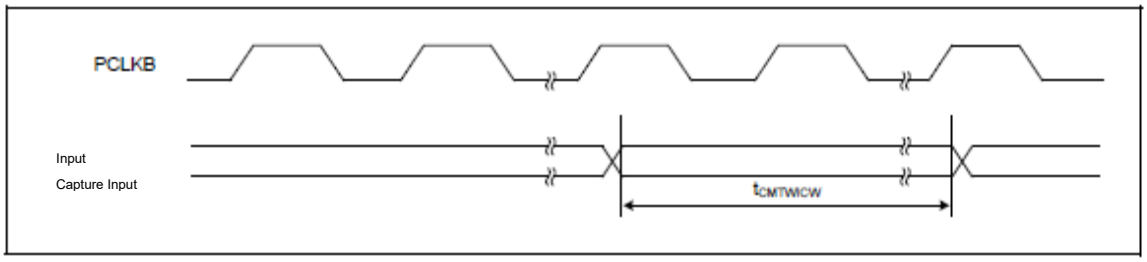
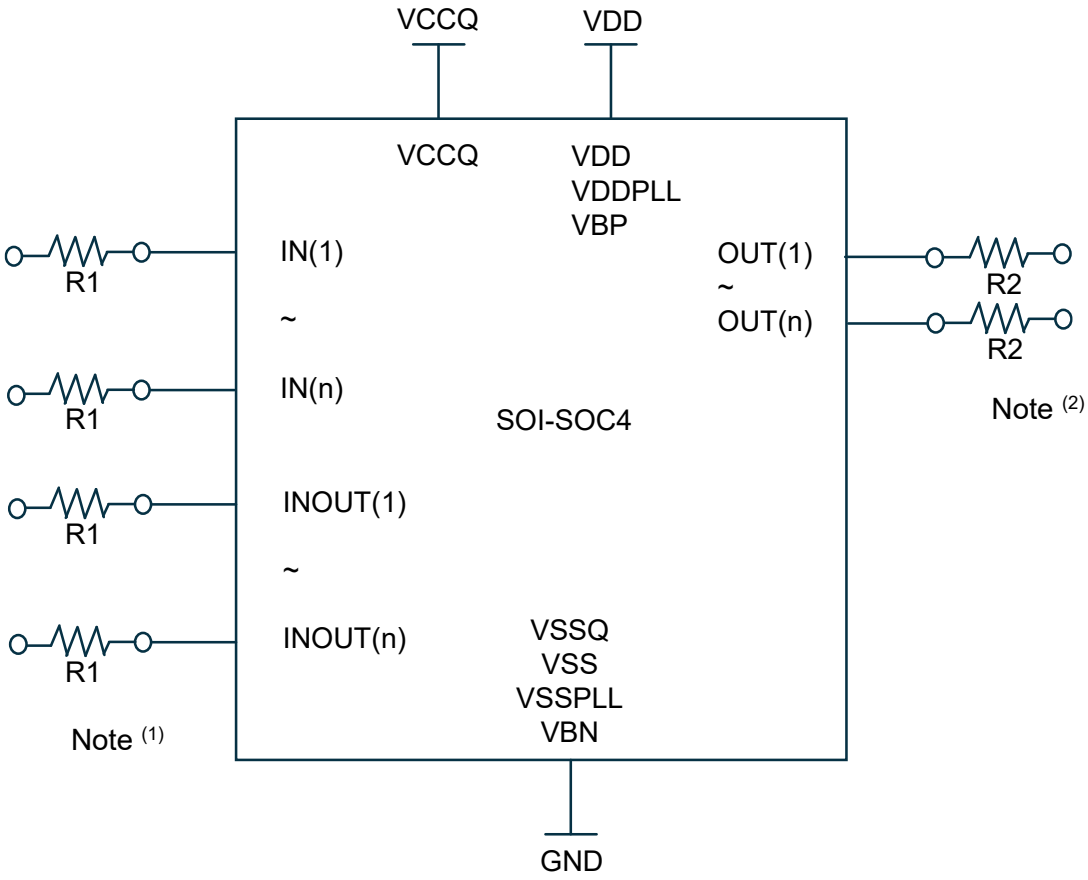


Figure 43. CMTW Input Capture Input Timing

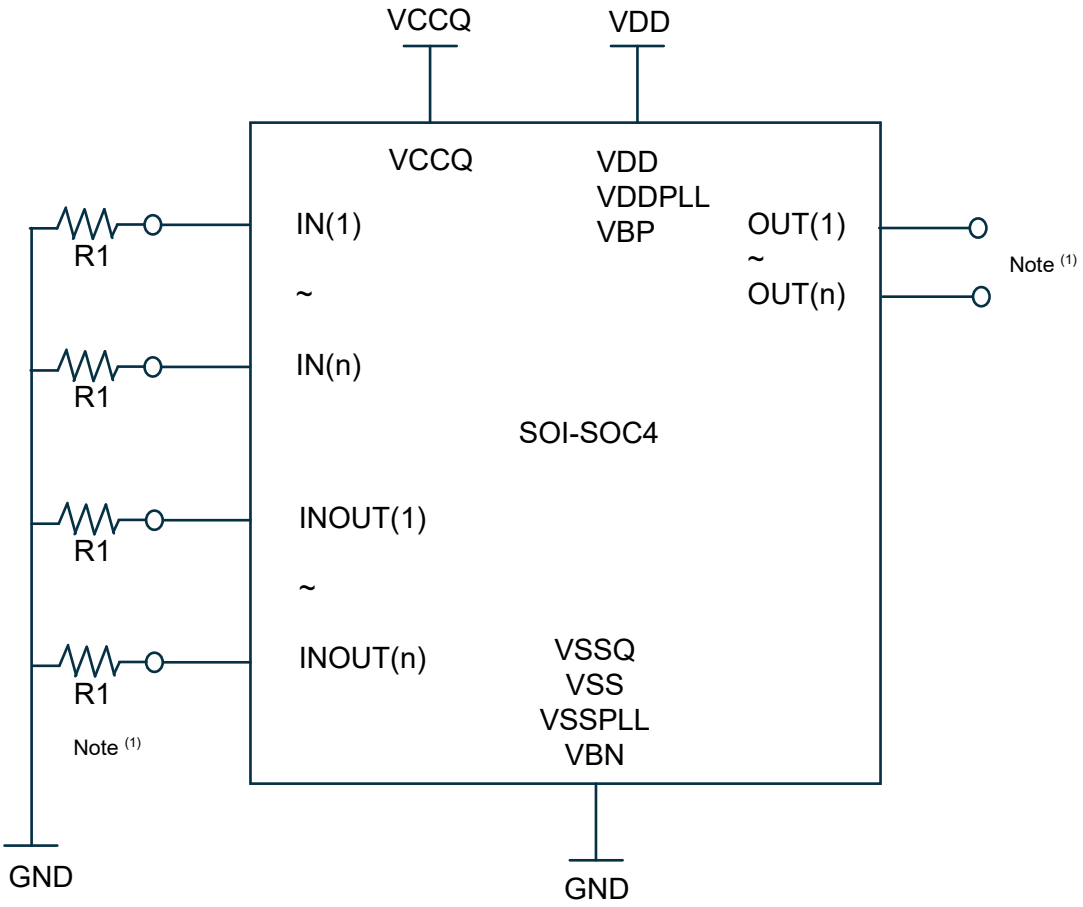


VCCQ: 3.6V (3)
VDD: 1.3V (3)
VIN: Test pattern (Set value)
VH=VCCQ±0.2V, VL=0.0V±0.2V
VOUT: Test pattern (Expected value)
VH=VCCQ±0.2V, VL=0.0V±0.2V
VIO: Test pattern (Input mode: set value,
Output mode: expected value)
VH=VCCQ±0.2V, VL=0.0V±0.2V
R1: 1kΩ
R2: 22Ω

Note (1): Unused input terminals shall be pulled down (resistance value: 10kΩ).
Note (2): Unused output terminals shall be open.
Note (3): The power supply voltage set value on the board in operation.

Figure 44. Burn-in and Steady State Life Test Circuit

VET25310



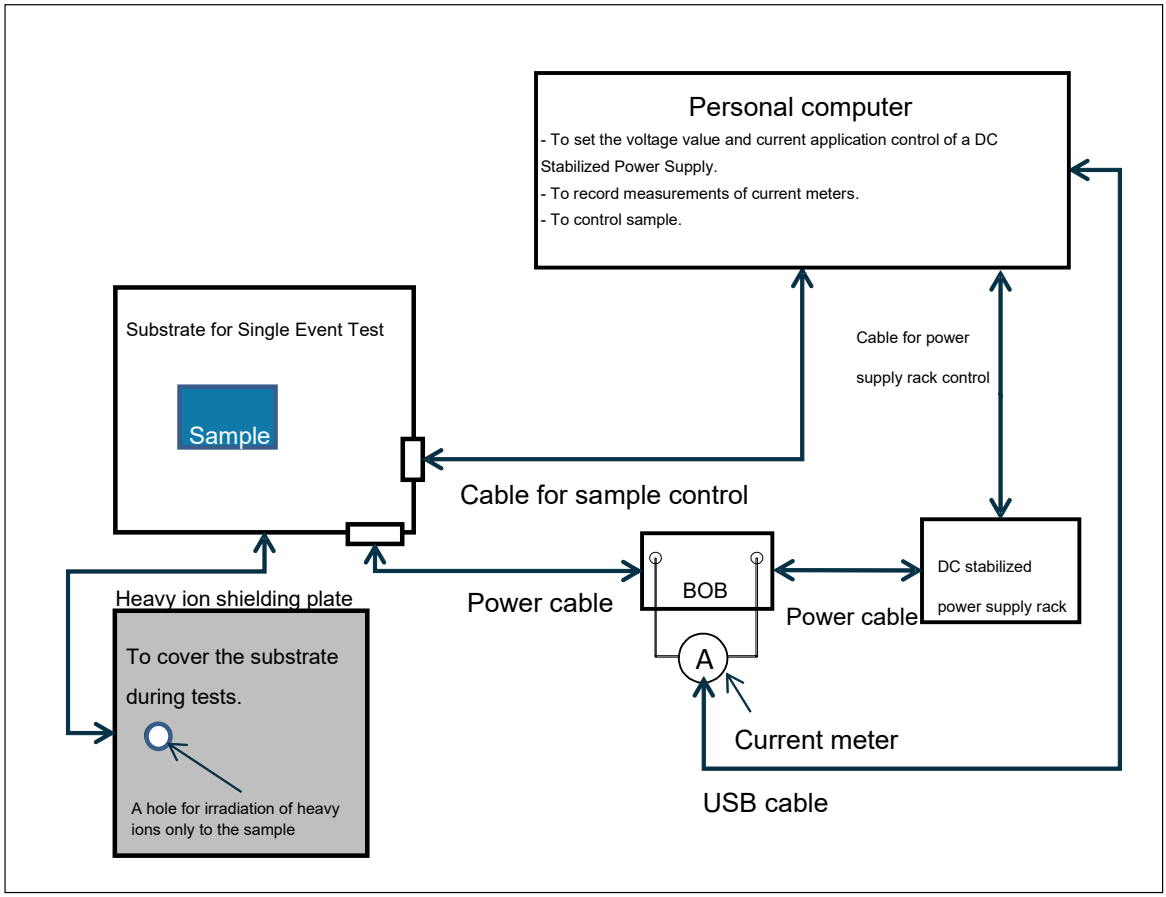
VCCQ:	3.6V (3)
VDD:	1.3V (3)
VSS, VSSQ:	GND
R1 (Pulldown resistor):	1kΩ
Operating condition:	Reset state (2), No lock supply

Note (1): Terminal treatment for IN/INOUT pins: Pulldown as shown in Table 6.
Terminal treatment for OUT pins: Open as shown in Table 6.

Note (2): In the reset state, all GPIO pins are set to be input pins, and all pins other than GPIO pins are set to be in high-Z state.

Note (3): The power supply voltage set value on the board in operation.

Figure 45. Steady State Total Ionizing Dose Test Circuit for Subgroup 1 of Group E Tests



Note: For power supply voltage in tests, refer to Table 17.

Figure 46. Single Event Test Circuit for Subgroup 2 of Group E Tests