Registration No.1265

JAXA-QTS-2140F 30 March 2023

Superseding JAXA-QTS-2140E Cancelled 30 March 2023

PRINTED WIRING BOARDS, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

JAXA JAPAN AEROSPACE EXPLORATION AGENCY This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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Revision	Date	Description
NC	25 Dec. 2001	Original
A	31 March 2004	
A	31 March 2004	(1) Revised to reflect the organizational change from NASDA to JAXA.
		(2) Clarified the contents of the provisions.
В	17 Nov. 2008	(1) Revised to reflect the revision of JAXA-QTS-2000 from revision B to revision C
		 Changed "NASDA***" to "JAXA***" in the part number definition.
		 Specified the part number for the transition to the QML certification system.
		(2) Appendix C
		Added the provision regarding lead-free surface finish
		(3) Other changes to clarify the requirements and to correct inconsistency.
		Paragraph 2.2:
		Reflected the change of document identification for JAXA Design Standard for Printed Wiring Boards and Assemblies NASDA-HDBK-8 → JERG-0-042
		Reflected the change of document identification for JAXA Parts Application Handbook. NASDA-HDBK-4 \rightarrow JERG-0-035
С	9 July 2009	(1) Added Printed wiring boards, CIC controlled thermal expansion, glass base woven polyimide resin base material (Appendix F).
		(2) Changes associated with the addition of Appendix F.
		(3) Other changes to correct errors.
D	14 Jan. 2014	(1) Added Printed wiring boards, Area array packaging (Appendix G) and some changes accompanied with the addition.
		(2) Others: Corrected errors.
E	2 April 2015	(1) Added Printed wiring boards for High Speed Signals (Appendix H) and some changes accompanies with the addition (main document)
		 (2) Clarified the test method of Terminal Pull Strength (Appendixes A through F)
		(3) Others; Corrected errors, etc.
F	30 March 2023	(1) Added Printed wiring boards, high heat radiation (Appendix J).
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Appendix C	ase Woven Epoxy Resin Base Mat	erial			
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Appendix E Rigid-Flex Printed Wiring Boards					
Appendix F Printed Wiring Boards, CIC Cont Base Material	rolled Thermal Expansion, Glass B	ase Woven Poly	imide Resin		
Appendix G Printed Wiring Boards, Area Arra	y Packaging				
Appendix H Printed Wiring Boards for High S	peed Signals				
Appendix J Printed Wiring Boards, High Hea	t Radiation				

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			<u> </u>	ļ
		PRINTED WIRING BOARDS,		
		HIGH RELIABILITY, SPACE USE,		
	(GENERAL SPECIFICATION FOR		
1. 0	GENERAL			
1.1	Scope			
	for space use high reliable wiring boards") used for e complies with JAXA-QTS Specification for) which w	shes the general requirements and lity, printed wiring boards (hereinaf electronic equipment installed on sp -2000 (Common Parts/Materials, S vas recently established to transitio m and replaces the following specif	ter referred to as bacecraft. This s bace Use, Gene n to the qualified	"printed pecification ral
	a) NASDA-QTS-1046A	Printed Wiring Boards, High Relia Specification for	bility, Space Use	, General
	b) NASDA-QTS-1047	Fine Pitch Printed Wiring Boards, General Specification for		
	c) NASDA-QTS-1051	Discrete Wiring Boards, High Relia Specification for		
	d) NASDA-QTS-1026A	Flexible Printed Wiring Boards, Hi General Specification for	gn Reliability, Sp	ace Use,
	e) NASDA-QTS-1066	Rigid-Flex Printed Wiring Boards, General Specification for	High Reliability,	Space Use,
1.2	Terms and Definitions			
	terminology shall be prov	used herein are as follows and as s ided in paragraph 6.3.	specified in JIS C	5603. The
	 a) Outgassing The gas released from the methods specified 	om a printed wiring board or its sub ed in ASTM E 595.	stance, which is	measured by
	 b) Workmanship The appearance and 	d conditions of finished products.		
1.3	.3 Classification			
	Products covered by this	specification are classified into the	types specified i	n Table 1.

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	Table 4 Classification		

Table 1. Classificat	ion
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Classification	Appendix	Previous QPL specification
Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	А	NASDA-QTS-1046A
Fine Pitch Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	В	NASDA-QTS-1047
Discrete Wiring Boards, Glass Base Woven Epoxy Resin Base Material	С	NASDA-QTS-1051
Printed Wiring Boards, Flexible, Polyimide Film Base Material	D	NASDA-QTS-1026A
Rigid-Flex Printed Wiring Boards	E	NASDA-QTS-1066
Printed Wiring Boards, CIC Controlled Thermal Expansion, Glass Base Woven Polyimide Resin Base Material	F	_
Printed Wiring Boards, Area Array Packaging	G	_
Printed Wiring Boards for High Speed Signals	н	_
Printed Wiring Boards, High Heat Radiation	J	

1.4 Part Number

The part number shall be in accordance with paragraph A.3.1.4 of JAXA-QTS-2000. The details shall be in accordance with the detail specification.

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents

The documents listed below form a part of this specification as specified herein. These documents are the latest issues available at the time of contract award or application. If it is necessary to designate an issue, the issue shall be specified in the detail specification.

a) JAXA-QTS-2000	Common Parts/Materials, Space Use, General Specification for
b) JIS C 5603	Terms and Definitions for Printed Circuits
c) MIL-STD-202	Test Method Standard, Electronic and Electrical Component
	Parts
d) IPC-4101	Specifications for Base Materials for Rigid and Multilayer Printed
	Boards
e) IPC-SM-840	Qualification and Performance of Permanent Solder Mask
f) A-A-113	Tape, Pressure-Sensitive Adhesive
g) ASTM E595	Standard Test Method for Total Mass Loss and Collected Volatile
	Condensable Materials from Outgassing in a Vacuum
	Environment
h) SAE-AMS-QQ-N-290	Nickel Plating (Electrodeposited)
i) JIS C 5012	Test Methods for Printed Wiring Boards
j) JIS Z 9015-1	Sampling Procedures for Inspection by Attributes - Part 1:
	Sampling Plans Indexed by Acceptable Quality Level (AQL) for
	Lot-by-Lot Inspection

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	I) JPCA/NASDA-SCL01m) IPC-4203n) IPC-4204	Printed Wiring Bo Materials for, Det Adhesive Coated Flexible Printed C	e Adhesive Cellop ards, High Reliab ail Specification fo Dielectric Films fo Circuitry and Flexib ad Dielectrics for U	ility, Space Use, or or Use as Cover S ole Adhesive Bon	Sheets for ding Films
2.2	 b) JERG-0-0035 c) IPC-2221 d) IPC-2222 e) IPC-2223 f) IPC J-STD-004 g) IPC J-STD-006 	JAXA Design Sta JAXA Parts Appli Generic Standard Sectional Design Sectional Design Requirements for Requirements for	nents. ndard for Printed ¹ cation Handbook I on Printed Board Standard for Rigio Standard for Flex Soldering Fluxes Electronic Grade Solders for Electr	l Design d Organic Printed ible Printed Board Solder Alloys and	l Boards ds d Fluxed and
2.3	Order of Precedence In the event of a conflict documents, the following a) Detail specification b) This specification c) JAXA-QTS-2000 d) Applicable documen 2000)	between the text order of precede	of this specification nce shall be appli	n and the applica ed.	ble
2.4	Detail Specification Detailed requirements for in each detail specification The detail specification s accordance with paragra be registered and issued to as 'JAXA').	on. hall be prepared ph A.4 of JAXA-C	and implemented TS-2000. The de	by a manufacture stailed specification	er in on shall also
2.4.1	1 Detail Specification Number The detail specification number shall be indicated in the following form in accordance with paragraph A.2.2.2 of JAXA-QTS-2000. The individual identification shall be a three digits number and the first digit represents the QML manufacturer and the remaining two digits are a series number.				
	Example: <u>JAXA-QTS-2</u> This specific number	ation Appen		A T Revision letter	

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2.4.2	Revision Letter of the D A revision letter in the d paragraph A.2.2.2.4 of .	etail specification number shall be	assigned in acco	ordance with
2.4.3	Independency of Detail The detail specification accordance with paragr	shall be a stand-alone document v	vith a unique nun	nber in
2.4.4	•	cation format shall be in accordance with ecify each requirement in accordar		,
3. RE	EQUIREMENTS			
3.1	Certification			
3.1.1	Qualification Coverage Qualification coverage s specifications.	hall be as specified in the append	ixes and the deta	il
3.1.2	a manufacturer shall es paragraph 3.2.1 of JAX/ paragraph 4.4 of this sp specified in paragraph 3	of the printed wiring board in comp ablish a quality assurance program A-QTS-2000, perform the qualificat ecification, and acquire a certificat 3.4.1 of JAXA-QTS-2000. The ma rer List of the Japan Aerospace E	m in accordance tion tests specifie ion status from J nufacturer shall b	with ed in AXA as e listed on
3.1.3	manufacturer must appl 3.4.2.1 of JAXA-QTS-20 date of the certification If products were not shi conformance inspection	n rinted wiring boards in accordance y for retention of certification in ac 000 commencing between 30 and period (paragraph 3.1.4). oped during the effective period of was not conducted, the manufact ducting the quality conformance in	cordance with pa 60 days prior to t certification and urer may apply fo	ragraph he expiratior a quality
3.1.4	Effective Period of Certi The effective period of c three (3) years.	fication ertification granted in compliance	with this specifica	ation shall be

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3.1.5 Change of Quali	ation Coverage	•	•

To change the qualification coverage, the manufacturer shall perform procedures for requalification in accordance with paragraph 3.4.3 of JAXA-QTS-2000.

3.2 Quality Assurance Program

3.2.1 Establishment of a Quality Assurance Program

To acquire certification in compliance with this specification, the manufacturer shall be responsible for establishing a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall generate a quality assurance program plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to JAXA for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.

3.2.2 TRB Formation

To acquire a certification status in compliance with this specification, the manufacturer shall form and operate the Technical Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.

3.3 Materials

Materials used in the printed wiring boards shall be as specified herein. When definite materials are not specified in this specification, materials shall be used which meet the requirements of this specification and shall be specified in the document defining the manufacturing conditions of the quality assurance program.

3.3.1 Outgassing

The outgassing test shall be performed in accordance with ASTM E 595 as part of the qualification test or when the materials are changed. The following outgassing data shall be specified in the application data sheet (ADS).

- a) Total Mass Loss (TML)
- b) Collected Volatile Condensable Materials (CVCM)

3.4 Design and Construction

The design and construction shall be as specified in appendixes. The detail requirements such as circuit dimensions and layer structure shall be specified in the detail specification.

3.5 Externals, Dimensions, Marking and OthersThe externals, dimensions, marking and others shall be as specified in appendixes.

3.6 Workmanship

The workmanship of the printed wiring boards shall be as specified in the appendixes.

3.7 Electrical PerformanceRequirements on the electrical performance shall be as specified in the appendixes.

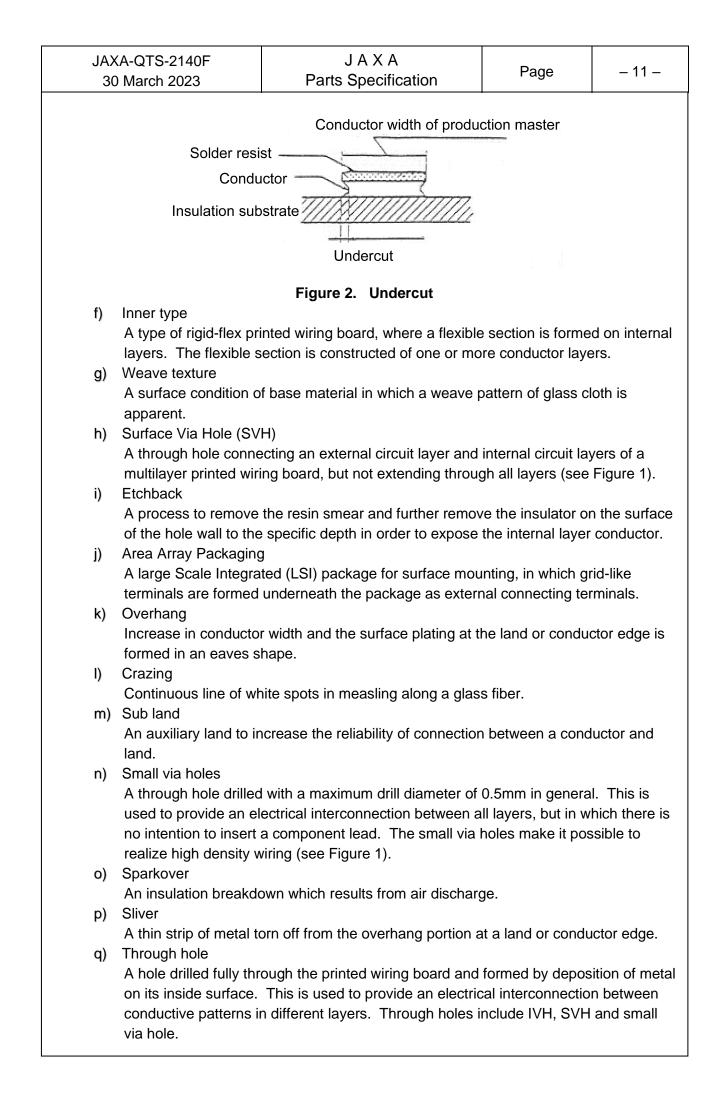
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3.8 Mechanical Performance Requirements on the mechanical performance shall be as specified in the appendixes.					
3.9	3.9 Environmental Performance				
	Requirements on the environmental performance shall be as specified in the appendixes.				
4. C	QUALITY ASSURANCE PR	OVISIONS			
4.1	General Requirements				
		e responsible for implementing the of this specification and operating		e program	
4.2	Classification of Tests and	Inspections			
	The tests and inspections accordance with paragrapa) In-process inspectionb) Qualification testc) Quality conformance		ng three categorie	es in	
4.3	 In-Process Inspection The manufacturer shall perform the following in-process inspections during the manufacturing process to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize properties which cannot be measured using the finished products. The manufacturing flowchart in the quality assurance program plan shall define the inspection process. a) Internal visual inspection of semi-finished products (100% or sampled inspection for non-destructive inspection) b) Physical and chemical inspection of semi-finished products (destructive or non-destructive, 100% or sampled inspection) c) Characterization of semi-finished products (100% or sampled inspection for non-destructive inspection) 				
4.4	Qualification Test				
4.4.1	process and control as	factured in accordance with the maspecified in the quality assurance p ge. The details shall be in accorda	programs and sha	all also typify	
4.4.2	certification, receiving ir	h intends to acquire certification st spection data or test data of mate ration, and in-process inspection o equest.	rials used, work i	records	

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4.4.3	Test Items and Sample	Size		
	Test items, order of test appendixes.	s and number of samples shall be	as specified in th	ie
4.4.4	Criteria for Pass/Fail			
A failure of any test specified in the appendixes shall constitute failure of the qualification tests. If the failure mode of the defectives is catastrophic such as open or short circuit where the function of the printed wiring board might be lost, the printed wiring board fails the qualification test.				
4.4.5	Disposition after Tests			
	same inspection lot that passed the Group A qua qualification test, the ma manufacturing processe action has been taken, t	e qualification test shall not be deli have passed the qualification test ality conformance inspections. If a anufacturer shall review applicable is and take corrective actions on the he qualification tests specified in e JAXA has the authority to determined.	may be delivered sample fails to p materials and/or nem. After the co each appendix sh	d if they bass the prrective ball be
4.5 C	Quality Conformance Insp	ection		
4.5.1	Quality Conformance In All products shall be sul	spection (Group A) ojected to the Group A inspections	s at the time of pr	oduction.
4.5.1.1	Sample			
4.0.1.1	•	mitted for the Group A inspection	shall be as speci	fied in the
4.5.1.2	Inspection Items and	Sample Size		
	The inspection items, the appendixes.	number of samples and test orde	r shall be in acco	rdance with
4.5.1.3	Criteria for Pass/Fail			
	constitute failure of th catastrophic such as board might be lost, t	a the Group A inspections specified e Group A inspections. If the failu open or short circuit where the fun he printed wiring board fails the G ordance with the appendixes.	re mode of the d	efectives is ed wiring
4.5.1.4	Disposition after Insp	ections		
	The lots rejected in th	e Group A inspection shall not be	delivered.	
4.5.2	Quality Conformance In	spection (Group B)		
		I be performed for the first product en no products were manufactured		

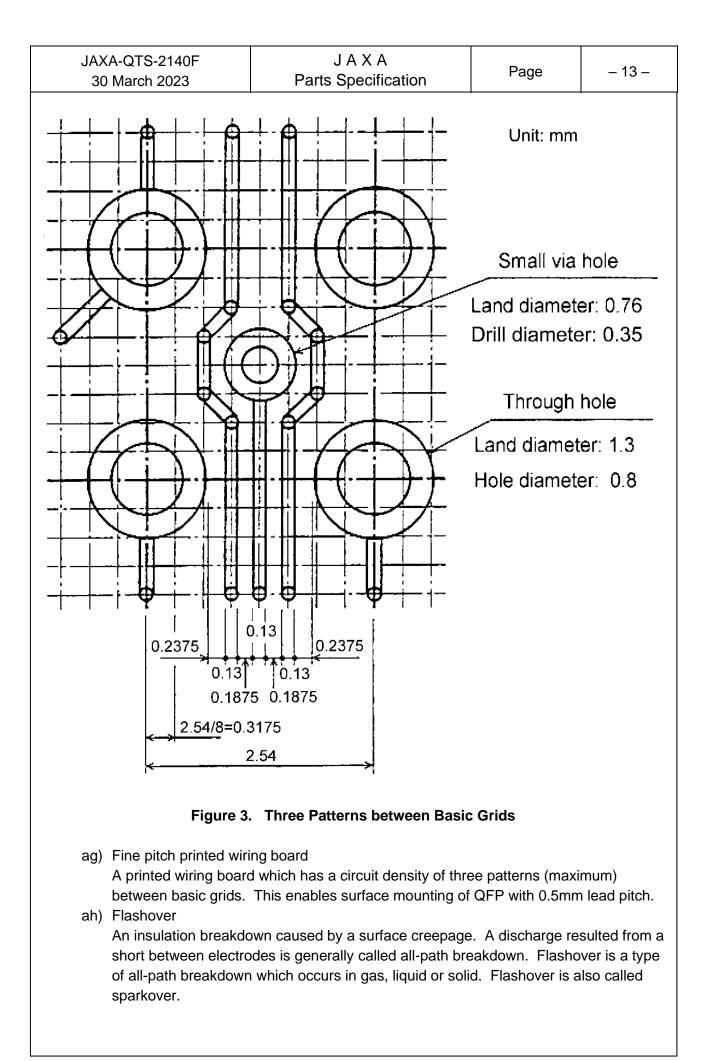
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	•	he recertification was obtained wi , it shall be performed at the time	•		
4.5.2.1	Sample				
	The test coupons submitted for the Group B inspection shall be as specified in the appendixes. Inspection lots for the Group B inspection shall consist of samples that have passed the Group A inspections.				
4.5.2.2	Inspection Items and	Sample Size			
	Items, sample size ar appendixes.	nd order of the Group B inspectior	n shall be as spec	ified in the	
4.5.2.3	Criteria for Pass/Fail				
	constitute failure of th catastrophic such as	the Group B inspections specifie e Group B inspections. If the failute open or short circuit where the function he printed wiring board fails the G	ure mode of the d	efectives is ed wiring	
4.5.2.4	Disposition after Inspe	ections			
The samples used for the Group B inspections shall not be delivered. If the samples fail in the Group B inspections, the QML manufacturer shall conduct a failure analysis on the defectives and take corrective actions on applicable materials and/or manufacturing processes. Delivery of the products shall be suspended until JAXA confirms the outcome of corrective actions.					
4.6 N	Nethod for Test or Inspec	tion			
4.6.1	Externals, Dimensions,	Marking and Others			
		ns, marking and others shall be to	ested in accordan	ce with the	
4.6.2	Workmanship The workmanship of the appendixes.	printed wiring boards shall be tes	sted in accordanc	e with the	
4.6.3	Electrical Performance The electrical performar with the appendixes.	nces of the printed wiring boards s	shall be tested in a	accordance	
4.6.4	Mechanical Performanc The mechanical perform with the appendixes.	e nances of the printed wiring board	s shall be tested i	in accordance	
4.6.5	Environmental Performa The environmental performa accordance with the app	ormances of the printed wiring boa	ards shall be teste	ed in	

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4.7 Long-Term Storage				
This provision shall not a	pply.			
4.8 Change of Tests and Ins	pections			
Any change in the in-process inspection or quality conformance inspection specified in				
this specification shall be made in accordance with paragraphs 4.4 and 6.1 of JAXA-QTS-2000.				
5. PREPARATION FOR DELI	VERY			
Preparation for delivery shall be as follows and as specified in paragraph 5 of JAXA-QTS- 2000.				
5.1 Packaging				
	s shall be packaged with a materia			
	luctors. The packaging shall be pe			
manner to protect the pro	oducts from any damage during ha	nuling and transp	onalion.	
5.2 Marking on Package				
The following shall be ma a) Part name	arked on the packages.			
	defined in this specification and by	the purchaser		
c) Applicable specificat				
d) Year and month mare) Purchaser's name	nufactured, and production serial n	umber or lot ident	ification code	
f) Manufacturer's name	e			
g) Quantity of package	8			
h) Date of inspectioni) Inspection result				
· ·				
6. NOTES				
6.1 Notes for Manufacturer				
6.1.1 Preparation and Regis	tration of Application Data Sheet			
	I prepare the application data shee and register it with JAXA.	t in accordance v	vith Appendix	
6.2 Notes for Purchasers				
Refer to the application of	lata sheet for the detailed data of th	he products and r	notes.	
6.2.1 Items to be Specified for	or Procurement			
• •	ring boards manufactured in comp	liance with this sp	pecification,	
• •	wide the following information.	w the nurchaser		
a) Part number thoseb) This specification	e defined in this specification and b number.	y the purchaser.		
c) Detail specificatio				

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e) Others As mentioned in e), requ specified for special app requirements in this spe	ata or source inspection results to uirements other than those defined lications. However, if the required cification, the purchaser shall not wiring board complies with this sp	d in this specifica ments conflict wit request the man	tion may be h the existing	
 a) Artwork An original production part drawing. Or drav b) Artwork master An original drawing of production master. c) Interstitial Via Hole (IV A through hole conne 	sed in this specification shall be a master of photos for circuits, solo vings to produce the original prod the specified accuracy which is u /H) cting internal circuit layers of a mu / through all layers (see Figure 1).	der mask, symbo uction master of p used to produce a ultilayer printed w	ohotos. an original	
	Small via hole	SVH		
	s Section of Multilayer Printed	-		
 with Small Via Hole, IVH and SVH d) Outer type A type of rigid-flex printed wiring board, where a flexible section is formed on one side of an external layer. The flexible section contains a single conductor layer. e) Undercut The reduction of conductor cross-section on a printed circuit board, caused by etching (see Figure 2). 				



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r)	Original production m				
	•	th a 1:1 scale pattern which is use	ed to produce the	productior	
	master.				
s)	Manufacturing drawin	g			
	•	nes specifications and characteris	•	•	
	•	uctive pattern arrangement, hole	structure, etching	and finish	
t)	Solder resist				
	• • • •	o the surface of a printed wiring bo			
		ded to prevent bridges between p	atterns during so	ldering.	
u)	Dewetting				
		curs when molten solder has coate			
		ning, leaving irregularly shaped g	lobules or granule	es of solde	
	and a thin solder film				
v)	Delamination				
	-	a layers within the base material.			
w)	Copper-invar-copper				
		ee metals; copper, invar (Fe64 Ni3	6 alloy) and coppe	er.	
X)	Conductor				
	• •	tching or plating. The conductor of	loes not include a	i wire, unle	
	specified.				
y)	Nail heading		6 1.11		
		of copper on internal conductor lay	-	-	
,	-	by hole drilling. This is formed in	a nail head shap	е.	
Z)	Negative Etchback		6 :		
	-	o recess the conductor material o	r internal layer mo	ore than th	
~~)	insulation material are	Suna the noie.			
aa)	Nodule	which is formed inside a through	hala during dana	aition	
2 b)			noie during depu	511011.	
aD)	Non-plated-through h	the printed wiring board, which co	ontaine no plating	on the he	
	•	d as a mounting hole for inserting			
	an electrical interconr	6 6	a screw and use	s not prov	
20)	Via hole				
ac)		with a drill diameter of 0.35mm to	0.5mm used for	highor	
	-	ype). This is used to provide an e		-	
		It in which there is no intention to			
	•	sible to realize high density wiring	•	int leau. T	
(he	Non-functional land	sible to realize high density winny			
auj		ectrically interconnected to the co	nductive nattern (on the san	
	layer.				
2e)	Fusing				
ae)	•	ng process performed by heating a	a solder laver afte	ar soldar	
	•	in etching resist for circuit forming	-		
af)	Three patterns betwe				
ur)		circuit density of three patterns of	0.13mm conduct	or width ir	
	• •	veen basic grids (see Figure 3).			

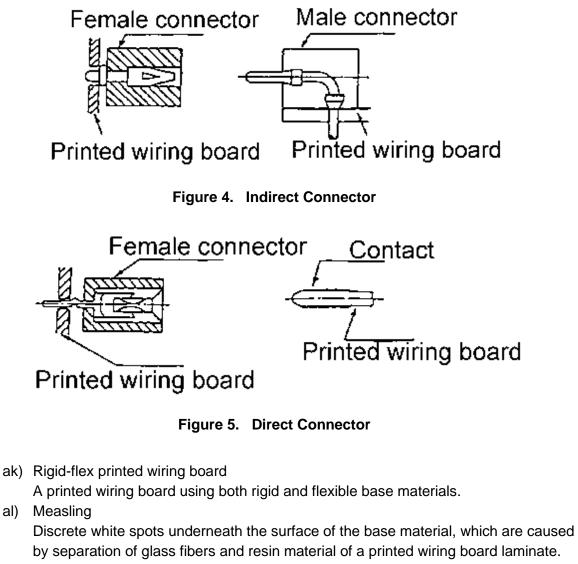


ai) Blister

A localized swelling and separation on the material surface caused by the pressure of air or gas entrapped within the laminate.

aj) Printed wiring board connectors

A component mounted on an edge of a printed wiring board, which is used to provide electrical connection with external equipment. The printed wiring board connectors are classified into two types, an indirect connector and a direct connector. An indirect connector (e.g. male connector) is attached on a printed wiring board and connected to a circuit of the board. This type is intended to provide connect mating with another connector (see Figure 4). A direct connector (one-part connector or edge-board connector) is intended for mating and interconnecting with edge board contacts on an edge of a printed wiring board (see Figure 5).



- am) Effective bonded conductor width The width of a conductor adjacent to an insulating plate.
- an) Work board
 A board containing one or more printed wiring boards and test coupons, which is used for manufacturing products.

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ao) Split board

The printed wiring board which can be divided into two or more after mounting or soldering. For easy division, the board has a deep-hole-shape slit, V-groove cut, continuous perforation or a combination of them.

ap) Land

A portion of a conductive pattern used for connecting a plated-through hole and a surface circuit or internal circuit.

aq) Resin smear

Resin transferred from the base material onto the wall of a through hole or portion used for connection. This is caused by softening or melting the base material due to the frictional heat during drilling.

ar) Resin recession

A void between the barrel of a plated-through hole and the wall of the hole, which is detected by microsectioning the printed wiring board.

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		APPENDIX A				
		PRINTED WIRING BOARDS,				
	GLASS	BASE WOVEN POLYIMIDE RES	IN OR			
	GLA	SS BASE WOVEN EPOXY RES	IN			
	BASE MATERIAL					
A.1. General				A-1		
A.1.1 Scope	e			A-1		
A.1.2 Class	sification			A-1		
A.1.3 Part N	Number			A-1		
A.1.3.1 E	Base Materia	al Code		A-2		
A.1.3.2 F	Processing C	Code		A-2		
A.1.3.3 N	Number of La	ayers		A-2		
A.2. Applicable	e Documents	S		A-2		
A.2.1 Refer	ence Docun	nents		A-2		
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		nance				
		thstanding Voltage				
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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	APPENDIX A	•	<u> </u>				
PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL							
A.1. General							
 A.1. General A.1.1 Scope This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards which use glass base woven polyimide resin (GI) or glass base woven epoxy resin (GF) as a base material (hereinafter referred to as "printed wiring boards"). A.1.2 Classification Products covered by this specification shall be classified as specified in Table A-1. Table A-1. Classification Base material Construction Remarks 							
Glass base woven epoxy resin	Single-sided printed wiring board	Including double-si wiring boards withon holes					
	Double-sided printed wiring board						
	Multilayer printed wiring board						
Glass base woven polyimide	Single-sided printed wiring board	Including double-si wiring boards witho holes					
resin	Double-sided printed wiring board						
1							

A.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Multilayer printed wiring board

Example: JAXA ⁽¹⁾ 2140/A	<u>101</u>	<u>GF</u>	<u>III</u>	<u>6</u> ⁽²⁾
	Individual	Base material	Processing	Number of layers
	identification	code	code	
		(see A.1.3.1)	(see A.1.3.2)	(see A.1.3.3)

Notes:

 $^{(1)}$ "JAXA" indicates the part is for space use and may be abbreviated "J".

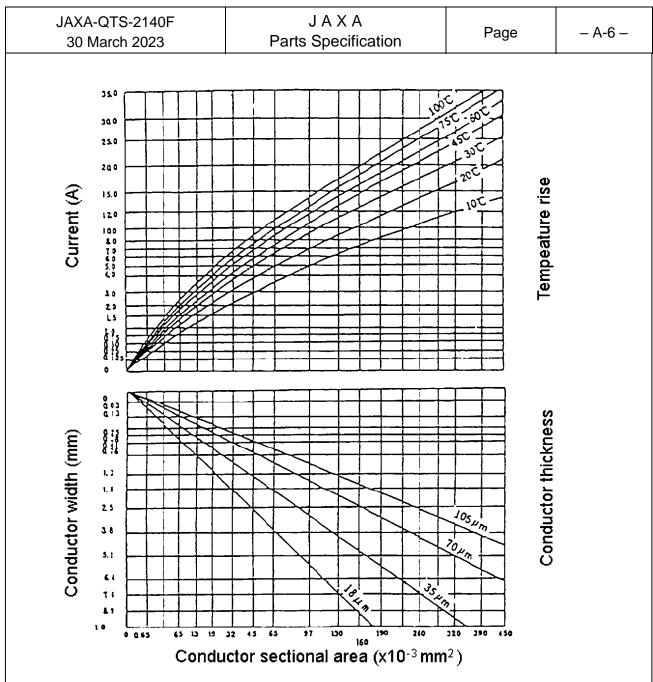
⁽²⁾ Number of conductor layers

	JAXA-QTS-2140F JAXA 30 March 2023 Parts Specification Page		– A-2 –						
A.1.	A.1.3.1 Base Material Code The base material code is as specified in Table A-2.								
	Table A-2. Base Material Code								
	Base ma	terial code ⁽¹⁾	Bas	se material					
		GF	Glass base woven ep compliant to IPC-4101		ASDA-SCL01				
		GI	Glass base woven po compliant to IPC-4101						
A.1.	sp te .3.2 Processing	pecification. mperature (1 Code	ndards for GF and GI Details of GI base ma g), shall be specified	aterial, incluing in the App	uding type and gl	ass transition			
	The proces	C C	as specified in Table Ible A-3. Processin						
	Processing code		onstruction	J	Remarks				
			printed wiring board		double-sided printe				
	II	Double-sideo	d printed wiring board						
		Multilayer pri	inted wiring board						
A.1. A.2.	The maxim	um number o	of layers shall be spec	cified in ea	ch detail specific	ation.			
A.2.	.1 Reference Do	ocuments							
The following documents are reference documents. NHB 5300.4(3I) Requirements for Printed Wiring Boards NHB 5300.4 (3K) Design Requirements for Rigid Printed Wiring Boards and Assemblies									
A.3.	. Requirements								
A.3.	.1 Qualification	Coverage							
 A.3.1 Qualification Coverage Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs A.3.2 to A.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are 									

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	used for the qualified sa used for qualification tes manufacture is allowed	urface plating and solder coating mple units are considered qualifients are considered qualified. With to supply qualified products in co ary, additional qualification covera	ed. Only solder re hin this coverage, mpliance with the	esist inks the detail
A.3.2	Materials			
	The materials shall be s	pecified as follows and as specifi	ed in paragraph 3	.3.
A.3.2.1	Metal-Clad Laminate	and Prepreg		
	4101 or JPCA/NASD, material shall be epo thickness of the base outermost layer shall foil for an internal laye the material used in t specification. Details	ate and prepreg shall conform to A-SCL01, and shall be as specific xy resin or polyimide resin (parag material shall be not less than 0. have a nominal thickness of a mi er shall have 35µm as a minimum he printed wiring boards shall be of GI base material, including typ all be defined in the Application D	ed on the drawing raph A.1.3.1). Th 05mm. The meta inimum of 18µm, a n. The applicable specified in each oe and glass trans	s. The base e nominal I foil for the and the meta standards fo detail
A.3.2.2 Solder Coating				
	The solder used for s	older coating shall contain 50 to	70 percent tin.	
A.3.2.3	Solder Resist			
	The solder resist app Class H or the equiva	lied on the printed wiring boards s lent.	shall conform to IF	PC-SM-840
A.3.2.4	Plating			
	electrolytic solder pla specified in this appe required on the surfact shall be applied, follo overlap of the two pla	ting shall be electrolytic solder plating is applied, the plating shall be ndix. If plating other than electro ce to be covered with electrolytic wed by the electrolytic solder plat tings. All through holes shall be urface plating as the plating applie	e selected from th lytic solder plating solder plating, the ting, in order to mi covered with copp	e types is partially other plating nimize the
A.3.2.4.	1 Electroless Copper	Plating		
	•	oper plating shall be applied as a inside through holes to form a co	•	
A.3.2.4.2	2 Electrolytic Copper	Plating		
A.J.Z.T.	2 11	8		

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A.3.2.4.3	A.3.2.4.3 Electrolytic Gold Plating The electrolytic gold plating shall be as specified in Table A-4. The electrolytic nickel plating specified in paragraph A.3.2.4.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.					
	Tab	le A-4.	Electrolytic Gold Platin	g		
	Item		Specificatio	n		
	Purity		Min. 99.7 perc	cent		
	KNOOP hard	ness	91 to 129 (inclu	sive)		
A.3.2.4.4	Electrolytic Nickel I The electrolytic nic equivalent, and sha	kel plating	shall conform to SAE-A low stress type.	MS-QQ-N-290 o	r the	
A.3.2.4.5	.3.2.4.5 Electrolytic Solder Plating The electrolytic solder plating shall contain 50 to 70 percent tin and shall have the thickness specified in paragraph A.3.3.6 as a minimum before fusing. The fusing process shall be performed in the final stage of the manufacturing process of printed wiring boards.					
A.3.2.5	Marking Ink The marking shall be produced using epoxy resin base inks that do not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.					
A.3.3 C	A.3.3 Design and Construction					
A.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master) Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.						
 A.3.3.2 Interlayer Connection Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes. 			d wiring			

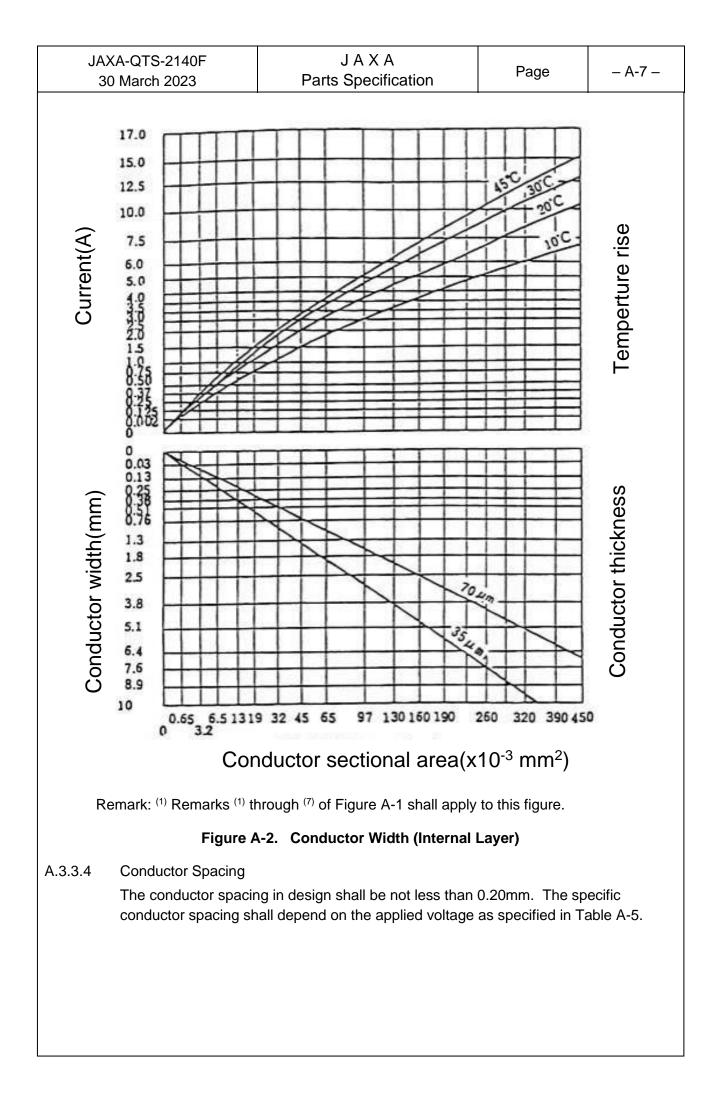
.14)	XA-QTS-2140F	JAXA		
			Page	– A-5 –
50				
	0 March 2023 Conductor Width The design width of t	Parts Specification he conductor shall be not less that ternal and internal layers shall be		



Remarks:

- ⁽¹⁾ This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations due to etching techniques, conductor thickness and width and cross-sectional areas.
- ⁽²⁾ Additional derating of 15 percent for the allowable current is suggested under the following conditions:
 - a) Where dielectric layer thickness is less than 0.8mm.
 - b) Where conductor thickness is greater than 105µm.
- ⁽³⁾ In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.
- ⁽⁴⁾ For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperature rises.
- ⁽⁵⁾ For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.
- ⁽⁶⁾ The effect of heating due to heat generating parts is not considered.
- ⁽⁷⁾ The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure A-1. Conductor Width (External Layer)



AXA-QTS-2140F 30 March 2023	J A X A Parts Specification			Page	_	A-8 –
-	Table A-	5. Conductor Spaci	ing			
				Uni	it: mm	
Voltage applied betwo		Minimum conduc		ctor spacing		
conductors, DC or AC_{p-p} (V)		External layer		Internal layer		
0 - 100		0.20		0.20		
101 - 300		0.48		0.30		
301 - 500		0.86		0.35		
501 or higher		(0.003xV)+0.1		(0.003xV)+0.1		

A.3.3.5 Annular Ring

The design value for the annular ring of a plated-through hole shall be not less than 0.325mm at the conductor connecting area of an external layer and 0.3mm on an internal layer. The design value of the annular ring of a non-plated-through hole shall be a minimum of 0.55mm.

A.3.3.6 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table A-6.

	Unit: µm
Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 25
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	Min. 5
Electrolytic solder	Min. 8 on surface Min. 4 inside a through hole
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.

Table A-6. Plating or Coating Thickness

A.3.3.7 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph A.3.10.2) and as specified in Table A-7.

	JAXA-QTS-2140F 30 March 2023 Pa		rts Specification	Page	– A-9 –
	Table /	А-7. Оре	rating Temperatur	e Range	
Unit: °C					
	Base mater	ial	Temperat	_	
	GF		-65 to	_	
	GI		-65 to	+170	
A.3.4 Extern	als, Dimensions,	Marking a	nd Others		
A.3.4.1 Exte	ernals and Constru	uction			
A.3.4.1.1 C	onductive Pattern				
	ne conductive pat r original producti		••	proved or provided a	rtwork master
	foil or composed The conductors roughness, nick reduce the cond conductor width length of any de number of defee conductor or pe roughness at ve	d from etc shall con s, pinhole ductor wid . The mir efect shall cts exceed r unit area ertical con een the co	hing and plating on tain no tears or crac s or scratches expo th to less than 80 pe nimum finished cond not exceed the des ding 0.05mm in widt a of 100×100mm on ductor edges shall b	all be formed by etc a metal foil. ks. Any combination sing the base mater ercent of the minimum luctor width shall be ign width of the conc h shall be no more th the printed wiring bo be not more than 0.1 portions in any range	n of edge ial shall not m finished 0.1mm. The luctor. The nan one per pards. The 3mm in the
	↓ ▼ R		Nick Pinhole W3 W4 W4	· · · · · · · · · · · · ·	
	$\label{eq:unit:mm} \begin{array}{l} \text{Unit:mm}\\ \text{W1} \geq (\text{Minimum finished conductor width}) \geq 0.1\\ \text{W2} \geq 0.80 \times (\text{Minimum finished conductor width}) \geq 0.1\\ \text{W3+W4} \geq 0.80 \times (\text{Minimum finished conductor width}) \geq 0.1\\ \text{R} \leq 0.13 \text{ in any range of 13 in length} \end{array}$				
	F	igure A-3	. Conductor Defe	cts	

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A.3.4.1.3	Minimum Annular F When measured in plated-through hole 0.05mm on an inte		n an external laye	er and	
A.3.4.1.4	3.4.1.4 Electrolytic Solder Plating The electrolytic solder plating shall be uniform, free from pinholes or pits, and completely cover conductive patterns after fusing. This provision shall not apply to vertical conductor edges.				
A.3.4.1.5	•	shall be uniform, free from pinhole atterns. This provision shall not a	•	• •	
A.3.4.1.6	U U	Edges of Printed Wiring Board There shall be no nicks, cracks or peeling at edges of the printed wiring boards.			
A.3.4.1.7	Surface of Printed Wiring Board On the surface of the printed wiring boards, there shall be no cracks or peeling from the portions around holes.				
A.3.4.1.8	Measling, Crazing and Delamination The printed wiring boards shall exhibit no delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board and the spacing between conductors which have no electrical continuity is not reduced exceeding 25 percent. Crazing along edges of the printed wiring boards shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.				
A.3.4.1.9	Solder Resist The solder resist shall completely cover the range of conductors specified on drawings. Visual damage such as significant thin spots or uneven color shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the manufacturing drawings.				
A.3.4.2	manufacturing drawin	ich part of the printed wiring board igs. Unless otherwise specified, d e requirements specified in Table	limensional tolera		

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Table A-8. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	$^{+0.10}_{-0.15}$ for any hole diameter
Conductor width	±0.10 for any conductor width
Conductor spacing	-0.10 for any conductor spacing. The positive side tolerance is not specified. The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.4.3 Marking

The marking shall be produced with the marking ink specified in paragraph A.3.2.5 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

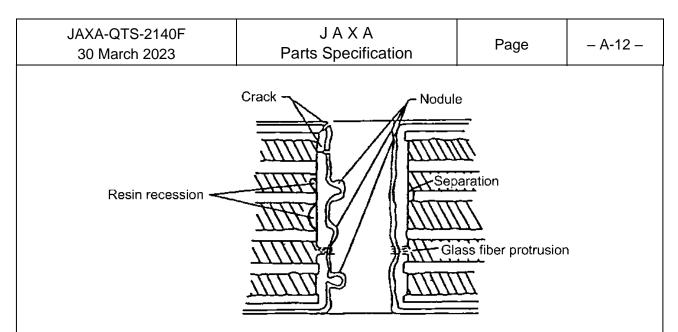
All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

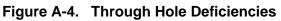
- a) Part number
- b) Year and month manufactured
- c) Manufacturer's name or its identification code
- d) Product serial number⁽¹⁾ or lot number

Note: ⁽¹⁾ Product serial number shall be provided so that the complete manufacturing process can be traced.

A.3.4.4 Through Holes

When printed wiring boards are tested as specified in paragraph A.4.4.2.2, the plating inside through holes shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall be acceptable, provided that the hole diameter is not reduced below its lower limit specified on drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 80µm and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure A-4).





a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure A-5).

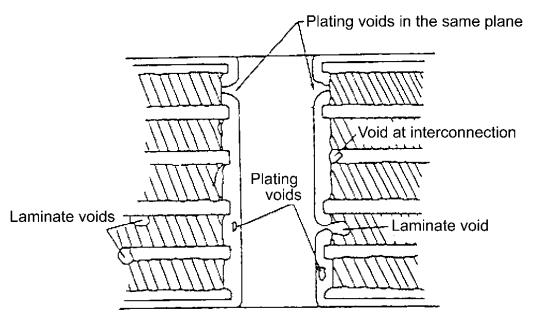
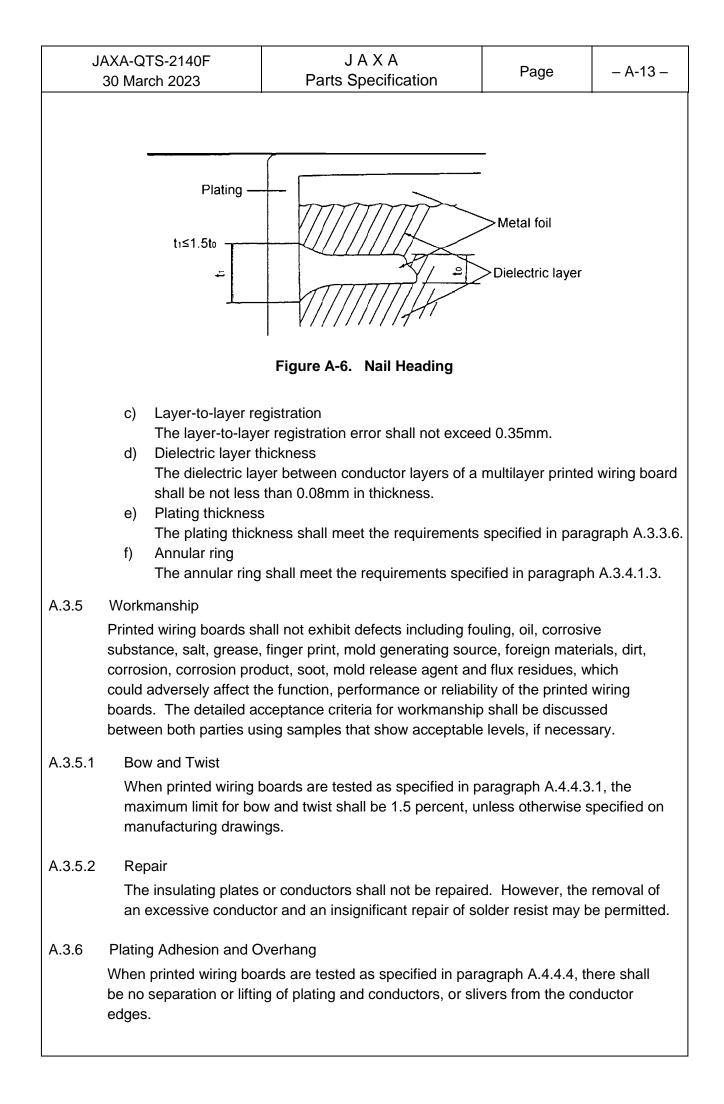


Figure A-5. Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure A-6).



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A.3.7	Cleanliness When printed wiring boa	ards are tested as specified in para on. The resistivity of the solvent ex	•				
A.3.8	Electrical Performance						
	Printed wiring board sha	all meet the following electrical req	uirements.				
A.3.8.1		ng Voltage poards are tested as specified in p kdown, flashover or sparkover.	aragraph A.4.4.6	.1, there shal			
A.3.8.2 Circuitry							
A.3.8.2.1 Continuity When printed wiring boards are tested as specified in paragraph A.4.4.6.2 a), there shall be no open circuits between circuit patterns.							
A.3.8.2.2 Circuit Shorts When printed wiring boards are tested as specified in paragraph A.4.4.6.2 b), the shall be no circuit shorts between circuit patterns.							
A.3.8.3 Connection Resistance When printed wiring boards are tested as specified in paragraph A.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall no exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately unti- connection resistance is measured.							
	$Ri = 2\rho \frac{I}{W \cdot t} (m\Omega)$						
 p: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm) l: Distance between lands (mm) W: Conductor width (mm) t: Conductor thickness (mm) 							
A.3.9	Mechanical Performance		equirements				
 Printed wiring board shall meet the following mechanical requirements. A.3.9.1 Terminal Pull Strength When tested as specified in paragraph A.4.4.7.1, printed wiring boards shall meet the following requirements. 							

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b)	 a) Bond strength The land shall withstand 89.2N pull or 1380N/cm², whichever is smaller. b) Conductor and land When printed wiring boards are inspected visually as specified in paragraph A.4.4.2.1, there shall be no loosening around the through holes. c) Microsection of through hole When printed wiring boards are microsectioned and inspected in accordance with paragraph A.4.4.2.2 a), there shall be no cracks, blistering, measling or delamination. 					
A.3.9.2 Solderability						
A.3.9.2.1	•	g boards are tested as specified ir wall and land surface shall exhibi				
A.3.9.2.2	Surface Solderabili	ty				
	minimum 95 percei new solder. The so	g boards are tested as specified in nt of the surface conductor area sh cattered existence of pinholes, dev eptable, provided that they are not	nall be covered u vetting or small re	niformly with oughened		
A.3.10 Envi	ironmental Performa	ance				
Print	ed wiring board sha	Ill meet the following environmenta	al requirements.			
A.3.10.1 Th	nermal Shock					
A.3.10.1.1	Thermal Shock (I)	applicable to qualification test)				
	shall be no open ci wiring boards shall	g boards are tested as specified in rcuit, blistering, measling, crazing meet the requirements specified i le in connection resistance betwee an 10 percent.	or delamination. n paragraph A.3.	Printed 8.2 after the		
A.3.10.1.2	Thermal Shock (II)	(applicable to quality conformance	e inspection)			
	shall be no open ci wiring boards shall	g boards are tested as specified in rcuits, blistering, measling, crazing meet the requirements specified in the in connection resistance betweet an 10 percent.	or delamination n paragraph A.3.	. Printed 8.2 after the		
A.3.10.2 H	umidity and Insulation	on Resistance				
be	e no blistering, meas	poards are tested as specified in p sling or delamination. The insulati ot less than 500MΩ.	• .			

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A.3.10.3		poards are tested as specified in p resistance between circuits befor	•			
A.3.10.4	Thermal Stress When tested as specified in paragraph A.4.4.8.4, printed wiring boards shall meet the following requirements.					
	 a) Externals There shall be no measling, cracks, separation of plating and conductors, blistering or delamination. b) Copper foil There shall be no cracks in internal copper foils in the vertical microsection of through holes. c) Laminate voids Laminate voids with the longest dimension of a maximum of 76µm shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings. 					
A.3.10.5 Radiation Hardness When printed wiring boards are tested as specified in be no defects such as measling, delamination or weav resistance between conductors shall be not less than requirements specified in paragraph A.3.8.1 shall be s			e texture. The ins 00MΩ. After the	sulation		
A.4. Qua	ality Assurance Provisi	ons				
A.4.1 In-Process Inspection The in-process inspection shall be as specified in Table A-9.						

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				Quantity of samples			
No.	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring board	Test coupon		
	Externals, construction and dimensions of internal layers		A.4.4.2.1				
	Metal-clad laminate and prepreg	A.3.2.1					
	Conductor spacing	A.3.3.4					
	Annular ring	A.3.3.5					
1	Conductive pattern	A.3.4.1.1		100%	100%		
	Conductor	A.3.4.1.2					
	Surface of printed wiring board	A.3.4.1.7					
	Dimensions	A.3.4.2					
	Workmanship ⁽¹⁾	A.3.5					
2	Cleanliness ⁽²⁾	A.3.7	A.4.4.5	2 ⁽³⁾			

Notes:

⁽¹⁾ The requirements specified in paragraph A.3.5.1 are not applied.

⁽²⁾ The cleanliness inspection shall be performed for the production printed wiring boards which are to be coated with solder resist, immediately before the application of solder resist.

⁽³⁾ Two production printed wiring boards shall be selected from the lot which is to be coated with solder resist at the same time.

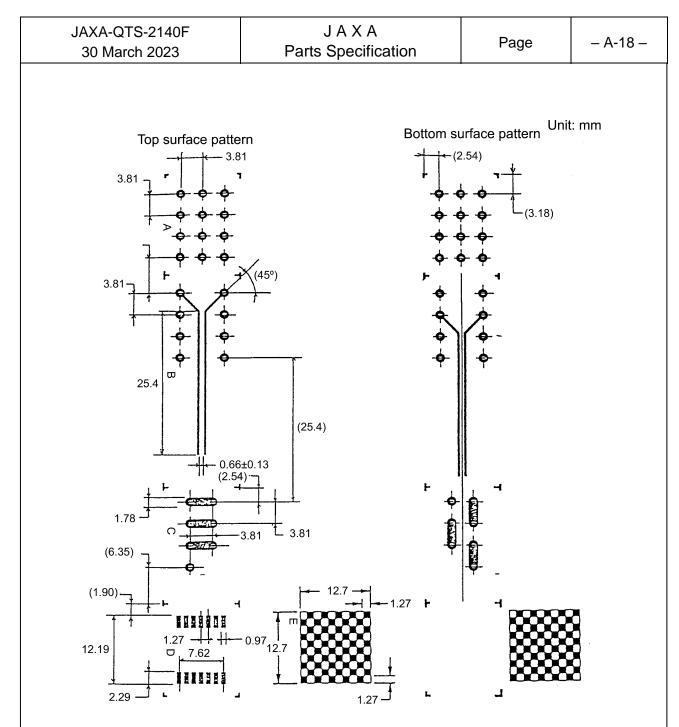
A.4.2 Qualification Test

A.4.2.1 Sample

Samples shall be approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure A-7 for single-sided or double-sided printed wiring boards and Figure A-8 for multilayer printed wiring boards.

A.4.2.2 Test Items and Number of Samples

Tests of each group shall be performed in the order listed in Table A-10. Upon completion of Group I and II tests, Group III through VIII tests shall be performed as specified in Table A-10, using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order shown in Table A-10. The sample shall include six production printed wiring boards and one for each test coupon.



Notes:

⁽¹⁾ For the test coupons except for coupon A, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter shall be the minimum hole diameter of the corresponding printed wiring board. For the test coupon A, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land.

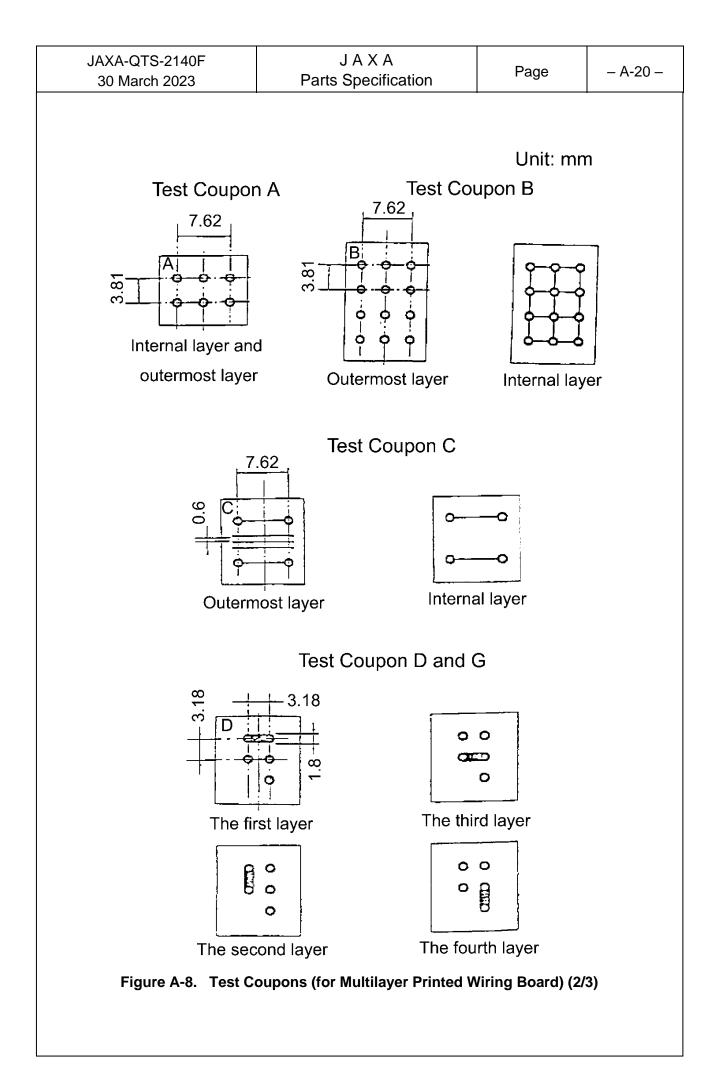
All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

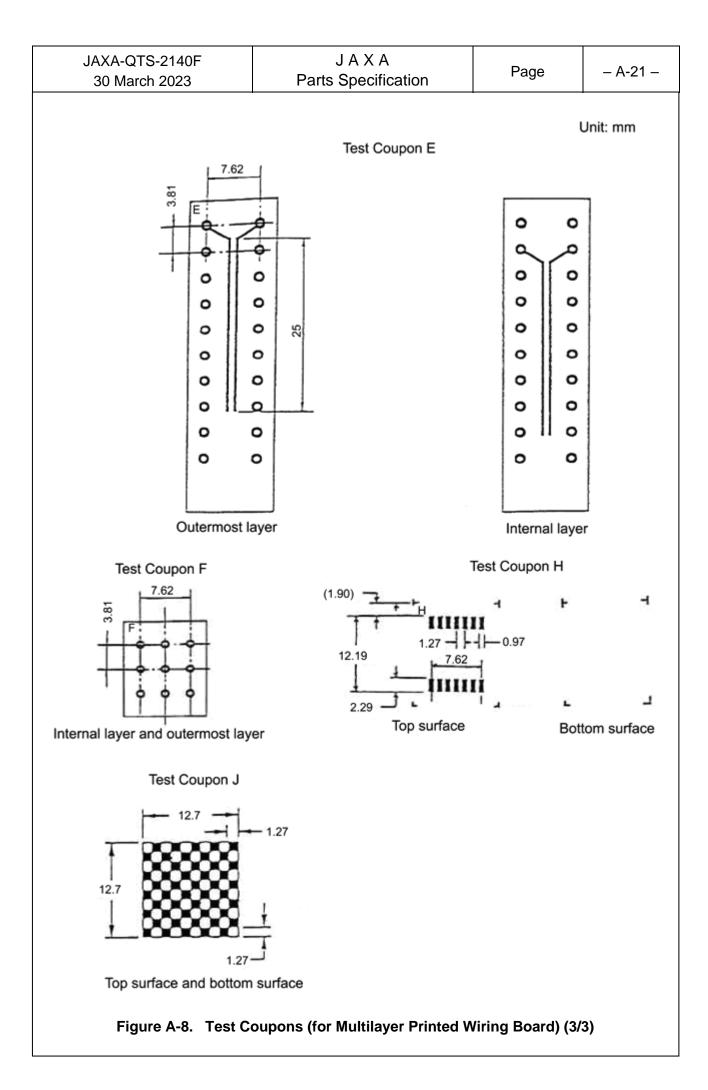
- $^{(2)}$ The conductor width shall be 0.5 \pm 0.1mm unless otherwise specified.
- ⁽³⁾ The dimensions in the parentheses are reference dimensions.
- ⁽⁴⁾ Solder resist shall apply to both sides of the test coupon E, only when solder resist is required for the products.

Figure A-7. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board)

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	Arrangement of Test Coupons		
12.7 Marking A O O O O O O B O O B O O C O O B O O C O O O C O O O C O C	 Notes: ⁽¹⁾ The conductor width shall be specified. ⁽²⁾ For the test coupons of A a the minimum land diameter wiring board, and the hole of hole diameter of the corress. For the test coupons of B, 0 shall be 1.8±0.13mm, and the typical land shape of the print tolerance shall be the tolerat printed wiring board. ⁽³⁾ The test coupons of D, E are of conductors, depending of layers. Therefore, the correst is an example; a different at the arrangement of test coupons of test coupons of the toleration and not for marking method is not specification. 	nd B, the land dian of the correspond diameter shall be to ponding minimum C, E and F, the lan the land shape sha oducts. The hole ance for the correst and G are different in the number and onductors shall be his figure. upons shown in the rrangement is also to (A to H and J) so the object of inspecified.	meter shall be ling printed the maximum lands. Ind diameter all be the diameter sponding in the number construction formed on all is appendix o acceptable. hall be used ection. The







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		Test				Pass/fail		
			Requirement	Test method	Sampl	es ⁽¹⁾	Quantity	
Group Order	Order	Test item	paragraph	paragraph	Production printed wiring boards	Test coupon ⁽²⁾	Quantity allowable defects	
	1	Design and construction Interlayer connection Conductor width Conductor spacing Annular ring	A.3.3.2 A.3.3.3 A.3.3.4 A.3.3.5	A.4.4.2				
I	2	Externals, dimensions, marking and others Design and construction Dimensions Marking	A.3.4.1 A.3.4.2 A.3.4.3	A.4.4.2.1	No. 1 to No. 6	A, B, C, D, E, F, G H,Kand L ⁽³⁾		
	3	Workmanship ⁽⁴⁾	A.3.5	A.4.4.3				
	1	Plating adhesion and overhang	A.3.6	A.4.4.4		С		
II	2	Bow and twist	A.3.5.1	A.4.4.3.1	No. 1 to No. 6	N/A		
	1	Through holes	A.3.4.4	A.4.4.2.2	- No. 1	A or F		
III	2	Terminal pull strength	A.3.9.1	A.4.4.7.1		A or F		
	1	Connection resistance	A.3.8.3	A.4.4.6.3				
IV	2	Hot oil resistance	A.3.10.3	A.4.4.8.3	No. 2	D	0	
	3	Connection resistance	A.3.8.3	A.4.4.6.3				
	1	Circuitry Continuity Circuit shorts	A.3.8.2.1 A.3.8.2.2	A.4.4.6.2 a) A.4.4.6.2 b)		G E		
	2	Connection resistance	A.3.8.3	A.4.4.6.3		G		
V	3	Thermal shock (I)	A.3.10.1.1	A.4.4.8.1 a)	No. 3	E and G		
	4	Circuitry Continuity Circuit shorts	A.3.8.2.1 A.3.8.2.2	A.4.4.6.2 a) A.4.4.6.2 b)		G E		
	5	Connection resistance	A.3.8.3	A.4.4.6.3		G		
VI	1	Humidity and insulation resistance	A.3.10.2	A.4.4.8.2	No. 4	E		
	2	Dielectric withstanding voltage	A.3.8.1	A.4.4.6.1				
	1	Thermal stress	A.3.10.4	A.4.4.8.4		В		
VII	2	Solderability Hole solderability Surface solderability	A.3.9.2.1 A.3.9.2.2	A.4.4.7.2 a) A.4.4.7.2 b)	No. 5	В ⁽³⁾ Н		
VIII	1	Radiation hardness	A.3.10.5	A.4.4.8.5	No.6	-	ノ	
	1	Materials	A.3.2	N/A	(5)	1	N/A	

Table A 10 Qualification Test

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above.

⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

⁽³⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

⁽⁴⁾ Bow and twist (paragraph A.3.5.1) of the samples shall be tested during the second test of Group II tests.

⁽⁵⁾ Data to certify compliance with design specifications shall be submitted.

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A.4.3 Quality Co	A.4.3 Quality Conformance Inspection							
A.4.3.1 Quality Conformance Inspection (Group A)								
A.4.3.1.1 Sample								
coupc	The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be manufactured simultaneously and one test coupon is subjected to each of Group IV and V tests.							
A.4.3.1.2 Inspe	ction Items and Samp	le Size						
The items and test order of Group A inspection shall be in accordance with Table A-11. The inspections within each group shall be performed in the order listed.								
Table A-11. Quality Conformance Inspection (Group A)								
Ins	Inspection Pass/fail							

	Inspection			Pass/fail				
					Quantity of	samples ⁽¹⁾		
Group	Order	Inspection item		Test method paragraph	Production printed wiring boards	Test coupon ⁽¹⁾	Quantity of allowable defects	
		Externals, dimensions, marking and others		A.4.4.2.1				
	1	Design and construction	A.3.4.1		All			
I		Dimensions	A.3.4.2			N/A		
		Marking	A.3.4.3					
	2	Workmanship ⁽²⁾	A.3.5	A.4.4.3				
II	1	Bow and twist	A.3.5.1	A.4.4.3.1	All	N/A		
111	1	Circuitry	A.3.8.2	A.4.4.6.2	All	N/A	<u>ہ ح</u>	
	1	Thermal stress	A.3.10.4	A.4.4.8.4	N/A	B (A)		
157		Through hole						
IV	2	Conductive interface	A.3.4.4 b)	A.4.4.2.2	N/A	B (A)		
		Plating thickness	A.3.4.4 e)					
		Solderability						
V	1	Hole solderability	A.3.9.2.1	A.4.4.7.2 a)	N/A	B (A)	J	
		Surface solderability	A.3.9.2.2	A.4.4.7.2 b)		H (D)		

Notes:

⁽¹⁾ A letter in the parentheses indicates the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

⁽²⁾ Bow and twist (paragraph A.3.5.1) of the samples shall be tested during the first test of Group II tests.

A.4.3.2 Quality Conformance Inspection (Group B)

A.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

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A.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table A-12. The inspections within each group shall be performed in the order listed. Test coupons and products shall be manufactured simultaneously and one test coupon shall be subjected to each of Group I and IV tests and two test coupons shall be subjected to each of Group II and III tests.

		Inspection			Pass	/fail
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	A.3.6	A.4.4.4	С	<u>\</u>
	1	Terminal pull strength	A.3.9.1	A.4.4.7.1	F	
1	2	Connection resistance	A.3.8.3	A.4.4.6.3		
	3	Hot oil resistance	A.3.10.3	A.4.4.8.3	D	
	4	Connection resistance	A.3.8.3	A.4.4.6.3		
	1	Connection resistance	A.3.8.3	A.4.4.6.3	G	
	2	Thermal shock (II)	A.3.10.1.2	A.4.4.8.1 b)	E and G	> 0
111		Circuitry				
	3	Continuity	A.3.8.2.1	A.4.4.6.2 a)	G	
		Circuit shorts	A.3.8.2.2	A.4.4.6.2 b)	E	
	4	Connection resistance	A.3.8.3	A.4.4.6.3	G	
IV	1	Humidity and insulation resistance	A.3.10.2	A.4.4.8.2	E	
IV	2	Dielectric withstanding voltage	A.3.8.1	A.4.4.6.1		

 Table A-12.
 Quality Conformance Inspection (Group B)

A.4.4 Methods for Test and Inspection

A.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 20% to 80%, and a luminance of 750 lx as a minimum.

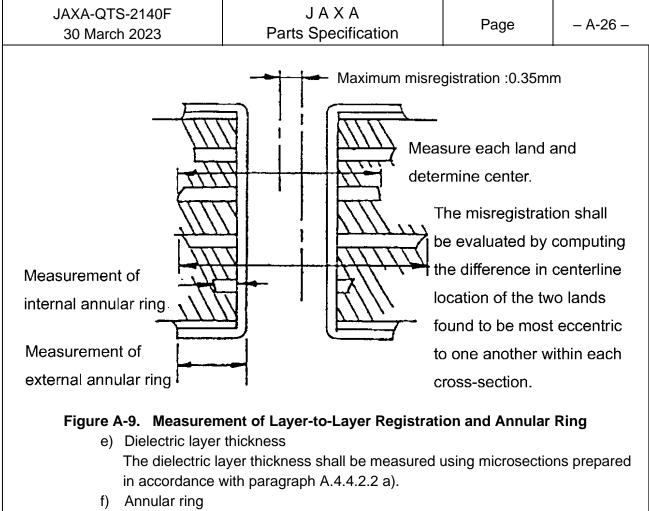
A.4.4.2 Externals, Dimensions, Marking and Others

A.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of printed wiring boards shall be tested. External surfaces shall be inspected visually.

- a) Conductive patterns and edges
 Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument with a sufficient accuracy.
- b) Annular ring Annular rings on the external layer shall be measured from the internal surface

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	(within the hole) surface of the p measured using) of the plated hole to the outer ed printed wiring board. Dimensions of g an optical measuring instrument	of annular rings s	hall be
A.4.4.2.2	 center of a hole center of the hole each work boar prepared outsid microsection sh connection of th thickness and p the layer-to-laye in parallel to the microsectioned b) Horizontal micro Only multilayer inspection. Mu polished. A cor microsection is through hole (in magnification of c) Plating thickness The plating thic accordance with Measurements through hole. Is d) Layer-to-layer r The layer-to-layer r The layer-to-layer r 	ing board specimen shall be cut in a. The sample shall be encapsulated ble. At least three plated-through le rd. The through holes for the vertical a of the effective product area on hall be inspected for the plating inten- ne vertical side, layer-to-layer regis- plating thickness) at a magnification are registration, one of the through a length direction of the multilayer perpendicular to the board's lengent osection boards shall be subjected to the her Itilayer boards with through holes inductor layer shall be polished in the prepared to expose the conductor aternal connection in horizontal direction f 50 to 100X. as kness shall be measured using mention h paragraph A 4.4.2.2 a) at a magnification solated thick or thin sections shall	ted and polished in holes shall be insp cal microsection in the work board. egrity (plating void stration, base main n of 50 to 100X. holes shall be mid board and the oth th direction. horizontal microse shall be encapsul the parallel direction shall be encapsul the parallel direction r layer. The integ ection) shall be in icrosections prep- inification of minine minimations for a p not be used for a at a magnification e with paragraph a hole in the direct	to expose th pected for may be The vertical ds, internal terial To inspect crosectioned her shall be ection lated and on. The rity of the hspected at a ared in num 200X. blated- hveraging. n of 25 to A.4.4.2.2 a)



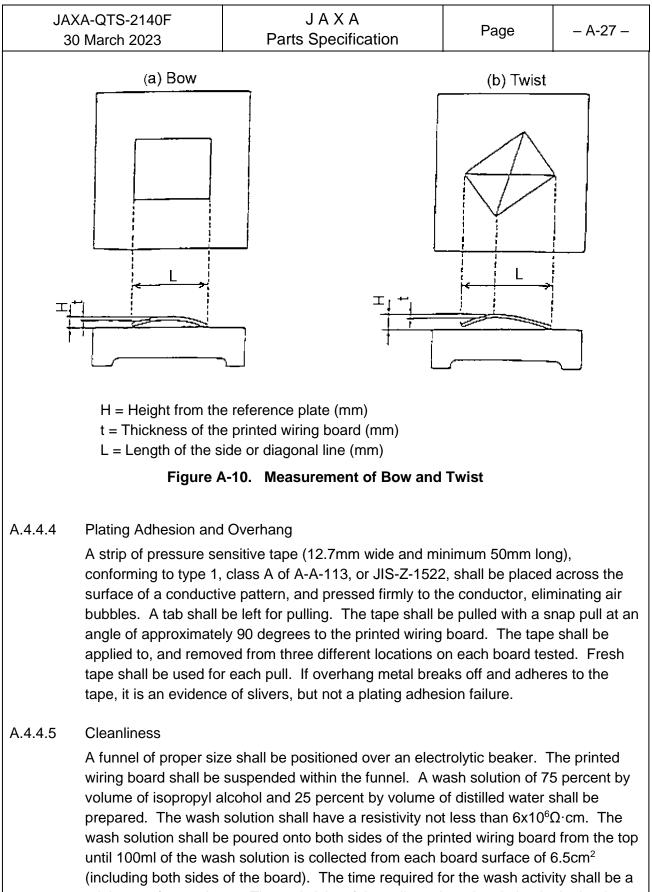
The annular ring shall be measured using microsections prepared in accordance with paragraph A.4.4.2.2 a). The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure A-9).

A.4.4.3 Workmanship

The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

A.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure A-10). The percent bow and twist shall be calculated by the following formula. Percent bow and twist = $\frac{H-t}{L} \times 100$ (%)



minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table A-13 may be used to perform the cleanliness test.

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		· · ·			<u> </u>
		Table A-13. Eq	uivalent Factors		
	Method	Resistivity (×10 ⁶ Ω·cm)	Equivalent factor	Equivalents sodium chlor (µg/cm²)	
	Conductivity bridge	2	1	1.56	
	Omega Meter ⁽¹⁾	2	1.39	2.20	
	lonograph ⁽²⁾	2	2.01	3.10	
	Ion Chaser ⁽³⁾	2	3.25	3.81	
	The dielectric with	y, Incorporated, ' ice mance tests sha nding Voltage istanding voltage of MIL-STD-202. 1000V 30 sec ication: Betwe	flon Chaser" Il be performed as fo test shall be perfor The following cond Ac peak or 1000V _{DC}	med in accordar ditions shall app rns of each laye	ly. r and the
A.4.4.6.	 a) Continuity A current of 2A interconnected b) Circuit shorts A voltage of 28 conductive pate 	d circuits to verify 50V _{DC} shall be a _l ttern and all adja	shall be flown throu connectivity. oplied between all c cent common termin of short-circuiting.	ommon terminal	s of each
A.4.4.6.	The resistance be	tween the throug	gh hole terminals sh inal method capable		-
A.4.4.7	Mechanical Perform The mechanical perf		hall be performed a	s follows.	

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 A.4.4.7.1 Terminal Pull Strength A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength. Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron. a) Solder a lead wire in to the through hole. b) Remove the lead wire from the through hole (solder removal) c) Re-solder the lead wire from the through hole. d) Remove the lead wire from the through hole. e) Re-solder the lead wire in to the through hole. 					
	The edge of the lead wire in to the through hole. The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum. After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula. L $\ge 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$				
A.4.4.7.2	L = Pull strength (N d ₁ = Hole diameter d ₂ = Land diameter Solderability	(cm)			
	 a) Hole solderabili The wetting of store to the inspection b) Surface solderate After the specing STD-202, the flate Test Method 200 clean stainless range between removed from to 	solder shall be inspected using a n n specified in paragraph A.4.4.8.4	d in Test Method s. Solder complia I in a bath and sti I that the tempera and burnt flux sha tely before the sp	208 of MIL- ant with the rred with a ature is in the all be pecimen	

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	25±6mm per se vertical state in	econd, kept in the bath for 4 ± 0.5 second. After the pull-up, the species the air, until the solder is solidified condition of solder on the conduct is solidified.	men shall be kept I. No quick coolir	t in the ng shall be
A.4.4.8	Environmental Perfor	mance		
	The environmental pe	erformance tests shall be performe	ed as follows.	
A.4.4.8.1	 The environmental performance tests shall be performed as follows. 1 Thermal Shock The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply. a) Thermal shock (I) (applicable to qualification test) 1) For GF base material The test shall be performed under the test condition B. The low temperature shall be -30°C and the high temperature shall be +125°C. The time for step 2 and 4 shall be within 2 minutes each, and the number of cycles shall be 1000. 2) For GI base material The test shall be performed under the test condition F. The low temperature shall be -30°C and the high temperature shall be +150°C. The time for step 2 and 4 shall be within 2 minutes each, and the number of cycles shall be 1000. 2) For GI base material The test shall be performed under the test condition F. The low temperature shall be -30°C and the high temperature shall be +150°C. The time for step 2 and 4 shall be within 2 minutes each, and the number of cycles shall be 1000. b) Thermal shock (II) (applicable to quality conformance inspection) For GF base material The test shall be performed under the test condition B-3. The time for step 2 and 4 shall be within 2 minutes each. 2) For GI base material The test shall be performed under the test condition F-3. The high temperature shall be +170°C, and the time for step 2 and 4 shall be within 2 minutes each. 			
A.4.4.8.2	 a) Humidity resists The first 6 steps cycles. The po 6 of the final cy immediately by b) Insulation resis The test shall b 	performed in the following order. ance s in Test Method 106 of MIL-STD- larization voltage shall not be appl cle, the specimen shall be taken o blowing air at 25±5°C and evalua	ied. Upon compl ut of the bath and ted. ne test condition E	etion of step d dried 3, Test
A.4.4.8.3	•	l be dried at 120±5°C for 2 hours a that, the specimen shall be imme		

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for 5 seconds and cooled to room temperature. Immersion and cooling shall be performed for 10 cycles.

A.4.4.8.4 Thermal Stress

The specimen shall be conditioned by drying for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 percent maintained at 288±5°C for a period of 10 seconds. After thermal stressing, the specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for cracks on the internal copper foil and laminate voids using the microsection prepared in accordance with A.4.4.2.2 a). Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

A.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4 Gy to 1×10^4 Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4 Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with A.4.4.6.1 and A.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

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			I				
	AFFENDIAB						
FINE	FINE PITCH PRINTED WIRING BOARDS,						
	BASE WOVEN POLYIMIDE RES	•					
GL	ASS BASE WOVEN EPOXY RESI	Ν					
	BASE MATERIAL						
•							
	al Code						
-	Code						
	ayers						
	ance						
	ts						
	ments						
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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		APPENDIX B		
	GLA	NE PITCH PRINTED WIRING BOA SS BASE WOVEN POLYIMIDE RI GLASS BASE WOVEN EPOXY RE BASE MATERIAL	ESIN OR	
B.1. General				
provis polyim	ppendix estab ions for the fin hide resin (GI)	lishes the general requirements an e pitch printed wiring boards which or glass base woven epoxy resin ((to as "printed wiring boards").	use glass base wo	ven
	ification cts covered by	this specification shall be classifie	d as specified in Ta	ble B-1.
		Table B-1. Classification		
	Base material	Construction	Remarks	
	Glass base	Single-sided printed wiring board	Including double-side wiring boards without	
	woven epoxy resin	Double-sided printed wiring board		
Classification		Multilayer printed wiring board		
	Glass base woven	Single-sided printed wiring board	Including double-side wiring boards without	
	polyimide resin	Double-sided printed wiring board		
		Multilayer printed wiring board		
The pa	Number art number of t ple: JAXA ⁽¹⁾ 21	Individual Base Proce identification material co	bllowing form. $\underline{4^{(2)}}$ essing Number ode of layers .3.2) (B.1.3.3)	Y Heat resistance (B.1.3.4)
		he part is for space use and may b	e abbreviated "J".	

	JAXA-QTS-2140F 30 March 2023			J <i>ا</i> Parts Sp	A X A pecificat	ion	Pa	age	– B-2 –
B.1.3			ial Code naterial code	is as specifie	ed in Tat	ole B-2.			
			Tab	ole B-2. Bas	se Mater	ial Code			
	E	Base ma	terial code ⁽¹⁾		Ba	se material			
			GF	Glass base v compliant to			NASDA-S	SCL01	
			GI	Glass base v compliant to				SCL01	
Note: ⁽¹⁾ Applicable standards for GF and GI types are as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), are as specified in the Application Data Sheet (ADS). B.1.3.2 Processing Code									
The processing code is as specified in Table B-3.									
Table B-3. Processing Code									
Processing code			С	onstruction Remarks					
_	I Single-side		Single-sided	d printed wiring board Including do boards with			ided printe ough holes		
_	II		Double-sideo	ed printed wiring board					
			Multilayer pri	nted wiring bo	ard				
B.1.3		nber of e maxim	•	of layers shal	l be spe	cified in ea	ch deta	il specific	ation.
B.1.3		•	on of printed	wiring board: Heat Resista	-				ed in Table
						٦	Thermal	shock	
	Base materia	al code	Heat re	sistance	Tempe	rature rang	e (°C)	Numbe	er of cycles
			No	code	-	30 to +125		1	,000
	GF			/(1)	-	30 to +125			800
					-	30 to +100		1	,000
			No	code	-	30 to +150		1	,000
	GI			/(1)	-	30 to +150			800
					-	30 to +125		1	,000
Not	e: ⁽¹⁾ The p	orinted w	riring boards	shall meet tv	vo test c	onditions f	or heat	resistance	Э.

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B.2. A	Applicable Documents			
B.2.1	Reference Documents			
	The reference documen	ts shall be as specified in paragra	ıph 2.2.	
B.3. F	Requirements			
B.3.1	Qualification Coverage			
	manufacturing line that performance specified in shall be fully represente Products with fewer laye considered qualified. S used for the qualified sa used for qualification tes with the same base and with a different number sample shall have more coverage, the manufact	lid for printed circuit boards that a conforms to materials, designs, co in paragraphs B.3.2 to B.3.10. The d by samples that have passed th ers and less thickness than the qu urface plating and solder coating t imple units are considered qualifies are considered qualified. Test the same metal foil may be used of layers except for the thermal sh l layers than the samples for qualified ure is allowed to supply qualified p tion. If necessary, additional qualities becification.	onstructions, ratin e qualification cov he qualification test alified sample un types other than the data taken using as test data for s hock test. In this of fication test. With products in compl	gs and verage st. its are hose esist inks samples amples case the hin this iance
B.3.2	Materials			
	The materials shall be s	pecified as follows and as specifie	ed in paragraph 3	.3.
B.3.2.1	Metal-Clad Laminate	and Prepreg		
	4101 or JPCA/NASD material shall be epo- thickness of the base copper regardless of shall have a thickness conductor thickness f holes (SVH), the cop of 9µm (nominal) as a nominal thickness of (nominal) in consider interstitial vial holes (material used in the p	ate and prepreg shall conform to t A-SCL01, and shall be as specifie xy resin or polyimide resin (paragr material shall be not less than 0.0 the base material type. The copp s of 18µm (nominal) as a minimum for plating. Only when printed wirin per foil for the outermost layer sha a minimum. The copper foil for an 35µm as a minimum. However, it ation of additional conductor thickn IVH) and SVH are provided. The printed wiring boards shall be spect of GI base material, including typ	ed on drawings. T raph B.1.3.1). Th D5mm. The meta er foil for the outer n in consideration ng boards have s all have an addition internal layer sha shall be a minim ness for plating, o applicable standa cified in each deta	The base e nominal of foil shall be ermost layer of additionation surface via onal thicknes all have a um of 18µm only when ards for the ail

B.3.2.2 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

temperature (Tg), shall be defined in the Application Data Sheet (ADS).

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30	J March 2023	Parts Specification	_	
B.3.2.3		ed on the printed wiring boards s ent. The application shall be in a		
B.3.2.4	Marking Ink The marking shall be produced using epoxy resin base ink that does not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.			
B.3.2.5	5.3.2.5 Plating Unless otherwise specified the solder coating specified in paragraph B.3.2.2 shall be applied to all through holes (excluding IVH, SVH and small via holes), lands and surface conductive patterns, except for where solder resist is applied. All through holes except IVH and SVH shall be coated with copper plating and subsequently with the same type surface plating as the plating applied on lands. When plating other than the plating applied on lands is partially required in through holes except for the fine pith patterns, electrolytic gold plating may be applied.			
B.3.2.5.1	Electroless Copper Plating The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.			
B.3.2.5.2	Electrolytic Copper The electrolytic cop	Plating per plating shall have a minimum	n purity of 99.5 pe	rcent.
 B.3.2.5.3 Electrolytic Gold Plating The electrolytic gold plating shall be as specified in Table B-5. The electrolytic nickel plating specified in paragraph B.3.2.5.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness. 				
B.3.2.5.4 Electrolytic Nickel Plating The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.				
	Tab	e B-5. Electrolytic Gold Platir	ng	
	Item	Specification	on	
	Purity	Min. 99.7 per	cent	
	KNOOP hard	ness 91 to 129 (incl		

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B.3.3 Design and Construction

B.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

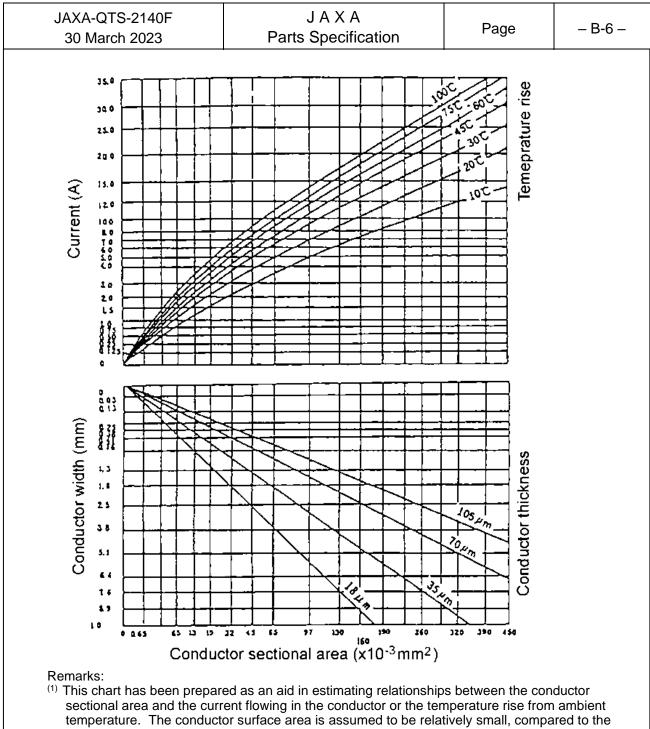
B.3.3.2 Connector for Printed Wiring BoardsA direct connector (one-part connector or edge-board connector) shall not be used.

B.3.3.3 Interlayer Connection

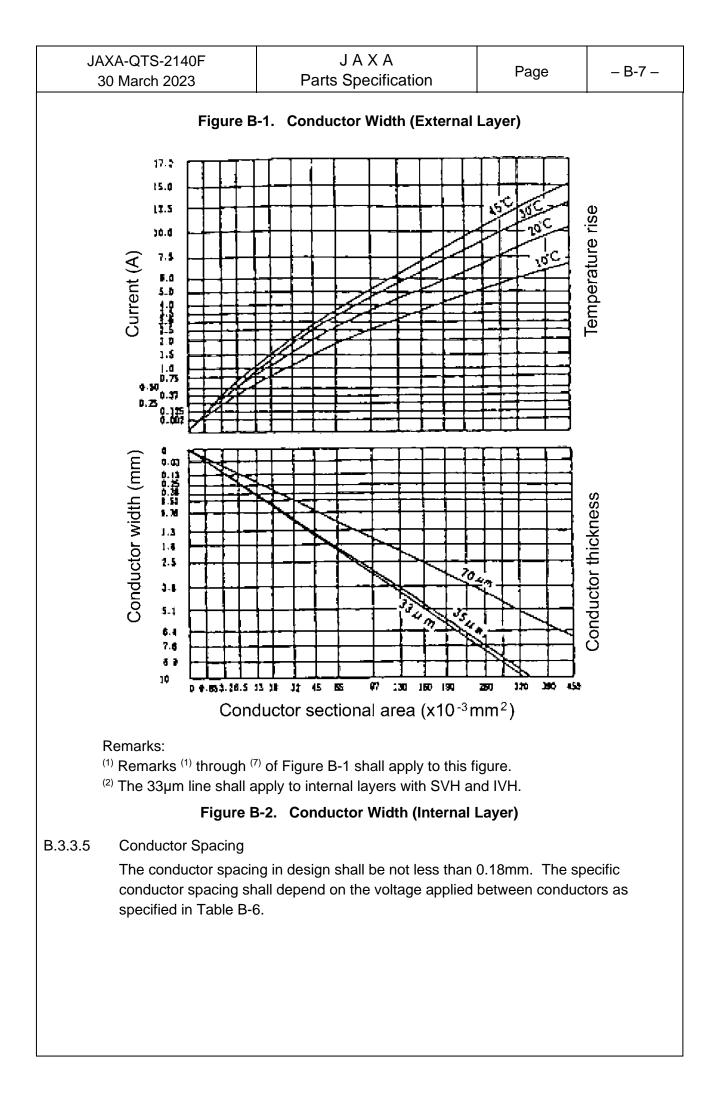
Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes including small via holes, IVH and SVH. The small via holes shall be a minimum of 0.35mm in its drill diameter. The IVH and SVH shall have a minimum of 0.2mm in their drill diameters.

B.3.3.4 Conductor Width

The design width of the conductor shall be not less than 0.13mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures B-1 and B-2.



- sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations due to etching techniques, conductor thickness and width and cross-sectional areas.
- ⁽²⁾ Additional derating of 15 percent for the allowable current is suggested under the following conditions:
 - a) Where dielectric layer thickness is less than 0.8mm.
 - b) Where conductor thickness is greater than 105µm.
- ⁽³⁾ In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.
- ⁽⁴⁾ For single conductor applications, the chart may be used for determining conductor widths, crosssectional area and allowable current (current-carrying capacity) for various temperature rises.
- ⁽⁵⁾ For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.
- ⁽⁶⁾ The effect of heating due to heat generating parts is not considered.
- ⁽⁷⁾ The final conductor thickness in the chart does not include plating thickness of metals other than copper.
- ⁽⁸⁾ The 54µm line shall apply to an external layer with SVH.



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Table B-6. Conductor Spacing for Coated Printed Wiring Board

Voltage applied between conductors, DC or AC _{p-p} (V)	Minimum conductor spacing		
	External layer	Internal layer	
0 - 100	0.18	0.18	
101 - 300	0.48	0.30	
301 - 500	0.86	0.35	
501 or higher	(0.003xV)+0.1	(0.003xV)+0.1	

B.3.3.6 Land Diameter

The minimum design value of land diameter shall be as specified in Table B-7 (see Figure B-3).

Table B-7. Land Diameter

Unit: mm

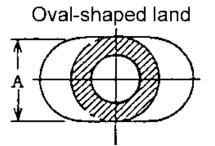
Unit: mm

Hole	Minimum land diameter ⁽¹⁾
IVH, SVH and small via holes	Drill diameter + 0.4 ⁽²⁾
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

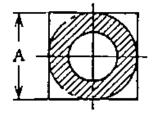
Notes:

⁽¹⁾ The minimum diameter of lands other than round shaped lands shall be measured as the length "A", as shown in Figure B-3.

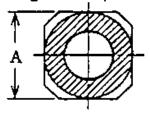
⁽²⁾ The minimum diameter of the land provided with a small via hole shall be 0.76mm.



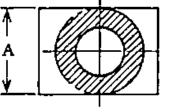
Square-shaped land



Octagon-shaped land



Rectangular-shaped land





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B.3.3.7 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table B-8.

Table B-8. Plating or Coating Thickness	Table B-8.	Plating or Coating Thickness
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Unit: µm

Plating material	Surface and through hole plating thickness	
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating	
	Component hole	Min. 25
Electrolytic copper	Small via hole	Min. 30
	IVH and SVH	Min. 15
Electrolytic gold	1.3 to 4.0	
Electrolytic nickel	Min. 5	
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.	

B.3.3.8 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph B.3.10.1.2) and as specified in Table B-9.

Table B-9. Operating Temperature Range

Unit: °C

Base material	Temperature range	
GF	-65 to +125	
GI	-65 to +170	

B.3.4 Externals, Dimensions, Marking and Others

B.3.4.1 Externals and Construction

B.3.4.1.1 Externals of Conductive Pattern, Base Material and Solder Resist

a) Conductive pattern

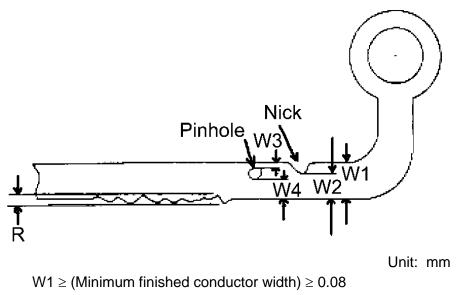
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor

The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The

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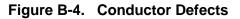
length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100 mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is not less than 0.2mm, the roughness shall be maximum 0.13mm (see Figure B-4).



 $\label{eq:W12} W12 (Minimum Inished conductor Width) \geq 0.08 \\ W2 \geq 0.80 \times (Minimum finished conductor width) \geq 0.08 \\ W3+W4 \geq 0.80 \times (Minimum finished conductor width) \geq 0.08 \\ R \mbox{ in any range of 13 in length}$

 $R \le 0.08$, when the design width of the conductor is less than 0.2

 $R \le 0.13$, when the design width of the conductor is 0.2 or more



c) Annular ring

When the annular ring on the internal and external layers are measured in accordance with paragraph B.4.4.2.2 f), the annular ring of a plated-through hole shall be not less than 0.05mm. The annular ring of a non-plated-through hole shall be not less than 0.38mm and shall not contain any defect. When the annular ring for plated-through hole on an external layer shall be a minimum of 0.13mm in diameter, a sub-land or other equivalent alternative shall be provided.

d) Dielectric layer between conductor layers The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.

 e) Electrolytic solder plating and solder coating The electrolytic solder plating and solder coating shall be free from pinholes or pits, and completely cover conductive patterns.

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 f) Edges of printed wiring board Printed wiring boards shall not exhibit nicks, cracks or separation at their edge This provision shall not apply to separate parts of a split board. g) Surface of printed wiring board Surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board, and the spacing between conductors is not reduced exceeding 25 percent. Crazing along edges of the printed wiring board shall b permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller. h) Solder resist The cured solder resist shall be free from tackiness, blistering and delamination Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the provisions of manufacturing drawings. 		ion around Measling acceptable, urface area of ot reduced board shall be conductor is on drawings I delamination. ess on the e permitted. specified, ductors are onto	
manufacturing drawin	ach part of the printed wiring board igs. Unless otherwise specified, o e requirements specified in Table	limensional tolera	

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Unit: mm

	Unit. mini
ltem	Dimensional tolerance
External dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of IVH, SVH and small via holes is not specified.
Conductor width	0.13 or more and less than 0.20: ± 0.05 0.20 or more and less than 0.50: ± 0.10 0.50 or more: ± 20 percent of circuit width
Conductor spacing	For the design of three patterns between basic grids, the tolerance of conductor spacing shall be -0.08. (The positive side tolerance is not specified.) For the design of maximum two patterns between basic grids, the tolerance of conductor spacing shall be -0.10. (The positive side tolerance is not specified.) The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

B.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph B.3.2.4 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.

All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

- a) Part number
- b) Year and month manufactured
- c) Manufacturer's name or its identification code
- d) Product serial number⁽¹⁾ or lot number

Note: ⁽¹⁾ Product serial number shall be provided so that the complete manufacturing process can be traced.

B.3.4.3.1 Marking on Split Board

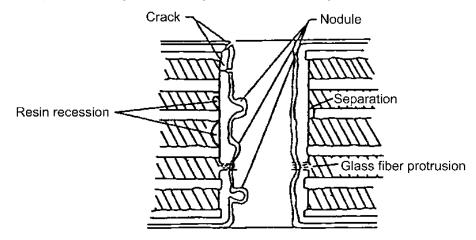
If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

B.3.4.4 Through Holes

When printed circuit boards are tested as specified in paragraph B.4.4.2.2, the plating of small via holes, IVH and SVH shall not exhibit cracks, conductive interface

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	•		

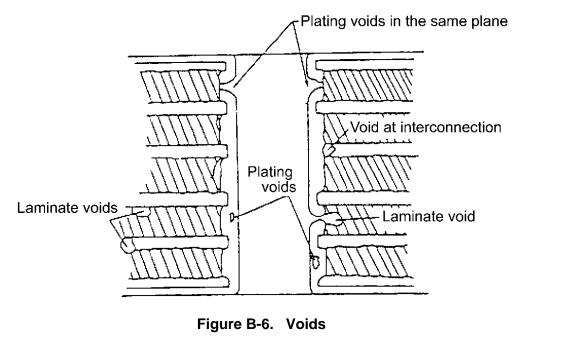
separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80µm, and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure B-5).





a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure B-6).



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	conductor layer horizontal micros vertical microsed	face at the interface of the hole wall pl shall not exceed 25 percent of the section, and 50 percent of the inte stion. Nail heading of a conductor etal foil thickness (see Figure B-7	e through hole circ erface in the same r layer shall not ex	umference in plane in		
	Plating — t₁≤1.5to		Metal foil	/er		
		Figure B-7. Nail Heading				
	 d) Dielectric layer the dielectric lay shall be not less e) Plating thickness The plating thick f) Annular ring 	er registration error shall not exceen nickness ver between conductor layers of a than 0.08mm in thickness.	multilayer printed	graph B.3.3.7		
B.3.4.5	Solder Resist Thickness When printed circuit boards are tested as specified in paragraph B.4.4.2.3, the solder resist thickness shall be not less than 17.5µm, measured at the center of conductors.					
B.3.5	Workmanship The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.					
B.3.5.1	•	boards are tested as specified in p w and twist shall be 0.8 percent, u	•			

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	manufacturing drawings. For a split board, the percent bow and twist shall not exceed the value specified above, before separation.						
B.3.5.2	Repair The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.						
B.3.6	Plating Adhesion and Overhang When printed circuit boards are tested as specified in paragraph B.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.						
B.3.7	Cleanliness The printed wiring boards shall exhibit no fouling including dirt, oil, corrosion, corrosion product, salt, soot, grease, finger print, mold release agent, foreign inclusion and flux residues, or ionic contamination. When printed circuit boards are tested as specified in paragraph B.4.4.5, the resistivity of the solvent extract shall be not less than $2x10^6\Omega\cdot cm$.						
B.3.8	Electrical Performance Printed wiring board shall meet the following electrical requirements.						
B.3.8.1	Dielectric Withstanding Voltage When tested as specified in paragraph B.4.4.6.1, printed circuit boards shall not exhibit insulation breakdown, flashover or sparkover.						
B.3.8.2	Circuitry When tested as specified in paragraph B.4.4.6.2, printed circuit boards shall not exhibit open circuit or short-circuiting between circuit patterns.						
B.3.8.3	Connection Resistance When printed circuit boards are tested as specified in paragraph B.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.						
	$Ri = 2\rho \ \frac{I}{W \boldsymbol{\cdot} t} \ (m\Omega)$						
	ρ: Volume resistivity a l: Distance between la W: Conductor width (t: Conductor thicknes	mm)	rms the conducto	or (mΩ∙mm)			
B.3.9	Mechanical Performanc Printed wiring boards sh	e hall meet the following mechanical	requirements.				

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		·			
W	llowing requirement Bond strength The land shall wi Conductor and la When printed win B.4.4.2.1, there s Microsection of t When printed win	ified in paragraph B.4.4.7.1, printe is. This provision shall not apply to ithstand 89.2N pull or 1380N/cm ² , and ring boards are inspected visually shall be no loosening around the th	o IVH, SVH or sm whichever is sma as specified in pa nrough holes. d inspected in ac	nall via holes. aller. aragraph cordance	
W fol a)	 B.3.9.2 Solderability When tested as specified in paragraph B.4.4.7.2, printed wiring boards shall meet the following requirements. a) Hole solderability The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to IVH, SVH or small via holes. b) Surface solderability A minimum of 95 percent of the surface conductor area shall be covered uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area. 				
B.3.10 Envi	ronmental Performa	ance			
Printe	ed wiring boards sh	all meet the following environmen	tal requirements.		
B.3.10.1 Th	nermal Shock				
	When printed circu there shall be no of completion of the te accordance with pa measured in accord meet the requirement	(applicable to qualification test) it boards are tested as specified in pen circuit, blistering, measling, cra est, circuit continuity and circuit sh aragraph B.4.4.6.2, and connectior dance with paragraph B.4.4.6.3. F ents specified in paragraph B.3.8.2 on resistance between circuits bef rcent.	azing or delamina orts shall be teste n resistance shall Printed wiring boa 2 after the test, ar	ation. At the ed in be ards shall nd the	
	When printed circu there shall be no of completion of the te accordance with pa measured in accord	(applicable to quality conformance it boards are tested as specified in pen circuit, blistering, measling, cra est, circuit continuity and circuit sh aragraph B.4.4.6.2, and connectior dance with paragraph B.4.4.6.3. F ents specified in paragraph B.3.8.2	a paragraph B.4.4 azing or delamina orts shall be testa n resistance shall Printed wiring boa	ation. At the ed in be ards shall	

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	change in connection resistance between circuits before and after the test shall be less than 10 percent.						
B.3.10.2	When printed circuit to be no blistering, mea	Humidity and Insulation Resistance When printed circuit boards are tested as specified in paragraph B.4.4.8.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be not less than $500M\Omega$.					
B.3.10.3	3 Hot Oil Resistance When printed circuit boards are tested as specified in paragraph B.4.4.8.3, the change in connection resistance between circuits before and after the test shall be less than 10 percent.						
B.3.10.4	 .4 Thermal Stress When tested as specified in paragraph B.4.4.8.4, printed wiring boards shall meet the following requirements. a) Externals There shall be no measling, cracks, separation of plating and conductors, blistering or delamination. b) Copper foil There shall be no cracks in internal copper foils in the vertical microsection of through holes. c) Laminate voids Laminate voids with the longest dimension of 76µm as a maximum shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings. 						
B.3.10.5	 B.3.10.5 Radiation Hardness When printed circuit boards are tested as specified in paragraph B.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph B.3.8.1 shall be satisfied. 						
B.4. Qua	B.4. Quality Assurance Provisions						
T b B a	oards shall meet the re 3.3.7.	on specified below shall be perforn equirements of paragraphs B.3.4.1 internal layers, construction and c ing)	, B.3.4.2, B.3.4.3	and			

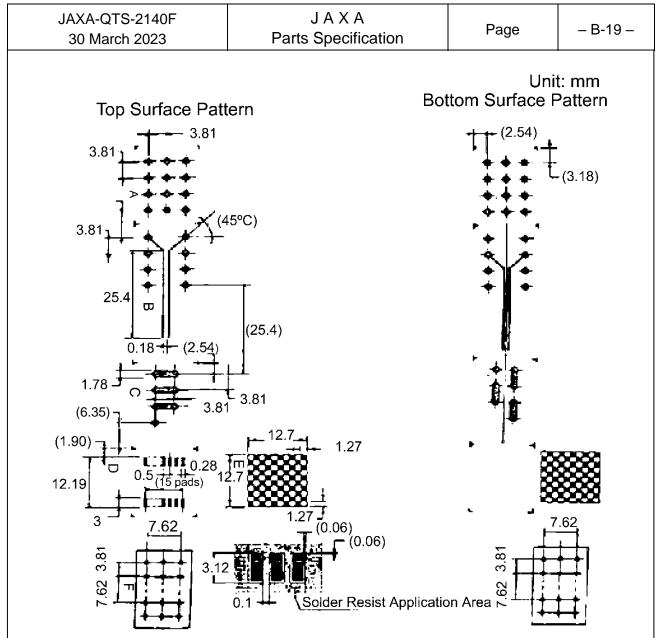
B.4.2 Qualification Test

B.4.2.1 Sample

Samples shall be approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure B-8 for single-sided or double-sided printed wiring boards and Figure B-9 for multilayer printed wiring boards. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board.

B.4.2.2 Test Items and Number of Samples

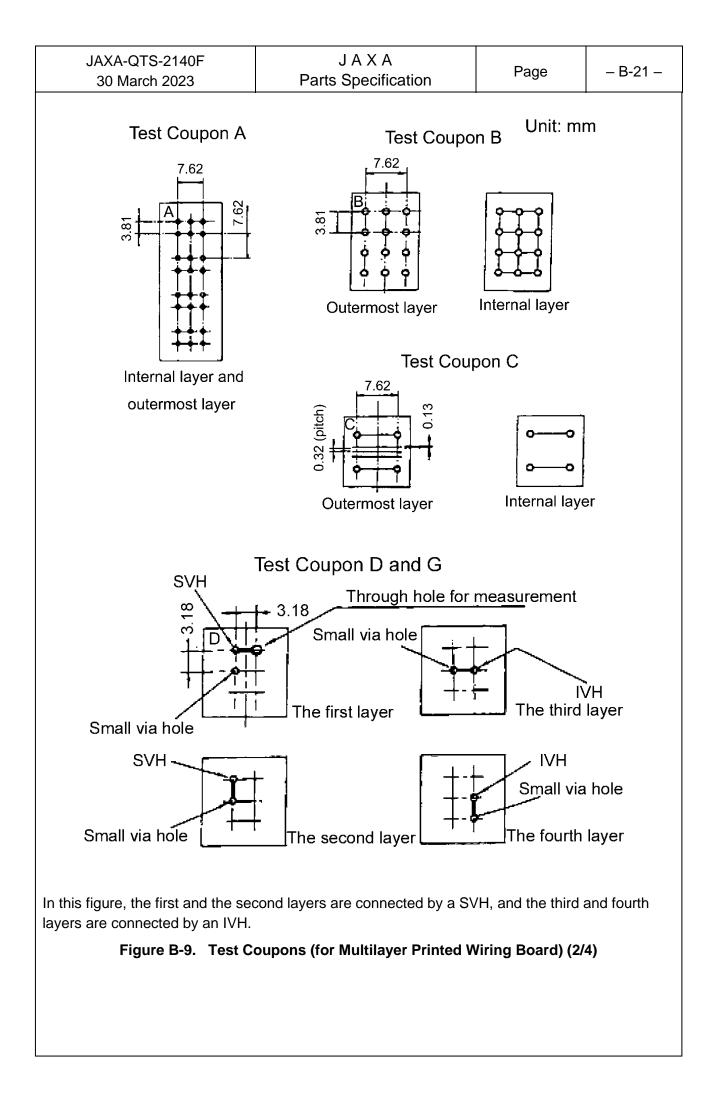
The tests of each group shall be performed in the order listed in Table B-11. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Three combined conditions of temperature range and number of cycles shall apply to each base material type, as specified in Table B-4. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table B-11.



Notes:

- ⁽¹⁾ For the test coupons A and B, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter shall be 0.8mm. For the test coupons C and F, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land. The test coupon F shall be prepared, only when the corresponding product has small via holes. All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.
- ⁽²⁾ The conductor width shall be 0.5 ± 0.1 mm unless otherwise specified.
- ⁽³⁾ The dimensions in the parentheses are reference dimensions.
- ⁽⁴⁾ Solder resist shall apply to the test coupons B, D, and E, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon B shall be the land diameter increased by 0.2mm. For coupon E, the solder resist shall apply to the entire layer.

Figure B-8. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board) Arrangement of Test Coupons



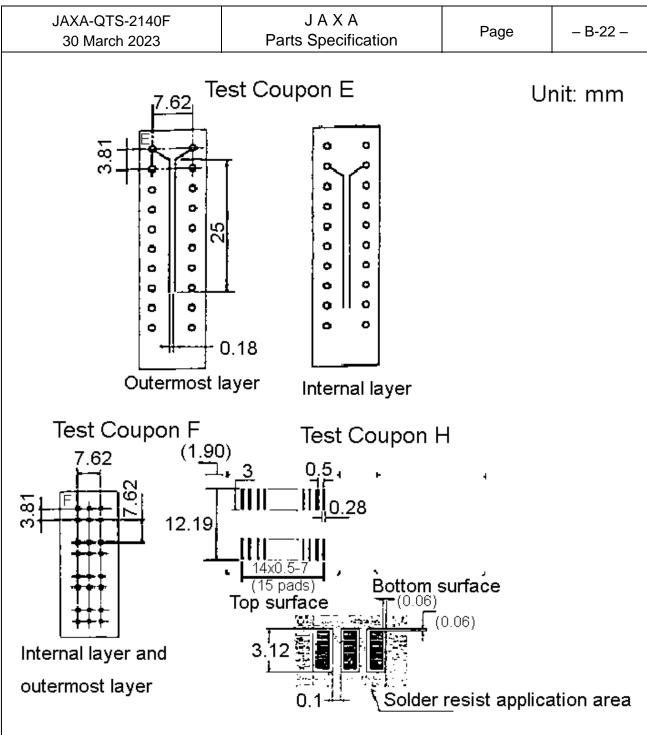
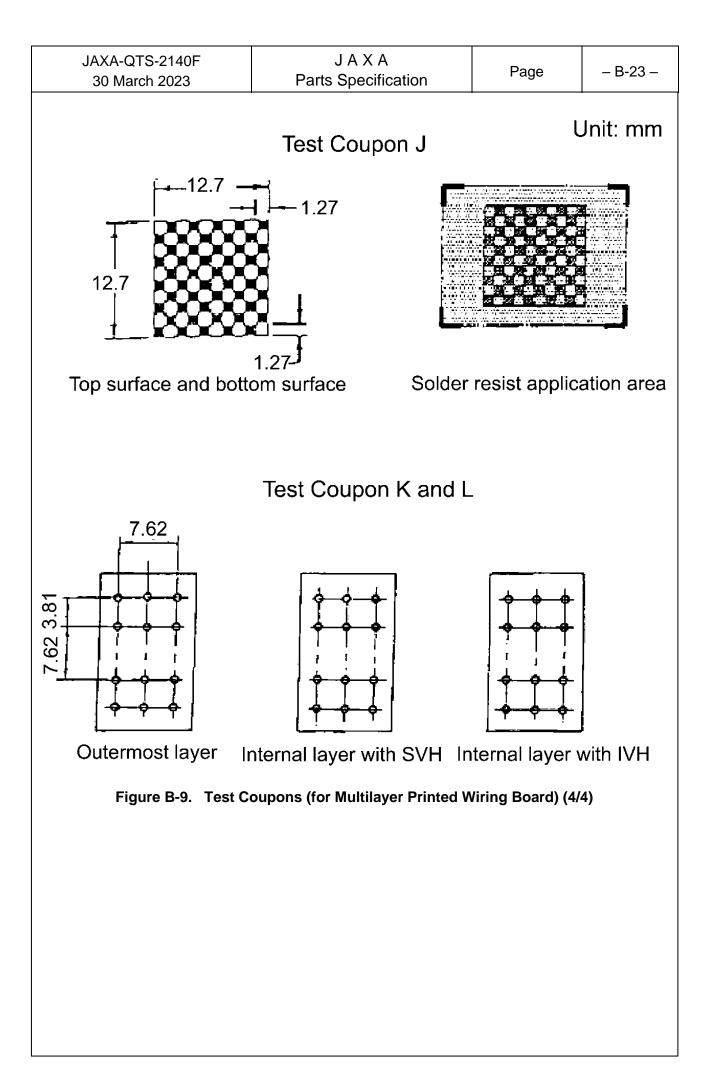


Figure B-9. Test Coupons (for Multilayer Printed Wiring Board) (3/4)



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$ \begin{array}{ c c c } \hline \begin matrix \\ \hline \begin matrix $		Table B-11. Qualification Test							
$ \begin{array}{ c c c c c } \hline Group & Order & Test item & Requirement Test method paragraph & Perduction printed wiring coupon (c) & Coupon (c) &$			Test			Pass/fail			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Group	Order	Test item	•		Production printed wiring	Test coupon	allowable	
$ \begin{array}{ c c c c c c } & & & & & & & & & & & & & & & & & & &$		1	Design and construction	B.3.3	B.4.4.2				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	I	2	marking and others Externals and construction Dimensions Marking	B.3.4.2		No. 1 to No. 6	D, E, F, G, H, K		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		3	Workmanship ⁽³⁾	B.3.5	B.4.4.3				
$\begin{array}{ c c c c c c c } \hline 1 & Through holes & B.3.4.4 & B.4.4.2.2 \\ \hline 1 & Through holes & B.3.4.4 & B.4.4.2.2 \\ \hline 2 & Terminal pull strength & B.3.9.1 & B.4.4.7.1 \\ \hline 3 & Solder resist thickness & B.3.4.5 & B.4.4.2.3 \\ \hline 1 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 2 & Hot oil resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 3 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 3 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 2 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 1 & Humidity and insulation \\ resistance & B.3.8.1 & B.4.4.6.3 \\ \hline 1 & Humidity and insulation \\ resistance & B.3.8.1 & B.4.4.6.1 \\ \hline 1 & Thermal stress & B.3.10.4 & B.4.4.8.4 \\ \hline 1 & Thermal stress & B.3.10.4 & B.4.4.8.4 \\ \hline 1 & Thermal stress & B.3.10.5 & B.4.4.8.5 & No.6 & N/A \\ \hline \hline \hline VII & 1 & Radiation hardness & B.3.10.5 & B.4.4.8.5 & No.6 & N/A \\ \hline \hline \hline VII & 1 & Radiation hardness & B.3.10.5 & B.4.4.8.5 & No.6 & N/A \\ \hline \hline \end{array}$	Ш	1	5	B.3.6	B.4.4.4	No. 1 to No. 6	С		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		2	Bow and twist	B.3.5.1	B.4.4.3.1		N/A		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		1	Through holes	B.3.4.4	B.4.4.2.2				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	111	2	Terminal pull strength	B.3.9.1	B.4.4.7.1	NO. 1	F		
$\begin{array}{ c c c c c c } \hline \mathbb{V} & \hline 2 & Hot oil resistance & B.3.10.3 & B.4.4.8.3 \\ \hline 3 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 1 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 2 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline 1 & Humidity and insulation resistance & B.3.8.1 & B.4.4.6.1 \\ \hline 2 & Dielectric withstanding voltage & B.3.10.4 & B.4.4.8.4 \\ \hline 1 & Thermal stress & B.3.10.4 & B.4.4.8.4 \\ \hline 1 & Thermal stress & B.3.10.5 & B.4.4.8.5 & No.6 & N/A \\ \hline \hline \\ \hline VII & 1 & Radiation hardness & B.3.10.5 & B.4.4.8.5 & No.6 & N/A \\ \hline \end{array}$		3	Solder resist thickness	B.3.4.5	B.4.4.2.3		J		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		1	Connection resistance	B.3.8.3	B.4.4.6.3				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	IV	2	Hot oil resistance	B.3.10.3	B.4.4.8.3	No. 2	D		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		3	Connection resistance	B.3.8.3	B.4.4.6.3				
$ \begin{array}{c c c c c c c c c } \hline V & 3 & Thermal shock (I) & B.3.10.1.1 & B.4.4.8.1 a) \\ \hline 4 & Circuitry & B.3.8.2 & B.4.4.6.2 \\ \hline 5 & Connection resistance & B.3.8.3 & B.4.4.6.3 \\ \hline & & & & & & & \\ \hline & & & & & & \\ \hline & & & &$		1	Circuitry	B.3.8.2	B.4.4.6.2				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		2	Connection resistance	B.3.8.3	B.4.4.6.3		Eand		
4CircuitryB.3.8.2B.4.4.6.25Connection resistanceB.3.8.3B.4.4.6.3 VI 1Humidity and insulation resistanceB.3.10.2B.4.4.8.22Dielectric withstanding voltageB.3.8.1B.4.4.6.1VII1Thermal stressB.3.10.4B.4.4.8.4VII2SolderabilityB.3.9.2B.4.4.7.2VIII1Radiation hardnessB.3.10.5B.4.4.8.5No.6	V		Thermal shock (I)	B.3.10.1.1	B.4.4.8.1 a)	No. 3			
VI1Humidity and insulation resistanceB.3.10.2B.4.4.8.2No. 4E2Dielectric withstanding voltageB.3.8.1B.4.4.6.1No. 4EVII1Thermal stressB.3.10.4B.4.4.8.4No. 5A, B and LVII2SolderabilityB.3.9.2B.4.4.7.2No. 6N/A			Circuitry	B.3.8.2	B.4.4.6.2		0.7		
VI 1 resistance $B.3.10.2$ $B.4.4.8.2$ No. 4E 2 Dielectric withstanding voltage $B.3.8.1$ $B.4.4.6.1$ No. 4EVII 1 Thermal stress $B.3.10.4$ $B.4.4.8.4$ No. 5 $A, B and$ L 2 Solderability $B.3.9.2$ $B.4.4.7.2$ $No. 6$ N/A		5	Connection resistance	B.3.8.3	B.4.4.6.3				
2Dielectric withstanding voltageB.3.8.1B.4.4.6.1AVII1Thermal stressB.3.10.4B.4.4.8.4No. 5 $A, B and$ LVII2SolderabilityB.3.9.2B.4.4.7.2No. 6 $H^{(6)}$ VIII1Radiation hardnessB.3.10.5B.4.4.8.5No. 6N/A	M	1	-	B.3.10.2	B.4.4.8.2	No. 4	F		
VII1Thermal stressB.3.10.4B.4.4.8.4No. 5A, B and L2SolderabilityB.3.9.2B.4.4.7.2 $H^{(6)}$ VIII1Radiation hardnessB.3.10.5B.4.4.8.5No. 6N/A		2	-	B.3.8.1	B.4.4.6.1	INO. 4	E		
2 Solderability B.3.9.2 B.4.4.7.2 B and H ⁽⁶⁾ J VIII 1 Radiation hardness B.3.10.5 B.4.4.8.5 No.6 N/A		1		B.3.10.4	B.4.4.8.4				
	VII	2	Solderability	B.3.9.2	B.4.4.7.2	INO. 5			
- 1 Materials B.3.2 N/A (7) N/A	VIII	1	Radiation hardness	B.3.10.5	B.4.4.8.5	No.6	N/A		
	-	1	Materials	B.3.2	N/A	(7)		N/A	

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. In order to qualify split boards, split board specimens shall be submitted as the production samples.

⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

⁽³⁾ Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the second test of Group II tests.

⁽⁴⁾ Group I test shall be performed on the test coupons which are to be provided for Group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

⁽⁵⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽⁶⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

⁽⁷⁾ Data to certify compliance with design specifications shall be submitted.

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30 Warch 2023	1 413	opecification					
B.4.3 Quality Conformance Inspection							
B.4.3.1 Quality Conformance Inspection (Group A)							
B.4.3.1.1 Sample							
The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be manufactured simultaneously. Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen. A "split board" means a board constructed of parts of the same patterns or parts of different patterns.							
B.4.3.1.2 Inspection	Items and Sample S	ize					
B-12. The For Group	and test order of Gro inspections within ea IV and V tests, one to Table B-12.	ach group shall be p	performed in the or	der listed.			

	Inspection					Pass/fail		
						of samples		
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring boards	Test coupon ⁽¹⁾	allo	ntity of wable fects
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	B.3.4.1 B.3.4.2 B.3.4.3	B.4.4.2.1	All	N/A		
	2	Workmanship ⁽²⁾	B.3.5	B.4.4.3				
II	1	Bow and twist	B.3.5.1	B.4.4.3.1	All	N/A		0
III	1	Circuitry	B.3.8.2	B.4.4.6.2	All	N/A		\succ
	1	Thermal stress	B.3.10.4	B.4.4.8.4		A, F and K (A, B and F) ^{(3), (4)}		(
IV	2	Through holes Conductive interface Plating thickness	B.3.4.4 b) e)	B.4.4.2.2 a) and d) c)	N/A	A, B and L (A and F) ⁽³⁾ , (4)		
V	1	Solderability	B.3.9.2	B.4.4.7.2	N/A	B and H (A and D) ⁽⁵⁾	J	

Table B-12. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ A letter inside the parentheses shows the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.
 ⁽²⁾ Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the first test of Group II tests.

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- ⁽³⁾ For a multilayer printed wiring board, test coupon A shall be inspected, when the corresponding product is provided with small via holes. Test coupons K and L shall be inspected when the corresponding products have IVH or SVH.
- ⁽⁴⁾ For a single-sided or double-sided printed wiring board, test coupon F shall be inspected, only when the corresponding product is provided with small via holes.
- ⁽⁵⁾ Test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.
- B.4.3.2 Quality Conformance Inspection (Group B)

B.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

B.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table B-13. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

	Inspection				Pass/fail	
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	B.3.6	B.4.4.4	С	
	1	Terminal pull strength	B.3.9.1	B.4.4.7.1	F	
1	2	Connection resistance	B.3.8.3	B.4.4.6.3		
	3	Hot oil resistance	B.3.10.3	B.4.4.8.3	D	
	4 C	Connection resistance	B.3.8.3	B.4.4.6.3		
	1	Circuitry	B.3.8.2	B.4.4.6.2		
	2	Connection resistance	B.3.8.3	B.4.4.6.3		0 1
III	3	Thermal shock (II)	B.3.10.1.2	B.4.4.8.1 b)	E and G ⁽¹⁾	
	4	Circuitry	B.3.8.2	B.4.4.6.2		
5	Connection resistance	B.3.8.3	B.4.4.6.3			
IV	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	E	
IV	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1)

Table B-13. Quality Conformance Inspection (Group B)

Note: ⁽¹⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

B.4.4 Methods for Test and Inspection

B.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

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B.4.4.2	Externals, Dimension	s, Marking and Others			
B.4.4.2.1	 Externals and Construction Design, construction, externals, dimensions (conductive patterns and edges) and marking of the printed wiring board shall be tested. a) Conductive patterns and edges Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument which has sufficient accuracy. b) Annular ring The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular ring shall be measured using an optical measuring instrument which has sufficient accuracy. 				
B.4.4.2.2	sufficient accuracy.				

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to the board IVH or SVH. e) Dielectric lay The dielectri in accordance f) Annular ring The annular accordance on an extern plated hole t wiring board distance fror The IVH and However, the	length and the vertical direction (See Figure B-10.) /er thickness c layer thickness shall be meas ce with paragraph B.4.4.2.2 a). ring shall be measured using n with paragraph B.4.4.2.2 a). al layer shall be from the inside o the outer edge of the annular . The annular ring on an intern n the drilled hole wall to the edge I SVH shall not be subjected to ey shall be inspected for the an	nicrosections prepared ne measurement of the surface (within the ho ring on the surface of al layer shall be measu ge of the land (see Figu the cross-sectional obs	in annular ring le) of the the printed ired by the ure B-10). servation.			
However, they shall be inspected for the annular ring in accordance with paragraph B.4.4.2.1 b).						

measurement of Layer-to-Layer Registration and Annular Ring Figure

B.4.4.2.3 Solder Resist Thickness

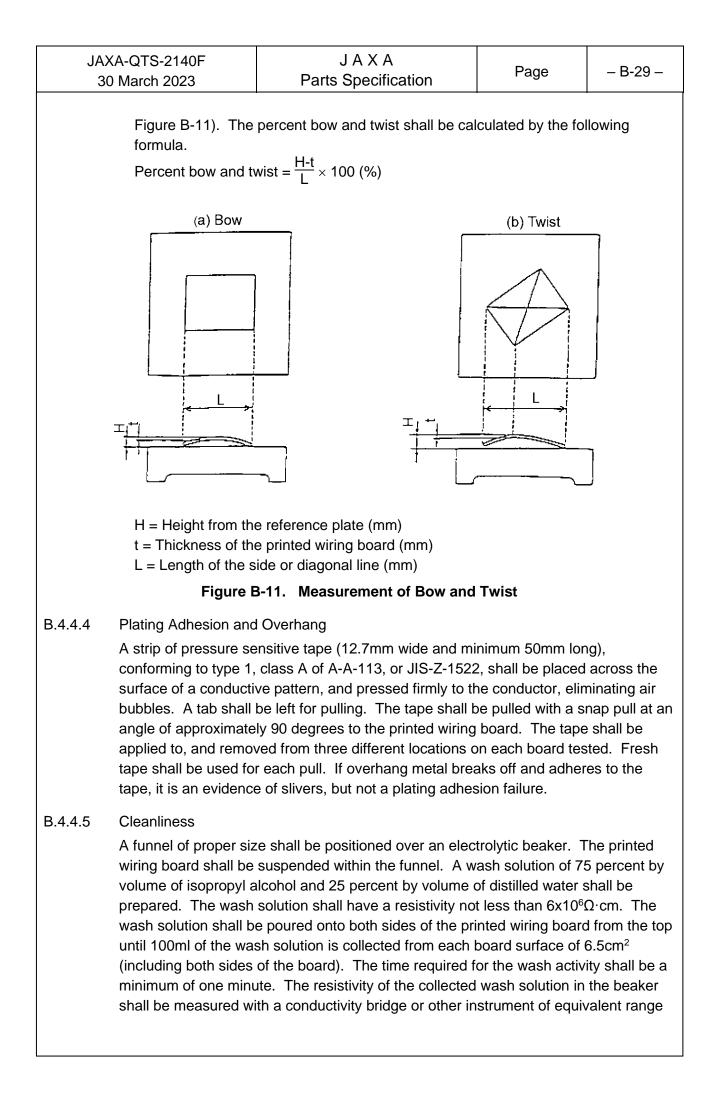
> The solder resist thickness shall be measured using a microsection prepared in accordance with paragraph B.4.4.2.2 a) at a magnification of minimum 200X.

B.4.4.3 Workmanship

The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

B.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see



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	and accuracy. The a perform the cleanline		thods specified in Ta	able B-14 may t	be used to
	-	Table B-14. Eq	uivalent Factors		
	Method	Resistivity (×10⁰Ω·cm)	Equivalent factor	Equivalents sodium chlor (µg/cm²)	
С	onductivity bridge	2	1	1.56	
0	mega Meter ⁽¹⁾	2	1.39	2.20	
B.4.4.6	Electrical Performan The electrical perform		ll be performed as fo	llows.	
		of MIL-STD-202. 1000V 30 sec ication: Betwe	e test shall be perform The following cond V _{AC} peak or 1000V _{DC} conds en conductive patter cally isolated pattern	itions shall appl ns of each laye	y. r and the
B.4.4.6.2	interconnected b) Circuit shorts A voltage of 25 conductive pat	l circuits to verify 50V _{DC} shall be aµ tern and all adja	shall be flown throug connectivity oplied between all co cent common termin of short-circuiting.	ommon terminal	s of each
B.4.4.6.3		tween the throug	gh hole terminals sha inal method capable		-
B.4.4.7	Mechanical Perform		hall be performed as	follows	
B.4.4.7.1	The mechanical perf		naii ne perioritieu as		
D.4.4.7.1	peeled and pulled	be cut with a sha toward the land	arp knife at minimum , and cut off by apply land so as not to deg	ring the sharp k	nife at the

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Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron. a) Solder a lead wire in to the through hole. b) Remove the lead wire from the through hole (solder removal) c) Re-solder the lead wire in to the through hole (solder removal) e) Re-solder the lead wire in the through hole (solder removal) e) Re-solder the lead wire in the through hole. The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum. After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula. $L \ge 1380 \times \frac{\pi \left\{ \left(d_a \right)^2 - \left(d_a \right)^2 \right\}}{4}$					
B.4.4.7.2	to the inspectio b) Surface soldera After the specir STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. The 25±6mm per se	ity solder shall be inspected using a n n specified in paragraph B.4.4.8.4	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp nto the solder ba econds and raise men shall be kep	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of t in the	

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	permitted. The after the solder	condition of solder on the conduc is solidified.	tive surface shall	be inspected
B.4.4.8	Environmental Perfor	mance		
	The environmental pe	erformance tests shall be performe	ed as follows.	
B.4.4.8.1	Thermal Shock			
	MIL-STD-202. The a) Thermal shock The temperatur The time for ste b) Thermal shock 1) For GF ba The test s step 2 and 2) For GI ba The test s temperatu	test shall be performed in accorda following conditions shall apply. (I) (applicable to qualification test) e range and number of cycles sha ep 2 and 4 shall be within 2 minute (II) (applicable to quality conforma- ase material shall be performed under the test of d 4 shall be within 2 minutes each se material shall be performed under the test of ure shall be +170°C, and the time hinutes each.) all be as specified as each. ance inspection) condition B-3. Th condition F-3. Th	l in Table B-4. le time for e high
B.4.4.8.2	Humidity and Insula	ation Resistance		
	cycles, and the during the test. be taken out of evaluated. b) Insulation resis The test shall b	s in Test Method 106 of MIL-STD- polarization voltage of 100V±10V Upon completion of step 6 of the the bath and dried immediately by	_{DC} shall be applie final cycle, the sp / blowing air at 25 ne test condition E	d to all layers becimen shall 5±5°C and 3, Test
B.4.4.8.3	Hot Oil Resistance			
	temperature. After	I be dried at 120±5°C for 2 hours a that, the specimen shall be imme cooled to room temperature. Imm cles.	rsed in oil or wax	at 260±5°C
B.4.4.8.4	Thermal Stress			
	shall be placed on specimen shall the floated in a solder l for a period of 10 s to be cooled. After shall be inspected	I be dried for 2 hours at 121 to 149 a ceramic plate in a desiccator, ar n be fluxed in accordance with the bath of composition Sn 63±5 perce econds. The specimen shall be p a check for any defects on the ex for any crack on the internal coppet tion prepared in accordance with I	nd cooled down. e detail specificati ent maintained at laced on a piece sternal surface, th er foil and lamina	The on and 288±5°C of insulator e sample te voids

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	temperature shall t molten surface of t	be measured at a probe depth not he solder.	to exceed 50mm	from the
B.4.4.8.5	Radiation Hardnes	S		
	• •	adiation shall be performed by usir ⁴ Gy per hour to the specimen in o	•	

 0.5×10^4 Gy to 1×10^4 Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4 Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph B.4.4.6.1 and B.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

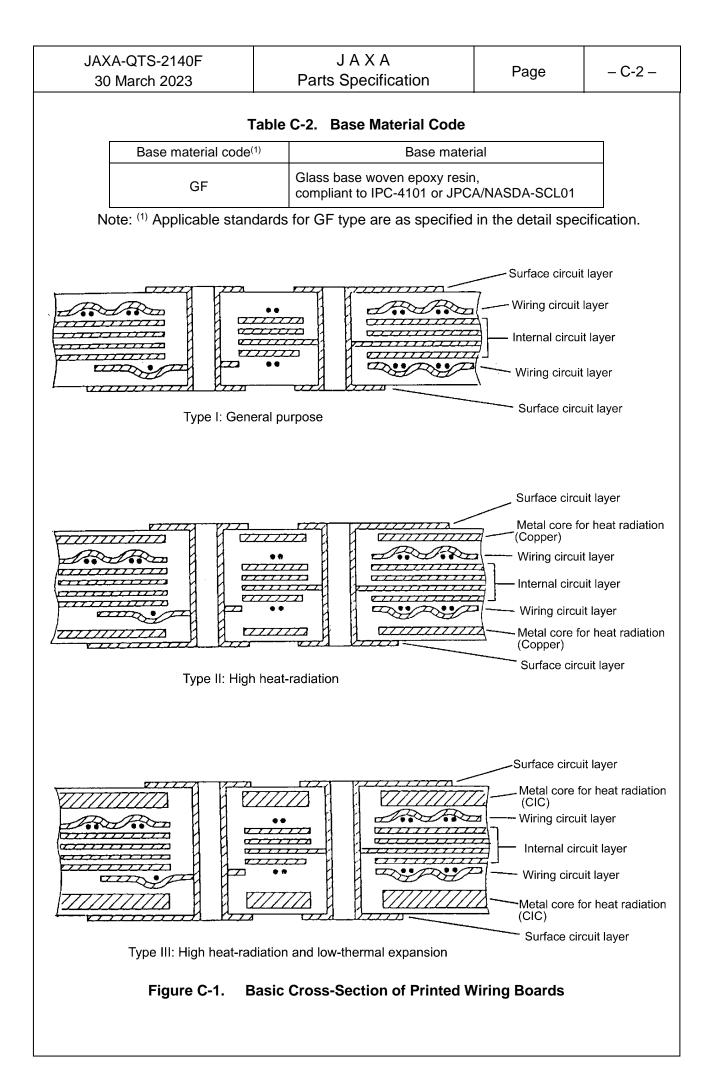
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	APPENDIX C		
	DISCRETE WIRING BOARDS,		
GL/	ASS BASE WOVEN EPOXY RES	N	
	BASE MATERIAL		
			0.4
•			
	al Code		
	n of Metal Cores for Heat Radiatio		
	ts ments		
-			
	/erage		
	d Laminate and Prepreg		
	for Heat Radiation		
-			
	st		
•			
C C	struction ng Drawings and Artwork Master (
	ng Drawings and Artwork Master (0	,
	Printed Wiring Board		
	Pattern		
	onnection		
,	Vidth		
	g		
•	g and Conductor Spacing		
	emperature Range		
	nsions, Marking and Others		
,	nd Construction		
5	les		
5			
1	<i>r</i> ist		
I. I.	and Overhang		
0			
	nance		
	ithstanding Voltage		

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

					-	
	JAXA-QTS-2 30 March 2		-	A X A pecification	Page	– C-1 –
			APPE			
				RING BOARDS, IVEN EPOXY RES	SIN	
			BASE N	IATERIAL		
C.1.	General					
C.1.1	Scope					
	provisions boards"). purpose s plates, and	for the discre The printed w tructure witho d high heat-ra	ete wiring board viring boards pr ut a metal core	requirements and ls (hereinafter refe ovide three types o , high heat-radiatio /-thermal expansio 5 "CIC").	rred to as "printed of structure; the go on structure with c	wiring eneral- opper
		•	rpe is as shown	shall be classified in Figure C-1. Classification		
	Туре		Structure		Metal core for heat	radiation
	I		General-purpo	se	No metal co	ore
	11		High heat-radia	tion	Copper	
	III	High heat-rac	diation and low-th	nermal expansion	CIC	
C.1.3					<u>N</u> letal core code of ir	<u>4</u> Number Iternal circuit layers
			es the part is fo	r space use and m	,	•
C.1.3.1		aterial Code				
	The bas	se material co	de is as shown	in Table C-2.		



	XA-QTS-2140F		JAXA	Pa	age	– C-3 –
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C.1.3.2	Classification	of Metal Cores for	r Heat Radiatio	n		
	The metal co	re for heat radiation	n is identified b	y a single capital	letter sy	mbol as
	shown in Tab					
	Table C	-3. Classification	n of Metal Cor	es for Heat Rad	iation	
		Symbol	Metal core for	heat radiation		
		Ν	No me	tal core		
		С	Cop	oper		
		Ι	С	IC		
C.2. Ar	oplicable Docum	ients				
C.2.1	Reference Docu	uments				
	The following do	ocuments are refer	ence documer	its of this append	ix.	
	•	110 Printed Wiring	g Board, Rigid,	General Specific	ation for	
	b) IPC-DW425	Design and E	nd Product Re	quirements for Di	screte W	iring Board
C.3. R	equirements					
C.3.1	Qualification Co	overage				
		all be valid for print	ted circuit boar	ds that are produ	ced by th	е
		ne that conforms t		•	•	
	• •	ecified in paragrap				
		diation listed in Tab		•		
	• •	e units are conside	•		•••••	
		3.2.4 is considered	•		0 71	
		solder resist inks u this coverage, the				
	•	pliance with the de			• •	
	•	he detail specificat	•			
	•	be specified in the		•	amoutor	
	0	·				
		Table C-4.	Qualification (Coverage		
					Nu	
		Number of lavers	Number of	Number of	1.01	imber of
Туре	Metal core for	Number of layers of metal core for	Number of surface	Number of wiring circuit	maxim	Imber of Tum internal
Туре	Metal core for heat radiation				maxim	
Туре		of metal core for	surface	wiring circuit	maxim	num internal

Copper

CIC

Ш

Ш

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C.3.2 Materia		pecified as follows and as specifie	d in paragraph 3	.3.
C.3.2.1 Cop The 410 ⁴ thick have base thick minin	per-Clad Laminat copper-clad lami 1 or JPCA/NASD ness of a dielect a nominal thickr a material type. T ness of 18µm as mum thickness o		the applicable st d on drawings. T 3mm, and a prep all be copper reg er shall have a n an internal layer for the material u	andard, IPC- The nominal reg shall ardless of the ominal shall have a
The coat copp coat	ing of phenoxy-e per wire shall be r ing shall be a mir	Sheets sulated mainly with polyimide resin poxy resin over the insulating coat not less than 0.10mm. The nomina himum of 0.01mm. The adhesive s as a main component.	ing. The nomina al thickness of th	l diameter of e insulating
The shall a)	I meet the following The metal core of constructed of co and the nominal The metal core of	eat radiation for the type II and III ng requirements. of the type II structure (high heat-ra opper. The copper purity shall be thickness of the core shall be not of the type III structure (high heat-r shall be constructed of CIC. The	adiation type) sha a minimum of 99 more than 0.15m adiation and low-	III be .8 percent, m. thermal
throu to th The whic	plating type shall ugh holes shall be e requirements o surface plating ty	be selected from the types specif e covered with copper plating. Pla f this specification. Surface plating rpe and the application area shall l by purchasers. Lands and through ting.	ting thickness sh g may be applied be as defined on	all conform l, if necessary. drawings
Tł ele	-	Plating oper plating shall be applied as a p nside through holes to form a con-	• •	
	ectrolytic Copper ne electrolytic cop	Plating oper plating shall have a minimum	purity of 99.5 pe	rcent.

JAXA-QTS-2140F 30 March 2023		J A X A Parts Specification	Page	– C-5 –
C.3.2.4.3	EN (Electroless Nic (Electroless Gold) as an undercoat wh on top of it. EN plating is a nick plating is cyan-free	oless Ni, Electroless Pd, Immersion ckel)/EP (Electroless Palladium)/IC plating is conditioned by EN plated hich are plated with EP and then of cel/phosphorus type, EP plating is type and IG plating is cyan type. EP and EG plating shall be 99.9%	G (Immersion Gol d on the copper c coated with IG and pure palladium ty	d)/EG ircuit pattern d EG plating
C.3.2.5	Solder Resist The solder resist app Class H or the equiva	lied on the printed wiring boards s llent.	hall conform to IF	PC-SM-840
C.3.2.6	vanish by any solven	produced by using epoxy resin ba t. The marking shall not adversely ility of the printed wiring boards.		•
C.3.3 [Design and Constructio	n		
C.3.3.1	Printed wiring boards prepared in accordant be indicated at grid p deviating from grid po If manufacturing draw created based on the dimensions of the loc manufacturing drawing lists shall be approve manufacturing drawing	ngs and Artwork Master (or Original shall be designed and their manu ce with this appendix. As a rule, a points, and the grid spacing shall be points shall be indicated, showing the rings and artwork masters (or original ations deviating from grid points in the grid points in the state of the purchaser. In the event of the grid attwork masters (or original attwork masters (or original)	facturing drawing all locations on dr e 1.27mm. Any lo ne corresponding inal production m cation of grid poin nay be omitted. T roduction masters of conflict betwee	gs shall be rawings shall ocation dimensions. asters) are nts and The s) and net n the
C.3.3.2	with etched patterns, layers, and two surfa- wiring board. A meta circuit layer and wirin	Viring Board shall be basically constructed of tw two wiring circuit layers which sar ce circuit layers with etched patter I core for heat radiation shall be for g circuit layer. The structure of the -1. In this figure, the printed wiring	ndwich the interna ns on both sides ormed between a e printed wiring b	al circuit of the printed surface oard shall be

planes.

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C.3.3.3 Conductive Pattern			

The circuit patterns on internal and surface layers shall conform to the approved artwork master (or original production master). The signal patterns of the wiring shall meet the approved wiring patterns.

C.3.3.4 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. The dimensional tolerance shall be in accordance with the requirements specified in Table C-5, unless otherwise specified.

Table C-5. Dimensional Tolerance

Unit: mm

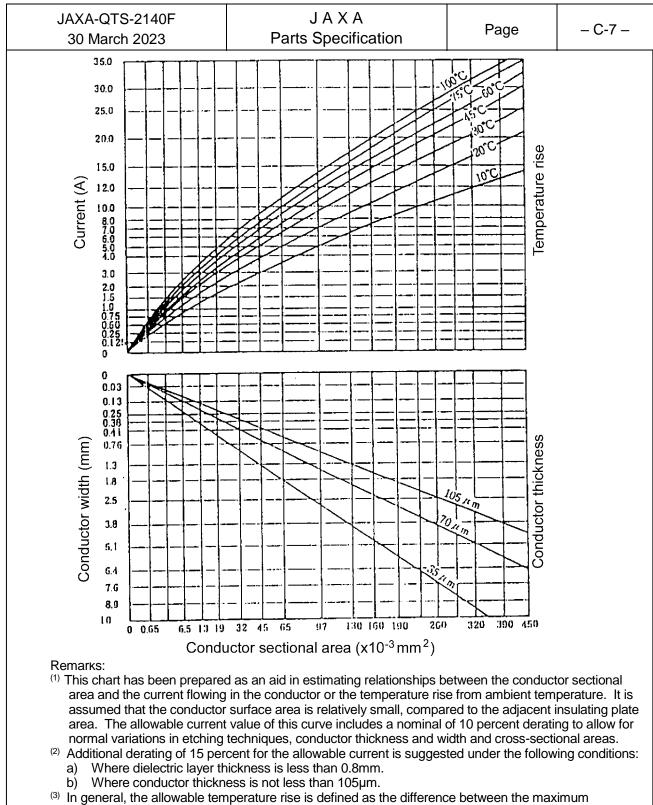
Item	Dimensional tolerance
External dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$.
Conductor width	± 0.10 for any conductor width. The minimum tolerance of the finished conductor width shall be 0.08.
Conductor spacing	-0.10 for any conductor spacing. The positive side tolerance is not specified. The minimum tolerance of finished conductor spacing on an external layer shall be 0.13.

C.3.3.5 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes.

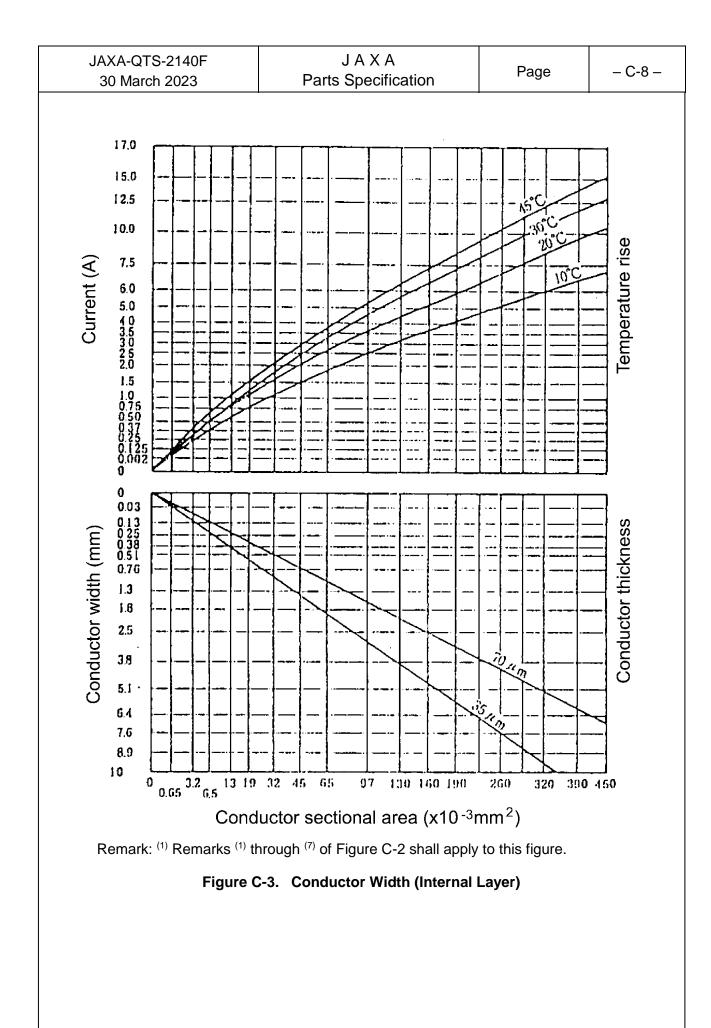
C.3.3.6 Conductor Width

The design width of the conductor shall be not less than 0.13mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures C-2 and C-3.



- (9) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.
- ⁽⁴⁾ For single conductor applications, the chart may be used for determining conductor widths, crosssectional area and allowable current (current-carrying capacity) for various temperatures rises.
- (5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current. The equivalent cross section is equal to the sum of the cross sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
- ⁽⁶⁾ The effect of heating due to heat generating parts is not considered.
- ⁽⁷⁾ The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure C-2. Conductor Width (External Layer)



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C.3.3.7	Annular Ring			
	inserting a lead, the d When a plated-throug annular ring shall be a	h hole provides an electrical lesign value of the annular rin h hole is used for inserting a a minimum of 0.30mm. The o ple shall be not less than 0.55	ng shall be not less th lead, the design valu design value of an an	an 0.25mm. ie of the
C.3.3.8	Wire Spacing and Co	nductor Spacing		
C.3.3.8.1	The design value o	f spacing between wires in p wires are crossed is not spe		ss than 0.3mr
C.3.3.8.2	Conductor Spacing			
	•	tor spacing on a circuitry laye		an 0.20mm.
	The specific condu	tor spacing on a circuitry laye ctor spacing shall be as spec uctor Spacing and Wire Spa	ified in Table C-6. acing (Design Value)
Γ	The specific condu	ctor spacing shall be as spec uctor Spacing and Wire Space en Minimum conductor	ified in Table C-6. acing (Design Value) nit: mm g
	The specific conduction Table C-6. Conduction Voltage applied between the specific conduction of the s	ctor spacing shall be as spec uctor Spacing and Wire Space en Minimum conductor	ified in Table C-6. acing (Design Value U Minimum spacin) nit: mm g
	The specific conduction Table C-6. Conductors, DC or AC _p -	ctor spacing shall be as spec uctor Spacing and Wire Space een Minimum conductor p (V) spacing	ified in Table C-6. acing (Design Value U Minimum spacin) nit: mm g
	The specific conductors, DC or AC _p -00 - 15	ctor spacing shall be as spec uctor Spacing and Wire Space en Minimum conductor p (V) Spacing 0.20	ified in Table C-6. acing (Design Value U Minimum spacin) nit: mm g
	The specific conductors, DC or AC _p - 0 - 15 16 - 30	ctor spacing shall be as spec uctor Spacing and Wire Space en Minimum conductor (V) Spacing 0.20 0.25	ified in Table C-6. acing (Design Value U Minimum spacin) nit: mm g
	The specific conduct Table C-6. Conduction Voltage applied betwee conductors, DC or AC _p - 0 - 15 16 - 30 31 - 50	ctor spacing shall be as spec uctor Spacing and Wire Space en (V) Minimum conductor spacing 0.20 0.25 0.38	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa) nit: mm g
	The specific conductors, DC or AC _p - 0 - 15 16 - 30 31 - 50 51 - 100	ctor spacing shall be as spec uctor Spacing and Wire Space en (V) Minimum conductor spacing 0.20 0.25 0.38 0.51	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa) nit: mm g
	The specific conductors, DC or AC _p - 0 - 15 16 - 30 31 - 50 51 - 100 101 - 300	ctor spacing shall be as spec uctor Spacing and Wire Space Pen Minimum conductor (V) 0.20 0.25 0.38 0.51 0.76	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa) nit: mm g
C.3.3.9	The specific conductors, DC or AC _p - 0 - 15 16 - 30 31 - 50 51 - 100 101 - 300 301 - 500 501 or higher	ctor spacing shall be as spec uctor Spacing and Wire Space (V) Minimum conductor (V) 0.20 0.25 0.38 0.51 0.76 1.52 (0.003xV)+0.1 re Range	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa 0.3 {12 mil}) g rallel
C.3.3.9	The specific conductors, DC or AC _p - 0 - 15 16 - 30 31 - 50 51 - 100 101 - 300 301 - 500 501 or higher	ctor spacing shall be as spec uctor Spacing and Wire Spacing Minimum conductor (V) 0.20 0.25 0.38 0.51 0.76 1.52 (0.003xV)+0.1	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa 0.3 {12 mil}) g rallel
	The specific conductors, DC or AC _{p-1} 0 - 15 16 - 30 31 - 50 51 - 100 101 - 300 301 - 500 501 or higher Operating Temperatur The printed wiring box	ctor spacing shall be as spec uctor Spacing and Wire Space uen Minimum conductor spacing 0.20 0.25 0.38 0.51 0.76 1.52 (0.003xV)+0.1 0.10	ified in Table C-6. acing (Design Value U Minimum spacin between wires in pa 0.3 {12 mil}) g rallel

C.3.4.1.1 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

C.3.4.1.2 Externals

Printed wiring boards shall not exhibit cracks nor separation around holes. There shall be no delamination on each layer or base material. Measling and crazing

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underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board and the spacing between conductors shall not be reduced by a maximum of 25 percent. Crazing along edges of the printed wiring boards shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the smaller of the minimum conductor spacing specified on drawings or 1.6mm. The cured solder resist shall be free from tackiness, blistering and delamination. Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the provisions of manufacturing drawings.

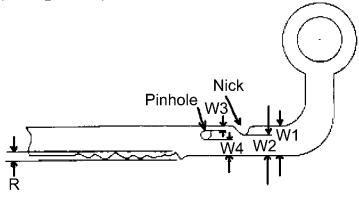
C.3.4.2 Dimensions

C.3.4.2.1 Externals

The external dimensions, finished hole diameter and conductor spacing shall be in accordance with the requirements of Table C-5.

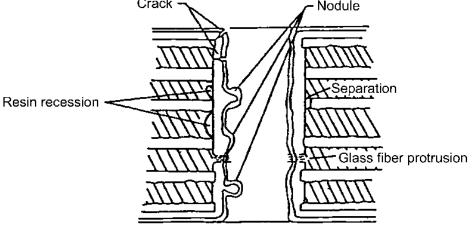
C.3.4.2.2 Conductor

The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100 mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.13mm in the difference between the convex and concave portions in any range of 13mm in length (see Figure C-4).



$$\begin{split} & \text{W1} \geq (\text{Minimum finished conductor width}) \geq 0.08 \text{ (mm)} \\ & \text{W2} \geq 0.80 \times (\text{Minimum finished conductor width}) \geq 0.08 \text{ (mm)} \\ & \text{W3+W4} \geq 0.80 \times (\text{Minimum finished conductor width}) \geq 0.08 \text{ (mm)} \\ & \text{R} \leq 0.13 \text{ (mm) in any range of 13 mm in length} \end{split}$$

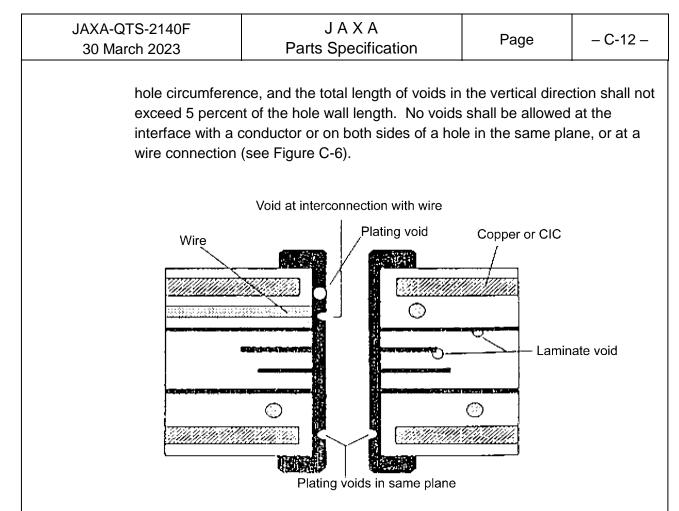
Figure C-4. Conductor Defects





a) Voids

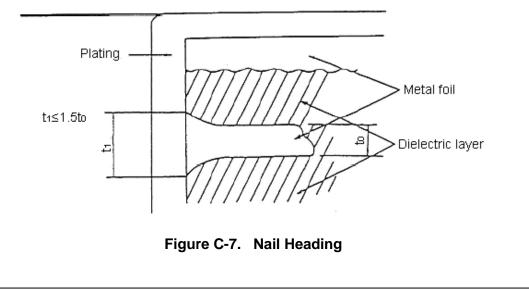
A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through





b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the interface circumference in horizontal microsection, and shall not exceed 50 percent of the interface in the same plane in vertical microsection. The resin smear at the interface of through hole plating and a wire shall be a maximum of 50 percent of the wire diameter in the same plane. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness. Nail heading at the interface with a wire is not specified (see Figure C-7).



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 Plating thickness and others The thickness of plating and solder coating shall be as specified in Table C-7. 							
Table C-7. Plating or Coating Thickness							
		Ur	nit: µm				
Plating material	Surface and through ho	Surface and through hole plating thickness					
Electroless copper	Min. 30 in design value	Min. 30 in design value					
Electrolytic copper	The finished thickness of elect	Min. 30 in design value The finished thickness of electroless and electrolytic copper plating shall be minimum 45µm in total.					
EN : Electroless nickel ⁽¹⁾	3.00 to 8.00						
EP : Electroless palladium ⁽¹⁾	0.05 to 0.36						
IG + EG : Immersion gol	d + 0.10 to 0.40						
Electroless gold plating ⁽¹⁾							
	eet the requirements specified in drav	vings. If not specif	ied in the				
drawings, it shall be as	s specified here.						
 d) Layer-to-layer registration The layer-to-layer registration error shall not exceed 0.35mm, except for wiring layers. e) Dielectric layer thickness The dielectric layer between conductor layers shall be no less than 0.08mm in thickness. The thickness of a dielectric layer where wires are crossed is not specified. f) Annular ring When the annular rings of internal and external layers are measured in accordance with C.4.4.2.2 f), the annular ring of a plated-through hole shall be a minimum of 45µm in diameter. The annular ring of a non-plated-through hole shall be not less than 0.38mm in diameter and contain no defects. g) Undercut The undercut along a conductor edge shall not exceed the total thickness of the copper foil and plated copper. h) Spacing between hole wall plating and internal conductor The spacing between the hole wall plating and an internal conductor shall be not less than 0.20mm. 							
C.3.5 Workmanship Printed wiring boards shall not exhibit defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.							

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C.3.5.1	Bow and Twist					
	When printed wiring boards are tested as specified in paragraph C.4.4.3.1, the maximum limit for bow and twist shall be 1.5 percent, unless otherwise specified on					
	manufacturing drawings.					
C.3.5.2	Repair					
	The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.					
C.3.6	Plating Adhesion and Overhang					
	When printed wiring boards are tested as specified in paragraph C.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.					
C.3.7	Cleanliness					
	When tested as specified in paragraph C.4.4.5, printed wiring boards shall meet the following requirements.					
	a) The printed wiring boards shall exhibit no ionic contamination and fouling including					
		corrosion product, salt, soot, greas erial and flux residues.	se, finger print, m	old release		
	• •	e solvent extract shall be not less	than 2×10 ⁶ Ω·cm.			
C.3.8	Electrical Performance					
	The printed wiring board shall meet the following electrical requirements.					
C.3.8.1						
		boards are tested as specified in p breakdown, flashover or sparkove	0 1	.1, there		
C.3.8.2	Insulation Resistance					
	not less than $500M\Omega$	ified in paragraph C.4.4.6.3, the in where wires are crossed, betweer sircuit layers or at metal core for he	n wires in parallel			
C.3.8.3	Circuitry					
		boards are tested as specified in p uit or short-circuiting between circu	•			

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C.3.8.4							
	time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured. Ri= $2\rho \frac{I}{W \cdot t}$ (m Ω)						
	(mΩ·mm) I: Distance be W: Conductor w t: Conductor th b) Test pattern G						
	Mechanical Performance Printed wiring board shall meet the following mechanical requirements.						
C.3.9.1	 C.3.9.1 Terminal Pull Strength When tested as specified in paragraph C.4.4.7.1, printed wiring board shall meet the following requirements. a) Terminal pull 						
	C.4.4.2.1, there c) Microsection of t When printed wi	ring boards are inspected visually shall be no loosening around the t	hrough holes.	cordance			
C.3.9.2	Solderability When tested as spec	ified in paragraph C.4.4.7.2, printe	ed wiring boards s	shall meet the			
	 following requirement a) Hole solderabilit The through hole solder. b) Surface solderal 	ts. y e inside wall and land surface shal	l exhibit proper w	etting of			

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	uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they shall not be concentrated at a point.						
C.3.10 E	nvironmental Perform	ance					
P	rinted wiring board sha	all meet the following environmenta	al requirements.				
C.3.10.1	Thermal Shock						
C.3.10.1.1	When printed wirin shall be no open c wiring boards shall	(applicable to qualification test) g boards are tested as specified in rcuit, blistering, measling, crazing meet the requirements specified in ge in connection resistance betwee han 10 percent.	or delamination. n paragraph C.3.	Printed 8.3 after the			
C.3.10.1.2	When printed wirin shall be no open ci wiring boards shall	(applicable to quality conformance g boards are tested as specified in rcuit, blistering, measling, crazing meet the requirements specified in ge in connection resistance betwee han 10 percent.	n paragraph C.4.4 or delamination. n paragraph C.3.	Printed 8.3 after the			
C.3.10.2	Hot Oil Resistance						
When printed wiring boards are tested as specified in paragraph C.4.4.8.3, there shall be no open circuit, blistering, measling, crazing or delamination. The printed wiring boards shall meet the requirements specified in paragraph C.3.8.3 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.				he printed 3 after the			
C.3.10.3	Thermal Stress						
	When tested as spec following requiremen	ified in paragraph C.4.4.8.4, printe ts.	d wiring boards s	shall meet the			
	blistering or dela		plating and condu	uctors,			
	There shall be n	s, metal cores for heat radiation o cracks in the vertical microsectio es or metal cores for heat radiation	•	es in internal			
	permitted, provid	with the longest dimension of 76µn led the conductor spacing within a requirements of the minimum conc rawings.	layer or betweer	n layers shall			

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		50 March 2025		cation		
C.3.′	10.4	4 Humidity Resistance				
		When tested as speci the following requirem		4.4.8.2, printe	ed wiring boards	shall meet
		a) Bow and twist	nit for bow and twist	shall be 1.5 n	ercent	
		b) Dielectric withsta	nding voltage			
		c) Insulation resista	o insulation breakdov nce	vn, nasnover (or sparkover.	
		between wires in	sistance shall be not parallel, at the surfa			
		core layer for hea d) Externals	at radiation.			
		There shall be no blistering or dela	o measling, cracks, s mination.	eparation of p	plating and condu	ctors,
C.3.	10.5	5 Radiation Hardness				
		When printed wiring b		• •	•	
		shall be no defects su resistance between co	•			
		requirements specifie				
C.4.	C	Quality Assurance Provision	ons			
C.4.	1	In-Process Inspection				
		The in-process inspection	on shall be as specifi	ed in Table C·	-8.	
		Та	ble C-8. In-Proces	s Inspection		
			Deguirement	Test metho		of samples
N	lo.	Inspection item	Requirement paragraph	Test metho paragrapl		Test
		Externals, construction and dimensions of internal layers		C.4.4.2.1	~~~~~	
		Externals and constructio	n C.3.4.1 C.3.4.2		100%	100%

Notes:

Dimensions Marking

2 Cleanliness⁽²⁾

Workmanship⁽¹⁾

⁽¹⁾ The requirements specified in paragraph C.3.5.1 are not applied.

⁽²⁾ The cleanliness inspection shall be performed for the production printed wiring boards which are to be coated with solder resist, immediately before the application of solder resist.

C.4.4.3

C.4.4.5

2(3)

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C.3.4.2

C.3.4.3

C.3.5

C.3.7

⁽³⁾ Two production printed wiring boards shall be selected from the lot to be coated with solder resist at the same time.

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C.4.2 Qualification Test

C.4.2.1 Sample

Samples shall be production printed wiring boards approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons specified in Table C-8 shall also be submitted. The samples shall consist of the test coupons and sample products manufactured simultaneously.

C.4.2.2 Test Items and Number of Samples

The tests within each group shall be performed in the order listed in Table C-9. Upon completion of Group I through IV tests, Group V through X tests shall be performed using specimens allocated to the appropriate group tests. Group V through X tests may be performed in any order regardless of group number. However, the tests within each group of V through X shall be performed in the specified order. The number of samples submitted for each test shall be as specified in Table C-9.

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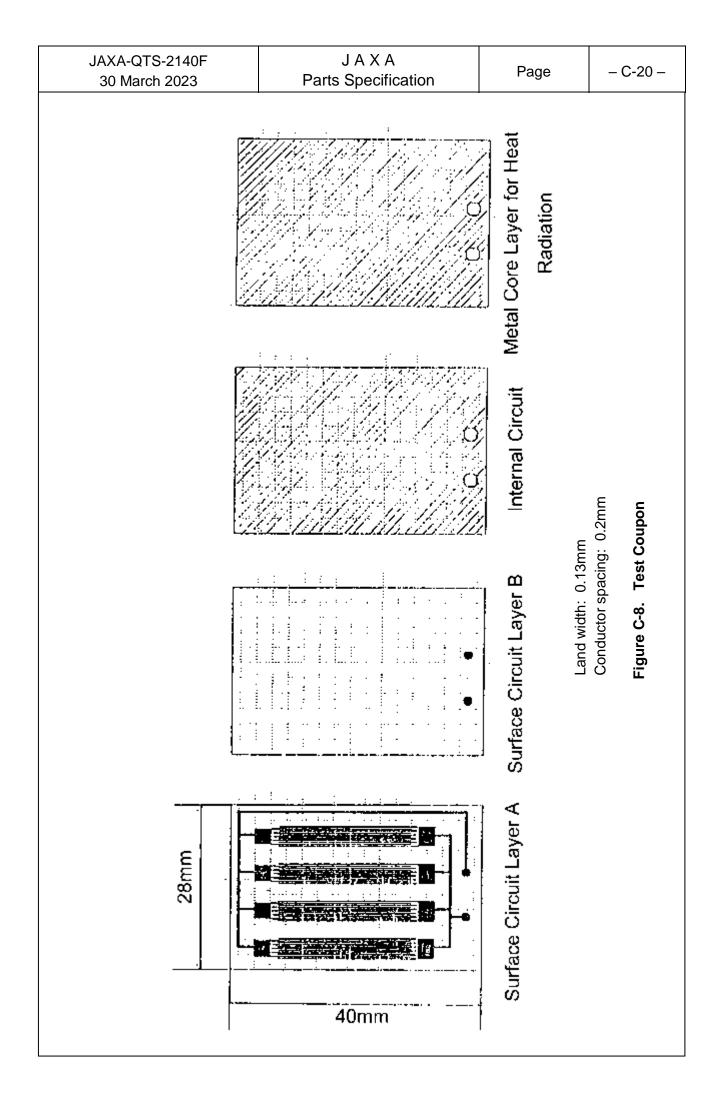
	Test		Requirement Test method	Sampl	Samples			
Group	Order	Test item			No. ⁽¹⁾	Test coupon	Quantity of allowable defects	
		Externals, dimensions, marking and others					1	
	1	Externals and construction	C.3.4.1	C.4.4.2.1	No. 1 to	A 45 C		
Ι		Dimensions	C.3.4.2		No. 6	A to G		
		Marking	C.3.4.3					
	2	Workmanship	C.3.5	C.4.4.3				
Ш	1	Circuitry	C.3.8.3	C.4.4.6.4	No. 1 to No. 6	A to E, G		
111	1	Connection resistance	C.3.8.4	C.4.4.6.2	No. 1 to No. 6	G		
	1	Dielectric withstanding voltage	C.3.8.1	C.4.4.6.1	No. 1 to No. 6	A to E		
IV	2	Insulation resistance	C.3.8.2	C.4.4.6.3	No. 1 to No. 6	A to E		
V	1	Through holes	C.3.4.4	C.4.4.2.2	No. 1	A, E, G		
VI	1	Plating adhesion and overhang	C.3.6	C.4.4.4	No. 2	F		
	2	Marking	C.3.4.3	C.4.4.2.3	No. 2	-		
VII	1	Thermal stress	C.3.10.3	C.4.4.8.4	No. 3	E		
VII	2	Solderability	C.3.9.2	C.4.4.7.2	No. 3	B, E		
	1	Terminal pull strength	C.3.9.1	C.4.4.7.1	No. 4	F		
VIII	2	Hot oil resistance	C.3.10.2	C.4.4.8.3	No. 4	A to E, G		
IX	1	Thermal shock (I)	C.3.10.1.1	C.4.4.8.1 a)	No. 5	A to E, G		
	2	Radiation hardness	C.3.10.5	C.4.4.8.5	No. 5	A to E, G		
Х	1	Humidity resistance	C.3.10.4	C.4.4.8.2	No. 6	A to E, G) 	
-		Materials	C.3.2	N/A	(2)	-	N/A	

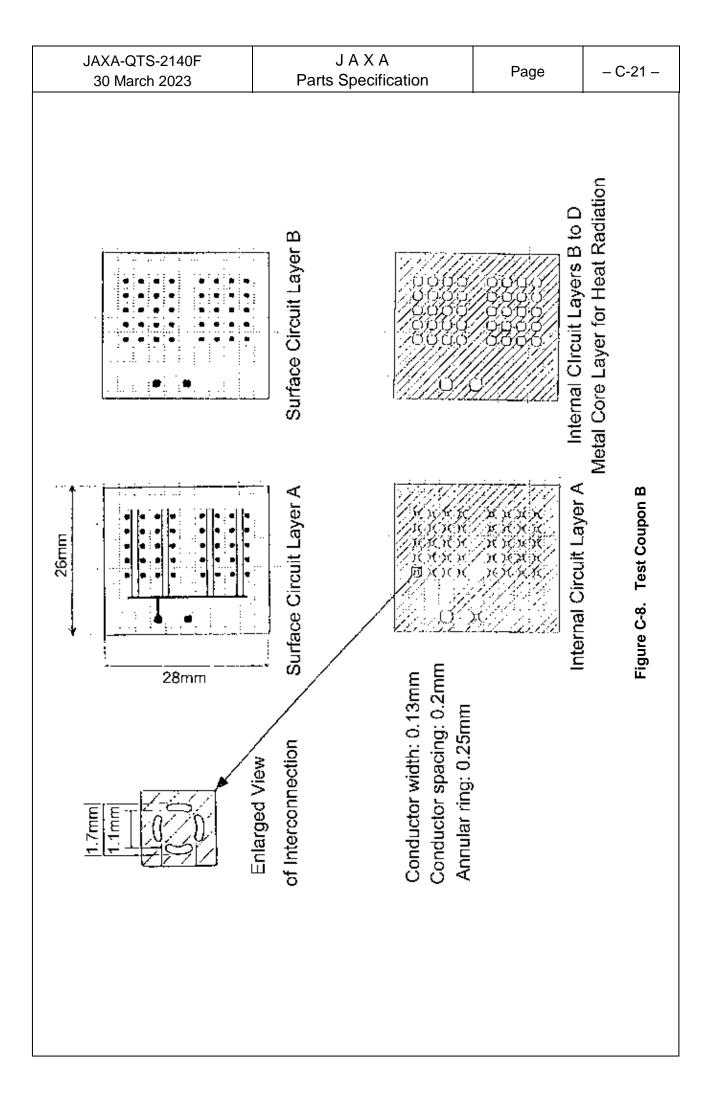
 Table C-9.
 Qualification Test

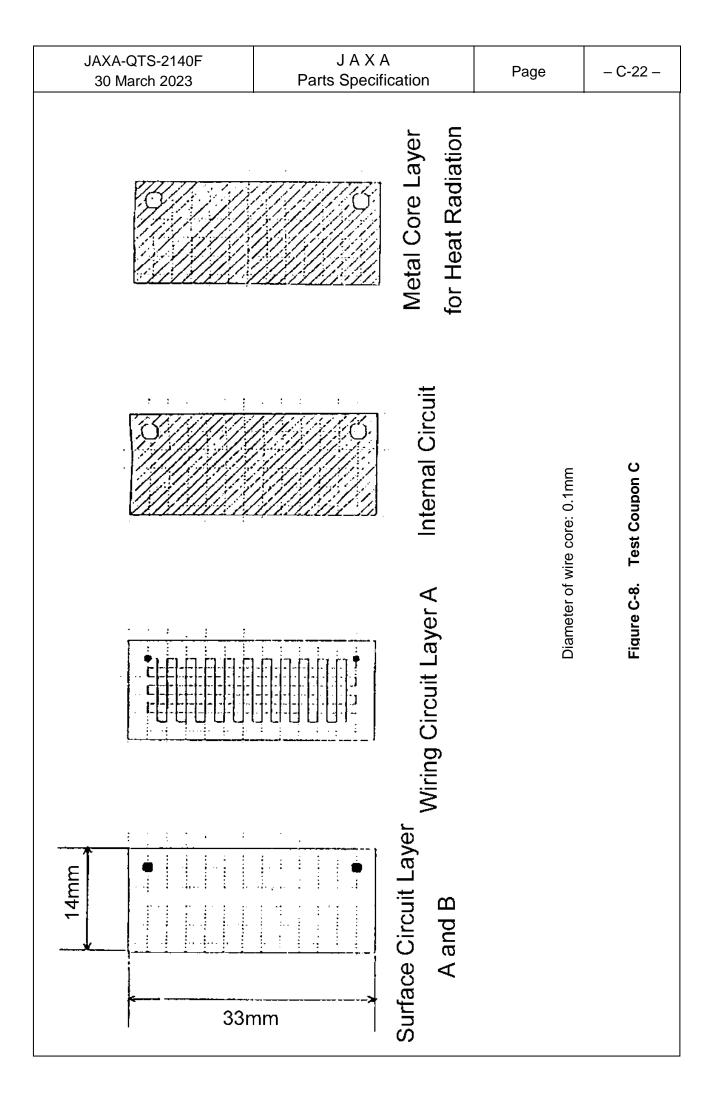
Notes:

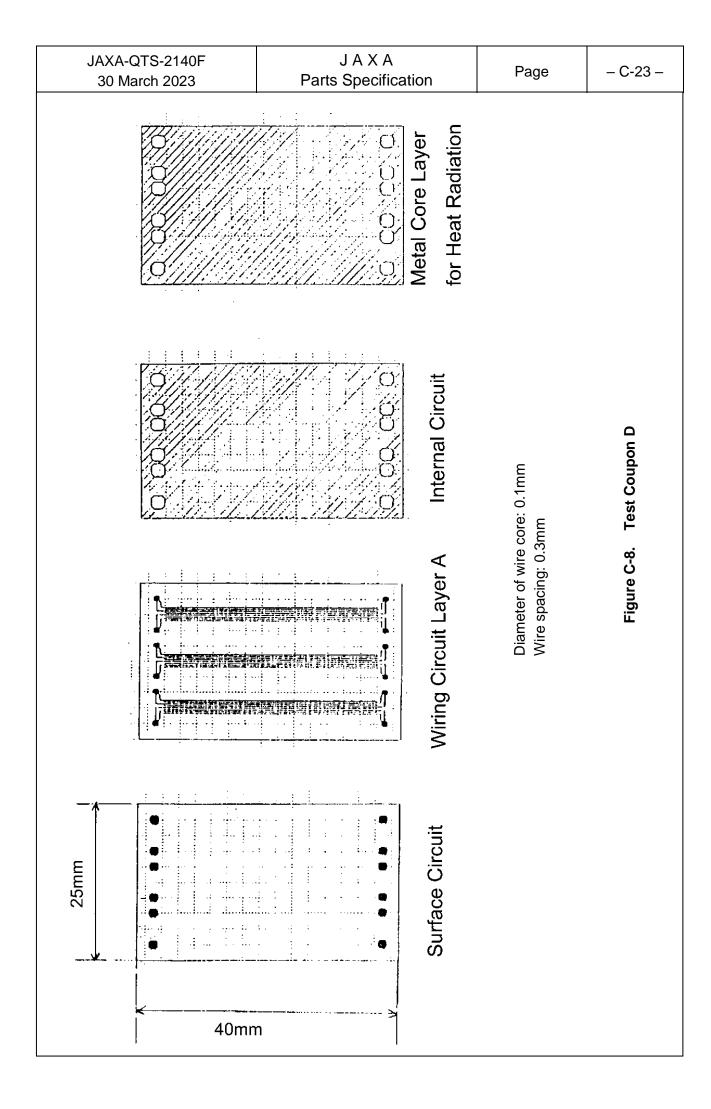
⁽¹⁾ Six production printed wiring boards shall be prepared for each structure type of the printed wiring board.

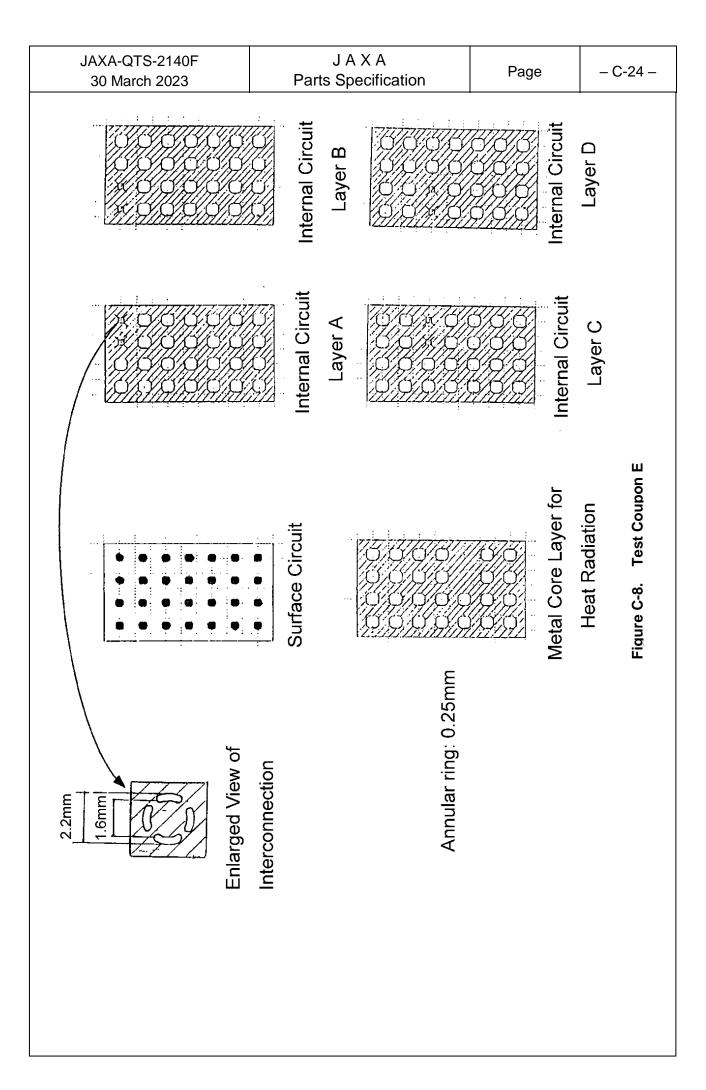
⁽²⁾ Data to certify compliance with design specifications shall be submitted.

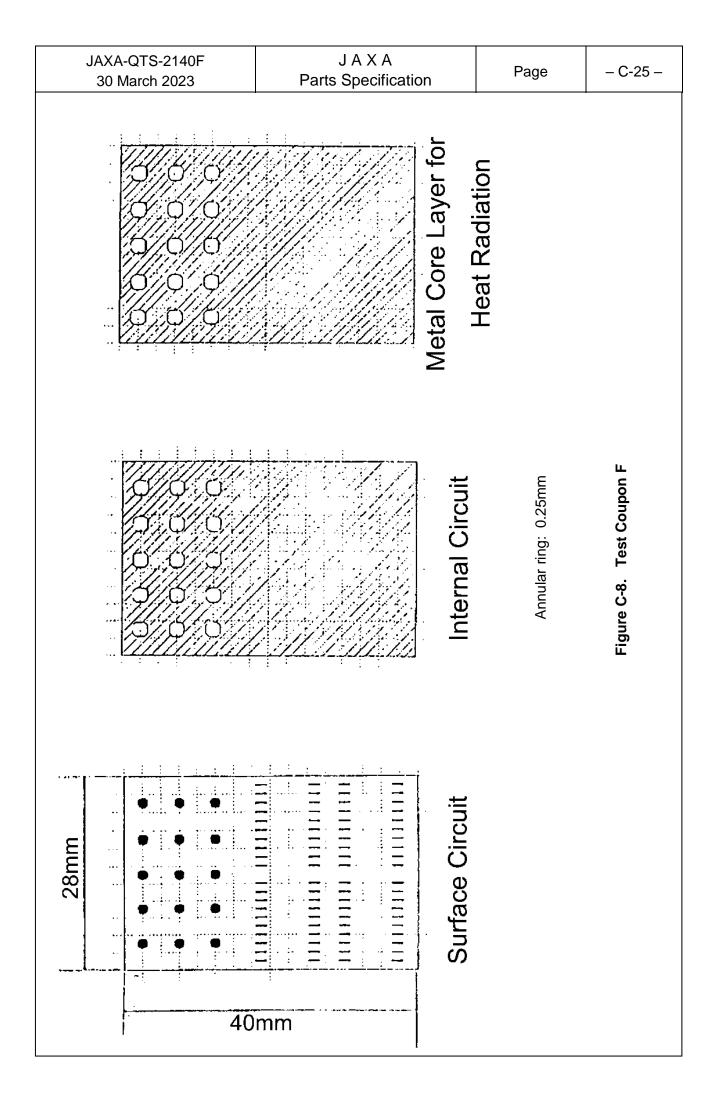


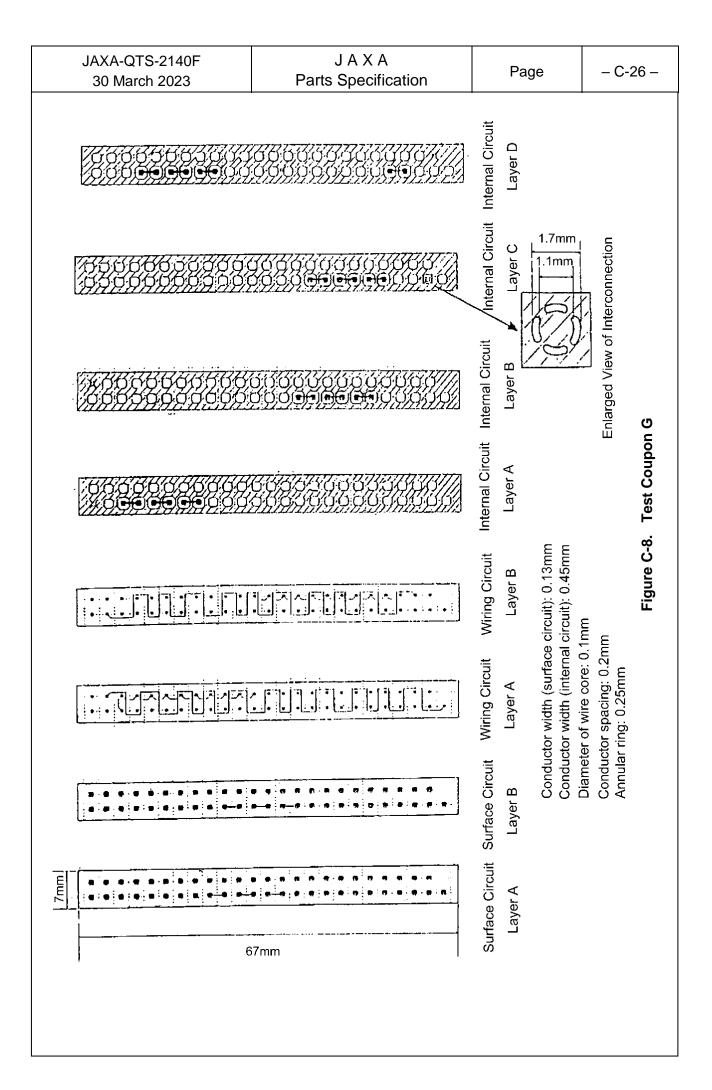












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C.4.3 Quality Conformance Inspection					
C.4.3.1 Quality Conformance	Inspection (Group A)				
C.4.3.1.1 Sample The quality conformance inspection shall be performed on all products. Test coupons and sample products shall be manufactured simultaneously.					
C.4.3.1.2 Inspection Items and Sample Size					

The items and test order of Group A inspection shall be in accordance with Table C-10. The inspections within each group shall be performed in the order listed.

Inspection			Test	Samples			
Group	Order	Inspection item	Requirement paragraph	method paragraph	Production printed wiring board	Test coupon	
		Externals, dimensions, marking and others					
	1	Externals and construction	C.3.4.1	C.4.4.2.1	A 11		
I		Dimensions	C.3.4.2 ⁽¹⁾		All	A to G	
		Marking	C.3.4.3				
	2	Workmanship	C.3.5	C.4.4.3			
Ш	1	Circuitry	C.3.8.3	C.4.4.6.4	All	-	
	1	Connection resistance	C.3.8.4	C.4.4.6.2	-	G ⁽²⁾	
IV	1	Dielectric withstanding voltage	C.3.8.1	C.4.4.6.1	All	-	
	2	Insulation resistance	C.3.8.2	C.4.4.6.3	-	A to E ⁽²⁾	
V	1	Through holes	C.3.4.4	C.4.4.2.2	-	G ⁽²⁾	
VI	1	Plating adhesion and overhang	C.3.6	C.4.4.4	Sampling ⁽²⁾	-	
VII	1	Thermal stress	C.3.10.3	C.4.4.8.4	-	E ⁽²⁾	
VII	2	Solderability	C.3.9.2	C.4.4.7.2	-	B, E ⁽²⁾	
VIII	1	Hot oil resistance	C.3.10.2	C.4.4.8.3	-	G ⁽²⁾	

Table C-10. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ Sampling inspection shall be performed and the AQL shall be 2.5%.

⁽²⁾ Sampling inspection shall be performed and the "Inspection Level II" of JIS Z 9015-1 and the AQL of 2.5% shall be applied.

C.4.3.2 Quality Conformance Inspection (Group B)

C.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

C.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table C-11. The inspections within each group shall be performed in the order listed.

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Table C-11.	Quality	Conformance	Inspection	(Group B)
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Inspection				Samples		
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring board	Test coupon
I	1	Terminal pull strength	C.3.9.1	C.4.4.7.1	-	F ⁽¹⁾
II	1	Thermal shock (II)	C.3.10.1.2	C.4.4.8.1 b)	-	A to E, $G^{(1)}$
111	1	Humidity resistance	C.3.10.4	C.4.4.8.2	-	A to E, G ⁽¹⁾

Note: ⁽¹⁾ Sampling inspection shall be performed and the "Inspection Level II" of JIS Z 9015-1 and the AQL of 2.5% shall be applied.

C.4.4 Methods for Test and Inspection

C.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 20% to 80%, and a luminance of 750 lx as a minimum.

C.4.4.2 Externals, Dimensions, Marking and Others

C.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of printed wiring boards shall be tested. The externals shall be inspected visually.

- a) Conductive patterns and edges
 Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument with a sufficient accuracy.
- b) Annular ring

The annular ring on an external layer shall be measured from the internal surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular ring shall be measured using an optical measuring instrument with a sufficient accuracy.

C.4.4.2.2 Through Holes

a) Vertical microsection

The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, base material thickness and plating thickness) at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board's length direction.

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 b) Horizontal micro The printed wiri observe the inter interface betwee hole shall be mi polished in para layer. The integ (interconnection magnification of c) Plating thickness (1) The plating thickness (2) EP and IG + observation usin shall be measure system on the the d) Layer-to-layer r The layer-to-layer r The layer-to-layer r 	psection ng board specimen shall be cut erface of the wire and plating ins en the internal conductor layer a crosectioned. Each microsection llel to the microsection to expose grity of the interfaces of wire and is in the horizontal direction) sha 50 to 100X. s hickness shall be measured usin paragraph C.4.4.2.2 a) at a ma shall be averaged from three de colated thick or thin sections sha EG plating thickness can not be ng an optical instrument. There red by using the X-ray fluoresce poard surface.	ide the through hol and plating inside the on shall be encapsu- se the wire and the l internal conductor all be inspected at a ng microsections p agnification of minin sterminations for a all not be used for a e measured by the fore, those plating the fore, those plating the fore with paragraph he hole in the direct	le. The ne through ulated and conductor a prepared in mum 200X plated- averaging. cross-sec thickness measurem n of 25 to C.4.4.2.2
	ne difference in centerline loca most eccentric to one anothe		ds
Copper or CIC Wire			
Measurement of		easure each land a determine center	and



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	 in accordance w f) Annular ring Measurement of surface (within on the surface of shall be measu land (see Figure g) Undercut g) Undercut The undercut se accordance with h) Spacing betwee The spacing betwee 	ayer thickness shall be measured with paragraph C.4.4.2.2 a). of the annular ring on an external la the hole) of the plated hole to the of the printed wiring board. The a red by the distance from the drilled	ayer shall be from outer edge of the nnular ring on an d hole wall to the section prepared onductor	n the inside annular ring internal layer edge of the in
C.4.4.2.3	Marking The marking test s deterioration shall a) The specimen 11 seconds.	hall be performed under the follow be inspected visually. shall be immersed in solder of 260 shall be immersed in isopropyl alc 35 minutes.) to 270°C for a p	eriod of 10 to
C.4.4.2.4		kness hickness shall be measured using aragraph C.4.4.2.2 a) at a magnific	•	•
				20070
-	Workmanship The workmanship sha as follows.	all be inspected visually. The bow	and twist shall b	e inspected

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C.4.4.3.1	with its convex side and the highest po	board specimen shall be placed h e facing upward, and the distance int of the printed wiring board shal how and twist shall be calculated b wist = $\frac{H-t}{L} \times 100$ (%)	between the refe I be measured (s	rence plate ee Figure C-
	T = Heigh $t = Thicknet$ $L = Length$	Bow T T T T T T T T T T T T T		
C.4.4.4	of pressure sensitive conforming to type I, surface of a conductive bubbles. A tab shall angle of approximate applied to, and remove tape shall be used for	Overhang ormed in accordance with paragra tape (12.7mm wide and a minimu class A of A-A-113, or JIS-Z-1522 ve pattern, and pressed firmly to the be left for pulling. The tape shall be ly 90 degrees to the printed wiring ved from three different locations of r each pull. If overhang metal breas slivers, but not a plating adhesion	m of 50mm in ler , shall be placed ne conductor, elir pe pulled with a s board. The tape on each board tes aks off and adher	ngth), across the ninating air nap pull at an e shall be sted. Fresh
C.4.4.5	wiring board shall be volume of isopropyl a prepared. The wash	e shall be positioned over an elect suspended within the funnel. A w lcohol and 25 percent by volume solution shall have a resistivity no e poured onto both sides of the pr	rash solution of 7 of distilled water s t less than 6x10 ⁶	5 percent by shall be Ω·cm. The

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until 100ml of the wash solution is collected from each board surface of 6.5cm² (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table C-12 may be used to perform the cleanliness test.

Method	Resistivity (×10 ⁶ Ω·cm)	Equivalent factor	Equivalents of sodium chloride (µg/cm²)
Conductivity bridge	2	1	1.56
Omega Meter ⁽¹⁾	2	1.39	2.20
lonograph ⁽²⁾	2	2.01	3.10
Ion Chaser ⁽³⁾	2	3.25	3.81

Table C-12. Equivalent Factors

Notes:

⁽¹⁾ Alpha Metals Incorporated, "Omega Meter"

⁽²⁾ Alpha Metals Incorporated, "Ionograph"

⁽³⁾ E. I. Dupont Company, Incorporated, "Ion Chaser"

C.4.4.6 Electrical Performance

The electrical performance tests shall be performed as follows.

C.4.4.6.1 Dielec	ric Withstanding	Voltage
------------------	------------------	---------

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: 1000V±25V_{DC}
- b) Duration: 30±3 seconds
- c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.
- C.4.4.6.2 Connection Resistance

The resistance between the through hole terminals shall be measured using a measuring instrument of four-terminal method capable of measuring a resistance below $0.5m\Omega$.

C.4.4.6.3 Insulation Resistance

The insulation resistance test shall be performed in accordance with the Test Method 302 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: 500V_{DC}
 - b) Duration: 1 minute

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C.4.4.6.4	interconnected b) Circuit shorts A voltage of 250 conductive patt	as a maximum shall be flown thro circuits to verify connectivity. DV _{DC} shall be applied between all o ern and all adjacent common term non-existence of short-circuiting.	common terminal	s of each
C.4.4.7	Mechanical Performa	nce		
	The mechanical perfo	ormance tests shall be performed a	as follows.	
C.4.4.7.1	 peeled and pulled ti joining point of the strength. Then, a lead wire si and the following pi using a soldering in a) Solder a lead with b) Remove the lead c) Re-solder the lead d) Remove the lead e) Re-solder the lead e) Re-solder the lead completely during the resoldering. The set the tip temperature iron without bringin board. The heating After the completion a tensile tester at re- forward and verticad (L) or any failure on be regarded as a failed. 	be cut with a sharp knife at minimu coward the land, and cut off by app conductor and land so as not to de ufficient in length for installing a ter rocedure shall be used for solderin on. wire in to the through hole. ad wire from the through hole (sold ead wire in to the through hole. ad shall not be clinched. The lead he solder removal and replaced w oldering iron shall be used at 15 to of 232 to 260°C. The lead wire sl g its tip into contact with the condu- g time shall be limited to the bare r n of re-soldering in e) above, the lead with the land until the pull stren ccurs. Disconnection or the lead w ailure, and a new lead wire shall be n. The pull strength shall be calcu $(\underline{d_1}^2)$	elying the sharp k egrade the land a ensile tester shall ng and solder rem der removal) der removal) wire shall be take ith a new one wh o 60W and adjust hall be heated by uctor of the printe minimum. ead wire shall be t the rate of 50mr ogth reaches the r vire being pulled e soldered and pu	nife at the adherence be selected noval by en off en ed to develop the solder ed wiring installed on n per minute requirement out shall not ull test shall

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a) H T to b) S A S T cl ra re in 2 v v p	the inspection Surface soldera (fter dipping the TD-202, the flucture (est Method 20 lean stainless ange between emoved from the semoved from the 5±6mm per se 5±6mm per se ertical state in	solder shall be inspected using a non- n-specified in paragraph C.4.4.8.4 ability e specimen into the flux specified ux shall be drained for 60 seconds 8 of MIL-STD-202 shall be melted steel paddle. It shall be confirmed 226 and 238°C. The solder slug a he molten solder surface immedia e specimen shall be put vertically i econd, kept in the bath for 4±0.5 second. After the pull-up, the specir the air, until the solder is solidified condition of solder on the conduct	in Test Method 2 s. Solder complia I in a bath and sti I that the tempera and burnt flux sha tely before the sp nto the solder ba econds and raised men shall be kept I. No quick coolir	08 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of d at a rate of t in the ng shall be
	nmental Perfor vironmental pe	mance erformance tests shall be performe	ed as follows.	
The t MIL-S acco cond a) T T b) T T T	STD-202. At t rdance with pa litions shall app Thermal shock The temperatur 1) Type I bo Test conc 1000 cycl 2) Type II ar Test conc 1000 cycl Thermal shock The temperatur	 (I) (applicable to qualification test) es specified below shall be reache ard litions: -30°C (for 30 minutes) ← es. Ind III board litions: -30°C (for 30 minutes) ← es. 	timen shall be ins C.4.4.6.2. The fol ed within five min → +125°C (for 30 → +100°C (for 30 ance inspection) ed within five min	spected in lowing utes. minutes); minutes); minutes);
The f cycle durin taker	es, and the pol ig the test. Up n out of the ba	Test Method 106 of MIL-STD-202 arization voltage of $100V\pm10V_{DC}$ s on completion of step 6 of the fina th and dried immediately by blowir paragraphs C.4.4.2, C.4.4.3.1, C.	hall be applied to Il cycle, the speci ng air at 25±5°C a	all layers men shall be and inspected

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C.4.4.8.3 Hot Oil Resistance The specimen shall be dried at 120±5°C for 2 hours and cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5 for 10 seconds and cooled in water at room temperature for 10 seconds. Immersion and cooling shall be performed for 10 cycles. At the completion of t test, the specimen shall be inspected in accordance with paragraphs C.4.4.2, C.4.4.6.4 and C.4.4.6.2.		at 260±5°C ds. letion of the		
C.4.4.8.4	the specimen shall The specimen shall solder bath (Sn: 63 The specimen shal for any defect on th on the internal cop voids using the mic	I be conditioned by drying for 2 ho be placed on a ceramic plate in a I then be fluxed (TYPE RMA MIL-I 3±5 percent, temperature: 288±5°C I be placed on a piece of insulator he external surface, the sample sh per foil, wire or metal core layer fo crosection prepared in accordance e shall be measured at a probe dep of the solder.	desiccator, and (F-14256) and floa c) for a period of to be cooled. Af all be inspected f r heat radiation a with paragraph (cooled down. ated in a 10 seconds. ter a check for any crack nd laminate C.4.4.2.2 a).
C.4.4.8.5	0.5×10 ⁴ Gy to 1×10 amounts to 1×10 ⁴ G to verify that there dielectric withstand accordance with pa	adiation shall be performed using of Gy per hour to the specimen in op Gy. After the irradiation, the specin is no degradation in any part of the ling voltage and insulation resistan aragraphs C.4.4.6.1 and C.4.4.6.3 measured in the same circuit as t	pen air, until the t nen shall be insp e specimen. Tes nce shall be perfo , respectively. Th	otal dose ected visually ts for ormed in ne insulation

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			ł	ł	
APPENDIX D					
		PRINTED WIRING BOARDS,			
	PC	FLEXIBLE, DLYIMIDE FILM BASE MATERIA			
	FU	I TIMIDE FILM DAJE MATERIA	Ŀ		
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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APPENDIX D							
PRINTED WIRING BOARDS, FLEXIBLE, POLYIMIDE FILM BASE MATERIAL							
D.1. (General						
D.1.1	Scope This appendix es provisions for fle constructed of a on one or both s element.	xible printe flexible ins	ed circuits (here sulating film sub	inafter referred t strate, etched c	to as "FPC"), who pper conducto	nich are r strands	
D.1.2	Classification Products covere	d by this s	pecification shal	l be classified a	s specified in Ta	able D-1.	
		r	Table D-1. Clas	ssification			
[Base material		Constru	iction	R	emarks	
	Polyimide film	Do	ingle-sided FPC v ouble-sided FPC v Single-sided FPC	without stiffeners with stiffeners	mount Applic	able for not ing parts. able for	
		I	Double-sided FPC	C with stiffeners	mount	ing parts.	
D.1.3	Part Number The part number Example: JAXA ⁽		Cs is in the follo <u>101</u> Individual identification	wing form. <u>I</u> Base materia code (see D.1.3.1)	COC	le	
	Note: ⁽¹⁾ " IAXA"	indicates t	he nart is for so	ace use and ma	w ha abbraviate	d " l"	
D.1.3.1	I: FPC bas I-GI: FPC bas	Code erial code se material se material	of the FPC is as is polyimide filn is polyimide filn SDA-SCL01.	s follows. n without stiffend	er.		

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D.1.3.2 Processing Code					
D.1.3.2 Processing Code The processing code for the FPC is as follows.					
	0	C without stiffeners			
		PC without stiffeners C with stiffeners			
l	Surger states in	PC with stiffeners			
D.2. App	plicable Documents				
The applicable documents shall be as specified in paragraph 2.					
D.3. Requirements					
D.3.1 C	Qualification Coverage				
 D.3.1 Qualification Coverage Qualification shall be valid for FPC that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs D.3.2 to D.3.8. Products shall have structures, types of flexible base material and base materials of stiffener listed in Table D-2. Products of each processing code are qualified if any representative sample of the processing code is qualified. As shown in Table D-3 processing code IV covers processing code I, II and III, processing code III covers processing code I and processing code II covers processing code I. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification. 					
	Тэ	ble D-2. Qualification Coverag	0		
	Design				

Design conditions Processing code	Construction	Flexible base material	Stiffener base material
I	Single-sided FPC without stiffeners	Polyimide	-
П	Double-sided FPC without stiffeners	Polyimide	-
	Single-sided FPC with stiffeners	Polyimide	GI
IV	Double-sided FPC with stiffeners	Polyimide	GI

Processing code of	Processing code of FPC qualified			
sample FPC		II	III	IV
Ι	0			
I	0	0		
III	0		0	
IV	0	0	0	0

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D.3.2	D.3.2 Materials The materials shall be specified as follows and as specified in paragraph 3.3.					
D.3.2.1						
D.3.2.2		a cover lay shall be a polyimide filr . The material shall be as specifie				
D.3.2.3	JPCA/NASDA-SCL0 ² standards for the adh	be type GI prepreg which conforms I, or bonding film compliant with IP esives used shall be specified in th terial including type and glass tran S.	PC-4203. The ap	ation. The		
D.3.2.4	accordance with IPC- the material used for	e manufactured using GI type stiffe 4101 or JPCA/NASDA-SCL01. Th the stiffener shall be specified in th terial including type and glass trans.	he applicable sta ne detail specifica	ndards for ation. The		
D.3.2.5	•	produced by using epoxy resin ba t. The marking shall not affect any		•		
D.3.3	Design and Constructio	n				
D.3.3.1	FPCs shall be design accordance with this drawings shall be ind The secondary grid m grid points shall be in manufacturing drawin	ngs and Artwork Master (or Original ed and their manufacturing drawin specification. Unless otherwise sp icated at grid points. The basic gri nay be used with 1.27mm spacing. dicated, showing the correspondin ngs and artwork masters (or original haser. In the event of conflict betw	igs shall be prepa becified all locatio id spacing shall b Any location de ig dimensions. T al production mas	ared in ons on oe 2.54mm. oviating from he sters) shall be		

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	drawings and artwork drawings shall take pr	masters (or original production m ecedence.	asters), the man	ufacturing
D.3.3.2	Surface Treatment of	Exposed Terminals		
	Unless specified on d coating or plated with	rawings, the exposed terminals sh fused solder.	nall be covered w	ith solder
D.3.3.3	Plating			
D.3.3.3.1	•	Plating per plating shall be applied as a p nside through holes to form a cond	• •	
D.3.3.3.2	Electrolytic Copper Plating The electrolytic copper plating shall have a minimum purity of 99.5 percent.			
D.3.3.3.3	be more than that s solder plating shall	Plating ler plating shall contain 50 to 70 p pecified in Table D-4 before fusing be uniform, free from pinholes and . However, this provision shall no	g. After fusing, th d pits, and comple	ne electrolytic etely cover
D.3.3.3.4	Plating Thickness a The thickness of the	and Others e plating and solder coating shall b	be as specified in	Table D-4.

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Table D-4. Plating Thickness and Others

	Unit: µm
Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 25
Electrolytic solder	Min. 8 on surface Min. 3 inside a through hole
Solder coating	There are no requirements on thickness, however, it shall meet the solderability requirements. The solder coating shall not exhibit any dewetting, and completely cover conductive patterns. This provision shall not apply to vertical conductor edges.

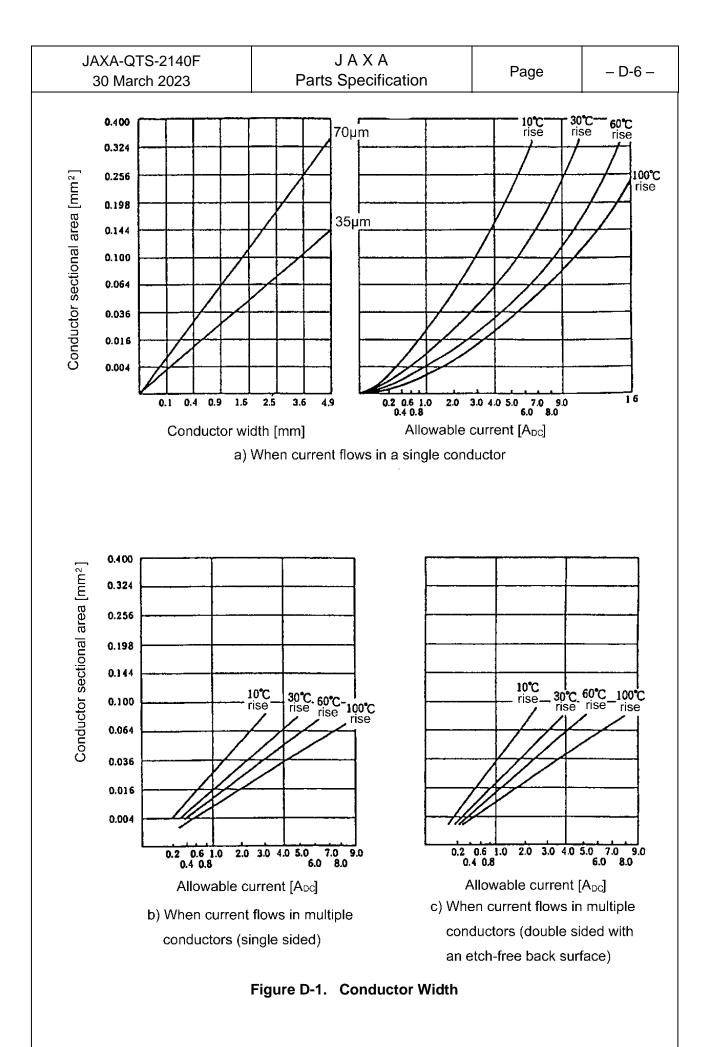
D.3.3.4 Interlayer Connection Connection between conductive patterns on both sides of the FPC shall be provided by through holes.

D.3.3.5 Through Hole Diameter After Plating

The through hole diameter after plating shall be a minimum of 0.5mm.

D.3.3.6 Conductor Width

The design value of the conductor width shall be a minimum of 0.3mm. The actual conductor width shall be determined by the current value, allowable temperature rise and conductor sectional area as shown in Figure D-1.



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D.3.3.7 Conductor Spacing

The design value for the conductor spacing shall be a minimum of 0.3mm. The specific conductor spacing shall depend on the applied voltage as specified in Table D-5.

Table D-5. Conductor Spacing

Unit: mm

Voltage applied between conductors, DC or AC _{p-p} (V)	Minimum conductor spacing	
0-100	0.30	
101-300	0.48	
301-500	0.86	
501 or higher	(0.003xV)+0.1	

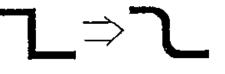
D.3.3.8 Annular Ring

The design value for the annular ring of a plated-through hole shall be a minimum of 0.3mm. The design value for the annular ring of a plated-through hole shall be a minimum of 0.6mm.

D.3.3.9 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

- a) Conductive patterns of FPC
 As a rule, the conductive patterns of the FPC shall be smoothly rounded at a pattern corner and at a terminal, as shown in Figure D-2.
- b) Lands in large conductive areas of FPC The lands which are located in large conductive areas shall be provided with relief areas, as shown in Figure D-3.



Smooth Curve Pattern

Smoothly shaped pattern

at at terminal

Figure D-2. Smooth Curve Pattern and Smoothly Shaped Pattern at a Terminal

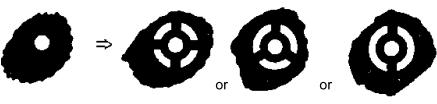


Figure D-3. Lands in Large Conductive Areas

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D.3.3.10	stiffeners and terminal lay clearance shall be such that the diameter with the polyimide film extruded adhesive or	ecified, a cover lay shall be applied als where a circuit element is solde as specified on drawings. The co or of the access hole, when measu n, shall not be reduced by greater nto lands. The registration shall no clearance diameter shall be deterr	ered. The shape over lay registration ired from the port than 0.2mm, due of reduce the effe	of the cover on shall be ion covered to the ctive annular
D.3.3.11	 perpendicular to b) Pattern density Unless otherwise uniform conductor shall be made by c) Number of conductor As a rule, the flexible d) Location of holes 	nductor routing at flexible sections the bend lines. e specified, the flexible sections sh or width and conductor spacing. T / dividing the pattern or adding dur uctor layers xible sections shall have a single of soles and non-plated-through holes	nall have a pattern The pattern densit mmy patterns. conductor layer.	n density with ty adjustment
D.3.3.12	soldered in order to p specified on drawings than the diameter of t at least 0.2mm larger	shall be bonded to the portion whe rotect conductors. The shape of t s. The stiffener hole diameter shal the corresponding plated-through l than the diameter of the correspo FPC plated-through hole without so	he stiffener shall Il be at least 0.2n hole and shall be nding non-plated	be as nm larger equal to or
D.3.3.12.1	holes or non-plated	er added to the FPC in order to reliev -through holes and protect conduct when components are being solde	ctors to prevent d	•
D.3.3.12.2	•	with stiffeners (processing code I ng code IV) shall be used for the F	,	
D.3.3.13		ach part of the FPC shall be as spe nerwise specified, dimensional tole		•

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Table D-6. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	± 0.5 for the dimension of 100 or smaller, and additional 0.15 for every 100 in excess of 100
Board thickness	$\pm 10\%$ of standard thickness or ± 0.18 , whichever is greater
Finished hole diameter	$^{+0.10}_{-0.15}$ for any hole diameter
Conductor width	±0.10 for any conductor width
Conductor spacing	-0.10 for any conductor spacing. The positive tolerance is not specified.
Cover lay	The diameter tolerance of a clearance hole on land shall be ± 0.3 . The diameter tolerance of a clearance hole on any other part shall be ± 0.5 .

D.3.3.14 Operating Temperature Range

The FPC shall operate within the temperature range of -65°C to +125°C.

D.3.3.15 Terminal Pull Strength

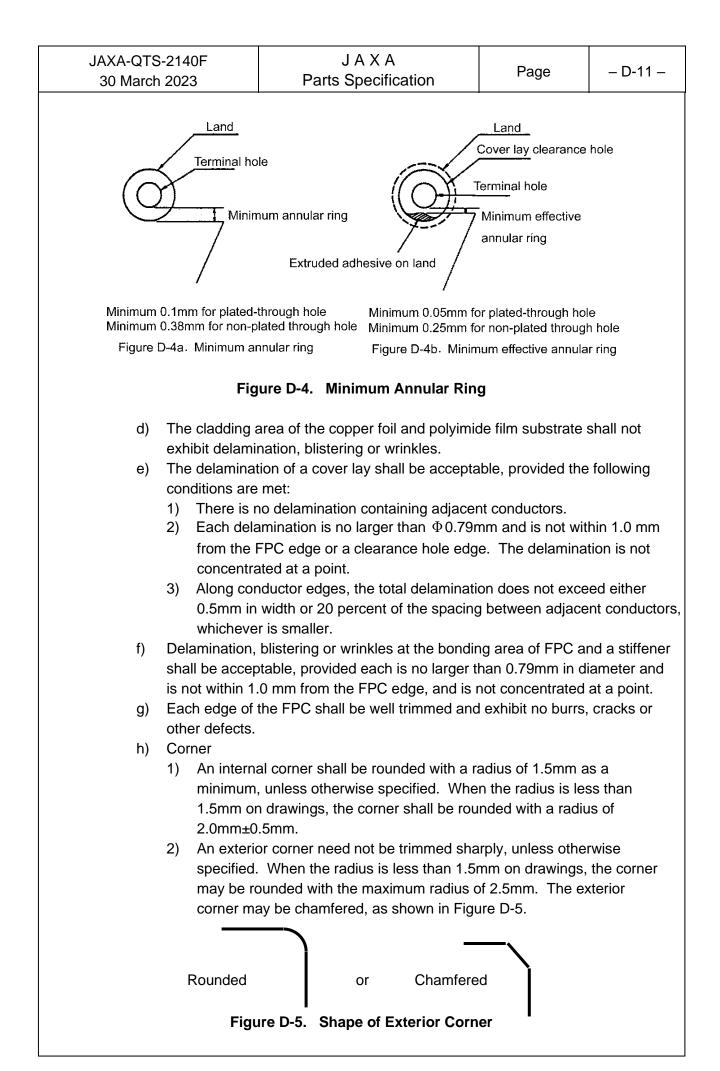
Implementation design on the FPC shall be designed to control a load for each terminal to be less than 8.83N/hole.

- D.3.4 Externals, Dimensions, Marking and Others
- D.3.4.1 Externals and Construction

D.3.4.1.1 Externals

- a) The FPC shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign material, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance and reliability of the FPC. A slight change of the external surface of the insulating material, such as an excessive conductor removal, shall be acceptable.
- b) Unless otherwise specified on drawings, exposed terminals shall be free of dewetting, and the solder shall completely cover conductive patterns. This provision shall not apply to vertical conductor edges.
- c) The plating inside through holes shall exhibit no cracks, and shall be continuously smooth from the land. There shall be no voids at through holes.
- d) Hole walls shall exhibit no burrs, blistering of plating or other deficiencies, and be well trimmed.

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D.3.4.1.2	When FPCs thickness ove than 25µm. b) Thickness of When FPCs thickness ove than 8µm and	copper plating are tested in accordance with parage er a surface conductor and inside a electrolytic solder plating are tested in accordance with parage er a surface conductor and inside a d 3µm, respectively. The solder sh atterns (see paragraph D.3.3.3).	through hole sha graph D.4.4.2.2, t through hole sha	he plating
D.3.4.2	Dimensions			
D.3.4.2.1		nsions, thickness and finished hole ne requirements of Table D-6.	diameter shall b	e in
D.3.4.2.2	 combination is base materia 1) The lenge 2) The widt conducte 3) The widt 4) The num one per 5) The roug the difference 13mm in b) The minimum specified the indimension specified the indimensin specified the indimension specified th	h of any defect shall not exceed 20 ber of defects exceeding 0.05mm conductor or per unit area of 100×1 ghness at vertical conductor edges rence between the convex and con	or scratches exp ents. The conductor widt of percent of the m of percent of the de in width shall be 100mm on the FP shall be less that cave portions, in fined on drawings of a plated the annular ring of a d cannot contain of the wall of the hole	osing the h. inimum efect length. no more than C. n 0.13mm for any range of . When not nimum 0.1mm when non-plated- defects (see ough hole . The



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D.3.4.3 Marking

The marking shall be in accordance with the drawings, and produced by the same process used in producing conductive patterns, by the marking ink specified in paragraph D.3.2.5, or by laser marking. The marking shall not adversely affect any function, performance or reliability of the FPC.

The marking shall remain legible and shall not adversely affect any function of the FPC. Unless otherwise specified, the FPC and test coupons shall be marked with the part number, year and month manufactured, manufacturer's name or its identification code, and production serial number or lot number. The production serial number shall be provided so that the complete manufacturing process can be traced. If marking on each product is impossible, the marking may be placed on a tag.

D.3.5 Workmanship

The FPC shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign material, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the FPC. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

D.3.5.1 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor may be permitted.

D.3.6 Electrical Performance

The FPC shall meet the following electrical performances.

D.3.6.1 Dielectric Withstanding Voltage

When tested as specified in paragraph C.4.4.4.1, there shall be no insulation breakdown, flashover or sparkover.

JAXA-QTS-2140F 30 March 2023J A X A Parts SpecificationPage $-D.13 - D.13 - D$								
D.3.6.2.1Conductor ResistanceWhen tested as specified in paragraph D.4.4.4.2 a), the conductor resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (R) which is calculated by the following formula. $R = R_p + R_T$ $= \sum \zeta \frac{2I_i}{W_i (r + i)} + \sum \zeta \frac{2T}{\pi (t^2 + D_i t)}$ (mΩ) R_p = Total conductor resistance of conductive pattern R_T = Total conductor resistance of through hole W_i = Conductor length (mm) T = Copper foil thickness (mm) ξ = Volume resistivity of copper at 20°C: 1.7×10^{2} mΩ·mm D _i = Through hole diameter (mm) T = FPC thickness excluding cover lay thickness (mm) T = FPC thickness excluding cover lay thickness (mm)D.3.6.2.2Change of Conductor Resistance U when FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent.D.3.6.3Insulation Resistance When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ.D.3.6.4Circuitry When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns.D.3.7Mechanical Performance				Page	– D-13 –			
value (R) which is calculated by the following formula. $R = R_p + R_T$ $= \sum_{i} \zeta \frac{2I_i}{W_i(\tau + t)} + \sum_{i} \zeta \frac{2T}{\pi(t^2 + D_i t)} (m\Omega)$ $R_p = \text{Total conductor resistance of conductive pattern}$ $R_T = \text{Total conductor resistance of through hole}$ $W_i = \text{Conductor width (mm)}$ $Ii = \text{Conductor width (mm)}$ $Ii = \text{Conductor length (mm)}$ $\tau = \text{Copper foil thickness (mm)}$ $t = \text{Plating copper thickness (mm)}$ $\zeta = \text{Volume resistivity of copper at 20°C: } 1.7 \times 10^2 \text{m}\Omega \cdot \text{mm}}$ $D_i = \text{Through hole diameter (mm)}$ $T = \text{FPC thickness excluding cover lay thickness (mm)}$ $T = \text{FPC thickness excluding cover lay thickness (mm)}$ $T = \text{FPC thickness excluding cover lay thickness (mm)}$ $T = \text{FPC thickness excluding cover lay thickness (mm)}$ $D_i = 1 \text{ for use in the test specified in paragraph D.3.6.2.2.}$ $D.3.6.2.2 \text{Change of Conductor Resistance}$ $When \text{FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent.$ $D.3.6.3 \text{Insulation Resistance}$ $When \text{FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100M\Omega.$ $D.3.6.4 \text{Circuitry}$ $When \text{FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns.$ $D.3.7 \text{Mechanical Performance}$		Conductor Resista When tested as spe	nce ecified in paragraph D.4.4.4.2 a), t					
 R_T = Total conductor resistance of through hole W_i = Conductor width (mm) Ii = Conductor length (mm) T = Copper foil thickness (mm) t = Plating copper thickness (mm) ζ = Volume resistivity of copper at 20°C: 1.7×10⁻²mΩ·mm D_i = Through hole diameter (mm) T = FPC thickness excluding cover lay thickness (mm) The resistance measurements shall be recorded not only at room temperature, but also for use in the test specified in paragraph D.3.6.2.2. D.3.6.2.2 Change of Conductor Resistance When FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent. D.3.6.3 Insulation Resistance When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ. D.3.6.4 Circuitry When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns. D.3.7 Mechanical Performance 		value (R) which is calculated by the following formula. $R = R_p + R_T$						
 but also for use in the test specified in paragraph D.3.6.2.2. D.3.6.2.2 Change of Conductor Resistance When FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent. D.3.6.3 Insulation Resistance When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ. D.3.6.4 Circuitry When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns. D.3.7 Mechanical Performance 	$\begin{split} R_T &= \text{Total conductor resistance of through hole} \\ W_i &= \text{Conductor width (mm)} \\ \text{Ii} &= \text{Conductor length (mm)} \\ \tau &= \text{Copper foil thickness (mm)} \\ \text{t} &= \text{Plating copper thickness (mm)} \\ \zeta &= \text{Volume resistivity of copper at } 20^\circ\text{C: } 1.7 \times 10^{-2}\text{m}\Omega \cdot \text{mm} \\ D_i &= \text{Through hole diameter (mm)} \end{split}$							
 When FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent. D.3.6.3 Insulation Resistance When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ. D.3.6.4 Circuitry When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns. D.3.7 Mechanical Performance 	The resistance measurements shall be recorded not only at room temperature, but also for use in the test specified in paragraph D.3.6.2.2.							
 When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ. D.3.6.4 Circuitry When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns. D.3.7 Mechanical Performance 	When FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed							
When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns.D.3.7 Mechanical Performance	D.3.6.3	When FPCs are teste	en FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance					
	D.3.6.4	When FPCs are teste		.4.4, there shall b	e no open			

				r				
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D.3.7.1	Flexibility							
D.3.7.1.1	.3.7.1.1 Folding Flexibility							
		sted as specified in paragraph D.4 ant degradation including delamina						
D.3.7.1.2	Flexibility Enduran	ce						
	accordance with pa	sted for the number of cycles spec aragraph D.4.4.5.1 b), there shall b ng delamination and conductor da ure 40 cycles.	e no evidence of	significant				
D.3.7.2	Terminal Pull Strengt	h						
	through hole shall wit plated-through hole s pull, whichever is sma	ed as specified in paragraph D.4.4. Instand a minimum of 8.83N {0.9kg Inhall withstand a minimum of 8.83N aller. When FPCs are inspected v mer through holes or conductors.	gf} pull, and the la I or 343.2N/cm² {	and of a non- (35.0kgf/cm ²)				
D.3.7.3	Solderability							
	When FPCs are tested as specified in paragraph D.4.4.5.3, a minimum of 95 percent of the area which is not covered with any insulator such as cover lays shall be covered uniformly with solder. The scattered existence of pinholes, dewetting or small roughened points on the surface shall be acceptable provided that they are not concentrated in one area. There shall be no delamination of any insulators such as cover lays.							
D.3.8 E	Environmental Performa	ance						
F	PCs shall meet the foll	lowing environmental requirements	5.					
D.3.8.1	Thermal Shock							
		ed as specified in paragraph D.4.4. e, corrosion or delamination identifi						
D.3.8.2	Humidity Resistance							
	insulators shall exhib	ed as specified in paragraph D.4.4. it no degradation such as corrosion The insulation resistance after the	n or delamination	, as identified				
D.3.8.3	Radiation Hardness							
	not exhibit any degra insulation resistance	ed as specified in paragraph D.4.4. dation specified in d), e) or f) of pa between conductors shall be not le s specified in paragraph D.3.6.1 sh	ragraph D.3.4.2. ess than 500MΩ.	The				

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D.4. Quality Assurance Provisions

D.4.1 In-Process Inspection

The in-process inspection shall be as specified in Table D-7.

		Boguiromont	Test method	Quantity of samples		
No.	Inspection item	Requirement paragraph	paragraph	Production FPC	Test coupon	
		D.3.3.13				
1	Externals and dimensions (before cover lay registration)	D.3.4.1.1	D.4.4.2.1	100%	100%	
		D.3.4.2				

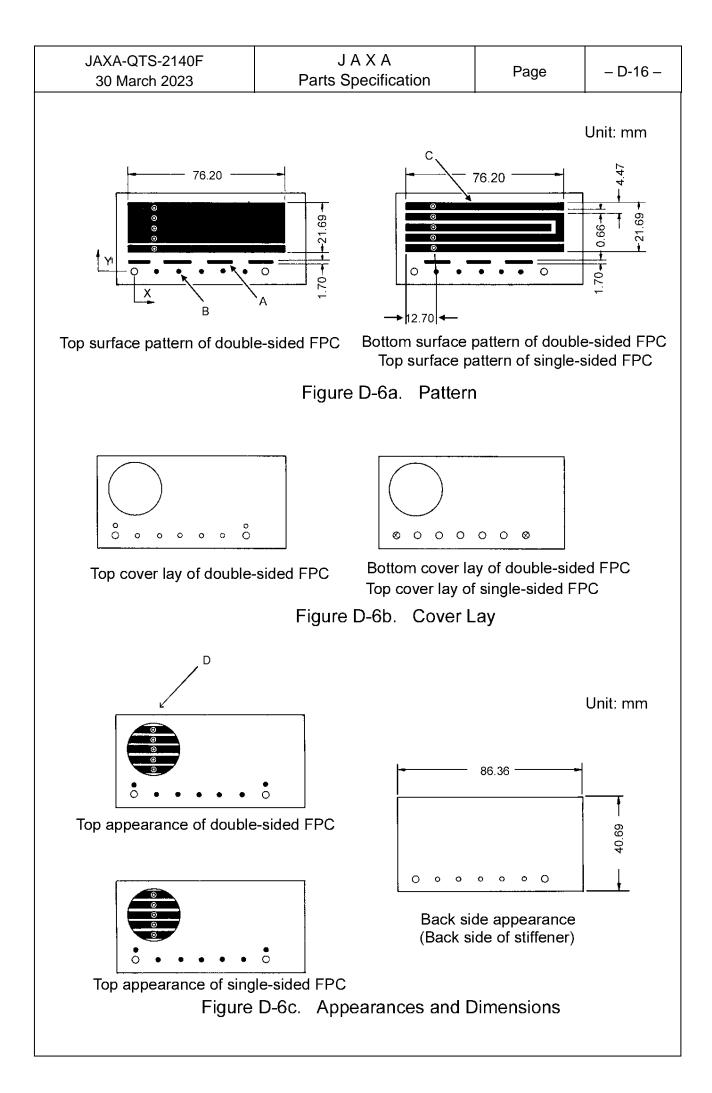
D.4.2 Qualification Test

D.4.2.1 Sample

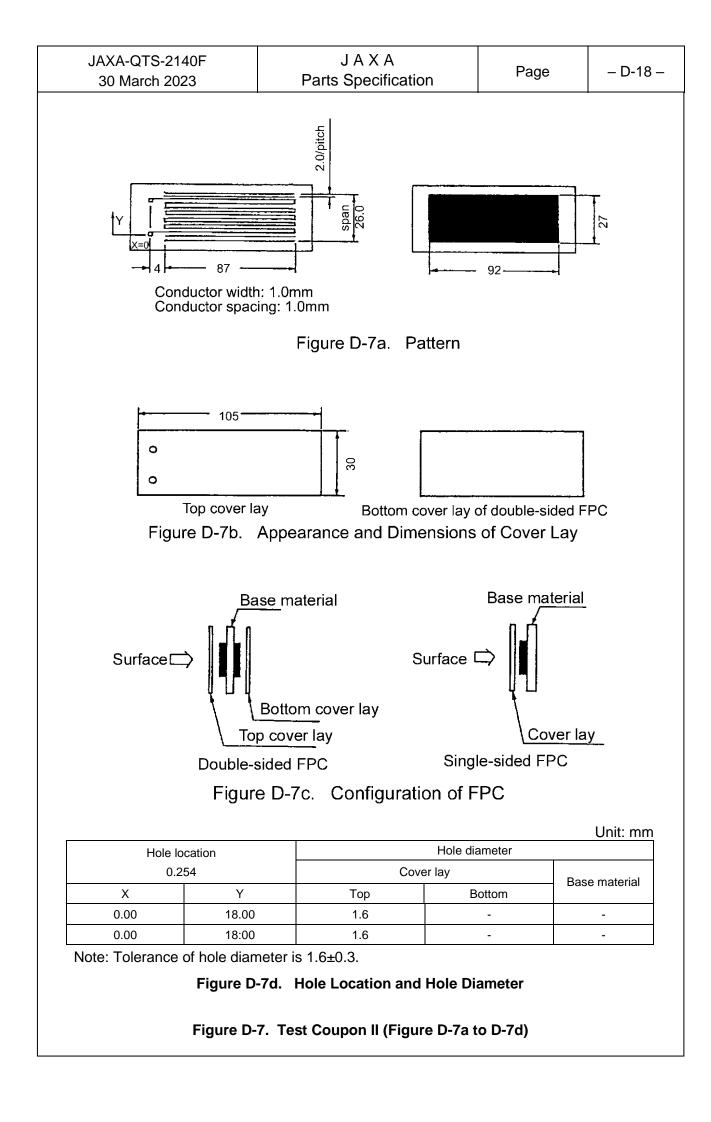
FPC with the minimum conductor width and conductor spacing, at the time the qualification test plan is developed, shall be selected and manufactured as the test specimens together with test coupons specified in Figures D-6 and D-7. If no production plan is available at the time the qualification test plan is developed, the manufacturer can use any pattern sufficient to verify compliance with the requirements of this appendix. Any test coupon may be subject to the approval of JAXA.

D.4.2.2 Test Items and Number of Samples

The tests within each group shall be performed in the order listed in Table D-8. Upon completion of Group I and II tests, Group III through VII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VII tests may be performed in any order regardless of group number. However, the tests in each group of III through VII shall be performed in the order listed. Six production FPCs and six each of test coupons I and II shall be submitted.



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		Base materia		Base ma	aterial ener
Surfac			 Surface ⊂⇒		
		Bottom c	over lay	1	
		Top cover	lav	Cove	rlov
	سيا الم	• • •	-		
	Dour	ple-sided FPC	,	Single-sided	FPC
I	Figure D-60	d. Configur	ation of FP	C with Stiffen	
Hole I	ocation		Hole	diameter	Unit: mm
Φ	0.254	Cove	r lay ⁽¹⁾		
X	Y	Тор	Bottom	Base material ⁽²⁾	Stiffener ⁽³⁾
0.00	0.00	3.26	3.26	3.26	3.26
10.16	0.00	2.21	1.60	1.09	1.30
20.32	0.00	2.21	1.60	1.09	1.30
30.48	0.00	2.21	1.60	1.09	1.30
40.64	0.00	2.21	1.60	1.09	1.30
50.80	0.00	2.21	1.60	1.09	1.30
60.96	0.00	3.26	3.26	3.26	3.26
0.00	5.08	2.21	-	-	-
5.08	5.08	-	-	1.09	-
15.24	5.08	-	-	1.09	-
25.40	5.08	-	-	1.09	-
35.56	5.08	-	-	1.09	-
45.72	5.08	-	-	1.09	-
55.85	5.08	-	-	1.09	-
60.96	5.08	2.21	-	-	-
10.16	10.87	-	-	1.09	-
10.16	15.37	-	-	1.09	1.30
10.16	19.81	22.10	22.10	1.09	1.30
10.16	24.28	-	-	1.09	1.30
10.16	28.75	-	-	1.09	-
Notes: (1) (2) and	^{d (3)} Tolerance (of hole diamete	r		
⁽¹⁾ Cover		⁽²⁾ Base m		(3) Stiffener	
22.10±0.5		3.26 ⁺⁰ -0	0.1	3.26 ^{+0.1} -0.15	
3.26	+0.1				
2.21±		1.09 ⁺⁰	0.15	1.30 ^{+0.30} _{-0.10}	
2.213					
	Figure D	-6e. Hole Loc	ation and Ho	le Diameter	
		6. Test Coupo	. /=		



	Test Requirement Test method Samples and sample number								
		1621	Requirement paragraph	Test method paragraph	Production FPC	Test coupon I	Test coupon II	Remarks	30
Group	Order	Test item	paragraph	paragraph	123456	123456	123456		Ma
I	1	Externals and dimensions	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	000000	All	000000		30 March 2023
	2	Workmanship	D.3.5	D.4.4.3					
II	1	Circuitry	D.3.6.4	D.4.4.4.4	000000	ΑΑΑΑΑ	-		
	1	Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1	-	СС	-		
	2	Solderability	D.3.7.3	D.4.4.5.3	-	DD	-		
Ш	3	Thickness of copper plating	D.3.4.1.2 a)	D.4.4.2.2	00 00 or	BB BB	-		σ
	4	Thickness of electrolytic solder plating	D.3.4.1.2 b)	D.4.4.2.2	00 00 00	BB BB	-		Parts S
	1	Conductor resistance	D.3.6.2.1	D4.4.4.2 a)	-	AA	-		pec
IV	2	Thermal shock (I)	D.3.8.1	D.4.4.6.1 a)	-	AA	-		cific
	3	Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)	-	A A	-		Specification
<	1	Humidity resistance	D.3.8.2	D.4.4.6.2	0 0 0	r CC	-	Test coupon I shall be used when the production FPC does not have conductor spacing of 0.4 to 0.9mm.	
VI	1	Terminal pull strength	D.3.7.2	D.4.4.5.2	00 00	вв	-	Test coupon II shall be used when tests on the production FPC are difficult.	- aye
	2	Radiation hardness	D.3.8.3	D.4.4.6.3	0 0	-	-		
	1	Folding flexibility	D.3.7.1.1	D.4.4.5.1 a)	0 0	-	000		
VII	2	Flexibility endurance	D.3.7.1.2	D.4.4.5.1 b)	0 0	-	000	The production FPC shall be used, if possible.	

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D.4.2.3 Criteria for Pass/Fail

If the number of the samples which fail to meet the requirements of this appendix exceeds the quantity of allowable defects specified in Table D-9, it shall constitute failure of the qualification tests.

Table D-9. Pass/Fail Criteria for Qualification Test and

I					
	Requirement	Test method	Quantity of	allowable defects	
Test and inspection item	paragraph	paragraph	Qualification test	Quality conformance inspection (Group B)	
	D.3.3.13				
Externals and dimensions	D.3.4.1.1	D.4.4.2.1			
	D.3.4.2			-	
Workmanship	D.3.5	D.4.4.3			
Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1			
Conductor resistance	D.3.6.2.1	D.4.4.4.2 a)			
Thermal shock	D.3.8.1	D.4.4.6.1 a)		0	
Thermal shock	D.3.0.1	D.4.4.6.1 b)		\geq	
Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)			
Insulation resistance	D.3.6.3	D.4.4.4.3			
Humidity resistance	D.3.8.2	D.4.4.6.2)	
Circuitry	D.3.6.4	D.4.4.4.4		-	
Terminal pull strength	D.3.7.2	D.4.4.5.2		0	
Solderability	D.3.7.3	D.4.4.5.3		-	
Plating thickness	D.3.4.1.2	D.4.4.2.2		-	
Flexibility	D.3.7.1	D.4.4.5.1		0	
Radiation hardness	D.3.8.3	D.4.4.6.3		-	

Quality Conformance Inspection (Group B)

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D.4.3 Quality Conformance Inspection									
D.4.3.1	Qu	ality Conformance	Inspection (G	Group A)					
D.4.3.1.	1 5	Sample							
	The quality conformance inspection shall be performed on all products. Group III tests may be performed using test coupon I manufactured at the same time as the production FPCs. If Group III tests are performed on the production FPCs in lieu of the test coupon I, the coupon I may not be manufactured. However, the production FPCs shall be treated as test coupons I and shall not be shipped as products.								
D.4.3.1.	2 I	nspection Items ar	nd Sample Siz	ze					
	 D.4.3.1.2 Inspection Items and Sample Size The items and test order of Group A inspection shall be as specified in Table D-10. The inspections within each group shall be performed in the order listed. When Group III tests are performed with production FPCs, the sampling test shall be performed. When multiple coupon types are submitted for inspection at one time, the randomly selected samples shall include at least one test coupon for each type, and the quantity of coupons of each type shall be as equal as possible. Criteria for pass/fail shall be specified in Table D-10. Table D-10. Quality Conformance Inspection (Group A) 								
Group	In Order	spection Inspection item	- Requirement paragraph	Test method	Production	nples Test	Quantity of allowable	Pass/fail	
				paragraph	FPC	coupon I	defects		
I	1	Externals and dimensions	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	All	-	0	-	
	2	Workmanship	D.3.5	D.4.4.3					
II	1	Circuitry	D.3.6.4	D.4.4.4.4	All	-	0	-	

Note: ⁽¹⁾ If the tests for solderability and plating thickness are performed on the production FPC in lieu of the test coupon I, the production FPC shall be regarded as test coupon I.

D.4.4.5.3

D.4.4.2.2

D.3.7.3

D.3.4.1.2

D.4.3.2 Quality Conformance Inspection (Group B)

D.4.3.2.1 Sample

1

2

Ш

Solderability

Plating thickness

The production FPCs and test coupons for Group B inspection shall be manufactured with the same materials and processes and basically in the same manufacturing conditions.

Production FPC or test

Production FPC or test

coupon I⁽¹⁾

coupon I⁽¹⁾

AQL

1.0%

AQL

1.0%

.

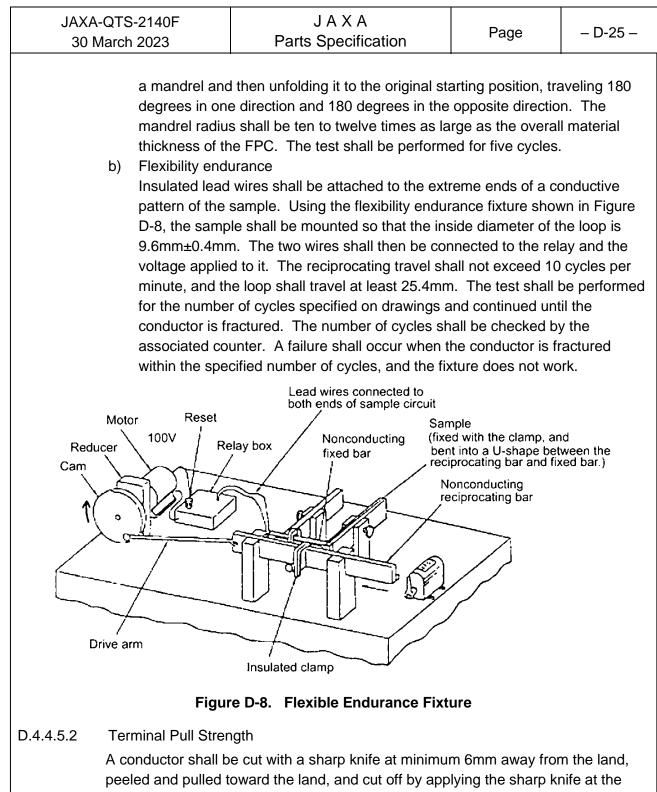
D.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table D-11. The inspections within each group shall be performed in the order listed.

		lagazetica			Sam	ples and sample num	nber	Remarks	
		Inspection	Requirement paragraph	Test method paragraph	Production FPC	Test coupon I	Test coupon II		30
Group	Order	Inspection item	paragraph	paragraph	1 2 3 4 5 6	123456	1 2 3 4 5 6		30 March 2023
	1	Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1	-	СС	-	-	30 March 2023
I	2	Solderability	D.3.7.3	D.4.4.5.3	-	D D	-	-	20
	1	Conductor resistance	D.3.6.2.1	D.4.4.4.2 a)	-	A A	-	-	23
	2	Thermal shock (II)	D.3.8.1	D.4.4.6.1 b)	-	A A	-	-	
	3	Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)	-	AA	-	-	
111	1	Insulation resistance	D.3.6.3	D.4.4.4.3	0 0 (or CC	-	Test coupon I shall be used when the production FPC does not have conductor spacing of 0.4 to 0.9mm.	Parts
	2	Humidity resistance	D.3.8.2	D.4.4.6.2	00 (or C C	-	-	rts Sp
IV	1	Terminal pull strength	D.3.7.2	D.4.4.5.2	0 0 (or BB	-	Test coupon II shall be used when tests on the production FPC are difficult.	Specification
	1	Folding flexibility	D.3.7.1.1	D.4.4.5.1 a)	0 0	-	0 0 0	-	17
V	2	Flexibility endurance	D.3.7.1.2	D.4.4.5.1 b)	0 0	-	0 0 0	The production FPC shall be used, if possible.	
V								The production FPC shall	

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D.4.4 N	Nethods for Test and Ir	nspection				
D.4.4.1	Condition of Test and	d Inspection				
	202. The reference of	nd inspection shall be as specified condition shall be performed at a te 20% to 80%, and a luminance of 1	emperatures of 1			
D.4.4.2	Externals, Dimensior	ns, Marking and Others				
D.4.4.2.1	Dimensions of rate	struction construction, dimensions and mark d values shall be measured using as sufficient accuracy. Externals s	an optical measu	iring		
D.4.4.2.2	Plating Thickness (Copper Plating and Electrolytic Solder Plating) FPCs having a minimum of three through holes shall be encapsulated in a plastic mold which can be cured without heating or pressurization. Then, the mold shall be polished to create a microsection. The minimum plating thickness shall be measured at a magnification of 50X as a minimum.					
D.4.4.3	Workmanship The workmanship sh	all be inspected visually.				
D.4.4.4	Electrical Performance	ce				
	The electrical perform	nance tests shall be performed as	follows.			
D.4.4.4.1	Dielectric Withstan	ding Voltage				
	The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply. a) Test voltage: $500V_{DC}$ b) Duration: 30 seconds c) Conductor spacing: 0.4mm to 0.9mm					
D.4.4.4.2	Electrical Conduct	vity				
	on drawings. well as the roo The conducto paragraph D.4 b) Change of con After the test s shall be meas	sistance shall be flown through conductive The conductor resistance shall be om temperature. r resistance measured before and 4.4.6.1 shall be defined as R ₀ and nductor resistance specified in paragraph D.4.4.6.1, th ured at the temperature (Tx) show h D.4.4.4.2 a).	measured and re after the test spe R _x , respectively.	ecorded, as cified in stance (Rx)		

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	Ta	ble D-12. Temperature (1	x)						
Unit: °C									
	Temperature test								
		Thermal shock [I]	Thermal shock [
	Low temperature	- 65 ⁰ -5	- 30 ⁰ ₋₅						
	Room temperature	15 to 35	15 to 35						
	High temperature	125 ⁺⁵ ₀	125 ⁺⁵ ₀						
	converted to the	esistance measured at each resistance at 20°C. The co st shall be defined as Rx^{20} . 20 - Tx)	• • • •						
	(Ro) shall be con resistance at 20°(from Ro to Rx con following formula. Conductor resista Rx ²⁰ - Ro ²⁰	sistance measured in accorverted to the resistance at 2 C before the test shall be denverted to the resistance at ance change converted to the test shall be denverted to the resistance at	20°C. The converted efined as Ro ²⁰ . The 20°C shall be calcul	l conductor change rate ated by the					
D.4.4.4.3	Insulation Resistance								
		nce test shall be performed The following conditions sh B 60 seconds ion: Where the condu 0.9mm.							
D.4.4.4.4	Circuitry								
	A test current shall be applied to each conductive pattern to verify that there is no open circuit in the pattern or short circuit between patterns.								
D.4.4.5	Mechanical Performanc The mechanical perform	e nance tests of the FPC shal	l be performed as fol	llows.					
D.4.4.5.1	Flexibility a) Folding flexibility A fold cycle shall	be defined as taking one e	nd of the sample, fol	ding it around					



joining point of the conductor and land so as not to degrade the land adherence strength.

Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the FPC sample shall have been baked for one hour at 90°C. The following procedure shall be used for soldering and solder removal by using a soldering iron.

- a) Solder a lead wire in to the through hole.
- b) Remove the lead wire from the through hole (solder removal)
- c) Re-solder the lead wire in to the through hole.
- d) Remove the lead wire from the through hole (solder removal)
- e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.

After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \ \frac{\pi \left\{ \left(d_{2} \right)^{2} - \left(d_{1} \right)^{2} \right\}}{4}$$

L = Pull strength (N)

 $d_1 = Hole \text{ diameter (cm)}$ -

d₂ = Land diameter (cm)

The condition shall be considered as a failure, when either of the followings occur.

- a) When the land around the through hole is loosened.
- b) When the through hole is loosened due to soldering a lead wire. In this case, the land condition does not matter.

D.4.4.5.3 Solderability

Solderability shall be tested as follows.

- a) The sample shall be baked at 90°C for one hour.
- b) Dip the specimen into the flux, composed of 20 percent by gravity of rosin and 80 percent of isopropyl alcohol.
- c) Samples shall be taken out from the flux and the flux shall be drained for 60 seconds. (The flux may flow along an edge of the sample until the alcohol evaporates.)
- d) Solder shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is 232±5°C. The sample, with the conductor surface remaining downward, shall be floated in a solder bath for 5 seconds.
- e) The specimen shall be taken out of the bath. The specimen may be dabbed to remove flux residues, and cooled until the solder is solidified. Fast cooling is not permitted.
- f) The condition of solder on the through hole and conductive surface shall be inspected.

D.4.4.6 Environmental Performance The environmental performance tests of FPCs shall be performed as follows.

	A-QTS-2140F March 2023	J A X A Parts Specification	Page	– D-27 –	
 D.4.4.6.1 Thermal Shock D.4.4.6.1 Thermal Shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply. a) Thermal shock (I) (applicable to qualification test) Test condition B shall be applied. The low temperature shall be changed to -30°C. The number of cycles shall be 1000. b) Thermal shock (II) (applicable to quality conformance inspection) Test condition B-3 shall apply. 					
D.4.4.6.2					
D.4.4.6.3					

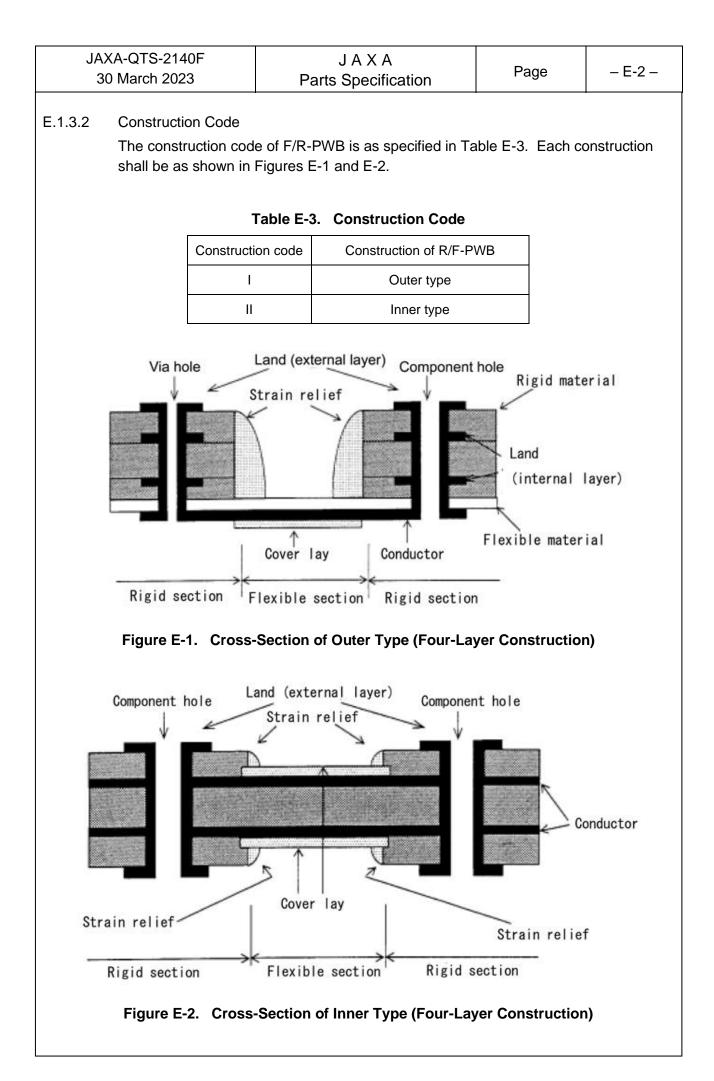
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	ļ			<u> </u>	
		APPENDIX E			
		-FLEX PRINTED WIRING BOAR	De		
	RIGIL	-FLEA FRINTED WIRING BOAR	05		
E.1. General				E-1	
E.1.1 Scope	e			E-1	
E.1.2 Class	sification			E-1	
E.1.3 Part N	Number			E-1	
E.1.3.1 E	Base Materia	al Code		E-1	
E.1.3.2 C	Construction	Code		E-2	
E.1.3.3 N	Number of La	ayers		E-3	
		· S			
• •		nents			
		erage			
		r-Clad Laminate and Prepreg			
	• • • •	per-Clad Laminate			
-	-				
	•				
		ng			
		t			
	0				
		truction			
•		ng Drawings and Artwork Master (
E.3.3.1 N	vianuiacium			E-5	
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	•	/idth			
		pacing			
		er			
		ness and Others			
	•	emperature Range			
		sions, Marking and Others			
		d Construction			
-					
-	E.3.4.2 Dimensions				
E.3.4.3 Marking					
	E.3.5 Workmanship				
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	E.3.7 Cleanliness				
		thstanding Voltage			
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E.4.4.1	Condition of	Test and Inspection		E-27
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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	30 March 2023	Pa	rts Specification			
		ļ	APPENDIX E			
	RIGI	D-FLEX P	RINTED WIRING BOAR	DS		
E.1. (General					
E.1.1	Scope					
	• •	•	neral requirements and o d wiring boards (hereinaf			
E.1.2	Classification					
	Products covered by thi	s specifica	ation shall be classified a	as specified in Ta	ble E-1.	
		Table E	E-1. Classification			
			Construction of F/R-PW	'B		
			Outer type			
	Classi	fication	Inner type			
E.1.3	Part Number					
	The part number of the	F/R-PWB	is in the following form.			
	Example: JAXA ⁽¹⁾ 2140/E <u>101</u> <u>GI</u> <u>I</u> <u>4</u> ⁽²⁾ Individual Base material Construction Number of layers identification code code (see E.1.3.1) (see E.1.3.2) (see E.1.3.3)					
	Notes: ⁽¹⁾ "JAXA" indicates the ⁽²⁾ Number of conductor	-	space use and may be a	abbreviated "J".		
E.1.3.1	Base Material Code					
	The base material co	de of F/R-	PWB is as specified in 1	Table E-2.		
	-		D			
	Table E-2. Base Material Code					
	Base material code		Base material base woven polyimide resi	in	4	
	GI		iant to IPC-4101 or JPCA/			
	Note: ⁽¹⁾ Applicable standards for GI type are as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), shall be as specified in the Application Data Sheet (ADS).					



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E.1.3.3 Number of Layers

The number of layers of F/R-PWB is as specified in Table E-4, based on the construction type.

Table E-4	4. Numbe	of Layers
-----------	----------	-----------

Construction	Number of layers at rigid section (Number of layers at flexible section)	Maximum number of layers
I	2 to 10 layers (1 layer)	10
II	3 to 8 layers (1 to 4 layers)	8

E.2. Applicable Documents

E.2.1 Reference Documents

The reference documents shall be as specified in paragraph 2.2.

E.3. Requirements

E.3.1 Qualification Coverage

Qualification shall be valid for F/R-PWB that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs E.3.2 to E.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. The maximum thickness and surface plating type shall be specified in the detail specification. All surface plating types specified in this specification are considered qualified if any one of those plating types is qualified. Only solder resist inks used for qualification tests are considered qualified. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

E.3.2 Materials

The materials of F/R-PWB shall be as follows and as specified in paragraph 3.3

E.3.2.1 Rigid Copper-Clad Laminate and Prepreg

The rigid copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The nominal thickness of the base material shall be not less than 0.05mm. The metal foil shall be copper regardless of base material type. The metal foil for the outermost layer shall have a nominal thickness of 18µm as a minimum, and the metal foil for an internal layer shall have a minimum of 35µm. The applicable standards for the material used in the R/F PWB shall be specified in each detail specification. Details of the GI base material, including type and the glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

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30 March 2023		Parts Specification	U	
E.3.2.2	compliant with IPC-42 drawings. The nomin The copper foil for the minimum in considera foil for an internal lay applicable standards specified in the detail	Laminate ad laminate shall be comprised of 204 or JPCA/NASDA-SCL01, and all thickness of the base material s e outermost layer shall have a non ation of additional conductor thickness for the material used in the printed specification. Details of the GI ba on temperature (Tg), shall be defire	shall be as speci shall be not less t ninal thickness of ness for plating. of minimum 35µn d wiring boards sl ase material, inclu	fied on han 0.05mm. 18µm as a The copper n. The nall be uding type
E.3.2.3	Cover Lay The cover lay specifie not less than 12.7µm	ed in IPC-4203 shall be used. The	e nominal thickne	ss shall be
E.3.2.4	flex interface. This w	be comprised of flexible epoxy res ill serve as strain relief during ben against the rigid corner.		•
E.3.2.5	Solder Coating The solder used for s	older coating shall contain 50 to 7	0 percent tin.	
E.3.2.6		/R-PWB shall conform to IPC-SM- sively to the rigid section. The app ufacturing drawings.		•
E.3.2.7	•	produced using epoxy resin base narking shall not affect any functio		•
E.3.2.8	applied to all through solder resist is applie subsequently with the When plating other th	cified, the solder coating specified holes, lands, and surface conduct d. All through holes shall be coate same type surface plating as the an the plating applied on lands is s, electrolytic gold plating may be a	tive patterns, exc ed with copper pla plating applied o partially required	ept for where ating and n lands.

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30 IVIA	rch 2023	Pa	irts Specification			
E.3.2.8.1	Electroless Copper	lectroless Copper Plating				
	The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.					
	lectrolytic Copper Plating The electrolytic copper plating shall have a minimum purity of 99.5 percent.					
- 1 -	Electrolytic Gold Plating The electrolytic gold plating shall be as specified in Table E-5. The electrolytic nickel plating specified in paragraph E.3.2.8.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.					
Table E-5. Electrolytic Gold Plating						
	Item	Item Specification				

E.3.2.8.4	Electrolytic Nickel Plating

Purity

KNOOP hardness

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and be low stress type.

Min. 99.7 percent

91 to 129 (inclusive)

- E.3.3 Design and Construction
- E.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master) The F/R-PWBs shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

E.3.3.2 Interlayer Connection

Connection between conductive patterns in different layers of F/R-PWBs shall be provided by through holes including small via hole (drill diameter of minimum 0.35).

E.3.3.3 Conductor Width

The minimum conductor width at the design value of F/R-PWB shall be as specified in Table E-6 on the basis of the construction type. The actual conductor width of

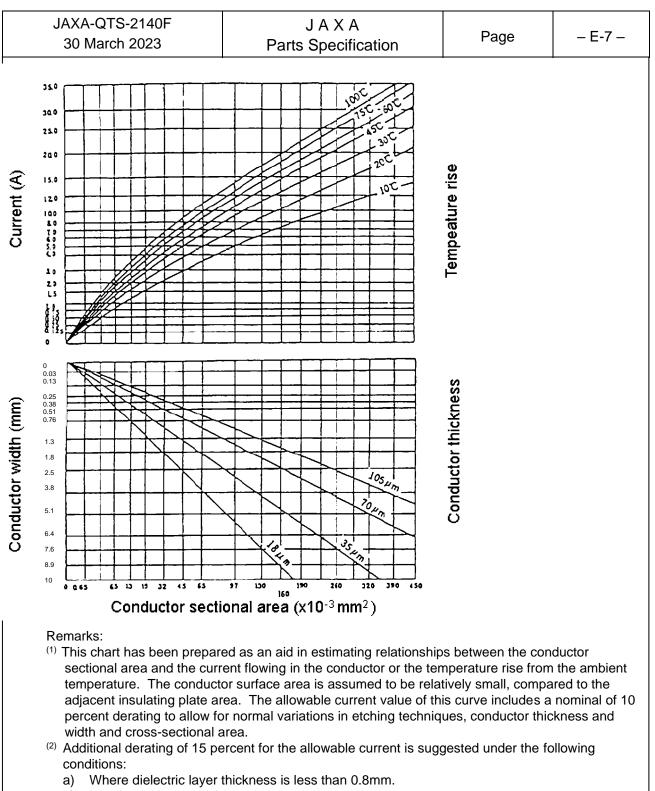
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external and internal layers shall be determined in accordance with Figures E-3 and E-4.

Table E-6. Minimum Design Width of Conductor

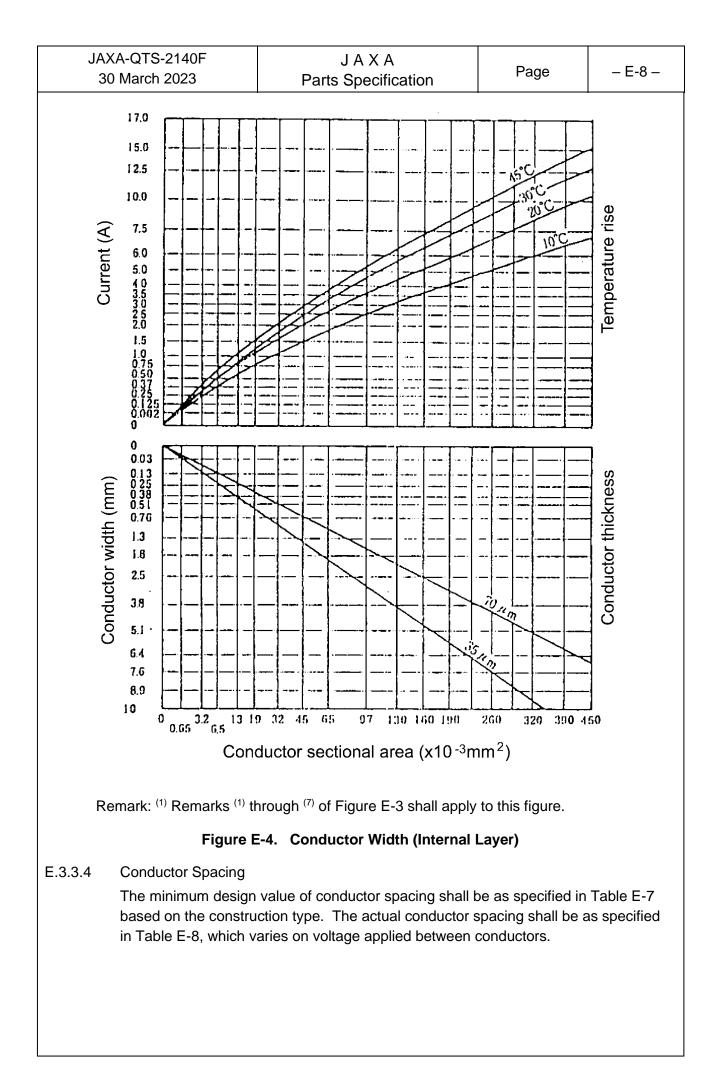
Unit: mm

Construction	Rigid section	Flexible section
I	0.13	0.30
II	0.25	0.30



- b) Where conductor thickness is greater than 105µm.
 ³⁾ In general, the allowable temperature rise is defined as the difference be
- ⁽³⁾ In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the R/F-PWB and the maximum ambient temperature in the location where the R/F-PWB will be used.
- ⁽⁴⁾ For single conductor applications, the chart may be used for determining conductor widths, crosssectional area and allowable current (current-carrying capacity) for various temperature rises.
- ⁽⁵⁾ For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.
- ⁽⁶⁾ The effect of heating due to heat generating parts is not considered.
- ⁽⁷⁾ The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure E-3. Conductor Width (External Layer)



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	Table E-	7. Conductor Spaci	ng	
			Unit: mr	n
Construction		Rigid section	Flexible section	
Ι		0.18	0.20	
II		0.25	0.25	
Table E-8. Conductor S		sist, Cover Lay or Pre	e preg Uni	bating,
S Voltage applied bet	ween	sist, Cover Lay or Pre	epreg	
s	ween	sist, Cover Lay or Pre	e preg Uni	
S Voltage applied bet	ween	sist, Cover Lay or Pre	epreg Uni luctor spacing (mm)	
S Voltage applied bet conductors, DC or A	ween	Minimum conc External layer	epreg Uni luctor spacing (mm) Internal layer	
S Voltage applied bet conductors, DC or A 0 - 100	ween	Minimum cond External layer 0.18	Epreg Uni luctor spacing (mm) Internal layer 0.18	

The design value of the minimum land diameter shall be as specified in Table E-9.

Table E-9. Land Diameter

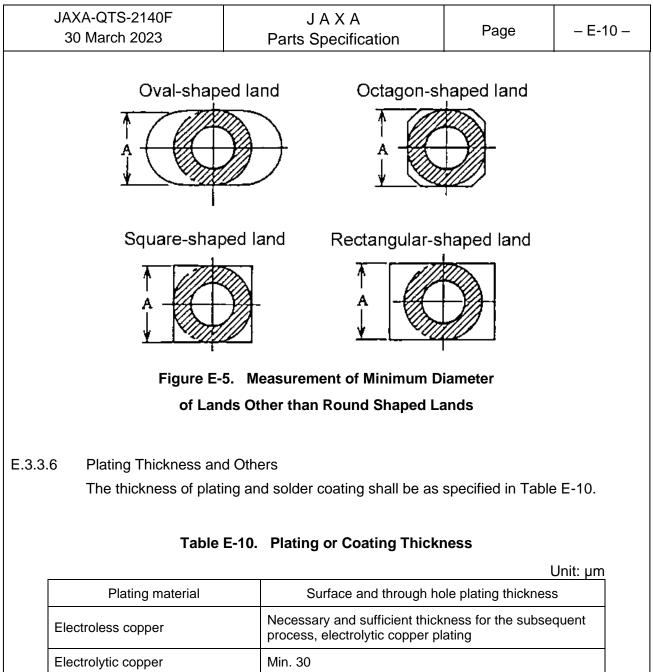
Unit: mm

Hala	Construction	
Hole	I II	
Small via holes ⁽¹⁾	Drill diameter + 0.4	
Plated-through holes ⁽²⁾	Finished hole diameter + 0.5	Finished hole diameter + 0.6
Non-plated-through holes	Dill diameter + 1.1	

Notes:

⁽¹⁾ The minimum diameter of the land provided with a small via hole shall be 0.76mm.

⁽²⁾ The minimum diameter of lands other than round shaped lands shall be measured as the length "A", as shown in Table E-5.



Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 30
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	Min. 5
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.

E.3.3.7 Operating Temperature Range

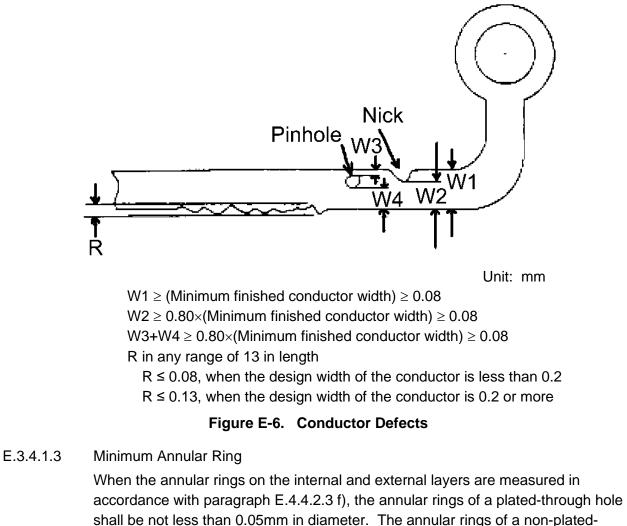
R/F-PWBs shall operate within the temperature range of the thermal shock (II) test, -65° C to $+125^{\circ}$ C (paragraph E.3.10.1.2).

- E.3.4 Externals, Dimensions, Marking and Others
- E.3.4.1 Externals and Construction
- E.3.4.1.1 Conductive Pattern The conductive patterns shall conform to the approved or provided artwork master (or original production master).

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E.3.4.1.2 Conductor

At rigid sections, the conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100mm×100mm on F/R-PWBs. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is greater than 0.2mm, the roughness shall be not more than 0.13mm (see Figure E-6). Conductors at the rigid-flex interface, including supporting conductive patterns, shall contain no defects including tears, cracks, edge roughness, nicks, pinholes and scratches, exposing the base material. A cover lay coating over the conductors shall not exhibit any scratches.



shall be not less than 0.05mm in diameter. The annular rings of a non-platedthrough hole shall be not less than 0.3mm in diameter and shall not contain defects. When the annular ring for plated-through hole on an external layer shall be a minimum of 0.13mm in diameter, a sub-land or other equivalent disposition shall be provided.

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E.3.4.1.4	The surface of the	etween Conductor Layers dielectric layer between conducto or foreign material.	or layers shall be f	ree from any
E.3.4.1.5	through holes shall protrusion, and sha holes shall be acce lower limit specified plated-through hole measured from the any side of the plat base material thick			
Res	in recession		dule	rusion
	Figu	re E-7. Through Hole Deficiend	cies	

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure E-8).

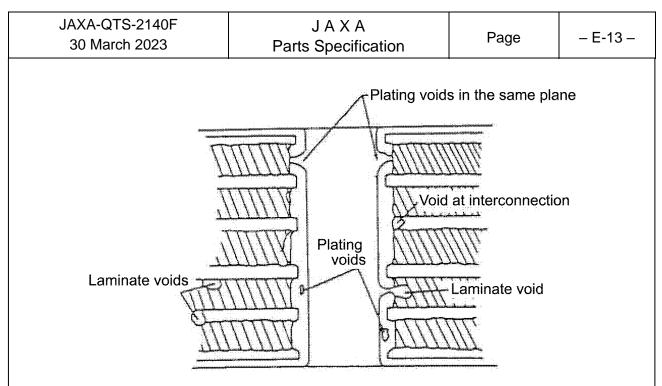


Figure E-8. Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure E-9).

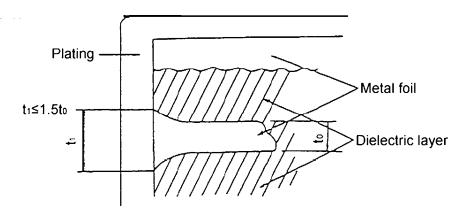


Figure E-9. Nail Heading

- c) Layer-to-layer registration The layer-to-layer registration error shall not exceed 0.20mm.
- d) Dielectric layer thickness
 The dielectric layer between conductor layers of a rigid dielectric material shall be not less than 0.08mm in thickness. The dielectric layer between conductor layers of a flexible dielectric material shall be greater than 0.038mm in thickness.
 a) Disting thickness
- Plating thickness
 The plating thickness shall meet the requirements specified in paragraph E.3.3.6.

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	f) Annular ring The annular ring	shall meet the requirements spec	ified in paragraph	n E.3.4.1.3.
E.3.4.1.6	Solder Coating The solder coating conductive patterns	shall be free from pinholes and pi s.	ts, and complete	y cover
E.3.4.1.7		icks, cracks or separation at edge apply to separate parts of a split b		This
E.3.4.1.8	layer and base may underneath the sur each area does no the spacing betwee along edges of the crazing and an adja	B Bs shall not exhibit cracks or sepa terial shall not exhibit delamination face of the base material shall be t exceed 1 percent of the surface a en conductors is not reduced exce F/R-PWB shall be permitted, whe acent conductor is equal to or great specified on drawings or 1.6mm, v	n. Measling and of acceptable, prov area of the F/R-P eding 25 percent in the spacing be ater than the mini	crazing ided that the WB, and that . Crazing tween the mum
E.3.4.1.9	Significant visual d uneven color and e resist shall not enc pinholes shall be a resist. The applica	esist shall be free from tackiness, l amage such as thin spots, separa exposed residual conductor shall n roach onto lands. Unless otherwis cceptable, provided that the condu tion area and registration onto cor anufacturing drawings.	tion, roughness of tot be permitted. se specified, scra uctors are covere	on the surface, The solder tches and d with solder
E.3.4.2	drawings. Unless oth	ich part of the F/R-PWB shall be a erwise specified, dimensional tole s specified in Table E-11.	-	•

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. . ..

	Unit: mm
Item	Dimensional tolerance
External dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. The tolerance of through hole diameters is not specified, when the drill diameter is 0.5 or smaller.
Conductor width	0.13 or more and less than 0.20: ± 0.05 0.20 or more and less than 0.50: ± 0.10 0.50 or more: ± 20 percent of circuit width
	0.18 ≤ design conductor spacing < 0.2 The tolerance of finished conductor spacing shall be 0.1 or more with respect to the design value.
Conductor spacing	Design conductor spacing ≥ 0.2 The tolerance of finished conductor spacing shall be -0.1 with respect to the design value. The positive side tolerance is not specified.
	The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

E.3.4.2.1 Solder Resist Thickness

When F/R-PWBs are tested as specified in paragraph E.4.4.2.4, the solder resist thickness shall be not less than $17.5\mu m$, measured at the center of conductors.

E.3.4.3 Marking

The marking shall be produced with the marking ink specified in paragraph E.3.2.7 by the same process as producing conductive patterns, or by laser marking as specified in the drawings. The marking shall not adversely affect any function, performance or reliability of the F/R-PWB.

All marking shall remain legible and in no manner affect the performance of the F/R-PWB. Unless otherwise specified, the following shall be marked on each F/R-PWB. If marking on the F/R-PWB is not practical, the marking may be placed on a tag.

- a) Part number
- b) Year and month manufactured
- c) Manufacturer's name or its identification code
- d) Product serial number⁽¹⁾ or lot number

Note: ⁽¹⁾ Product serial number shall be provided so that the complete manufacturing process can be traced.

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E.3.4.3.	If any separable pa it shall be clearly m	bard Irt (equivalent to a single F/R-PWE arked that the part cannot be used hat it does not easily vanish by an	d. This marking	
E.3.5	grease, finger print, mol corrosion product, soot, affect the function, perfo acceptance criteria for v	ibit defects including fouling, oil, c d generating source, foreign mate mold release agent or flux residue ormance or reliability of the F/R-PV vorkmanship shall be discussed be	rials, dirt, corrosi es, which could a VB. The detailed	on, dversely
E.3.5.1	for bow and twist sha	tested as specified in paragraph E Il be 1.5 percent for rigid sections, Igs. For a split board, bow or twist on.	unless otherwise	e specified on
E.3.5.2	• ·	or conductors shall not be repaired for and an insignificant repair of sc		
E.3.6		verhang sted as specified in paragraph E.4 ating and conductors, or slivers fro		
E.3.7	salt, soot, grease, finger residues, or ionic contar	no fouling including dirt, oil, corros print, mold release agent, foreign nination. When F/R-PWBs are tes esistivity of the solvent extract sha	inclusion and flu sted as specified	x in
E.3.8	Electrical Performance	, , , , , , , , , , , , , , , , , , ,		
E.3.8.1	Dielectric Withstandir When F/R-PWBs are	e following electrical requirements. ng Voltage tested as specified in paragraph E , flashover or sparkover.		hall be no
E.3.8.2		tested as specified in paragraph E t shorts between circuit patterns.	E.4.4.6.2, there s	hall be no

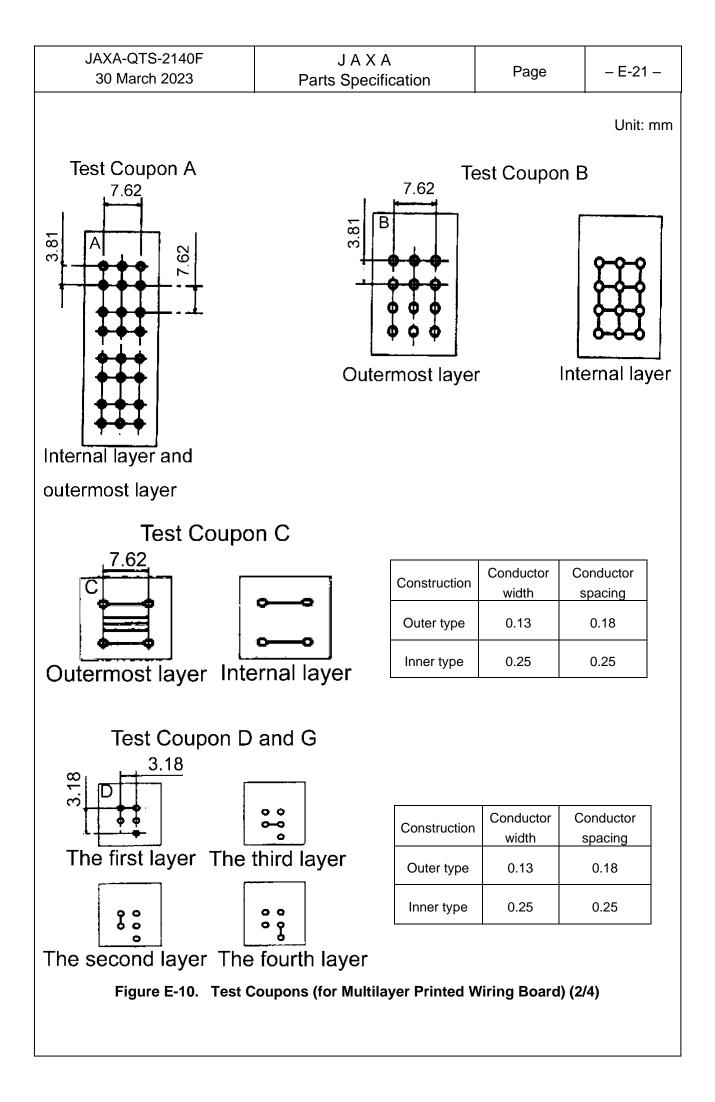
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E.3.8.3	between two lands co value (Ri) which is ca resistance between a connection resistance resistance is measure	tested as specified in paragraph E onnecting a circuit on all conductor lculated by the formula specified b Il layers can not be measured at a shall be repeatedly measured se	r layers shall not o below. When the time, the unmea	exceed the connection sured
	$Ri = 2\rho \frac{I}{W \cdot t} (m\Omega)$			
	ρ: Volume resistivity a l: Distance between la W: Conductor width (t: Conductor thicknes	mm)	rms the conducto	or (mΩ∙mm)
E.3.9	Mechanical Performanc F/R-PWB shall meet the	e following mechanical requiremen	ts.	
E.3.9.1	Terminal Pull Strengt When tested as spec requirements. a) Bond strength	h ified in paragraph E.4.4.7.3, F/R-F	WBs shall meet	the following
	The land shall with b) Conductor and la When F/R-PWBs shall be no loose c) Microsection of t When F/R-PWBs	s are inspected visually as specific ning around the through holes.	ed in paragraph E d in accordance [,]	with
E.3.9.2	degradation or rejecta	ified in paragraph E.4.4.7.1, R/F-P able delamination. After completic h E.3.8.2 shall be satisfied.		
E.3.9.3	paragraph E.4.4.7.2, delamination. After c	e number of cycles specified in dra F/R-PWBs shall not exhibit degrad ompletion of the test, the requirem ied. If the number of cycles is not	dation or rejectab nents specified in	le paragraph

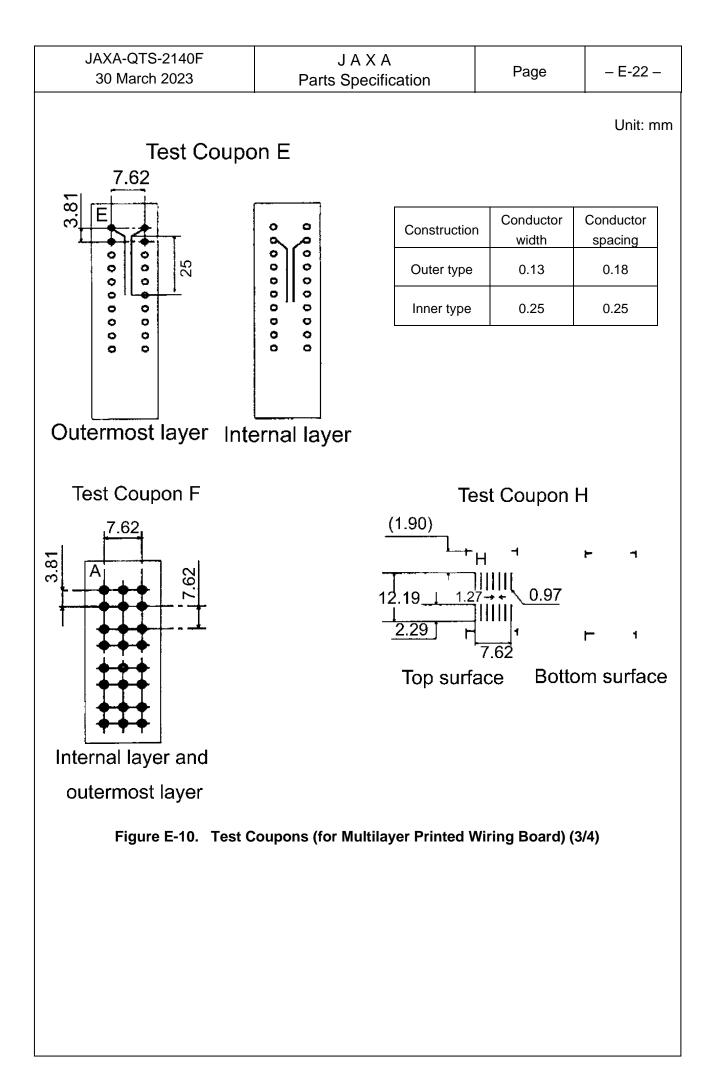
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W	olderability hen tested as speci quirements.	fied in paragraph E.4.4.7.4, F/R-P	WBs shall meet	the following
	-	iside wall and land surface shall ex not apply to small via holes.	xhibit proper wett	ting of solder.
	with new solder. T	ty ercent of the surface conductor are he scattered existence of pinholes hall be acceptable, provided that t	, dewetting or sm	nall
	ronmental Performa PWBs shall meet th	ance e following environmental requirer	nents.	
E.3.10.1 Th	ermal Shock			
	When F/R-PWBs a circuit, blistering, m circuit continuity an E.4.4.6.2, and conr paragraph E.4.4.6.2	applicable to qualification test) re tested as specified in E.4.4.8.1 easling, crazing or delamination. d circuit shorts shall be tested in a nection resistance shall be measur 3. The F/R-PWB shall meet the re after the test, and the change in co after the test shall be less than 10	At the completion accordance with p red in accordance equirements specton connection resista	n of the test, paragraph e with sified in
	When F/R-PWBs a no open circuit, blis the test, circuit con paragraph E.4.4.6.2 with paragraph E.4 paragraph E.3.8.2	(applicable to quality conformance re tested as specified in paragraph tering, measling, crazing or delam tinuity and circuit shorts shall be te 2, and connection resistance shall .4.6.3. The F/R-PWB shall meet t after the test, and the change in co after the test shall be less than 10	h E.4.4.8.1 b), the nination. At the c ested in accordar be measured in he requirements	ompletion of ace with accordance specified in
W		tested as specified in paragraph E r delamination. The insulation res		
WI co		tested as specified in paragraph E between circuits before and after		•

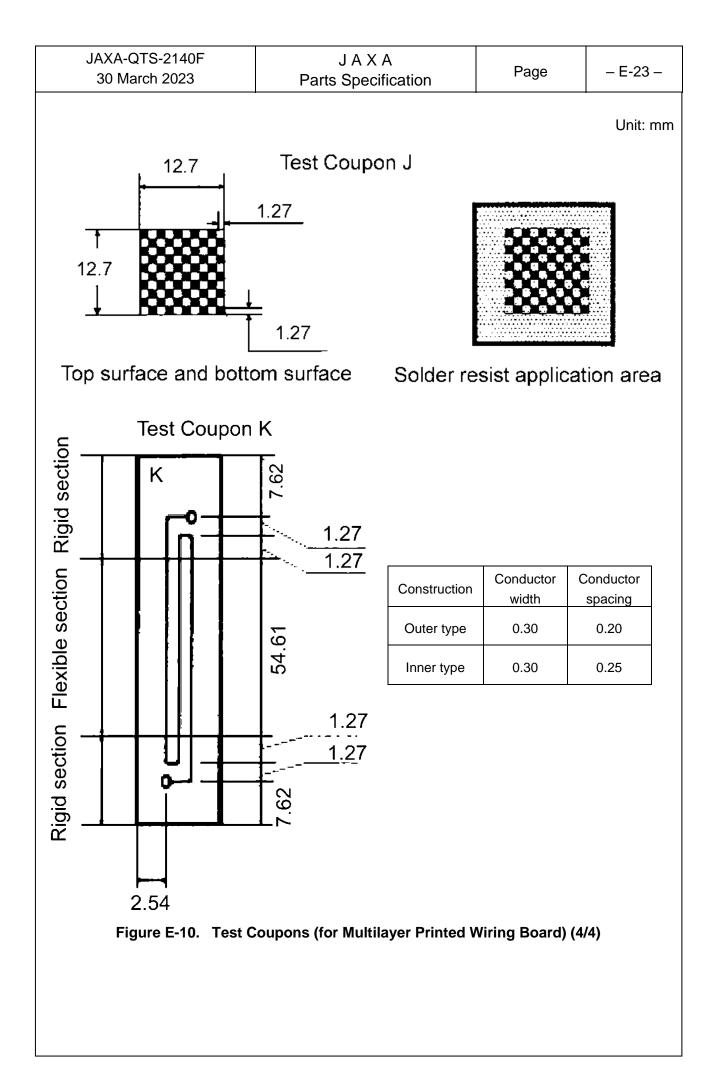
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E.3.10.4	 When tested as specified in paragraph E.4.4.8.4, F/R-PWBs shall meet the followi requirements. a) Externals There shall be no measling, cracks, separation of plating and conductors, blistering or delamination. b) Copper foil There shall be no cracks in internal copper foils in the vertical microsection of through holes. 			
	within a layer or	ess than 76µm is permitted, provid between layers shall comply with t ctor spacing specified on manufac	the requirements	
E.3.10.5	D.5 Radiation Hardness When R/F-PWBs are tested as specified in paragraph E.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph E.3.8.1 shall be satisfied.			
E.4. Q	uality Assurance Provisi	ons		
	 In-Process Inspection The in-process inspection specified below shall be performed, and F/R-PWBs shall meet the requirements of paragraphs E.3.4.1 and E.3.7. a) Visual inspection of internal layers, construction and dimensions (100 percent) b) Cleanliness (sampling) 			
E.4.2 Qualification Test				
E.4.2.1	conductor spacing ar requirements of this a In order to qualify spl qualification test. The and continuous perfo	proved by JAXA, and have the min of number of layers sufficient to ver appendix. The test coupons shall it boards, split board specimens sh e split boards shall include a deep- ration. Samples shall consist of the ed on the same work board as the	rify compliance v be as specified in nall be subjected -hole-shape slit, ^v ne production F/R	vith the r Figure E-10. to the V-groove cut e-PWB and
E.4.2.2	completion of Group using specimens allo may be performed in	per of Samples up shall be performed in the order I and II tests, Group III through VII cated to the appropriate group tes any order regardless of group nur shall be performed in the order lis	I tests shall be pe ts. Group III thro nber. However, t	erformed ugh VIII tests ests in each

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PWBs shall be prepared for each construction. The number of test coupons submitted for each test shall be as specified in Table E-12.						
	 Notes: ⁽¹⁾ The conductor width shall be specified. ⁽²⁾ For test coupon A, the land of land diameter applicable to the corresponding F/R-PWB the maximum hole diameter All holes shall be through hotolerance is not specified. ⁽³⁾ For test coupons B, C, E, F a be 1.8±0.13mm, and the land land shape of the products. holes. The hole diameter shall be the corresponding F/R-PWB. ⁽⁴⁾ Test coupons D, E and G are conductors, depending on the layers. Therefore, the conductors, depending on the layers. Therefore, the conductors of D and G, through measure the resistance. The 1.8mm and hole diameter shall be through hotolerance is not specified. ⁽⁵⁾ Solder resist shall apply to the only when solder resist is reacclearance spacing for the so coupon E shall be the land diameter and the land the land	diameter shall be he minimum drill . The hole diame among the minin les. The hole dia and K, the land d d shape shall be All holes shall be all be 0.8mm. The tolerance for the tolerance for s figure. At both holes shall be for s figure. At both holes shall be for a land diameter shall be 0.8mm. les. The hole dia ne test coupons E quired for the pro lder resist applied liameter +0.2mm pons shown in the age (A to H, J and K ot for the object o	the minimum diameter of eter shall be num lands. ameter iameter shall the typical e through he hole the number of onstruction of rmed on all ends of the med to shall be ameter a, H and J, ducts. The d on the test is appendix is acceptable. () shall be			

Figure E-10. Test Coupons (for Multilayer Printed Wiring Board) (1/4)







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		Test				Pass/fail			
Group	Order	Test item	Requirement paragraph	Test method paragraph	Sam Production R/F-PWB	ples ⁽¹⁾ Test coupon ⁽²⁾	alle	antity owab efects	le
	1	Design and construction	E.3.3	E.4.4.2					
I	2	Externals, dimensions, marking and others	E.3.4	E.4.4.2	No. 1 to No. 6	A, B, C, D, E, F, G, H, K and L ⁽⁴⁾			
	3	Workmanship ⁽³⁾	E.3.5	E.4.4.3					
II	1	Plating adhesion and overhang	E.3.6	E.4.4.4	No. 1 to No. 6	С			
	2	Bow and twist	E.3.5.1	E.4.4.3.1	NO. 6	N/A			
	1	Through holes	E.3.4.1.5	E.4.4.2.3		A and F			
	2	Terminal pull strength	E.3.9.1	E.4.4.7.3		F			
III	3	Solder resist thickness	E.3.4.2.1	E.4.4.2.4	No. 1	J			
	4	Folding flexibility	E.3.9.2	E.4.4.7.1]	К			
	5	Flexibility endurance	E.3.9.3	E.4.4.7.2		К			
	1	Connection resistance	E.3.8.3	E.4.4.6.3	No. 2	D		$\overline{)}$	
IV	2	Hot oil resistance	E.3.10.3	E.4.4.8.3				$\left(\right)$	
	3	Connection resistance	E.3.8.3	E.4.4.6.3				[
	1	Circuitry	E.3.8.2	E.4.4.6.2					
	2	Connection resistance	E.3.8.3	E.4.4.6.3					
V	3	Thermal shock (I)	E.3.10.1.1	E.4.4.8.1 a)	No. 3	E and G ⁽⁵⁾			
	4	Circuitry	E.3.8.2	E.4.4.6.2					
	5	Connection resistance	E.3.8.3	E.4.4.6.3					
VI	1	Humidity and insulation resistance	E.3.10.2	E.4.4.8.2	No. 4	Е			
VI	2	Dielectric withstanding voltage	E.3.8.1	E.4.4.6.1	NO. 4				
VII	1	Thermal stress	E.3.10.4	E.4.4.8.4	No. 5	A and B			
VII	2	Solderability	E.3.9.4	E.4.4.7.4		B and H ⁽⁶⁾	$\left \right. \right $		
VIII	1	Radiation hardness	E.3.10.5	E.4.4.8.5	No.6	N/A			
IX	1	Materials	E.3.2	-	((7)		-	

Table E-12. Qualification Test

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type. In order to qualify split boards, split board specimens shall be submitted.

⁽²⁾ Test coupons and production F/R-PWBs shall be manufactured simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production F/R-PWBs which shall be subjected to the same group test.

⁽³⁾ Bow and twist (paragraph E.3.5.1) of the samples shall be tested during the second test of Group II tests.

⁽⁴⁾ Group I test shall be performed on the test coupons which shall be provided for Group II through VIII tests.

⁽⁵⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽⁶⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

⁽⁷⁾ Data shall be submitted to certify compliance with design specifications.

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E.4.3 QI	uality Conformance In	spection		
E.4.3.1	Quality Conformance	Inspection (Group A)		
E.4.3.1.1	process and is mar lot. However, in or rejection shall not b	art of a split board fails an inspect ked with rejection, the board may der not to affect the inspection re be used as a specimen. A "split to s of the same patterns or parts of	y be included in a sult, the part man poard" means a b	an inspection rked with poard
E.4.3.1.2	Table E-13. The in order. The quality Test coupons and s	nd Sample Size order of the Group A inspection s spections within each group sha conformance inspection shall be sample product shall be fabricate subjected to each tests.	II be performed ir performed on all	n numerical products.
E.4.3.2	Quality Conformance	Inspection (Group B)		
E.4.3.2.1	•	or the Group B inspection may be cture of the test coupons for the		
E.4.3.2.2	E-14. The inspection	nd Sample Size order of Group B inspection sha ons within each group shall be pe nall be provided for each group.		

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		Inspection			Pass/fail				
			Requirement Test method		Sam	ples	Quantity of		
Group	Order	Inspection item paragraph paragraph		r Inspection item paragraph paragra		paragraph paragraph		Test coupon ⁽¹⁾	allowable defects
Ι	1	Externals, dimensions, marking and others	E.3.4	E.4.4.2	All	N/A			
	2	Workmanship ⁽²⁾	E.3.5	E.4.4.3					
II	1	Bow and twist	E.3.5.1	E.4.4.3.1	All	N/A			
111	1	Circuitry	E.3.8.2	E.4.4.6.2	All	N/A			
	1	Thermal stress	E.3.10.4	E.4.4.8.4					
IV		Through holes	E.3.4.1.5	E.4.4.2.3 a)	N1/A	A and B ⁽¹⁾			
IV	2	Conductive interface	b)	E.4.4.2.3 b)	N/A				
		Plating thickness	e)	E.4.4.2.3 c)					
V	1	Solderability	B.3.9.4	B.4.4.7.4	N/A	B and H ⁽³⁾			

Table E-13. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ The test coupon A shall be inspected only when the corresponding product is provided with small via holes of which drill diameter is a maximum of 0.5mm.

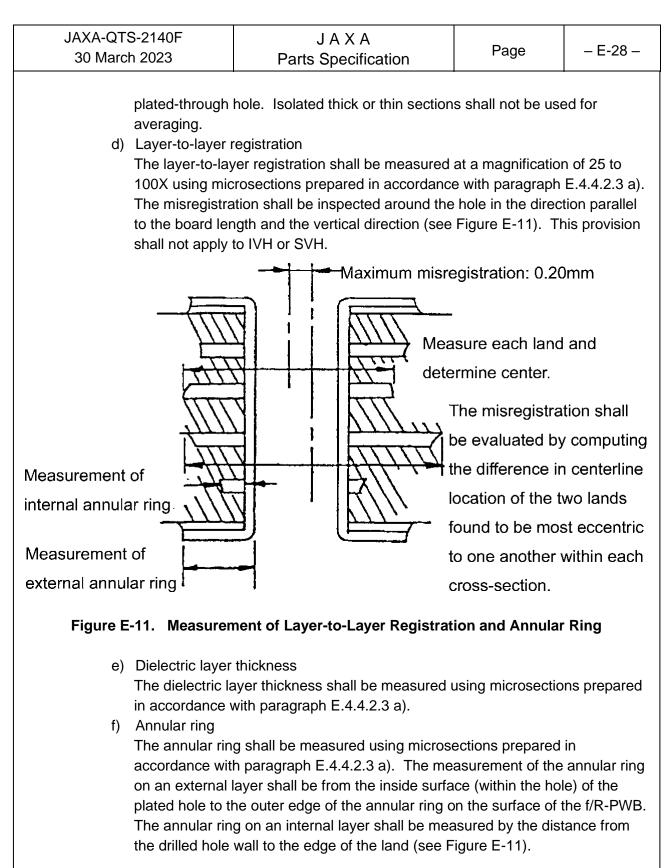
- ⁽²⁾ Bow and twist (paragraph E.3.5.1) of the samples shall be tested during the first test of Group II tests.
- ⁽³⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

		Inspection			Pass	/fail
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
Ι	1	Plating adhesion and overhang	E.3.6	E.4.4.4	С	<u>\</u>
	1	Terminal pull strength	E.3.9.1	E.4.4.7.3	F	
П	2	Connection resistance	E.3.8.3	E.4.4.6.3		
11	3	Hot oil resistance	E.3.10.3	E.4.4.8.3	D	
	4	Connection resistance	E.3.8.3	E.4.4.6.3		
	1	Circuitry	E.3.8.2	E.4.4.6.2		
	2	Connection resistance	E.3.8.3	E.4.4.6.3		
III	3	Thermal shock (II)	E.3.10.1.2	E.4.4.8.1 b)	E and G ⁽¹⁾	0
	4	Circuitry	E.3.8.2	E.4.4.6.2		
	5	Connection resistance	E.3.8.3	E.4.4.6.3		
11.7	1	Humidity and insulation resistance	E.3.10.2	E.4.4.8.2	-	
IV	2	Dielectric withstanding voltage	E.3.8.1	E.4.4.6.1	E	
V	1	Folding flexibility	E.3.9.2	E.4.4.7.1	К	
VI	1	Flexibility endurance	E.3.9.3	E.4.4.7.2	К	ן ן

Table F-14	Quality	Conformance	Inspection	(Group B)
	Quanty		mopeouon	

Note: ⁽¹⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

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E.4.4 M	ethods for Test and Ir	spection			
E.4.4.1	Condition of Test and	Inspection			
Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD- 202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.					
E.4.4.2	Externals, Dimension	s, Marking and Others			
	•	externals, dimensions (conductives) shall be tested. Externals shall be	-	•	
E.4.4.2.1	Conductive Pattern	s and Edges			
		ductive patterns and edges shall be and which has sufficient accuracy.		g an optical	
E.4.4.2.2	Annular Ring				
	surface (within the the surface of the F	of the annular ring on an external hole) of the plated hole to the oute F/R-PWB. Dimensions of annular ng instrument which has sufficient	er edge of the ani ring shall be mea	nular ring on	
E.4.4.2.3	Through Holes				
	 hole. The sample the hole. At lead board. The three of the effective be inspected for vertical side, lay thickness) and thickness) and thickness) and thickness) and thickness) and thickness) and thickness and the shall be mere of the through thickness of the through the inspected at a mere of the through the inspected at a mere of the plating thickness of the plating the p	specimen shall be cut in the vertical oles shall be encapsulated and po- st three plated-through holes shall ough holes for the vertical microse product area on the work board. If the plating integrity (plating voids ver-to-layer registration, dielectric the solder resist thickness at a mater- to-layer registration, one of the f parallel to the length direction of the parallel to the length direction of the boards shall be subjected to the h tilayer boards with through holes conductive layer shall be polished prepared so that the conductive layer nagnification of 50 to 100X.	lished to expose Il be inspected for ection may be pre The vertical micro s, internal connect layer thickness a agnification of 50 through holes sha the multilayer boa e board's length of horizontal microse shall be encapsu in the parallel dir ayer is exposed. ntal direction) sha	the center of r each work pared outside osection shall attion of the and plating to 100X. To all be ard and the direction. Eaction lated and ection. The The integrity II be	

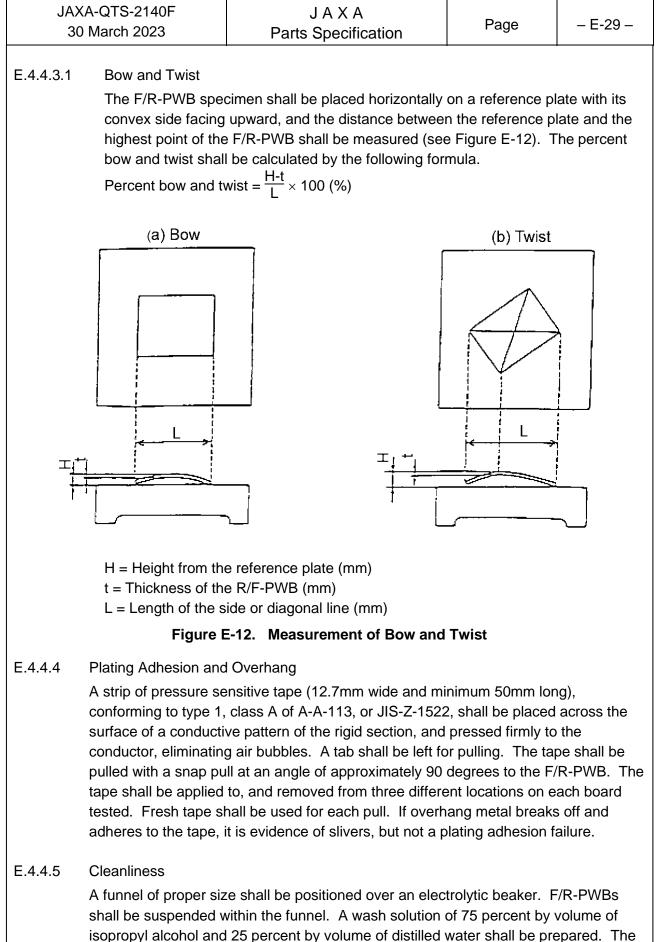


E.4.4.2.4 Solder Resist Thickness

The solder resist thickness shall be measured using a microsection prepared in accordance with paragraph E.4.4.2.3a) at a magnification of 200X as a minimum.

E.4.4.3 Workmanship

The workmanship of F/R-PWB shall be inspected visually. The bow and twist shall be inspected as follows.



wash solution shall have a resistivity not less than $6x10^6\Omega$ cm. The wash solution shall be poured onto both sides of the F/R-PWB from the top until 100ml of the wash

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solution is collected from each board surface of 6.5cm² (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. It is imperative that the initial washings be included in the sample to be measured for resistivity. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods given in Table E-15 may be used to perform the cleanliness test.

Method	Resistivity (×10⁰Ω·cm)	Equivalent factor	Equivalents of sodium chloride (µg/cm ²)
Conductivity bridge	2	1	1.56
Omega Meter ⁽¹⁾	2	1.39	2.20

Table E-15. Equivalent Factors

Note: ⁽¹⁾ Alpha Metals Incorporated, "Omega Meter"

E.4.4.6 Electrical Performance

The electrical performance tests of the F/R-PWB shall be performed as follows.

E.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: $1000V_{AC}$ peak or $1000V_{DC}$
- b) Duration: 30 seconds
- c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

E.4.4.6.2 Circuitry

a) Continuity

A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity.

b) Circuit shorts
 A voltage of 250V_{DC} shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

E.4.4.6.3 Connection Resistance

An electrical wire shall be soldered at two lands of through holes to obtain proper electrical conductivity. The resistance between the lands shall be measured using a measuring instrument capable of measuring a resistance below $0.5m\Omega$.

E.4.4.7 Mechanical Performance

The mechanical performance tests of the F/R-PWB shall be performed as follows.

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mandrel and ther in one direction a shall be ten to tw PWB. The test s shall be tested as	be defined as taking one end of the unfolding it to the original starting p nd 180 degrees in the opposite dire elve times as large as the flexible m hall be performed for five cycles. Af s specified in paragraph E.4.4.6.2 ar jectable delamination at the folded p	position, traveling ction. The mand laterial thickness fter the test, the F and shall not exhib	180 degrees rel radius of the F/R- F/R-PWB		
of the sample. U sample shall be r The two wires sh The reciprocating travel at least 25. specified on draw of cycles shall be the conductor is f does not work. A	res shall be attached to the extreme sing the flexibility endurance fixture nounted so that the inside diameter all then be connected to the relay ar travel shall not exceed 10 cycles p 4mm. The test shall be performed the rings and continued until the conduct checked by the associated counter ractured within the specified numbe fter the test, F/R-PWBs shall be tes all not exhibit degradation or rejectal	shown in Figure of the loop is 9.6 nd the voltage ap er minute, and th for the number of ctor is fractured. A failure shall o r of cycles, and the ted as specified i	E-13, the mm±0.4mm. plied to it. e loop shall cycles The number occur when he fixture in paragraph		
Lead wires connected to both ends of sample circuit Sample (fixed with the clamp, and bent into a U-shape between the reciprocating bar and fixed bar.) Nonconducting reciprocating bar					
Figu	re E-13. Flexible Endurance Fix	ture			
E.4.4.7.3 Terminal Pull Stre	enath				
A conductor shall peeled and pulled	be cut with a sharp knife at minimu toward the land, and cut off by app e conductor and land so as not to de	olying the sharp k	nife at the		

strength.

	070 04 405			
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	 and the following p using a soldering in a) Solder a lead w b) Remove the lead c) Re-solder the lead d) Remove the lead 	sufficient in length for installing a te rocedure shall be used for solderin on. vire in to the through hole. ad wire from the through hole (sold ead wire in to the through hole. ad wire from the through hole (sold ead wire in to the through hole.	ng and solder ren der removal)	
	completely during to resoldering. The s the tip temperature iron without bringin board. The heating After the completion a tensile tester at re forward and verticat (L) or any failure of be regarded as a failure	ad shall not be clinched. The lead the solder removal and replaced we oldering iron shall be used at 15 to e of 232 to 260°C. The lead wire s ag its tip into contact with the condu- g time shall be limited to the bare of an of re-soldering in e) above, the l oom temperature, and be pulled a ally with the land until the pull stren ccurs. Disconnection or the lead we ailure, and a new lead wire shall be n. The pull strength shall be calcu	vith a new one wh o 60W and adjust hall be heated by uctor of the printe minimum. ead wire shall be t the rate of 50mr ngth reaches the vire being pulled e soldered and p	en ed to develop the solder d wiring installed on m per minute requirement out shall not ull test shall
	L = Pull strength (N) d ₁ = Hole diameter d ₂ = Land diameter) (cm)		
E.4.4.7.4	 Solderability a) Hole solderabil The wetting of s accordance wit b) Surface soldera After the specin STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. The 25±6mm per se vertical state in 	ity solder shall be inspected using a r h paragraph E.4.4.8.4. ability nen is dipped into the flux specifie ux shall be drained for 60 seconds 08 of MIL-STD-202 shall be melted steel paddle. It shall be confirmed 226 and 238°C. The solder slug a he molten solder surface immedia e specimen shall be put vertically i econd, kept in the bath for 4±0.5 se econd. After the pull-up, the specie the air, until the solder is solidified condition of solder on the conduc	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp into the solder ba econds and raise men shall be kep d. No quick coolin	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of t in the ng shall be

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E.4.4.8	Environmental Perfor The environmental pe	mance erformance tests shall be performe	ed as follows.	
E.4.4.8.1	 MIL-STD-202. The a) Thermal shock A cycle shall conspecimen shall temperature to b) Thermal shock The test shall b 	test shall be performed in accordate following conditions shall apply. (I) (applicable to qualification test) onsist of 30 minutes at -30°C and 3 be subjected to 1000 cycles in tota the high temperature, or the rever (II) (applicable to quality conformate performed under the test condition within 2 minutes each.	30 minutes at +10 al. Transfer time se, shall not exce ance inspection)	00°C. The from the low eed 2 minutes
E.4.4.8.2	cycles, and the during the test. be taken out of evaluated. b) Insulation resis The test shall b	ance s in Test Method 106 of MIL-STD- polarization voltage of 100V±10V _I Upon completion of step 6 of the the bath and dried immediately by	bc shall be applie final cycle, the sp blowing air at 25 e test condition E	d to all layers becimen shall 5±5°C and 3, Test
E.4.4.8.3	temperature. After for 5 seconds and performed for 10 c	Il be dried at 120±5°C for 2 hours a that, the specimen shall be immer cooled to room temperature. Imm ycles. At the completion of the tes dance with paragraph E.4.4.6.3.	rsed in oil or wax ersion and coolin	at 260±5°C Ig shall be
E.4.4.8.4	the specimen shall The specimen shall floated in a solder a period of 10 seco cooled. After a che inspected for any c microsection prepa	Il be conditioned by drying for 2 ho be placed on a ceramic plate in a Il then be fluxed in accordance with bath of composition Sn 63±5 perce onds. The specimen shall be place eck for any defects on the external crack on the internal copper foil and ared in accordance with paragraph be measured at a probe depth not he solder.	desiccator, and on the detail speci- ent maintained at ed on a piece of i surface, the sam d laminate voids E.4.4.2.3 a). So	cooled down. fication and 288±5°C for nsulator to be nple shall be using the lder
E.4.4.8.5	Radiation Hardnes The gamma ray irr	s adiation shall be performed by usir	ng cobalt 60 at a	rate of

 0.5×10^4 Gy to 1×10^4 Gy per hour to the specimen in open air, until the total dose

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amounts to 1×10^4 Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests for dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph E.4.4.6.1 and E.4.4.8.2 b), respectively. The insulation resistance shall be measured in the same circuit as the one used for the dielectric withstanding voltage test.

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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			APPENDIX F	-		
			PRINTED WIRING B NTROLLED THERM S BASE WOVEN POL BASE MATERI	AL EXPANS	•	
F.1.	General					
1.1	provisions for characterist thermal exp mounted pa	or the fine pi ics using Cl ansion for th rts, and the	es the general require tch printed wiring boar C (Copper-Invar-Copp le purpose of improvin boards use glass base erred to as "printed wir	ds with a lo er-clad) that g the conne woven pol	w thermal expan t has a low coeffi ection reliability o yimide resin as a	sion cient of n surface
F.1.2	Classificatio Products co		s specification shall be	e classified a	as specified in Ta	ble F-1.
			Table F-1. Classif	ication		
	Base material		Construction		Remarks	
	Glass base	Single-sideo	d printed wiring board		ouble-sided printed ds without through	
	woven polyimide	Double-side	d printed wiring board			
	resin	Multilayer p	rinted wiring board			
F.1.3	·		printed wiring boards i F <u>105 GI</u> Individual Bas identification mate coc (F.1.3	<u>III</u> se Proces erial coc le (F.1.3	ssing Number le of layers	
	Notes: ⁽¹⁾ "JAXA" in ⁽²⁾ Number c		part is for space use a	·	abbreviated "J".	

F.1.3.1 Base Material Code

The base material code of the printed wiring boards is as specified in Table F-2.

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Table F-2. Base Material Code

Base material code ⁽¹⁾	Base material
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

Note: ⁽¹⁾ Applicable standards for GI types are as specified in the detail specification. Details of GI base material, including type and glass transition temperature (Tg), are as specified in the Application Data Sheet (ADS).

F.1.3.2 Processing Code

The processing code of the printed wiring boards is as specified in Table F-3.

Processing code	Construction	Remarks
I	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
II	Double-sided printed wiring board	
111	Multilaver printed wiring board	

Table F-3. Processing Code

F.1.3.3 Number of Layers

The maximum number of layers of the printed wiring boards shall be specified in each detail specification.

F.2. Applicable Documents

F.2.1 Reference Documents

The reference documents shall be as specified in paragraph 2.2.

F.3. Requirements

F.3.1 Qualification Coverage

Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs F.3.2 to F.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers, less thickness and fewer CIC than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. Test data taken using samples with the same base and the same metal foil may be used as test data for samples with a different number of layers except for the thermal shock test. In this case the sample shall have more layers than the samples for qualification test.

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	in compliance with the c	letail specification. If necessary, a fied in the detail specification.	dditional qualifica	ation
F.3.2	Materials The materials of the prir specified in paragraph 3	nted wiring boards shall be specifie 3.3.	ed as follows and	as
F.3.2.1	The metal-clad lamin 4101 or JPCA/NASD material shall be poly base material shall be The metal foil shall be of each other with pre thickness of 18µm (ne thickness for plating, the copper foil for the (nominal) as a minim	Prepreg and Metal Foil ate and prepreg shall conform to the A-SCL01, and shall be as specified imide resin (paragraph F.1.2). The e not less than 0.05mm. e copper if metal-clad laminate or re preg. The copper foil for the outer cominal) as a minimum in consideration Only when printed wiring boards he outermost layer shall have an add um. The copper foil for an internal a minimum. However, it shall be	d on drawings. T e nominal thickne metal foils are sta rmost layer shall ation of additiona have surface via ditional thickness l layer shall have a minimum of 18	The base less of the acked on top have a I conductor holes (SVH), of 9µm
	provided. The application shall be specified in e	Iditional conductor thickness for pla able standards for the material use each detail specification. Details of insition temperature (Tg), shall be	ed in the printed v f GI base materia	SVH is wiring boards al, including
F.3.2.2	provided. The application of the specified in end the glass transmitted in the glass transmitted in the glass transmitted by the specified of the specified in the specified of	ditional conductor thickness for pla able standards for the material use each detail specification. Details o	ed in the printed v f GI base materia defined in the Ap e printed wiring bo (Fe-Ni36% alloy)	SVH is wiring boards al, including oplication bards is in the middle
F.3.2.2	provided. The application of the specified in each of the glass transmission of the glass of the	Iditional conductor thickness for pla able standards for the material use each detail specification. Details of insition temperature (Tg), shall be unsion material, CIC utilized for the board (see figure F-1) with invar (ed in the printed v f GI base materia defined in the Ap e printed wiring bo (Fe-Ni36% alloy)	SVH is wiring boards al, including oplication bards is in the middle

Figure F-1. CIC Cross-section View

F.3.2.3 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

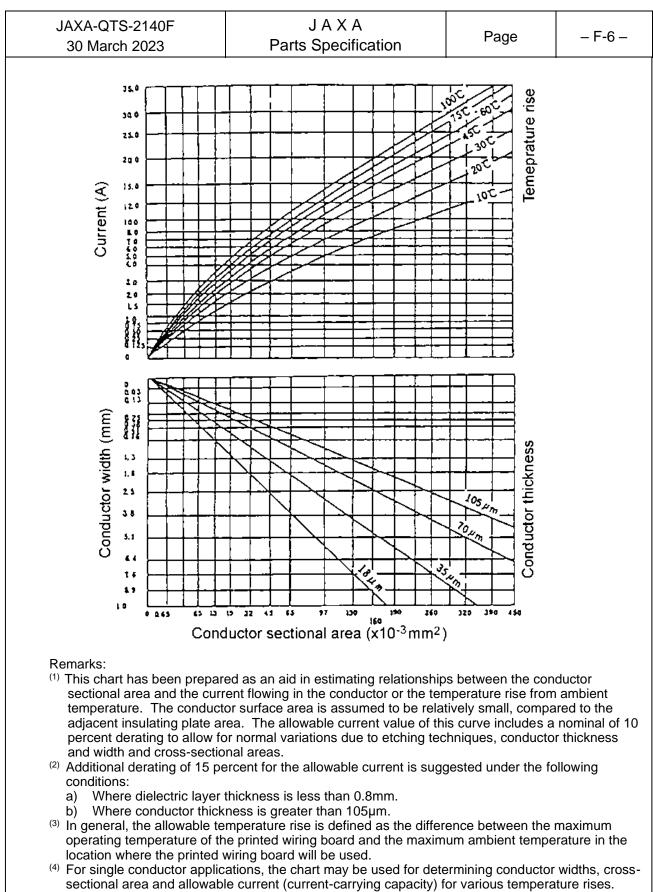
F.3.2.4 Solder Resist

The solder resist applied on the printed wiring boards shall conform to IPC-SM-840 Class H or the equivalent. The application shall be in accordance with manufacturing drawings.

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F.3.2.5	Marking Ink The marking shall be vanish by any solven performance or reliab	t. The marking	shall not adverse		•
F.3.2.6	Plating Unless otherwise spe applied to all through conductive patterns, except SVH shall be surface plating as the applied on lands is pa electrolytic gold platin	holes (excludin except for where coated with cop e plating applied artially required	g SVH and small e solder resist is a per plating and si on lands. When in through holes o	via holes), lands applied. All throu ubsequently with plating other that	and surface gh holes the same type n the plating
F.3.2.6.1	Electroless Copper The electroless cop electrolytic plating insulating material.	oper plating sha inside through h	• •	•	
F.3.2.6.2	Electrolytic Copper The electrolytic cop	-	ll have a minimur	n purity of 99.5 pe	ercent.
F.3.2.6.3	Electrolytic Gold Pl The electrolytic gol nickel plating speci The content rate of exceed 0.1 percent	d plating shall b ified in paragrap	h F.3.2.6.4 may l after the electroly	be applied as an rtic gold plating sh	undercoat. nall not
	Tat	ole F-4. Electro	olytic Gold Plati	ng	
		Item	Specification	n	
		Purity	Min. 99.7 perc	ent	
	KNC	OOP hardness	91 to 129 (inclu	sive)	
F.3.2.6.4	Electrolytic Nickel I The electrolytic nic equivalent, and sha	kel plating shall		AMS-QQ-N-290 (or the

F.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)
 Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are

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	dimensions of the location of the location of the location of the second	same CAD drawing data, the indi ations deviating from grid points n gs and artwork masters (or origin haser. In the event of conflict bet masters (or original production m recedence.	nay be omitted. T al production mas ween the manufa	The sters) shall be cturing
F.3.3.2	CIC CIC shall not be used	for conductor layer unless CIC is	s used as a groun	d layer.
F.3.3.3	Connector for Printed A direct connector (or	Wiring Boards ne-part connector or edge-board o	connector) shall n	ot be used.
F.3.3.4	boards shall be provid small via holes shall b	conductive patterns in different lay ded by through holes including sm be a minimum of 0.3mm in its drill 15mm in its diameter.	nall via holes and	SVH. The
F.3.3.5	•	ne conductor shall be not less tha ternal and internal layers shall be		



- ⁽⁵⁾ For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.
- ⁽⁶⁾ The effect of heating due to heat generating parts is not considered.
- ⁽⁷⁾ The final conductor thickness in the chart does not include plating thickness of metals other than copper.
- ⁽⁸⁾ The 54µm line shall apply to an external layer with SVH.

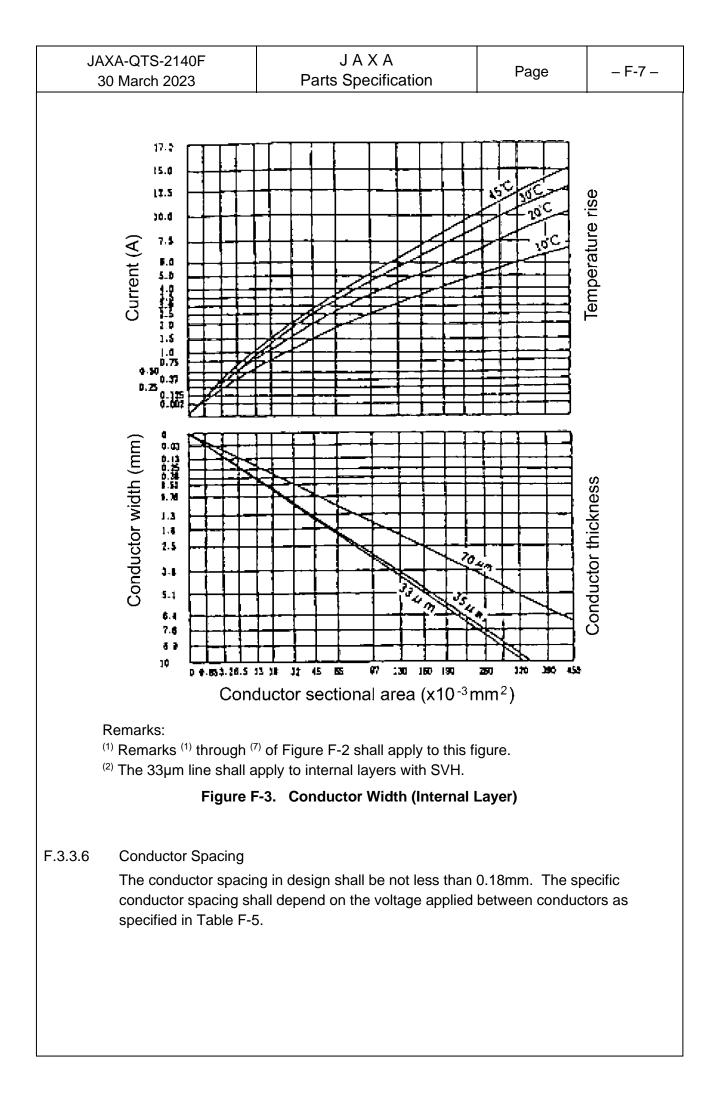


Table F-5. Conductor Spacing for Coated Printed Wiring Board

Voltage applied between	Minimum conductor spacing (mm)		
conductors, DC or AC_{p-p} (V)	External layer	Internal layer	
0 - 100	0.18	0.18	
101 - 300	0.48	0.30	
301 - 500	0.86	0.35	
501 or higher	(0.003xV)+0.1	(0.003xV)+0.1	

F.3.3.7 Land Diameter

The minimum design value of land diameter shall be as specified in Table F-6 (see Figure F-4).

Table F-6. Land Diameter

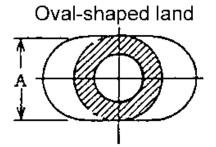
Unit: mm

Hole	Minimum land diameter ⁽¹⁾
SVH and small via holes	Drill diameter + 0.4 ⁽²⁾
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

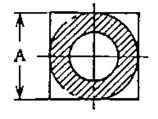
Notes:

⁽¹⁾ The minimum diameter of lands other than round shaped lands shall be measured as the length "A", as shown in Table F-4.

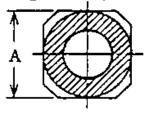
⁽²⁾ The minimum diameter of the land provided with a small via hole shall be 0.76mm.



Square-shaped land



Octagon-shaped land



Rectangular-shaped land

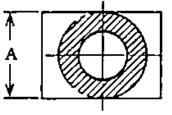


Figure F-4. Measurement of Minimum Diameter of Lands Other than Round Shaped Lands

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F.3.3.8 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table F-7.

Table F-7. Plating or Coating Thickness

Unit: µm

Plating material	Surface and through hole plating thickness		
	Necessary and sufficient thickness for the subsequent		
Electroless copper	process, electrolytic copp	per plating	
	Component hole	Min. 25	
Electrolytic copper	Small via hole	Min. 30	
	SVH	Min. 15	
Electrolytic gold	1.3 to 4.0		
Electrolytic nickel	Min. 5		
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.		

F.3.3.9 Operating Temperature Range

Printed wiring boards shall operate within the temperature range ($-65^{\circ}C$ to $+170^{\circ}C$) of the thermal shock (II) test (paragraph F.3.10.1.2).

- F.3.4 Externals, Dimensions, Marking and Others
- F.3.4.1 Externals and Construction

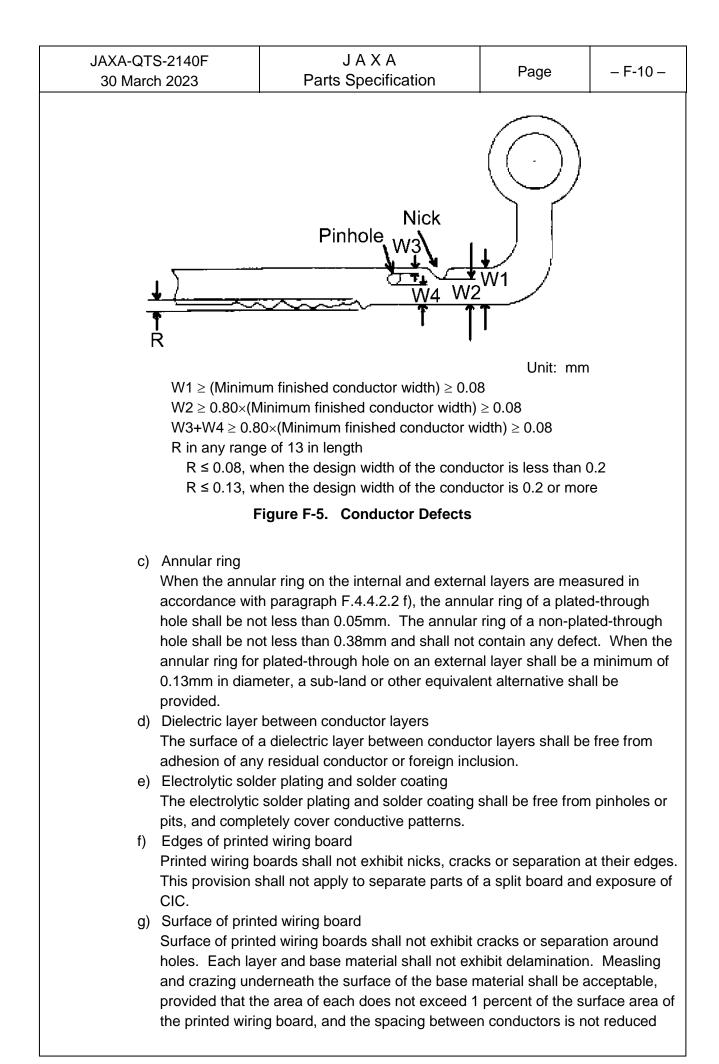
F.3.4.1.1 Externals of Conductive Pattern, Base Material and Solder Resist

a) Conductive pattern

The conductive patterns and CIC shall conform to the approved or provided artwork master (or original production master).

b) Conductor

The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100 mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is not less than 0.2mm, the roughness shall be maximum 0.13mm (see Figure F-5).



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permitted, when equal to or great or 1.6mm, which h) Solder resist The cured sold Significant visual surface, uneven The solder resist scratches and p	rcent. Crazing along edges of the the spacing between the crazing er than the minimum conductor se ever is smaller. I damage such as a thin spot, se color and exposed residual cond shall not encroach onto lands. I holes shall be acceptable, prov der resist. The application range	and an adjacent spacing specified ess, blistering and paration, roughne ductor shall not be Unless otherwise ided that the cond	conductor is on drawings delamination ess on the permitted. specified, ductors are

F.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table F-8.

Unit: mm

conductive patterns shall meet the provisions of manufacturing drawings.

ltem	Dimensional tolerance
External dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.
Conductor width	0.13 or more and less than 0.20: ± 0.05 0.20 or more and less than 0.50: ± 0.10 0.50 or more: ± 20 percent of circuit width
Conductor spacing	For the design of three patterns between basic grids, the tolerance of conductor spacing shall be -0.08. (The positive side tolerance is not specified.) For the design of maximum two patterns between basic grids, the tolerance of conductor spacing shall be -0.10. (The positive side tolerance is not specified.) The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

Table F-8. Dimensional Tolerance

F.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph F.3.2.5 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.

All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on

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	 marking may be place a) Part number b) Year and month c) Manufacturer's r d) Product serial number 	manufactured name or its identification code umber ⁽¹⁾ or lot number Il number shall be provided so that		
	process can			
F.3.4.3.1	usable, it shall be o	art (equivalent to a single wiring bo clearly marked that the part cannot	t be used. This n	narking shall
F.3.4.4	be made by a method such that it does not easily vanish by any solvent. Through Holes When printed circuit boards are tested as specified in paragraph F.4.4.2.2, the plating of through holes, small via holes and SVH shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80µm, and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated. The cross-section diagram for the area of through holes shall be show in Figure F-6. (The parts indicated in black are CIC)			
	Resin recession 	Crack Nodul		

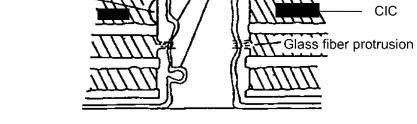


Figure F-6. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure F-7).

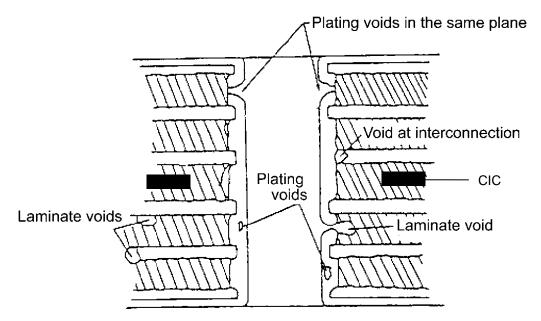
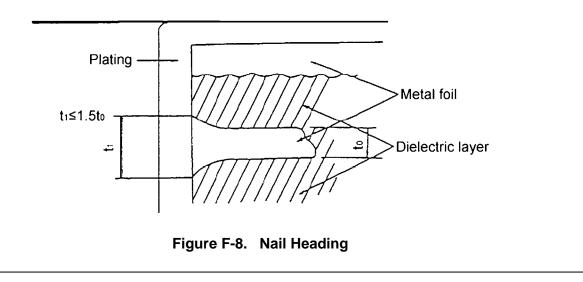


Figure F-7. Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure F-8).

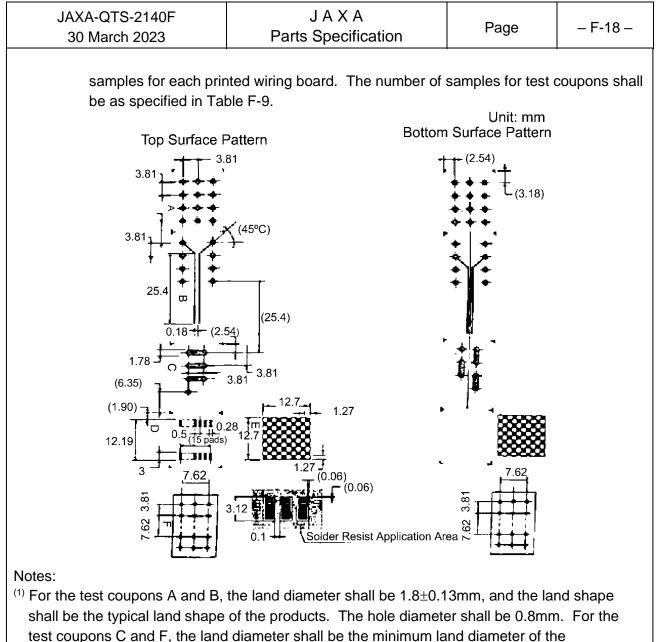


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	 d) Dielectric layer the dielectric lay shall be not less e) Plating thickness The plating thick f) Annular ring 	er registration error shall not excee hickness /er between conductor layers of a than 0.08mm in thickness.	multilayer printed	agraph F.3.3.6.	
F.3.4.5	Solder Resist Thickne	ess			
	•	boards are tested as specified in p be not less than 17.5μm, measure	• •		
F.3.5	Workmanship				
	The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.				
F.3.5.1	Bow and Twist				
	maximum limit for boy manufacturing drawir	boards are tested as specified in p w and twist shall be 0.8 percent, u ngs. For a split board, the percent ecified above, before separation.	nless otherwise s	specified on	
F.3.5.2	Repair				
	The insulating plates	or conductors shall not be repaire tor and an insignificant repair of so			
F.3.6	Plating Adhesion and O	verhang			
	•	ards are tested as specified in para ng of plating and conductors, or sli	• •		
F.3.7	corrosion product, salt, s inclusion and flux residu	ds shall exhibit no fouling including soot, grease, finger print, mold rele ues, or ionic contamination. When aragraph F.4.4.5, the resistivity of t	ease agent, foreig	gn bards are	
F.3.8	Electrical Performance Printed wiring board sha	all meet the following electrical req	uirements.		

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F.3.8.1		ig Voltage fied in paragraph F.4.4.6.1, printe ikdown, flashover or sparkover.	ed circuit boards s	shall not
F.3.8.2		fied in paragraph F.4.4.6.2, printe short-circuiting between circuit pa		shall not
F.3.8.3	resistance between to exceed the value (Ri) connection resistance	ooards are tested as specified in p vo lands connecting a circuit on a which is calculated by the formula between all layers can not be me on resistance shall be repeatedly	Il conductor layer a specified below easured at a time	s shall not . When the , the
	ρ: Volume resistivity a l: Distance between la W: Conductor width (t: Conductor thicknes	mm)	orms the conducto	or (mΩ∙mm)
F.3.9	Mechanical Performance			
F.3.9.1	 Terminal Pull Strengt When tested as spection following requirement a) Bond strength The land shall with the land shall with the land shall with the printed with the	fied in paragraph F.4.4.7.1, printe s. This provision shall not apply t thstand 89.2N pull or 1380N/cm ² , and ing boards are inspected visually shall be no loosening around the t	ed wiring boards s o SVH or small v whichever is sma as specified in pa hrough holes.	ia holes. aller. aragraph cordance
F.3.9.2	following requirement a) Hole solderability The through hole solder. This pro b) Surface solderab	/ e inside wall and land surface shal /ision shall not apply to SVH or sn	l exhibit proper w nall via holes.	retting of

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	•	ew solder. The scattered existence points shall be acceptable, provic one area.	•	•			
	F.3.10 Environmental Performance Printed wiring boards shall meet the following environmental requirements.						
F.3.10.1	Thermal Shock						
F.3.10.1.1	When printed circu there shall be no of completion of the to accordance with pa measured in accord meet the requirement	(applicable to qualification test) it boards are tested as specified in pen circuit, blistering, measling, cr est, circuit continuity and circuit sh aragraph F.4.4.6.2, and connection dance with paragraph F.4.4.6.3. F ents specified in paragraph F.3.8.2 on resistance between circuits beforcent.	azing or delamina orts shall be testo n resistance shall Printed wiring boa 2 after the test, ar	ation. At the ed in be ards shall nd the			
F.3.10.1.2	When printed circu there shall be no of completion of the to accordance with pa measured in accord meet the requireme	(applicable to quality conformance it boards are tested as specified in pen circuit, blistering, measling, cr est, circuit continuity and circuit sh aragraph F.4.4.6.2, and connection dance with paragraph F.4.4.6.3. F ents specified in paragraph F.3.8.2 on resistance between circuits beforcent.	n paragraph F.4.4 azing or delamina orts shall be test n resistance shall Printed wiring boa 2 after the test, ar	ation. At the ed in be ards shall nd the			
F.3.10.2	be no blistering, mea	on Resistance boards are tested as specified in p sling or delamination. The insulati een conductor and CIC shall be no	on resistances b	etween			
F.3.10.3	•	poards are tested as specified in p resistance between circuits befor	• .				
F.3.10.4	 following requirement a) Externals There shall be not blistering or dela b) Cross-section of 	o measling, cracks, separation of p mination.	plating and condu	uctors,			

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	CIC. c) Laminate voids Laminate voids v permitted, provid	r no separation of through hole pla with the longest dimension of 76µr led the conductor spacing within a requirements of the minimum cond rawings.	n as a maximum layer or betweer	shall be hayers shall
F.3.10.5	be no defects such as resistance between c	boards are tested as specified in p s measling, delamination or weave onductors shall be not less than 5 ed in paragraph F.3.8.1 shall be sa	e texture. The ins 00MΩ. After the	sulation
F.3.10.6	maximum value of the	Coefficient boards are tested as specified in p e measured thermal expansion co d wiring boards and the vertical di	efficient for the le	ngth
F.4. Qua	ality Assurance Provisi	ons		
T b a	 F.4.1 In-Process Inspection The in-process inspection specified below shall be performed, and printed wiring board shall meet the requirements of paragraphs F.3.4.1, F.3.4.2, F.3.4.3 and F.3.7. a) Visual inspection of internal layers, construction and dimensions (100 percent) b) Cleanliness (sampling) 			
F.4.2 C	Qualification Test			
F.4.2.1	layers sufficient to ve coupons shall be as s wiring boards and Fig split boards, split boa split boards shall inclu- perforation. Samples	he minimum conductor width, con- rify compliance with the requireme- specified in Figure F-9 for single-si- gure F-10 for multilayer printed wir rd specimens shall be subjected to ude a deep-hole-shape slit, V-groot s shall consist of the production pri- ed on the same work board as the	ents of this appen ided or double-sid ing boards. In or o the qualification ove cut and contin nted wiring board	dix. The test ded printed der to qualify test. The nuous ls and test
F.4.2.2	completion of Group using specimens allo may be performed in	per of Samples up shall be performed in the order I and II tests, Group III through VII cated to the appropriate group tes any order regardless of group nur /III shall be performed in the order	I tests shall be pe ts. Group III thro nber. However, t	erformed ugh VIII tests ests in each



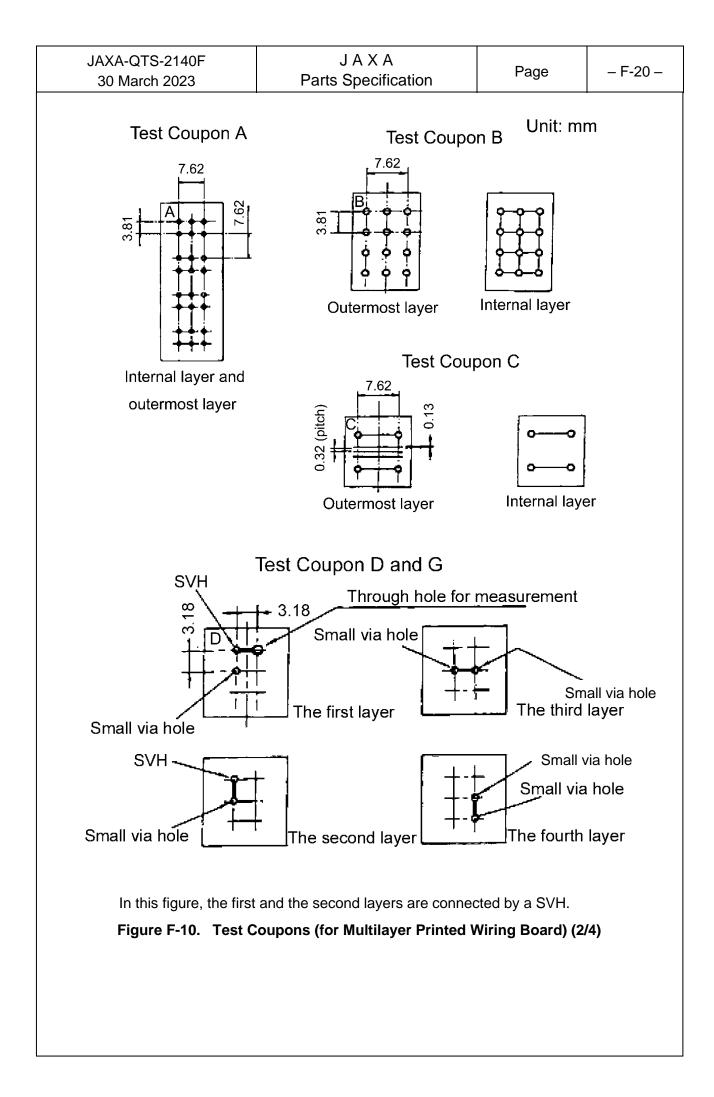
- test coupons C and F, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land. The test coupon F shall be prepared, only when the corresponding product has small via holes. All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board. The CIC shall be produced so as to form the same structure as those of the corresponding product, and the proper clearance shall be set between CIC and through hole wall surface for the test coupon containing through holes. However, for any product with CIC/through hole interface, the interface shall be set at A area in the figure.
- $^{(2)}$ The conductor width shall be 0.5±0.1mm unless otherwise specified.
- ⁽³⁾ The dimensions in the parentheses are reference dimensions.
- ⁽⁴⁾ Solder resist shall apply to the test coupons B, D, and E, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon B shall be the land diameter increased by 0.2mm. For coupon E, the solder resist shall apply to the entire layer.

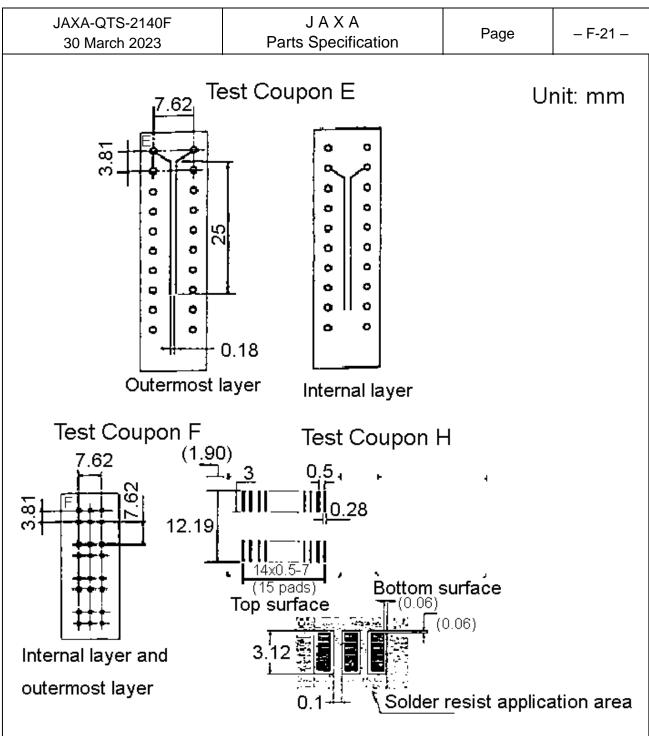
Figure F-9. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board) Arrangement of Test Coupons

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 (2) For tess small v diameter All holes secifie (3) For tess and the holes se diameter wiring be (4) Test construction of layer to have The lar correspondence the proor The hominimus shall be 1.8mm The hominimus shall be 1.8mm The hominimus shall be 0.8m not specifie (6) The Clocorrespondence the rest is resist is r	coupons B, C, E and F, the land dial and shape shall be the typical land s all be through holes. The hole diame tolerance shall be the tolerance for bard. pons D and G are different in the nu e. Each coupon shall be produced so and via hole structure as those of the a circuit continuity through all layers I diameter shall be that of each SVH onding products. The land shape sha ucts. diameter shall be the maximum hol n lands. On both ends of the printed formed to measure the resistance. The diameter tolerance is not specified. diameter for the test coupon M shale sponding products. The land shape oducts. The hole diameter shall be to or the minimum lands. Through hole tance. The land diameter shall be to or the minimum lands. Through hole tance. The land diameter shall be to or the minimum lands. Through hole tance is not specified. shall be produced so as to form the onding product, and the proper cleara ugh hole wall surface for the test coupons formed at B area. sist shall apply to the test coupons E required for the products. The cleara plied on the test coupon E shall be e mons K and L shall be prepared, whe H. Those coupons are different in the	e the minimum lar wiring board. The er among the mini- ameter tolerance meter shall be 1.8 shape of the produ- eter shall be 0.8m the corresponding by via holes. and small via hol all be the typical la e diameter applie wiring board, thro The land diameter all be the typical la e shall be the typical la e the maximum hole es shall be the typical for meter ance shall be formed same structure a ance shall be set l upon containing the ole interface, the es the correspond to be the typical la en the correspond to be number of laye which are connect number of condu of layers. Therefor coordance with the	ad diameter of e hole mum lands. is not B±0.13mm, ucts. All am. The hole g printed d via hole ame number product, and e of the and shape of d for the bugh holes r shall be hrough holes. via hole of cal land shape e diameter d to measure ameter shall er tolerance is s those of the between CIC brough holes. interface when solder the solder diameter d ing products rs and via ted by SVH. ctors, e, the is figure.

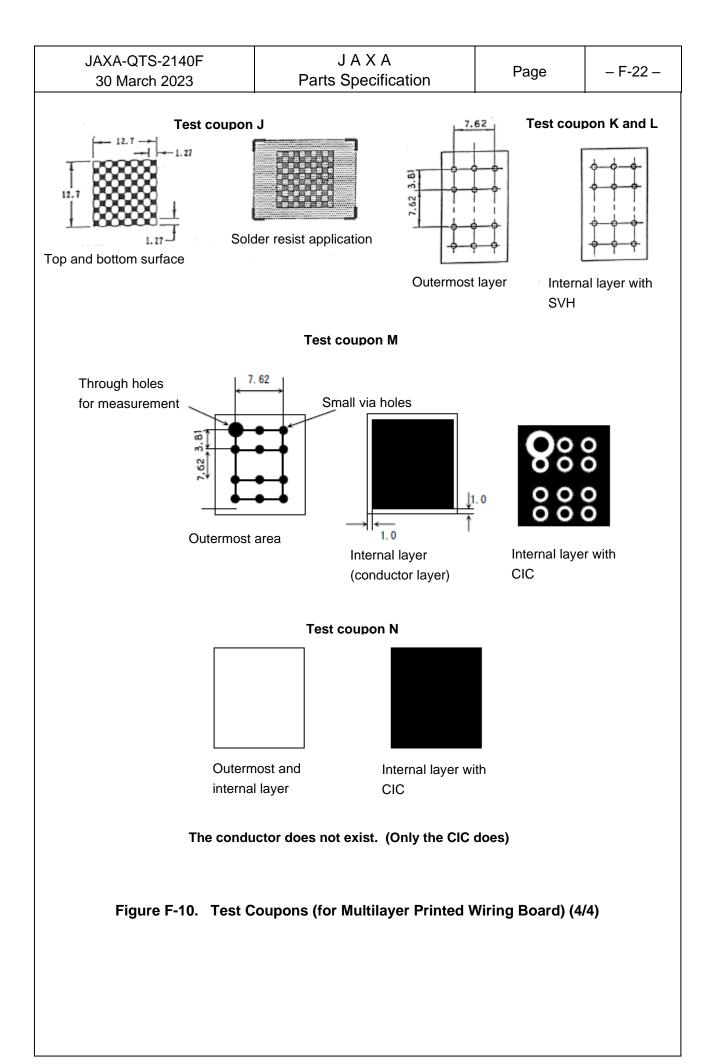
different arrangement is also acceptable.
 ⁽¹¹⁾ The symbols of test coupons (A to H and J to N) shall be used for identification and not for the object of inspection. The marking method is not specified.

Figure F-10. Test Coupons (for Multilayer Printed Wiring Board) (1/4)









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		Table F	-9. Qualif	ication Tes	t				
		Test				Pass/fail			
			Deguinement		Samples ⁽¹⁾		Samples ⁽¹⁾		Quantity of
Group	Order	Test item	paragraph	Test method paragraph	Production printed wiring boards	Test coupon (2)	Quantity of allowable defects		
	1	Design and construction	F.3.3	F.4.4.2.1		A, B, C,			
I	2	Externals, dimensions, marking and others Externals and construction Dimensions Marking	F.3.4.1 F.3.4.2 F.3.4.3	F.4.4.2.1	No. 1 to No. 6	A, B, C, D or E, F, G or H, K, L, M and N ⁽⁴⁾			
	3	Workmanship ⁽³⁾	F.3.5	F.4.4.3					
п	1	Plating adhesion and overhang	F.3.6	F.4.4.4	No. 1 to No. 6	С			
11	2	Bow and twist	F.3.5.1	F.4.4.3.1	NO. 1 10 NO. 0	N/A			
	1	Through holes	F.3.4.4	F.4.4.2.2	No. 1	A, F and K			
	2	Terminal pull strength	F.3.9.1	F.4.4.7.1		F			
	3	Solder resist thickness	F.3.4.5	F.4.4.2.3		J			
	1	Connection resistance	F.3.8.3	F.4.4.6.3					
IV	2	Hot oil resistance	F.3.10.3	F.4.4.8.3	No. 2	D	0		
	3	Connection resistance	F.3.8.3	F.4.4.6.3					
	1	Circuitry	F.3.8.2	F.4.4.6.2					
	2	Connection resistance	F.3.8.3	F.4.4.6.3					
V	3	Thermal shock (I)	F.3.10.1.1	F.4.4.8.1 a)	No. 3	E and G ⁽⁵⁾			
	4	Circuitry	F.3.8.2	F.4.4.6.2		G			
	5	Connection resistance	F.3.8.3	F.4.4.6.3					
VI	1	Humidity and insulation resistance	F.3.10.2	F.4.4.8.2	No. 4	E and M			
	2	Dielectric withstanding voltage	F.3.8.1	F.4.4.6.1					
VII	1	Thermal stress	F.3.10.4	F.4.4.8.4	No. 5	A, B and L			
VII	2	Solderability	F.3.9.2	F.4.4.7.2		B and H ⁽⁶⁾			
VIII	1	Thermal expansion coefficient	F.3.10.6	F.4.4.8.6	No. 5	N			
IX	1	Radiation hardness	F.3.10.5	F.4.4.8.5	No.6	N/A)		
-	1	Materials	F.3.2	N/A	(7)		N/A		

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. In order to qualify split boards, split board specimens shall be submitted as the production samples.

⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

⁽³⁾ Bow and twist (paragraph F.3.5.1) of the samples shall be tested during the second test of Group II tests.

⁽⁴⁾ Group I test shall be performed on the test coupons which are to be provided for Group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

⁽⁵⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽⁶⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

⁽⁷⁾ Data to certify compliance with design specifications shall be submitted.

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F.4.3 Qu	ality Conformance In	spection		
F.4.3.1 (Quality Conformance	Inspection (Group A)		
F.4.3.1.1	Sample			
	coupons and samp Even though any p process and is mar lot. However, in or marked with rejecti	nance inspection shall be perform le product shall be manufactured art of a split board fails an inspect ked with rejection, the board may der not to adversely affect the insp on shall not be used as a specime of parts of the same patterns or pa	simultaneously. ion in the manufa be included in ar pection result, the en. A "split board	acturing inspection e part " means a
F.4.3.1.2		nd Sample Size order of Group A inspection shall ons within each group shall be pe		

F-10. The inspections within each group shall be performed in the order listed. For Group IV and V tests, one test coupon shall be provided for each coupon type specified in Table F-10.

		Inspection				Pass/fail		
			Requirement	Test method	Quantity of samples		Quantity of	
Group	Order	Inspection item	paragraph	paragraph	printed wiring boards	Test coupon ⁽¹⁾	allowable defects	
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	F.3.4.1 F.3.4.2 F.3.4.3	F.4.4.2.1	All	N/A		
	2	Workmanship ⁽²⁾	F.3.5	F.4.4.3				
II	1	Bow and twist	F.3.5.1	F.4.4.3.1	All	N/A	0	
III	1	Circuitry	F.3.8.2	F.4.4.6.2	All	N/A	> °	
	1	Thermal stress	F.3.10.4	F.4.4.8.4		A, B and K ^{(3), (4)}		
IV 2	2	Through holes Conductive interface Plating thickness	F.3.4.4 b) e)	F.4.4.2.2 a) and d) c)	N/A	A,F and L (A and F) ^{(3) (4)}		
V	1	Solderability	F.3.9.2	F.4.4.7.2	N/A	B and H (A and D) ⁽⁵⁾)	

Table F-10. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ A letter inside the parentheses shows the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

⁽²⁾ Bow and twist (paragraph F.3.5.1) of the samples shall be tested during the first test of Group II tests.

⁽³⁾ For a multilayer printed wiring board, test coupon A shall be inspected, when the corresponding product is provided with small via holes. Test coupons K and L shall be inspected when the corresponding products have SVH.

⁽⁴⁾ For a single-sided or double-sided printed wiring board, test coupon F shall be inspected, only when the corresponding product is provided with small via holes.

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⁽⁵⁾ Test coupons A and B shall have been subjected to the test for Thermal stress. Also, test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.

- F.4.3.2 Quality Conformance Inspection (Group B)
- F.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

F.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table F-11. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

	Inspection				Pass/fail		
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects	
I	1	Plating adhesion and overhang	F.3.6	F.4.4.4	С		
П	1	Terminal pull strength	F.3.9.1	F.4.4.7.1	F		
	1	Connection resistance	F.3.8.3	F.4.4.6.3			
III	2	Hot oil resistance	F.3.10.3	F.4.4.8.3	D		
	3	Connection resistance	F.3.8.3	F.4.4.6.3	D		
	1	Circuitry	F.3.8.2	F.4.4.6.2			
	2	Connection resistance	F.3.8.3	F.4.4.6.3			
IV	3	Thermal shock (II)	F.3.10.1.2	F.4.4.8.1 b)	E and G ⁽¹⁾		
	4	Circuitry	F.3.8.2	F.4.4.6.2			
	5	Connection resistance	F.3.8.3	F.4.4.6.3			
V	1	Humidity and insulation resistance	F.3.10.2	F.4.4.8.2	E		
v	2	Dielectric withstanding voltage	F.3.8.1	F.4.4.6.1			
VI	1	Thermal expansion coefficient	F.3.10.6	F.4.4.8.6	N)	

 Table F-11. Quality Conformance Inspection (Group B)

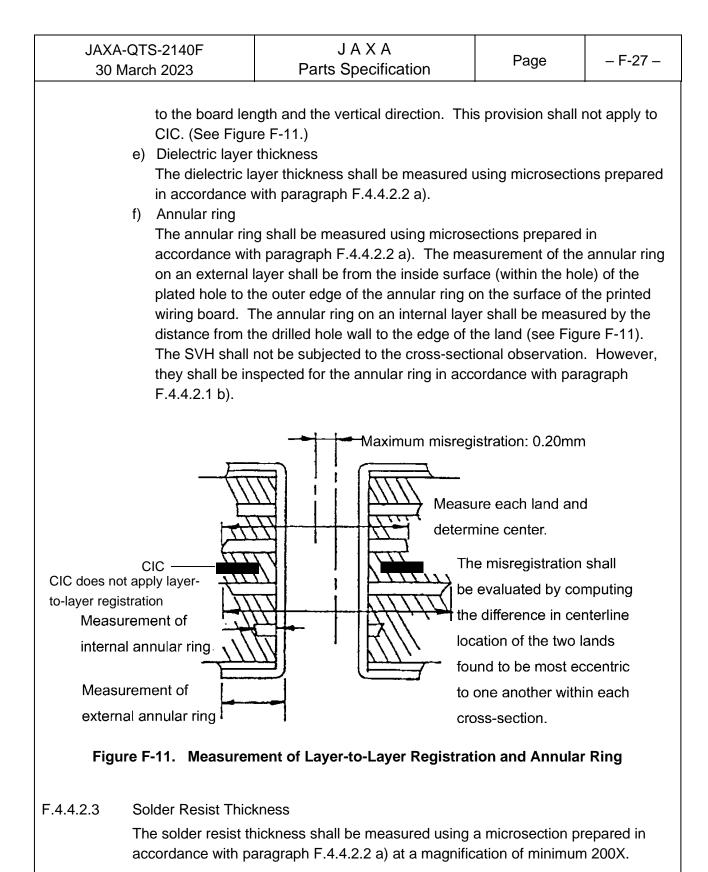
Note: ⁽¹⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

F.4.4 Methods for Test and Inspection

F.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

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F.4.4.2	Externals, Dimension	s, Marking and Others		
F.4.4.2.1	 marking of the prin a) Conductive pat Dimensions of optical measuri b) Annular ring The measurem inside surface (annular ring on 	on, externals, dimensions (conduct ted wiring board shall be tested. terns and edges conductive patterns and edges sha ng instrument which has sufficient ent of the annular ring on an exter within the hole) of the plated hole the surface of the printed wiring b easured using an optical measurin	all be measured u accuracy. nal layer shall be to the outer edge oard. Dimension	from the of the s of annular
F.4.4.2.2	 inside surface (within the hole) of the plated hole to the cannular ring on the surface of the printed wiring board. If ring shall be measured using an optical measuring instrusulficient accuracy. 7.4.4.2.2 Through Holes a) Vertical microsection The printed wiring board specimen shall be cut in the verticent of a hole. The sample shall be encapsulated and center of the hole. At least three plated-through holes sheach work board. The through holes for the vertical microsection shall be inspected for the solder resist thick integrity (plating voids, internal connection of the vertical registration, base material thickness and plating thickness 50 to 100X. To inspect the layer-to-layer registration, on shall be microsectioned parallel to the length direction of and the other shall be microsectioned perpendicular to the direction. b) Horizontal microsection Only multilayer boards shall be subjected to the horizont inspection. Multilayer boards with through holes shall be polished. A conductor layer shall be polished in the paramicrosection is prepared to expose the conductor layer. through hole (internal connection in horizontal direction) magnification of 50 to 100X. c) Plating thickness The plating thickness shall be measured using microsection descord ance with paragraph F 4.4.2.2 a) at a magnification of accordance with paragraph F 4.4.2.2 a) at a magnification of heasurements shall be averaged from three determination through hole. Isolated thick or thin sections shall not be d) Layer-to-layer registration shall be measured at a magnification of an expose the conduct at a magnification of heasurements in thickness or the sections shall not be 		ed and polished in noles shall be insp cal microsection in the work board. ist thickness and vertical side, laye hickness) at a ma- tion, one of the th ction of the multil lar to the board's norizontal microse shall be encapsul he parallel direction he parallel direction i layer. The integ ection) shall be in ficrosections prepa- nification of minin rminations for a p not be used for a at a magnification	to expose the pected for may be The vertical plating r-to-layer agnification of arough holes ayer board length ection lated and on. The rity of the aspected at a ared in num 200X. blated- iveraging. n of 25 to F.4.4.2.2 a).

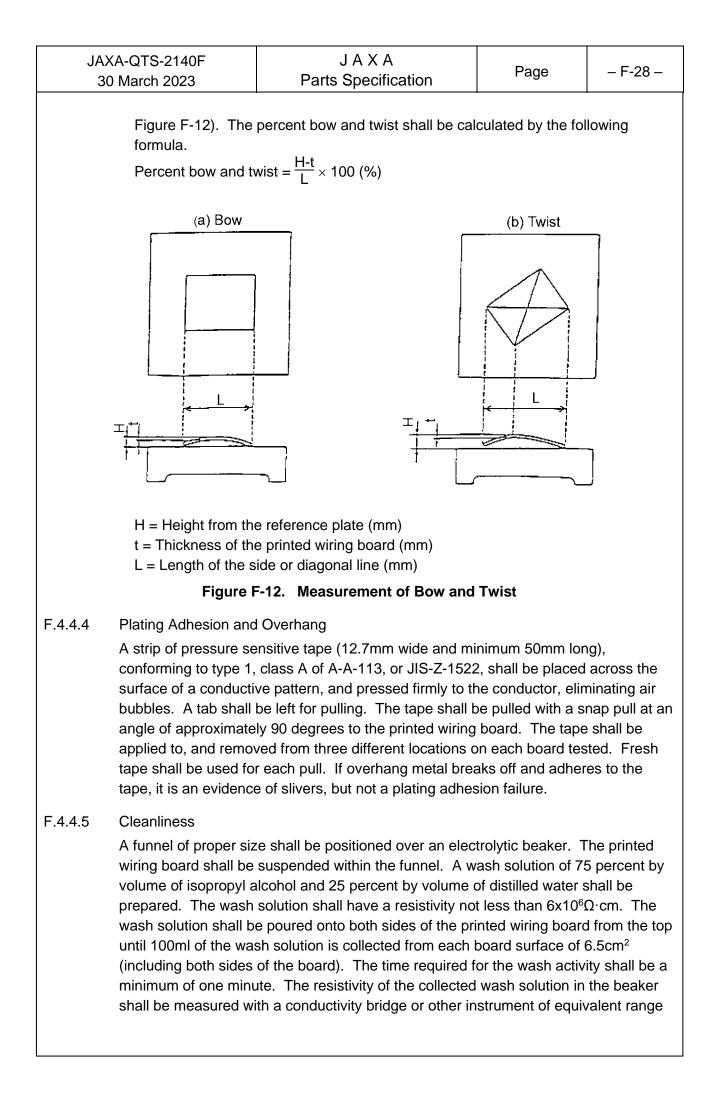


F.4.4.3 Workmanship

The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

F.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see



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	and accuracy. The a perform the cleanline		thods specified in Ta	ble F-12 may b	be used to
	-	Fable F-12. Eq	uivalent Factors		
	Method	Resistivity (×10 ⁶ Ω·cm)	Equivalent factor	Equivalents sodium chlor (µg/cm²)	
C	onductivity bridge	2	1	1.56	
0	mega Meter ⁽¹⁾	2	1.39	2.20	
No F.4.4.6	te: ⁽¹⁾ Alpha Metals In Electrical Performan The electrical perforr	се		llows.	
F.4.4.6.1		standing voltage of MIL-STD-202. 1000V 30 sec cation: Betwee electric	e test shall be perform The following cond $_{AC}$ peak or $1000V_{DC}$ conds en conductive patter cally isolated pattern ling CIC).	itions shall app ns of each laye	ly. er and the
F.4.4.6.2	interconnected b) Circuit shorts A voltage of 25 conductive pat	circuits to verify $50V_{DC}$ shall be aptern and all adjace	shall be flown throug connectivity oplied between all co cent common termin of short-circuiting.	mmon terminal	ls of each
F.4.4.6.3		tween the throug	gh hole terminals sha inal method capable		-
F.4.4.7	Mechanical Performa	ance			
	The mechanical perf	ormance tests sl	hall be performed as	follows.	
F.4.4.7.1	peeled and pulled	be cut with a sha toward the land,	arp knife at minimum and cut off by apply and so as not to deg	ing the sharp k	nife at the

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	March 2023 Then, a lead wire s and the following p using a soldering in a) Solder a lead w b) Remove the lead c) Re-solder the lead d) Remove the lead e) Re-solder the lead completely during the resoldering. The side velop the tip term solder iron without wiring board. The After the completion a tensile tester at main minute forward and requirement (L) or out shall not be required pull test shall be perfollowing formula. $L \ge 1380 \times \frac{\pi \left\{ (d_2)^2 - \frac{1}{4} \right\}^2 + \frac{1}{4} = \frac{1}{4}$	vire in to the through hole. ad wire from the through hole (sold ead wire in to the through hole (sold ead wire in to the through hole (sold ead wire in to the through hole. ad shall not be clinched. The lead the solder removal and replaced we oldering iron shall be used at 15 to operature of 232 to 260°C. The lead bringing its tip into contact with the heating time shall be limited to the n of re-soldering in e) above, the l oom temperature, and be pulled at d vertically with the land until the p any failure occurs. Disconnection garded as a failure, and a new lead erformed again. The pull strength $(\underline{d}_i)^2$	ensile tester shall ng and solder rem der removal) der removal) wire shall be tak with a new one wh o 60W and adjust ad wire shall be h e conductor of the bare minimum. ead wire shall be h t the rate of 50mr ull strength reach or the lead wire h d wire shall be so	be selected noval by en off en ed to eated by the e printed installed on m per nes the being pulled ldered and
	L = Pull strength (N d_1 = Hole diameter d_2 = Land diameter	(cm)		
F.4.4.7.2	Solderability a) Hole solderabil The wetting of s to the inspectio b) Surface soldera After the specir STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. The 25±6mm per se	ity solder shall be inspected using a n n specified in paragraph F.4.4.8.4	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp into the solder ba econds and raise men shall be kep	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of t in the

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	permitted. The after the solder	condition of solder on the conduct is solidified.	tive surface shall	be inspected
F.4.4.8	Environmental Perfor The environmental pe	mance erformance tests shall be performe	ed as follows.	
F.4.4.8.1	MIL-STD-202. The a) Thermal shock The test shall b shall be –30°C The number of b) Thermal shock The test shall b	test shall be performed in accordate following conditions shall apply. (I) (applicable to qualification test) e performed under the test condit and the time for step 2 and 4 shall cycle shall be 1000 cycles. (II) (applicable to quality conformate e performed under the test conditi C, and the time for step 2 and 4 shall	ion B. The low te l be within 2 minu ance inspection) on F-3. The high	emperature ites each. i temperature
F.4.4.8.2	cycles, and the (including CIC) specimen shall 25±5°C and eva b) Insulation resis The test shall b	ance s in Test Method 106 of MIL-STD- polarization voltage of 100V±10V _I during the test. Upon completion be taken out of the bath and dried aluated.	DC shall be applie of step 6 of the fi I immediately by I he test condition E	d to all layers nal cycle, the blowing air at 3, Test
F.4.4.8.3	temperature. After	Il be dried at 120±5°C for 2 hours a that, the specimen shall be imme cooled to room temperature. Imm	rsed in oil or wax	at 260±5°C
F.4.4.8.4	shall be placed on specimen shall the floated in a solder l for a period of 10 s to be cooled. After shall be inspected and for any connec microsection prepa	Il be dried for 2 hours at 121 to 149 a ceramic plate in a desiccator, ar n be fluxed in accordance with the bath of composition Sn 63±5 perce econds. The specimen shall be pl a check for any defects on the ex for any crack on the internal copper ction between internal copper/CIC ared in accordance with paragraph be measured at a probe depth not he solder.	nd cooled down. detail specificati ent maintained at laced on a piece ternal surface, th er foil and for lam and through hole F.4.4.2.2 a). So	The on and 288±5°C of insulator e sample inate voids, es using the lder

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F.4.4.8.5	Radiation Hardnes	s adiation shall be performed by usi	0			
	0.5×10^4 Gy to 1×10^4 Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4 Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph F.4.4.6.1 and F.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.					
F.4.4.8.6	 The test shall be performed a) Specimen concorrect The temperature hours. Eliminative temperature. b) Specimen dimension (mm). c) Measured temperature d) Direction of mericipative specimen of me	 performed in accordance with paragraph F.4.4.6.1 and F.4.4.8.2 b), respectively the insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test. Thermal Expansion Coefficient The test shall be performed in accordance with JIS K 7197 and as follows. a) Specimen conditioning The temperature for the specimen shall be kept between 121 and 149° hours. Eliminate any moisture from the specimen and cool it to the root temperature. b) Specimen dimensions The specimen shall be tabular form with 10mm x 10mm x board thicknee 				

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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	APPENDIX G						
PRINTED WIRING BOARDS, AREA ARRAY PACKAGING							
G.1. G	eneral						
G.1.1	Scope						
This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards capable of area packaging design such as BGA (Ball Grid Array) and CGA (Column Grid Array) (hereinafter referred to as "printed wiring boards").							
G.1.2	Part Number						
	The part number of the	printed wiring boards is in the fo	llowing form.				
	Example: JAXA(1) 2140	/ <u>G106</u> <u>GI</u> Individual Base identification material code (G.1.2.1)	<u>14(²)</u> Number of layers (G.1.2.2)				
	Notes:	(0.1.2.1)					
	 "JAXA" indicates the Number of conductor 	common part for space use and layers	d may be abbreviate	ed to "J".			
G.1.2.1	Base Material Code						
	The base material co	de is as specified in Table G-1.					
	т	able G-1. Base Material Cod	e				
	Base material code	Base materi	al				
	GF	Glass base woven epoxy resin, compliant to IPC-4101 or JPCA/N	IASDA-SCL01				
	GI Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01						

G.1.2.2 Number of Layers

The maximum number of layers shall be specified in each detail specification.

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G.2. A	Applicable Documents et	C.			
G.2.1	Applicable Documents		<i></i>		
	a) JERG-0-043 Sta	nts shall be as follows and as spea andards for Surface Mount Solderin Space Application		h 2.1.	
	c) IPC-2152 Sta	st methods of copper-clad laminate andard for Determining Current Ca ard Design	•	•	
G.2.2	Reference Documents				
	a) JERG-0-054 Sta	nts shall be as follows and as spec andards for BGA/CGA Soldering P Space Application		າ 2.2.	
	b) JIS C 6012 Qualification and Performance Specification for Rigid Printed Boards				
G.3. F	Requirements				
G.3.1	Qualification Coverage				
	Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs G.3.2 through G.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. If necessary, additional qualification coverage shall be specified in the detail specification.				
G.3.2	Materials				
	The materials shall be specified as follows.				
G.3.2.1	4101 or JPCA/NASE The nominal thickne	and Prepreg inate and prepreg shall conform to A-SCL01, and shall be as specifie as of the base material shall be no copper foil shall be as specified in	d on drawings. less than 0.05mr		

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Table G-2. Thickness of Copper Foil (Nominal)						
			Unit: µm	_		
Layer	Classification	Classification Copper foil				
		thic	kness			
External	With SVH	9 m	ninimum			
layer	Without SVH	18	minimum			

SVH layer

without SVH

Any layer other than SVH layer or a layer

The thermal expansion coefficient of the board thickness direction (direction Z) of GF
shall be less than 50ppm/°C when the test is performed in accordance with JIS C
6481.

9 minimum

35 minimum

The standard applied to the materials used in the printed wiring boards shall be clearly specified in the detail specification. The detailed information about base materials such as type of resin and glass-transition temperature shall be specified in the Application Data Sheet (hereinafter referred to as "ADS").

G.3.2.2 Via Hole Filling Materials (Filling Resin)

Internal

layer

The filling materials for SVH and small through hole shall be resin. The detailed information about the filling materials such as type of resin and glass-transition temperature shall be specified in ADS.

G.3.2.3 Solder Resist Ink

The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent.

G.3.2.4 Marking Ink

The marking shall be conducted using epoxy resin base ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

G.3.2.5 Plating

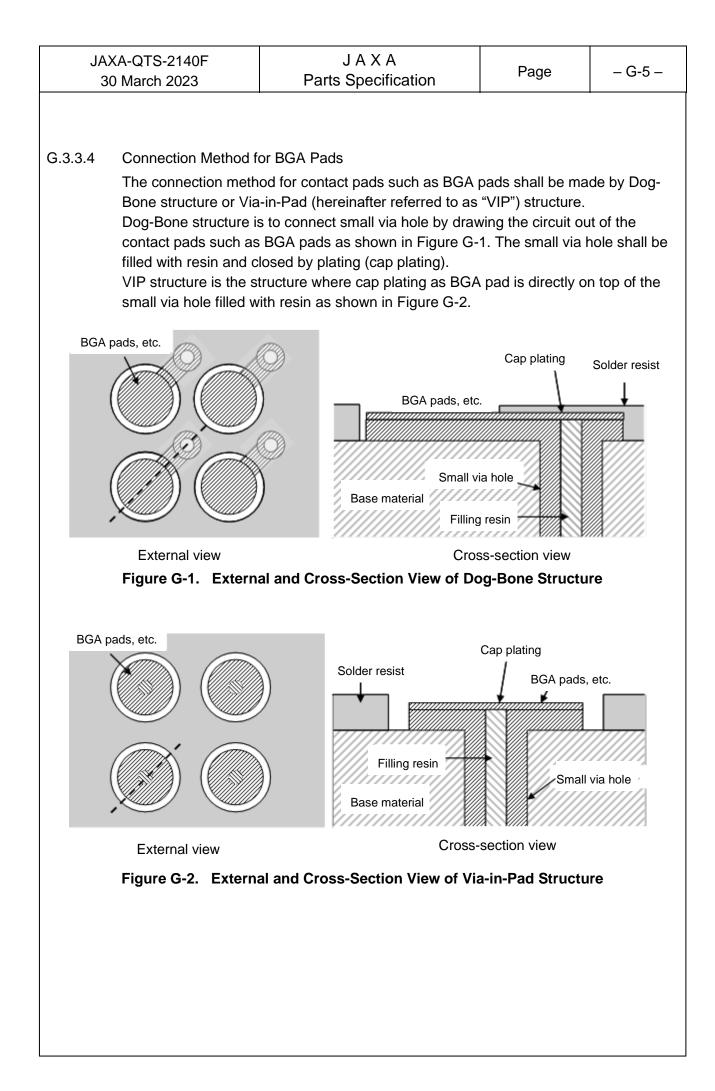
Electroless and electrolysis plating shall be applied to all through holes and for cap plating. Solder coating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.

G.3.2.5.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating to form a conductive layer over the insulating material.

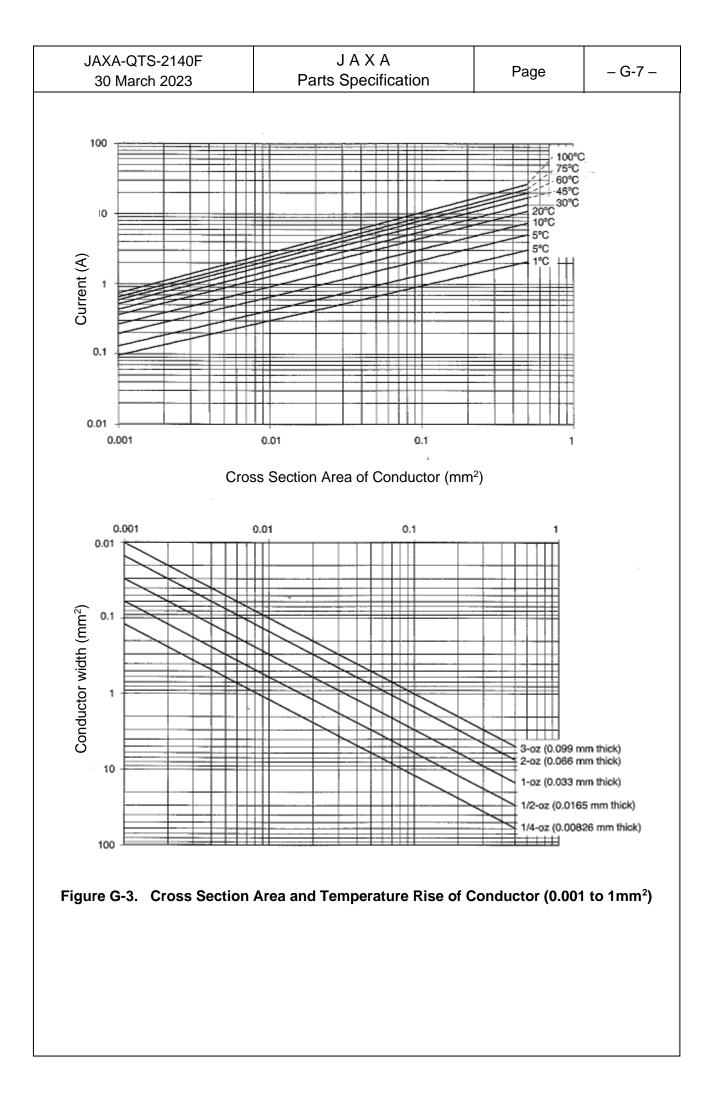
G.3.2.5.2Electrolytic Copper PlatingThe electrolytic copper plating shall have a minimum purity of 99.5 %.

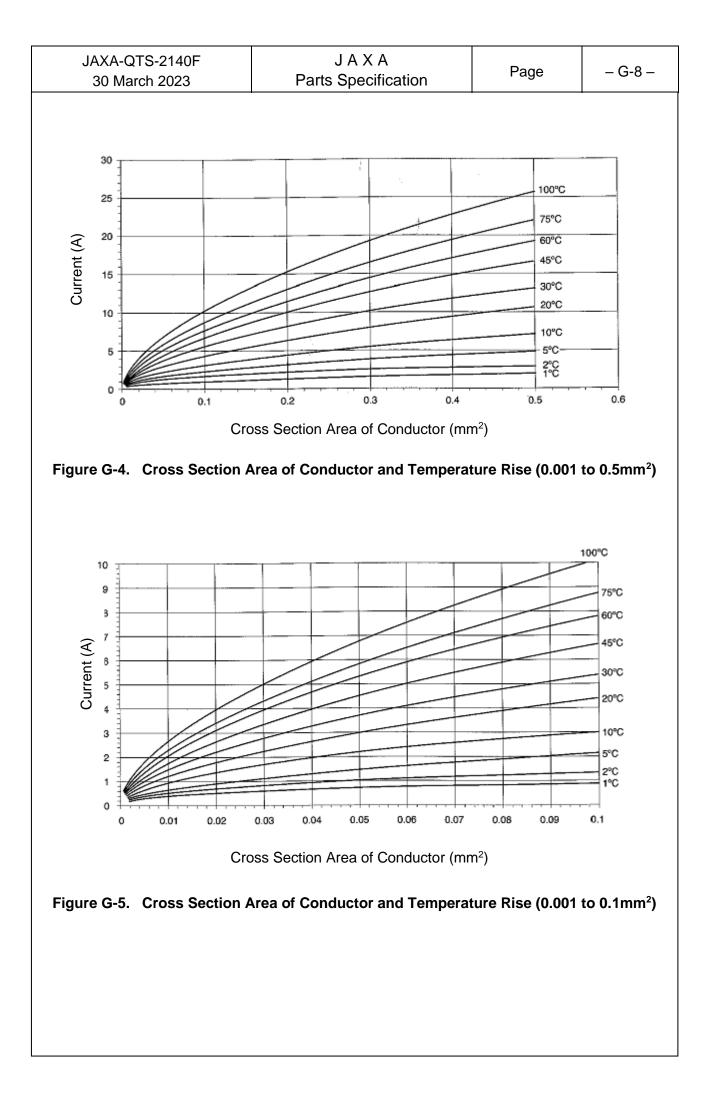
	A-QTS-2140F March 2023	J A X A Parts Specification	Page	– G-4 –	
G.3.2.5.3	nickel plating speci The content rate of exceed 0.1 % exce	d plating shall be as specified in fied in paragraph G.3.2.5.4 shal impure metals after the electrol pt for the metal added to increas	l be applied as an u ytic gold plating sh se the hardness.	undercoat.	
		le G-3. Electrolytic Gold Plat	_		
	Item	Specifica			
	Purity KNOOP hard	Min. 99.7 ness 91 to 129 (inc			
G.3.2.5.5	•	kel plating shall conform to SAE all be of a low stress type.	-AMS-QQ-N-290 o	r the	
G.3.3 D	The solder used fo Design and Constructio	r solder coating shall contain 50 n	to 70 % tin.		
G.3.3.1	Printed wiring boards prepared in accordan masters (or original p event of conflict betw	ngs and Artwork Master (or Orig shall be designed and their man ce with this appendix. The man roduction masters) shall be app een the manufacturing drawings asters), the manufacturing drawi	nufacturing drawing ufacturing drawing oved by the purch and artwork maste	is shall be s and artwork aser. In the ers (or	
G.3.3.2	 Connector for Printed Wiring Boards A direct connector (one-part connector or edge-board connector) shall not be used. 				
G.3.3.3		conductive patterns in different l ded by small via holes, SVH or t	•	d wiring	

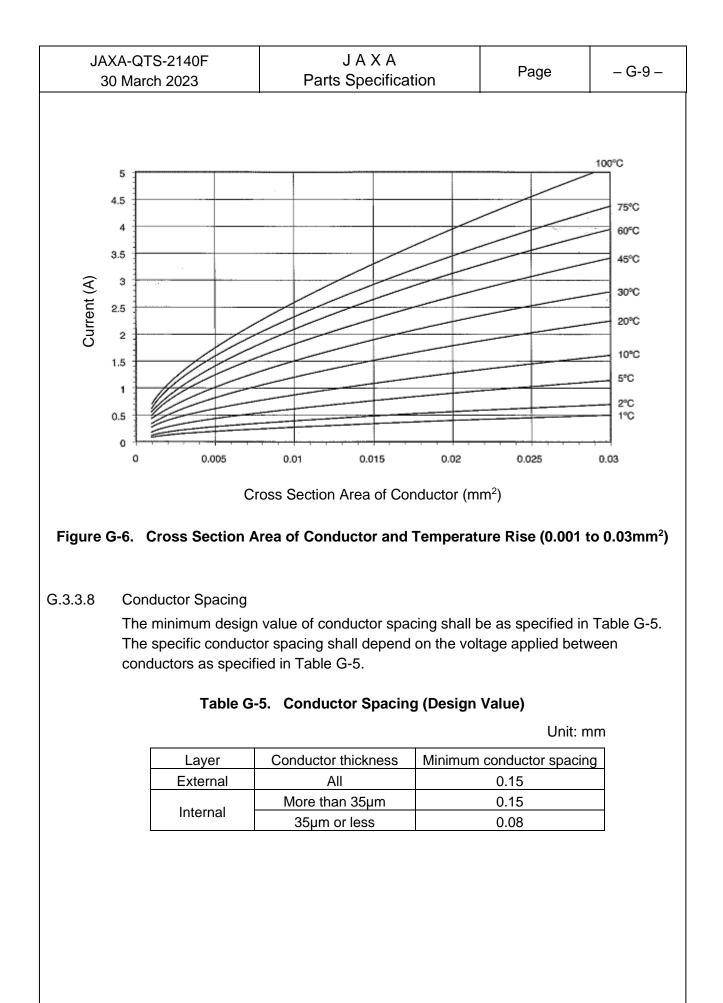


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G.3.3.5		ough Hole Diame minimum hole d	eter iameter for small via hole	e and SVH	shall be φ0.20m	ım as a drill
		. When the land I be φ0.20mm as	of via hole is used as BG s a maximum.	SA pads, e	tc., the drill hole	for via hole
G.3.3.6	Fillir	ng Resin for Thro	ough Hole			
	The small via hole to be filled with via filling materials shall be specified in the production drawing. The small via holes and SVH in VIP structure shall be filled with via filling materials.					
G.3.3.7	Con	ductor Width and	d Thickness			
	Conductor Width and Thickness The minimum design value for conductor width shall be as specified in Table G-4. The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor. Figures G-3, G-4, G-5, and G-6 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this will apply to both internal and external layers of the conductor under vacuum and space environmental conditions. The details shall be specified in IPC-2152. When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.					
		Table (G-4. Conductor Width	(Design V	alue)	
					Unit: mm	
		Layer	Conductor thickness	Minimum	conductor width	
		External	All		0.10	

Layer	Conductor thickness	Minimum conductor width	
External	All	0.10	
	More than 35µm	0.10	
Internal	35µm or less	0.08	







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Table G-6. Conductor Spacing for Printed Wiring Boards

Unit	mm
•	

Voltage applied between	Minimum conductor spacing		
conductors, DC or AC_{p-p} (V)	External layer	Internal layer	
0 to 50	0.15	0.08	
51 to 100	0.15	0.10	
101 - 300	0.40	0.20	
301 - 500	0.80	0.25	
501 or higher	(0.003xV)	(0.0025xV)	

G.3.3.9 Land Diameter

The minimum design value of land diameter shall be as specified in Table G-7 (see Figure G-7). Non-functional land is not necessary when maintenance of conductor spacing and electrical characteristics requirements are specified.

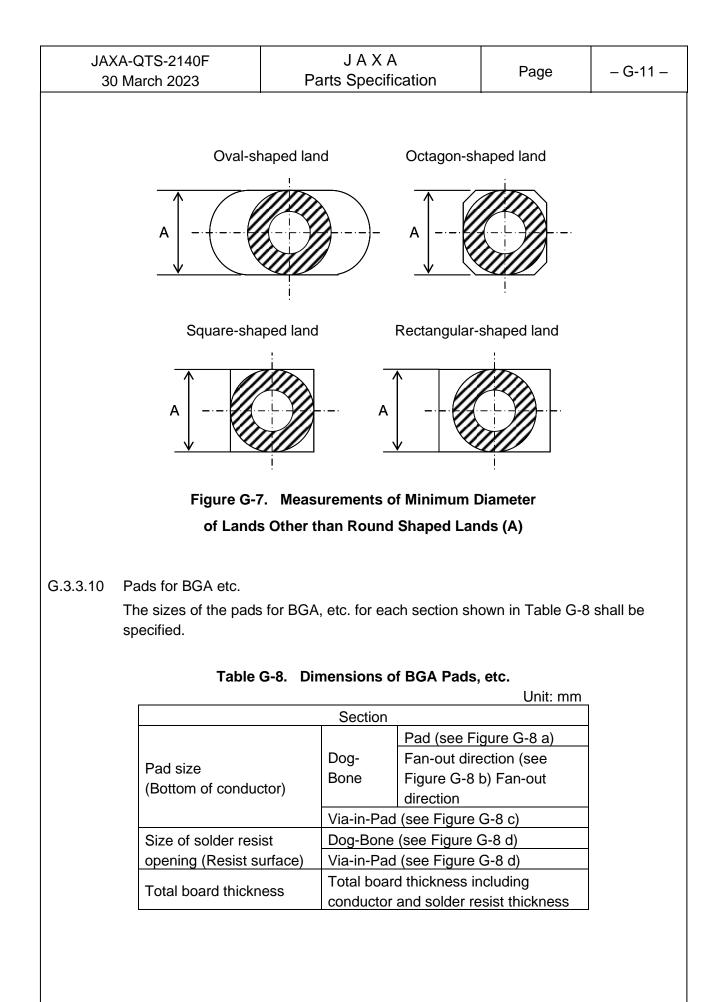
Table G-7. Land Diameter

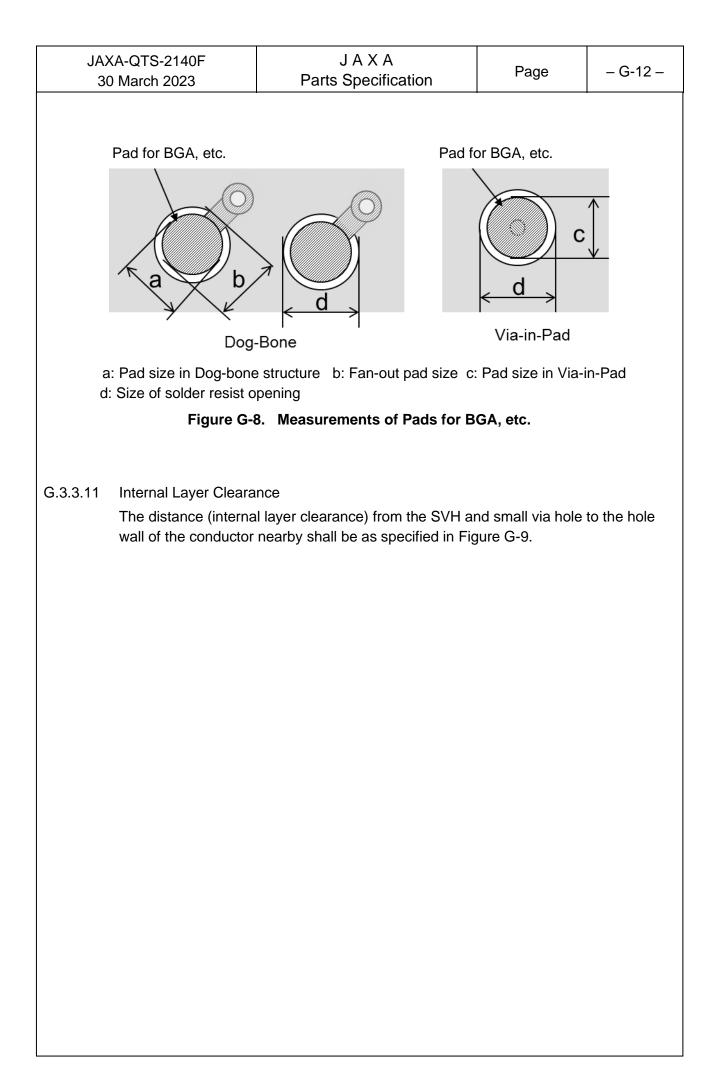
Unit: mm

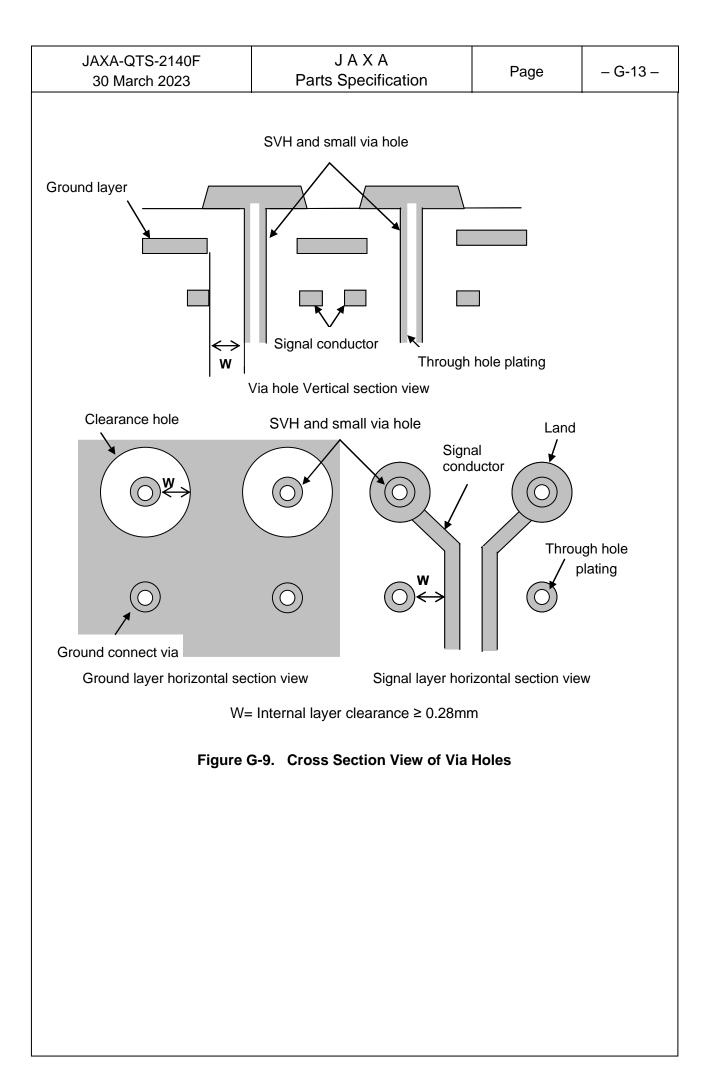
	Offit: Hilli
Hole	Minimum land diameter(1)
SVH and small via holes	Drill diameter + 0.25
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

Notes:

(¹) The minimum diameter of lands other than round shaped lands shall be the measure of the length "A" shown in Table G-7.







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 G.3.3.12 Surface Finish Plating The thickness of the surface finish plating and solder coating specified in the manufacturing drawing shall be in accordance with Table G-9. The electrolytic Nickel plating shall be applied as an undercoat of electrolytic gold plating, and shall not be used for the surface finish. If more strict requirements than the ones specified in Table G-9 are necessary, consult with manufacturer and specify on the manufacturing drawing. 				
Table G-9. Thickness of Surface Finish Plating Unit: µm				
	Plating material	Surface plating thic		
	Electrolytic gold	1.3 to 4.0		

Electrolytic nickel	5 as a minimum		
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (paragraph G.3.10.2).		

G.3.3.13 Solder Resist

The solder resist application shall be specified except for the land, pads (incl. Via-in-Pad), and the small via holes without resin filling.

The lands of small via hole and SVH in the dog-bone structure shall be coated with solder resist.

Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.

The minimum distance from the edge of the board to the solder resist shall be 0.3mm.

G.3.3.14 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph G.3.11.1.2) and within -65 to +125°C.

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- G.3.4 Externals, Dimensions, Marking and Others
- G.3.4.1 Externals of Conductor, Base Material and Solder Resist

G.3.4.1.1 Conductor

a) Conductive pattern

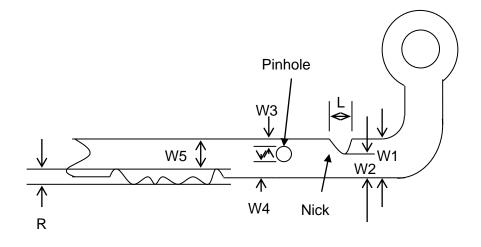
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor

The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the insulation board shall not reduce the conductor width to less than 80 % of the minimum finished conductor width. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall not be more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall meet the conductor width tolerance (see Figure G-10).

The tolerances of conductor width and conductor spacing shall be as specified in Table G-10.

The nicks and pinholes on the ground surface and power supply surface shall not exceed 1.0mm in the maximum length and 4 pieces per 625cm² in number.



- $\label{eq:W1} \begin{array}{l} W1 \geq (Minimum \mbox{ finished conductor width}) \\ W2 \geq 0.80 \times (Minimum \mbox{ finished conductor width}) \\ W4 = W44 + 0.00 \mbox{ bits} \mbox{ finished conductor width} \end{array}$
- W3 + W4 \ge 0.80 ×Minimum finished conductor width)
- W5 + R \geq Conductor width tolerance \geq W5-R

L = Length of defect

Figure G-10. Passing Criteria for Conductor Defects

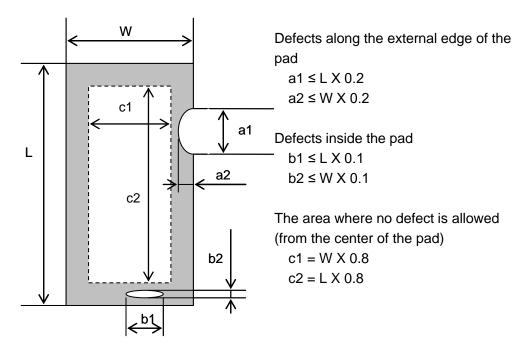
Table G-10.	Tolerance of Conductor Width and Conductor Spacing
-------------	--

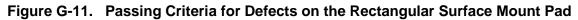
		Unit: mm
	Dimension	Tolerance
	0.08 to less than 0.13	+0.05
Conductor		-0.03
Conductor	0.13 to less than 0.20	±0.05
width	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
	Less than 0.10	0.05 as a minimum
Conductor	0.10 to less than 0.14	0.06 as a minimum
Conductor	0.14 and more	0.10 as a minimum
spacing	The positive side tolerance is not specified for all design	
	value.	

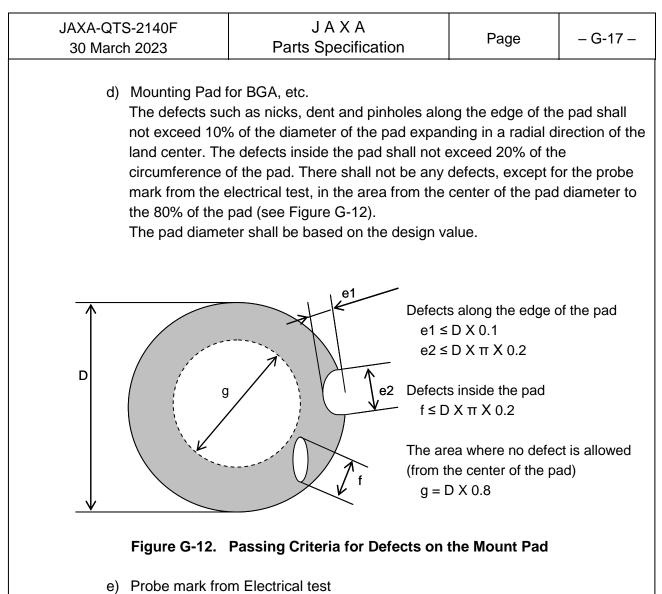
c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure G-11).

The pad length and width shall be based on the design value.







The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

- f) Dielectric layer between conductor layers
 The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.
- g) Solder coating The solder coating shall be free from pinholes or pits, and completely cover conductive patterns.
- h) Electrolytic nickel and electrolytic gold plating

The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on the conductor side is permitted.

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 G.3.4.1.2 Base Materials a) Edges of printed wiring board Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board. Crazing along the edges of printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller. b) Surface of printed wiring boards The surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall not be permitted. 				
G.3.4.1.3	 S.3.4.1.3 Solder Resist a) The cured solder resist shall be free from tackiness, blistering and delamination. b) Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. c) Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. d) The solder resist shall not encroach onto lands for mounting parts. e) The application range and misalignment of solder resist and conductive patterns shall meet the provisions of manufacturing drawings. f) Unless otherwise specified on the manufacturing drawings, adjacent conductor shall not be exposed in the solder resist shall completely cover the land of small 			
G.3.4.2	manufacturing drawing	ach part of the printed wiring board ngs. Unless otherwise specified, d ne requirements specified in Table	imensional tolera	

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 Table G-11.
 Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance	
Outline dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100	
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.	
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.	

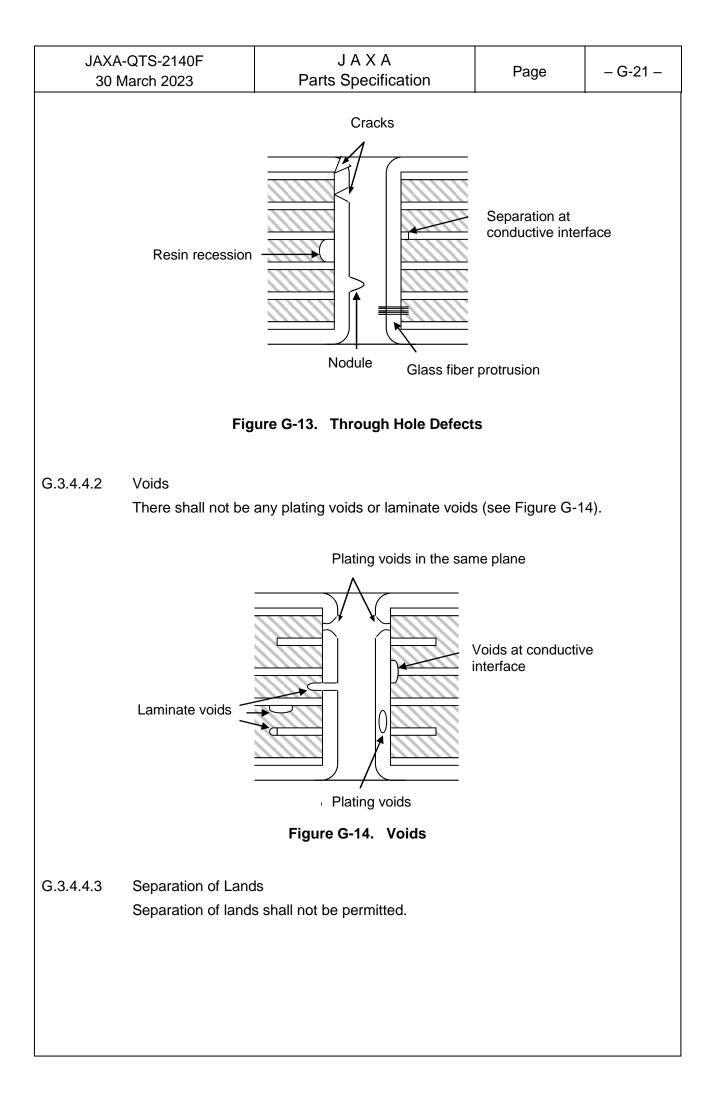
G.3.4.2.1 Dimensions of BGA Pads, etc.

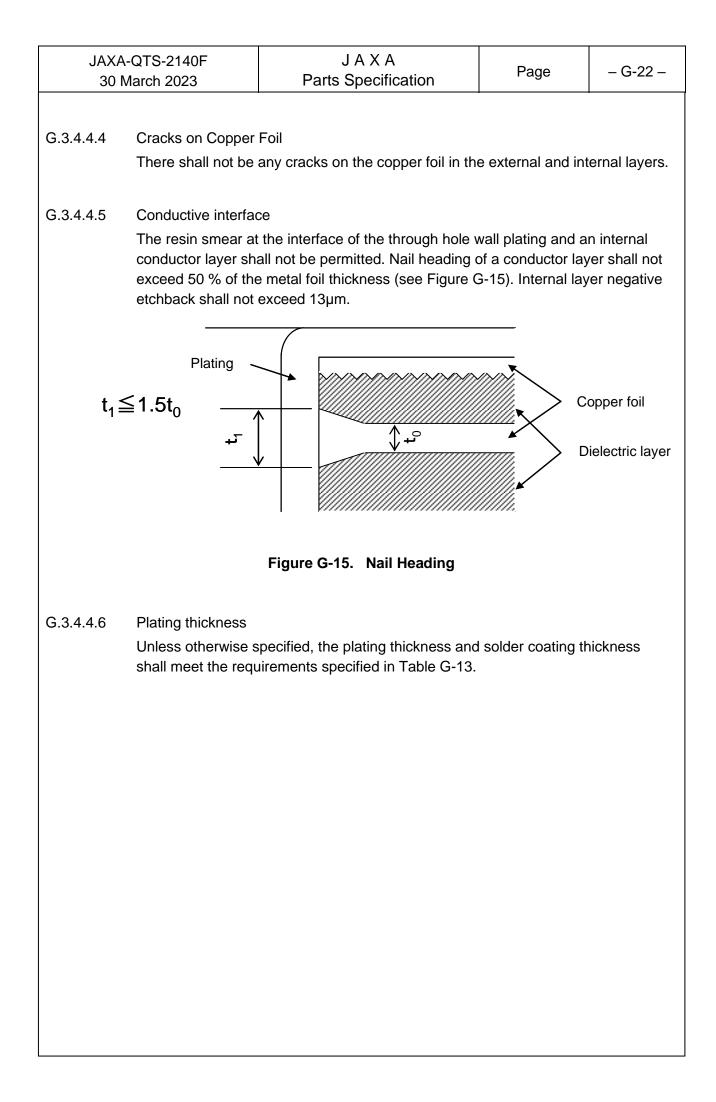
Unless otherwise specified, the dimension tolerance for BGA pads, etc. shall be in accordance with the requirements specified in Table G-12.

			Unit. (mm)
	Item		Tolerance
		Pad (Figure G-8 a)	±0.05
Pad size (conductor bottom size)	Dog-Bone	Fan-out direction (Figure G-8 b)	±0.075
	Via-in-Pad (Figure G-8 c)		±0.05
Solder resist opening	Dog-Bone (Figure G-8 d)		±0.05
diameter (resist surface)	Via-in-Pad (Figure G-8 d)		±0.05
Accurate alignment	Length of row of BGA pads		±0.05
Pad thickness (conductor thickness)		±0.01	
Total board thickness (incl. solder resist)		±8 %	
Co-planarity (flatness): Normal state		0.05mm or less for diagonal diameter of BGA pads	

Table G-12. Dimensions for BGA Pads, etc.

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G.3.4.3	 The marking shall be produced with the marking inks specified in paragraph G.3.2.4, by copper etching or laser marking. The marking shall remain legible and shall not adversely affect any function, performance or reliability of printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag. a) Part number b) Year and month manufactured c) Manufacturer's name or its identification code d) Product serial number⁽¹⁾ or lot number 				
G.3.4.3.1	 process can be traced. 4.3.1 Marking on Split Board If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent. 				
G.3.4.4	Structural Integrity				
G.3.4.4.1					

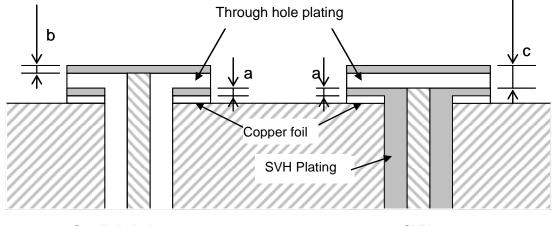




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Table G-13. Thickness of Plating and Solder Coating

	-		Unit: µm	
Туре	Surface and through hole wall thickness			
Electroless copper	Thic	kness necessary and sufficient fo	or electrolytic copper	
plating		plating in the subsequent	process	
		Via hole for part mount	25 as a minimum	
		Small via hole	25 as a minimum	
	SVH		30 as a minimum	
Electrolytic copper	SVH p	lating on land (Figure G-16 a)	5 as a minimum	
plating		Small via hole	As specified in detail	
	Сар	(Figure G-16 b)	specification	
	plating	SVH	As specified in detail	
		(Figure G-16 c)	specification	
Electrolytic gold plating	1.3 to 4.0			
Electrolytic nickel plating	5 as a minimum			
Ostalan as at in a	Thickness is not specified. However, the requirements of			
Solder coating	So	Solderability (paragraph G.3.10.2) shall be satisfied.		



Small via hole

SVH

a: SVH plating thickness on lands

b: Cap plating thickness on small via hole

c: Cap plating on SVH

Figure G-16. Cap Plating Thickness

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G.3.4.4.7	Laminate Cracks Cracks on laminate	shall not be permitted.		
G.3.4.4.8	Delamination and Blister Delamination and blister shall not be permitted.			
G.3.4.4.9	Layer-to-layer Registraion The layer-to-layer registration error shall not exceed 0.15mm.			
G.3.4.4.10	Annular Ring The minimum annu requirements spec	lar ring of internal and external lag	yer shall meet the)

		Unit: mm
Through hole type	Layer	Annular ring
Through hole	External	0.05
	Internal	0.025
Non-through hole	External	0.38

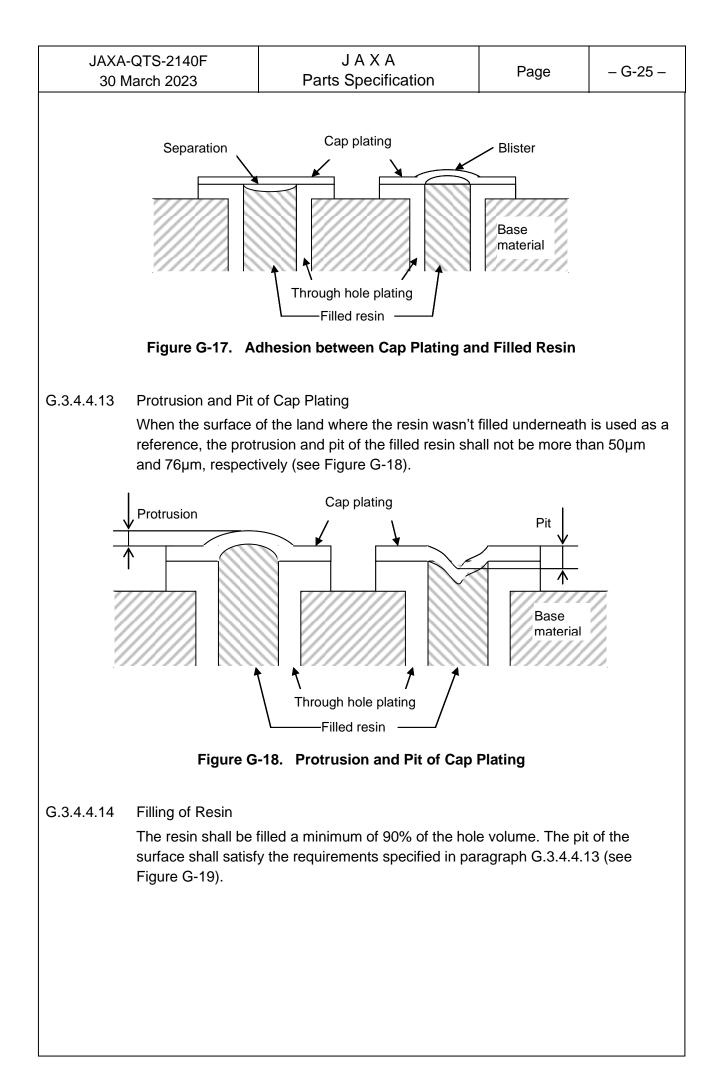
Table G-14. Annular Ring

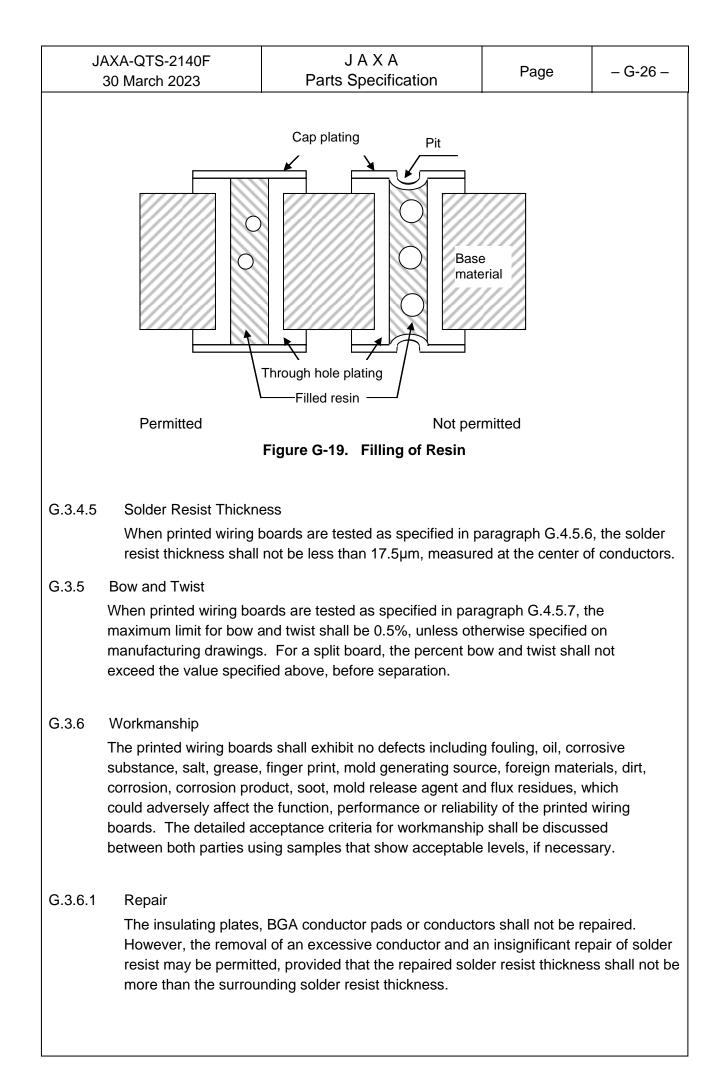
G.3.4.4.11 Dielectric Layer Thickness

The dielectric layer between conductor layers of a multilayer printed wiring board shall not be less than 0.08mm in thickness.

G.3.4.4.12 Adhesion between Cap Plating and Filled Resin

When the cap plating is used as BGA pad, the gap between cap plating and filled resin shall be less than 5µm. When the cap plating is not used as BGA pad, the requirements specified in paragraph G.3.4.4.13 shall be satisfied (see Figure G-17).





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G.3.7	 G.3.7 Plating Adhesion and Overhang When printed wiring boards are tested as specified in paragraph G.4.5.9, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges. 					
G.3.8	Cleanliness When printed wiring boards are tested as specified in paragraph G.4.5.10, the resistivity of the solvent extract shall not be less than $2x10^6\Omega$ cm.					
G.3.9	Electrical Performance Printed wiring board sha	Ill meet the following electrical req	uirements.			
G.3.9.1	Dielectric Withstanding Voltage When tested as specified in paragraph G.4.5.11.1, printed wiring boards shall not exhibit insulation breakdown, flashover or sparkover.					
G.3.9.2	Circuitry When tested as specified in paragraph G.4.5.11.2, printed wiring boards shall not exhibit open circuit or short-circuiting between circuit patterns.					
G.3.9.3	Connection Resistance When printed wiring boards are tested as specified in paragraph G.4.5.11.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.					
	$Ri = 2\rho \frac{I}{W \cdot t} (m\Omega)$					
	p: Volume resistivity a l: Distance between la W: Conductor width (t: Conductor thicknes	mm)	orms the conducto	or (mΩ∙mm)		
G.3.10	Mechanical Performanc Printed wiring boards sh	e all meet the following mechanical	requirements.			

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	 G.3.10.1 Terminal Pull Strength When tested as specified in paragraph G.4.5.12.1, printed wiring boards shall meet the following requirements. This provision shall not apply to SVH or small via holes. a) Bond strength The land shall withstand a minimum of 89.2N pull or 1380N/cm², whichever is smaller. 					
	When printed wi G.4.5.4.1, there c) Microsection of t When printed wi	When printed wiring boards are microsectioned and inspected in accordance with paragraph G.4.5.5, there shall be no cracks, blistering, measling or				
	 Solderability When tested as specified in paragraph G.4.5.12.2, printed wiring boards shall meet the following requirements. a) Through hole solderability The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to SVH or small via holes. b) Surface solderability A minimum of 95 % of the surface conductor area shall be covered uniformly with fresh solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area. 					
	nvironmental Performative structure inted wiring boards sh	ance nall meet the following environmen	tal requirements.			
G.3.11.1	Thermal Shock					
 G.3.11.1.1 Thermal Shock (I) (applicable to qualification test) When printed wiring boards are tested as specified in paragraph G.4.5.13.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph G.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. 						
 circuits before and after the test shall be less than 10%. G.3.11.1.2 Thermal Shock (II) (applicable to quality conformance inspection) When printed wiring boards are tested as specified in paragraph G.4.5.13.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph G.3.9 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. 			ation. aph G.3.9.2			

[1			
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G.3.11.2	Humidity and Insulation Resistance When printed wiring boards are tested as specified in paragraph G.4.5.13.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall not be less than $500M\Omega$.					
G.3.11.3	3 Hot Oil Resistance When printed wiring boards are tested as specified in paragraph G.4.5.13.3, the change in connection resistance between circuits before and after the test shall be less than 10%.					
G.3.11.4	 the following requirem a) Externals There shall be not blistering or delated b) Structural Integril In the vertical mit satisfied. 1) Through hole There shall be 2) Laminate voi When the conthe minimum spacing shaled 3) Lifting of land Lifting of land Lifting of land through hole 5) Internal layer There shall be through hole 6) Laminate Cracks other between adjated 7) Delamination There shall be through hole through hole 8) Adhesion of There shall be through through hole 8) Adhesion of The interface 	o measling, cracks, separation of mination. ty crosection of through holes, the for the no corner cracks or barrel crack d nductor spacing on the same plan conductor spacing specified in the not exceed 76µm. ds ds after thermal stress test shall be opper foil be no cracks which penetrate throu- connection be no separation between copper for plating. acks mal stress test, the laminate crack s or on the lands shall not exceed than the ones on the land area sha acent conductors fall below the mi	plating and condu- ollowing requirem as. The or between lay e manufacturing of e permitted. The copper for foil of internal layer ks between the la 80µm, and the la all not cause the nimum conductor	uctors, ents shall be ers satisfies drawings, the il. er and unds of a uminate spacing spacing.		

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G.3.11.5 Radiation Hardness

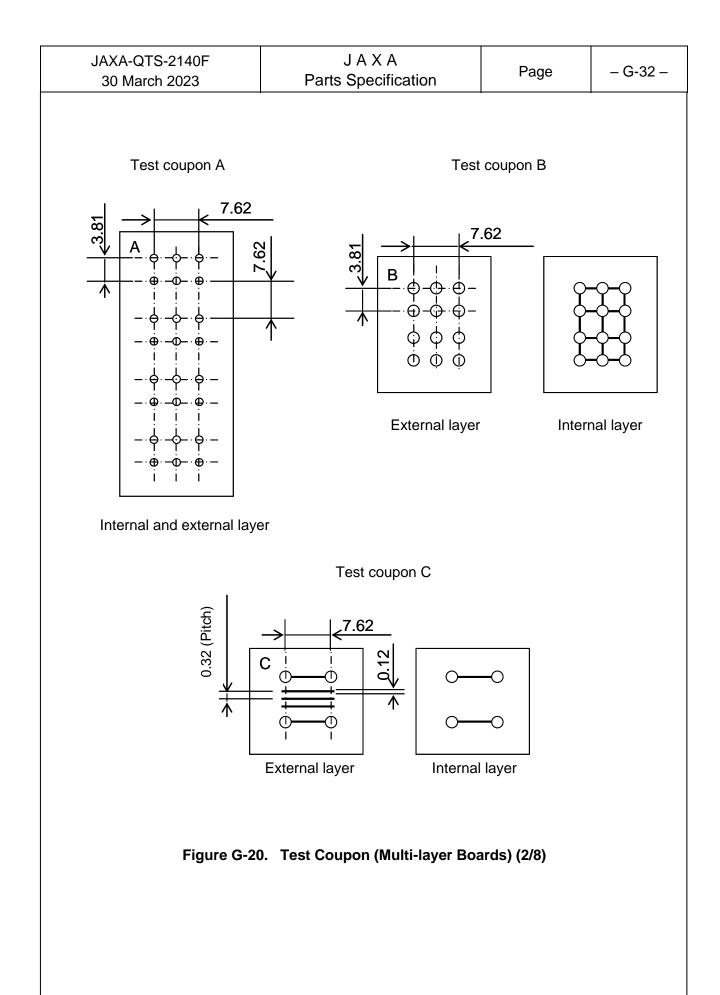
When printed wiring boards are tested as specified in paragraph G.4.5.13.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall not be less than $500M\Omega$. After the test, the requirements specified in paragraph G.3.9.1 shall be satisfied.

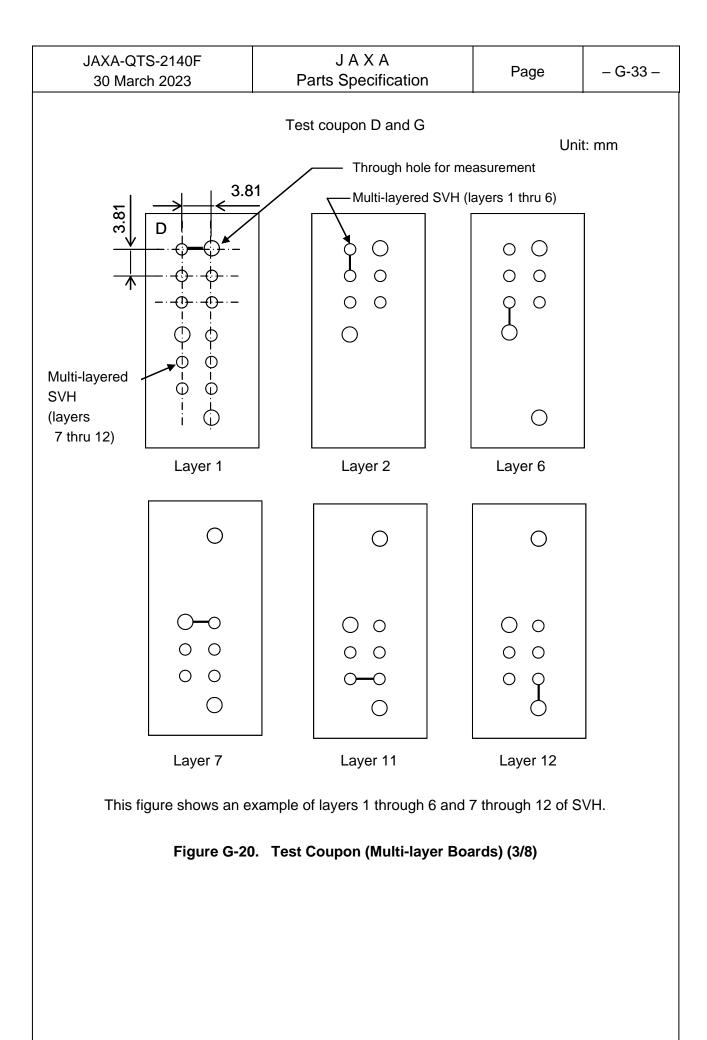
G.4. Quality Assurance Provisions

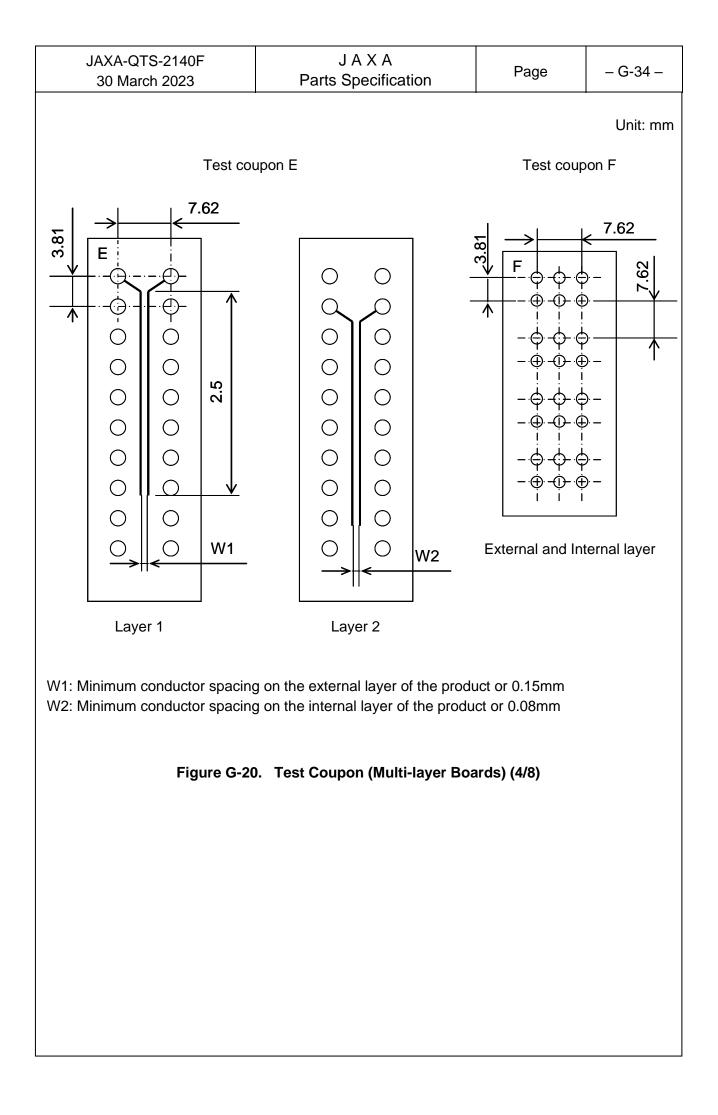
G.4.1 Test Pattern

The test pattern provided for qualification test and quality conformance inspection shall be in accordance with Figure G-20. The test pattern shall have the same structure as the product produced from the identical work board. A set of the test pattern shall be assigned for each printed wiring board.

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	Arrangement of test pattern						
Unit: mm	١	lotes					
< 15.24 →	(1) Unless otherwise specified, the conductor width shall be						
Αοοο	F ₀₀₀	through hole (incl. small via hole printed wiring board, and the la	e) for the corresp	onding			
000		minimum land diameter of the the small via holes shall be filled wi	hrough holes. W	hen applied,			
000	000	tolerance is not specified. 3) For test coupons B, C, E and F					
0 0 0 0 0 0		1.8±0.13mm, and the land shap shape of the products. All hole	e shall be the typ	oical land			
0 0 0 0 0 0		diameter shall be 0.8mm. The h be the tolerance for the corresp	nole diameter tole onding printed w	erance shall iring board.			
В	G (The patterns of test coupons D number of layers and via hole s 	tructure. Each co	oupon shall			
		be produced so as to form the s via hole structure as those of th to have a circuit continuity throu.	e corresponding Igh all layers by v	product, and via holes.			
C	J	The hole and land diameter sha for each SVH and small via hole	e of the correspo	nding			
		 products, and the land shape shall be the typical land shape of the products. On both ends of the printed wiring board, through holes shall be formed to measure the resistance, the diameter of the land and hole shall be φ1.8mm and φ0.8mm, 					
	К ₀₀₀ (respectively. The hole diameter 5) Solder resist shall apply to the t when solder resist is required for	tolerance is not est coupons E, H	specified. I, and J, only			
E		clearance spacing for the solde diameter for the corresponding hole diameter for the product is	r resist shall be the printed wiring bo	ne clearance ard. If the			
		shall be equal to the land diame (6) Test coupons K and L shall be corresponding products have S	eter + 0.2mm. prepared only wh	en the			
	0 0 0 0 0 0	depending on the number of lay The land shall be formed only o connected by SVH.	vers and via hole	structure.			
	H (Test coupons D, E and G are d conductors, depending on the r	umber and const	truction of			
		layers. The conductors shall be accordance with this figure.					
		 8) The arrangement of test coupor example; a different arrangeme 9) The symbols of test coupons (A 	nt is also accepta	able.			
	· · · · · · · · · · · · · · · · · · ·	used for identification and not for The marking method is not specific	or the object of in	•			
M1	M2 (Only when the BGA pads, e coupon M1 (Dog-bone structure structure) in accordance with th test coupons M1 and M2 is sho 	e) or test coupon e pad structure. /	M2 (VIP A example of			
		specification for the more detail					
Figure G-20. Test Coupon (1/8)							







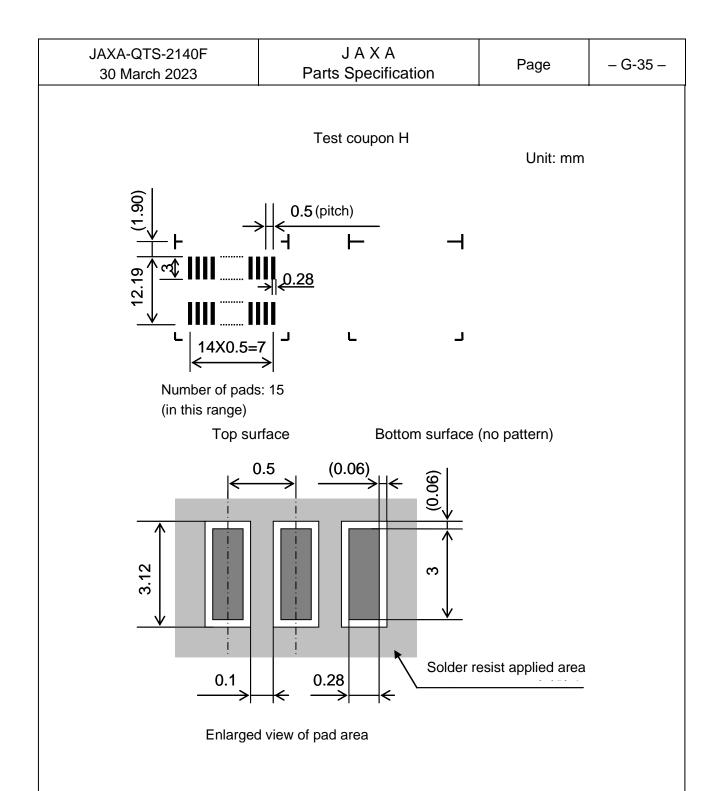
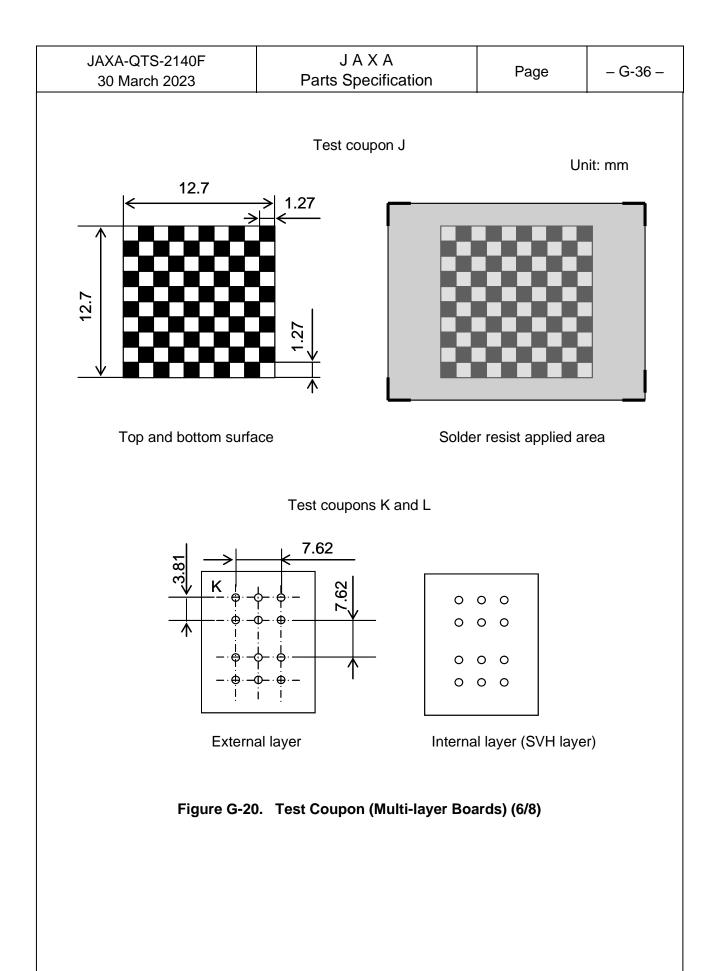


Figure G-20. Test Coupon (Multi-layer Boards) (5/8)



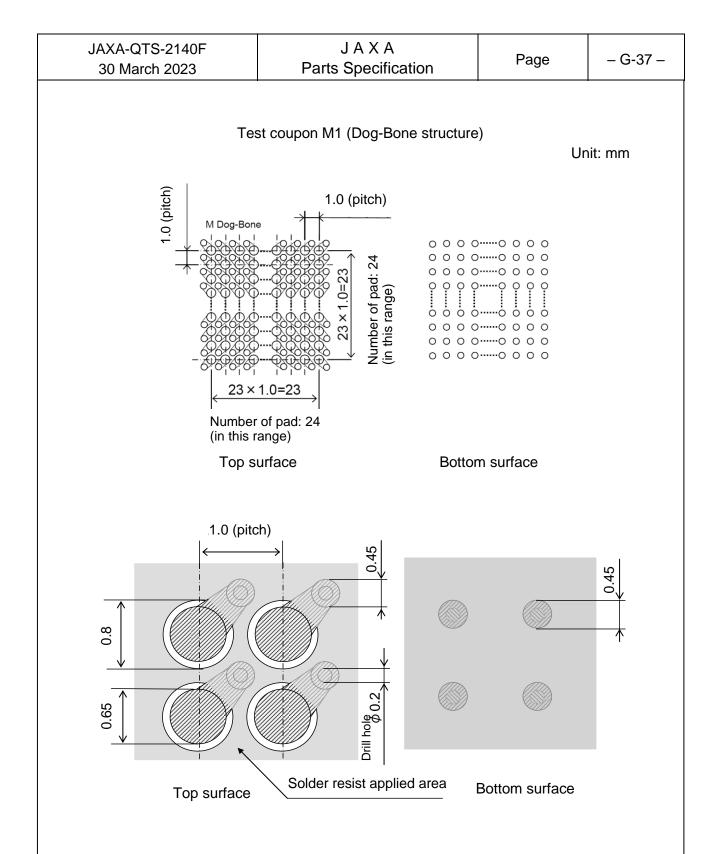
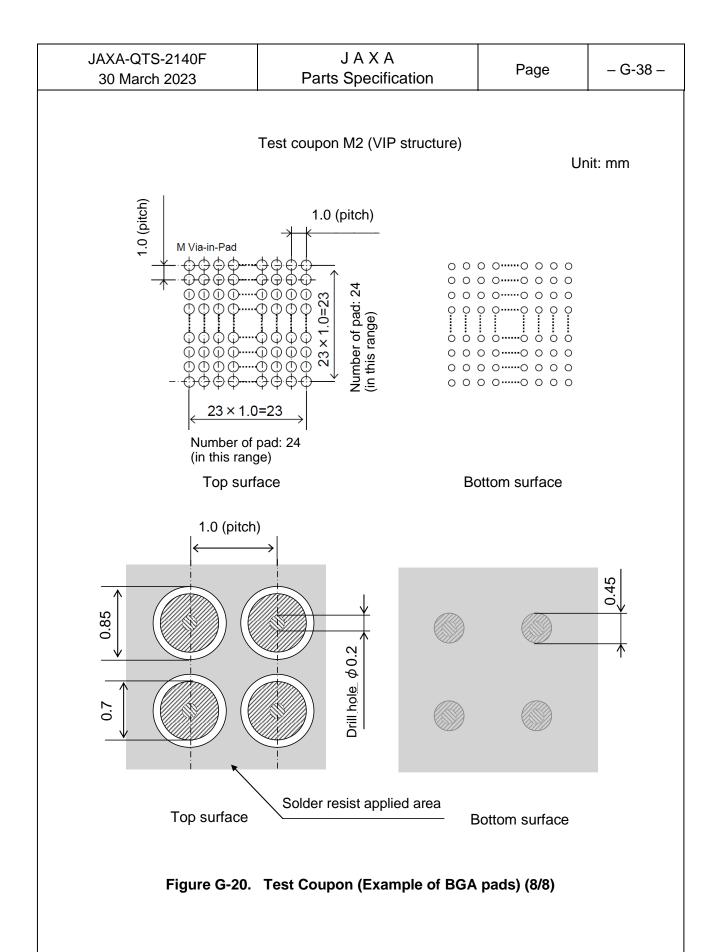


Figure G-20. Test Coupon (Example of BGA pads) (7/8)



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G.4.2 In-Process Inspection

The in-process inspection specified in Table G-15 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs G.3.4.1 (Externals of Conductor, Base Material and Solder Resist), G.3.4.2 (Dimensions), G.3.4.3 (Marking), G.3.8 (Cleanliness), and G.3.4.2.1 (Dimensions of BGA Pads, etc)

No.	Item	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	G.3.4.1 G.3.4.2 G.3.4.3	G.4.5.4.1 G.4.5.4.2 G.4.5.4.3	All	After forming internal circuit and before pre- treating the laminate layer
2	Conductor of external layer Base material of external layer	G.3.4.1.1 G.3.4.1.2	G.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	G.3.8	G.4.5.10	Sampling(1)	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	G.3.4.2.1	G.4.5.4.2	All	After forming solder resist and before solder coating

Note (¹) Sampling inspection shall be performed based on 1.0% of the acceptable quality level (AQL) in "Normal Inspection Level II" specified in JIS Z 9015-1. The lot shall be processed in the same circuit forming process on the same day the sampling inspection was performed and can be subjected to solder resist application.

G.4.3 Qualification Test

G.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole and number of layers sufficient to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation.

G.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table G-16. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table G-16.

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		Table C	<u>3-16. Quali</u>	fication Te	st		
		Test			Pass/fail Criteria		ia
Group	Order	Test item	Requirement paragraph	Test method paragraph	Sample Production printed wiring boards	Test coupon (1) (2)	Quantity of allowable defects
I	1	Externals of conductor, base materials, and solder resist Externals, dimensions,	G.3.4.1	G.4.5.4.1	No. 1 to No. 6	A, B, C, D, E, F,	
		Dimensions Marking	G.3.4.2 G.3.4.3	G.4.5.4.2 G.4.5.4.3		G, H, K, L and M	
	2	Workmanship ⁽³⁾	G.3.6	G.4.5.8			
II	1	Plating adhesion and overhang	G.3.7	G.4.5.9	No. 1 to No. 6	С	
	2	Bow and twist	G.3.5	G.4.5.7		N/A	
Ш	1	Structural integrity	G.3.4.4	G.4.5.5		A, F, K and M F	
111	2	Terminal pull strength	G.3.10.1	G.4.5.12.1	NO. 1		
	3	Solder resist thickness	G.3.4.5	G.4.5.6		J	
	1	Connection resistance	G.3.9.3	G.4.5.11.3		D	0
IV	2	Hot oil resistance	G.3.11.3	G.4.5.13.3	No. 2		Ŭ
	3	Connection resistance	G.3.9.3	G.4.5.11.3			
	1	Circuitry	G.3.9.2	G.4.5.11.2			
	2	Connection resistance	G.3.9.3	G.4.5.11.3		E and	
V	3	Thermal shock (I)	G.3.11.1.1	G.4.5.13.1a)	No. 3	G ⁽³⁾	
	4	Circuitry	G.3.9.2	G.4.5.11.2		0.7	
	5	Connection resistance	G.3.9.3	G.4.5.11.3			
VI	1	Humidity and insulation resistance	G.3.11.2	G.4.5.13.2	No. 4	с	
2	2	Dielectric withstanding voltage	G.3.9.1	G.4.5.11.1	NO. 4	E	
VII	1	Thermal stress	G.3.11.4	G.4.5.13.4		A, B, L and M	
VII	2	Solderability	G.3.10.2	G.4.5.12.2	No. 5 B and H ⁽⁴⁾]
VIII	1	Radiation hardness	G.3.11.5	G.4.5.13.5	No.6	N/A	
-	-	Materials	G.3.2	G.4.5.2	N/A		N/A

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

⁽³⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽⁴⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

 G.4.4 Quality Conformance Inspection G.4.4.1 Quality Conformance Inspection (Group A) G.4.4.1.1 Sample The quality conformance inspection shall be performed with the test courd the test coupons and sample product shall be manufactured simultaneous Even though any part of a split board fails an inspection in the manufacture process and is marked with rejection, the board may be included in an introduction of the test courd of parts of the same patterns or parts of different patterns and test order of Group A inspection shall be in accordance w G-17. The inspections within each group shall be performed in the order 	– G-41 –	Page	J A X A Parts Specification		JAXA-QTS-2140F 30 March 2023		
 G.4.4.1.1 Sample The quality conformance inspection shall be performed with the test could The test coupons and sample product shall be manufactured simultaneous Even though any part of a split board fails an inspection in the manufacture process and is marked with rejection, the board may be included in an inlot. However, in order not to adversely affect the inspection result, the process and with rejection shall not be used as a specimen. A "split board" moard constructed of parts of the same patterns or parts of different patters. G.4.4.1.2 Inspection Items and Sample Size Test items and test order of Group A inspection shall be in accordance w G-17. The inspections within each group shall be performed in the order 	G.4.4 Quality Conformance Inspection						
 The quality conformance inspection shall be performed with the test courting the test coupons and sample product shall be manufactured simultaneous Even though any part of a split board fails an inspection in the manufacture process and is marked with rejection, the board may be included in an inflot. However, in order not to adversely affect the inspection result, the process and with rejection shall not be used as a specimen. A "split board" moard constructed of parts of the same patterns or parts of different patterns of the same patterns or parts of different patterns and test order of Group A inspection shall be in accordance w G-17. The inspections within each group shall be performed in the order 			Inspection (Group A)	ance Ins	Quality Conformand	G.4.4.1	
 The test coupons and sample product shall be manufactured simultaneo. Even though any part of a split board fails an inspection in the manufacture process and is marked with rejection, the board may be included in an inlot. However, in order not to adversely affect the inspection result, the process and with rejection shall not be used as a specimen. A "split board" moard constructed of parts of the same patterns or parts of different patterns G.4.4.1.2 Inspection Items and Sample Size Test items and test order of Group A inspection shall be in accordance with order. The inspections within each group shall be performed in the order 					Sample	G.4.4.1.1	
Test items and test order of Group A inspection shall be in accordance v G-17. The inspections within each group shall be performed in the order	turing inspection part means a	on in the manufac be included in an i pection result, the p n. A "split board"	art of a split board fails an inspect ked with rejection, the board may der not to adversely affect the ins on shall not be used as a specim	any part s marked in order ejection	Even though any process and is m lot. However, in marked with reject		
One test coupon shall be provided for each of Group IV and V test.							

		Inspection			P	ass/fail criteria	a
					Quantity of samples		Quantita
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring boards	Test coupon	Quantity of allowable defects
	1	Design and construction	G.3.3	G.4.5.3	All	N/A	
I	2	Externals of conductor, base materials, and solder resist Externals, dimensions,	G.3.4.1	G.4.5.4.1	All N/A	N/A	
		Dimensions Marking	G.3.4.2 G.3.4.3	G.4.5.4.2 G.4.5.4.3	All	N/A	
	3	Workmanship	G.3.6	G.4.5.8			0
II	1	Bow and twist	G.3.5	G.4.5.7	All	N/A	
III	1	Circuitry	G.3.9.2	G.4.5.11.2	All	N/A	
IV	1	Thermal stress	G.3.11.4	G.4.5.13.4	N/A	A, F, K ⁽¹⁾ and M ⁽²⁾	
V	1	Solderability	G.3.10.2	G.4.5.12.2	N/A	F and H ⁽³⁾	

Table G-17. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the products is provided with SVH.

⁽²⁾ Test coupon M shall be inspected when the products is provided with BGA pads, etc.

⁽³⁾ Test coupons F and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

G.4.4.2 Quality Conformance Inspection (Group B)

G.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection are manufactured and selected from the lot which passed Group A inspection.

G.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table G-18. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

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	-	Inspection			Pass/fail	criteria
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
Ι	1	Plating adhesion and overhang	G.3.7	G.4.5.9	С	
II	1	Terminal pull strength	G.3.10.1	G.4.5.12.1	F	
	2	Connection resistance	G.3.9.3	G.4.5.11.3		
Ш	3	Hot oil resistance	G.3.11.3	G.4.5.13.3	D	
	4	Connection resistance	G.3.9.3	G.4.5.11.3		
	1	Circuitry	G.3.9.2	G.4.5.11.2		
	2	Connection resistance	G.3.9.3	G.4.5.11.3		0
IV	3	Thermal shock (II)	G.3.11.1.2	G.4.5.13.1b)	E and G ⁽¹⁾	
	4	Circuitry	G.3.9.2	G.4.5.11.2		
	5	Connection resistance	G.3.9.3	G.4.5.11.3		
V	1	Humidity and insulation resistance	G.3.11.2	G.4.5.13.2	E	
v	2	Dielectric withstanding voltage	G.3.9.1	G.4.5.11.1		

Table G-18. Quality Conformance Inspection (Group B)

Note: ⁽¹⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

G.4.5 Methods for Test and Inspection

G.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

G.4.5.2 Materials

The copper clad laminates and prepreg shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.

G.4.5.3 Design and Construction

The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.

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G.4.5.4 Externals, Dimensions, Marking and Others					
G.4.5.4.1	 .4.5.4.1 Externals of Conductor, Base Material and Solder Resist External inspection shall be performed with 4X to 10X magnifier. a) Conductors For conductive pattern inspection, Automatic Optical Inspection machine (AOI) can be used. Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy. b) Base Materials Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy. c) Solder Resist Pass or fail shall be determined by using 10X magnifier. 				
G.4.5.4.2	 accuracy. a) Dimensions of The dimension measured as for the largest area are the same s detailed measured 1) Dimension of Each section measured by 2) Position acc The direction measured w measuring in 3) Height from Each section measured by 4) Total board for For the total 	be measured by using a measuring BGA pads, etc. Is of printed wiring boards with BG/ pollows. For the board with multiple a shall be selected for measureme ize, any one of the pad shall be se urement sections shall be shown in f BGA pads and solder resist oper of grid corner (outer) of the center y an optical measuring instrument. uracy for BGA pads, etc. Ins of X and Y axes of circumference ith a 2-dimension end-measuring r instrument sufficient enough for me the base material for BGA pads, e of grid corner (outer) and the cent y the focal depth method using a methickness for BGA pads, etc. board thickness including solder co on shall be measured by using a methickness for BGA pads, etc.	A pads, etc. shall BGA pads, the B nt. If all the BGA elected for measu a Figure G-21. aning diameter er area (inner) sha ce for BGA pads s machine or an eq asurement. tc. (pad thickness ter area (inner) s metallograph.	be GA pad with pad areas irement. The all be shall be uivalent s) hall be	

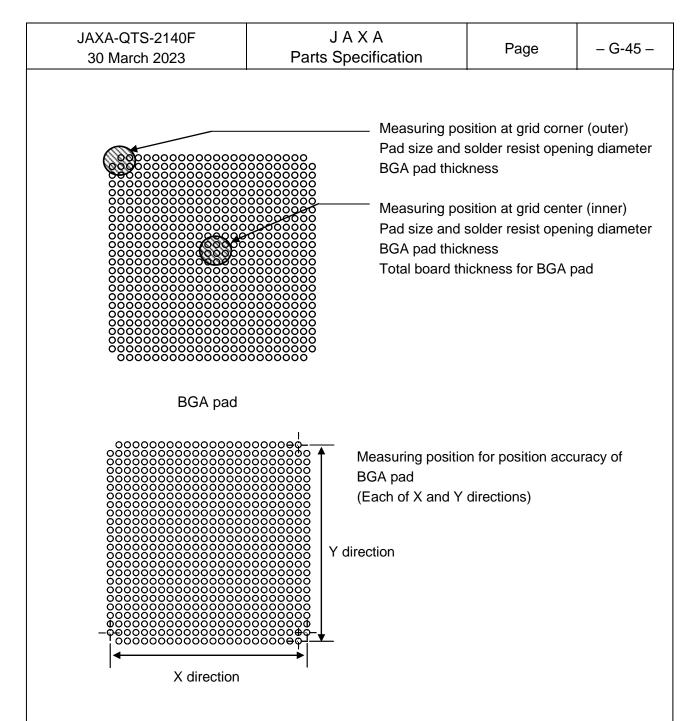
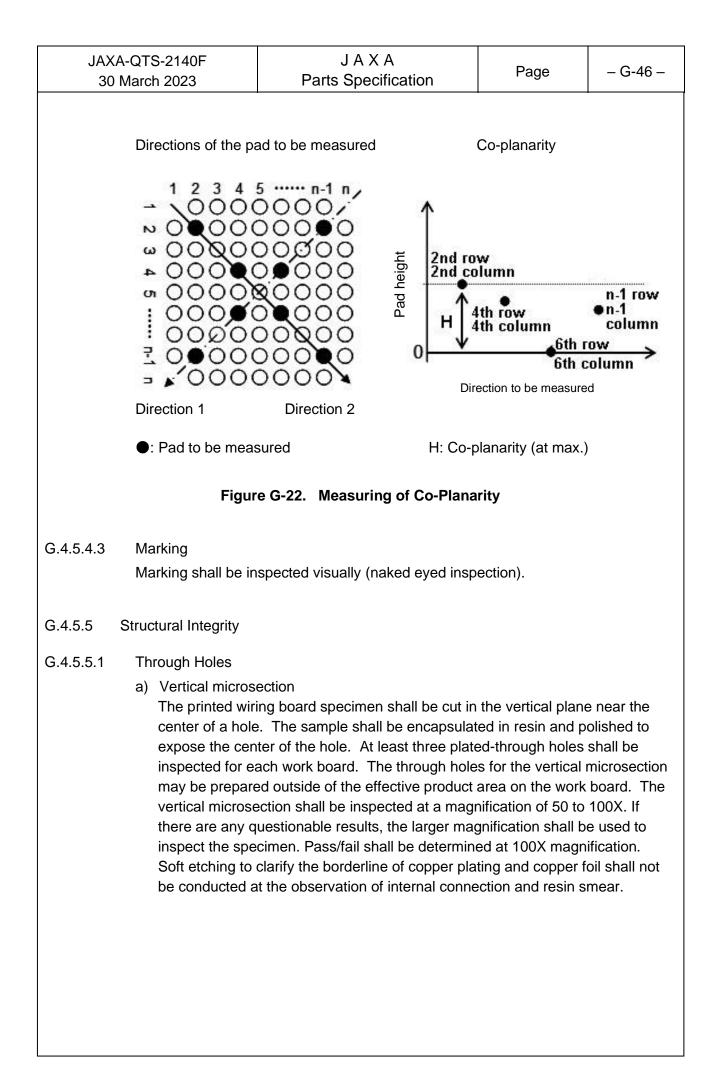


Figure G-21. Measuring Points for BGA Pad

5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

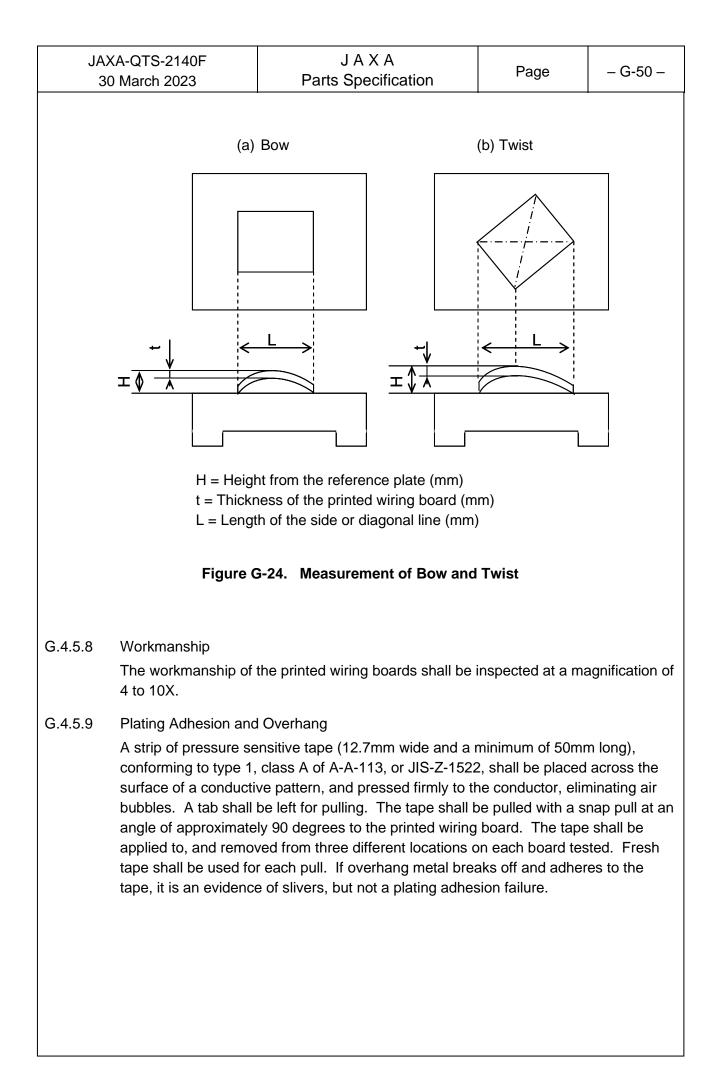
Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure G-22)



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	 b) Horizontal micro Multilayer board polished. A cor the conductor la horizontal direc are any questio the specimen. F 	·	the parallel directi hole (internal con hification of 50 to ation shall be use 00X magnification	ion to expose nection in 100X. If there d to inspect
G.4.5.5.2	void at a magnifica	repared in paragraph G.4.5.5.1 a tion of 50 to 100X. If there are any n shall be used to inspect the spe < magnification.	y questionable rea	sults, the
G.4.5.5.3	paragraph G.4.5.5. questionable result	bected for any lifting by using the 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are a e used to inspect	ny
G.4.5.5.4	paragraph G.4.5.5. questionable result	Foil e inspected for any crack by using 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are a e used to inspect	ny
G.4.5.5.5	paragraphs G.4.5.5 questionable result	nection ection shall be inspected by using 5.1 a) and b) at a magnification of s, the larger magnification shall b I shall be determined at 100X ma	50 to 100X. If the used to inspect	ere are any
G.4.5.5.6	paragraph G.4.5.5. thickness shall be the hole. If any of the not	hall be inspected by using the mid 1 a) at a magnification of 200X as he average value of three measu neasured value is significantly diff be used for calculating the averages shall be measured at the thinn	s a minimum. Plat rements for a plat erent from the oth ge.	ing ted through ner values,
G.4.5.5.7	paragraph G.4.5.5. questionable result	nspected for any crack by using t 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are a e used to inspect	ny

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G.4.5.5.8	delamination and b questionable result	Blister prepared in paragraph G.4.5.5.1 a plister at a magnification of 50 to 1 s, the larger magnification shall b I shall be determined at 100X ma	00X. If there are a used to inspect	any		
G.4.5.5.9	prepared in paragra misregistration sha board length and th to-layer misregistra board in the direction	stration registration shall be measured by aph G.4.5.5.1 a) at a magnificatio Il be measured around the hole in the vertical direction. The microsed ation shall be prepared by cutting on parallel to the board length for r another one hole as a minimum	n of 25 to 100X. T the direction par ctions for inspection the multi-layer prin at least one hole	The allel to the on of layer- nted wiring and the		
G.4.5.5.10	paragraph G.4.5.5. annular ring on an outer edge of the a annular ring on an	nall be measured by using the mid 1 a) at a magnification of 25 to 10 external layer shall be from the sundar ring on the surface of the internal layer shall be measured layer shall be measured be measured by the land (see Figure 0)	00X. The measur urface of the plate printed wiring boa by the distance fro	ement of the d hole to the rd. The		
	1	Maximum misregistration				
		positio calcula distant rightm	and shall be mease n of the center sha ated. The misregist ce from the center ost land to the cent st land.	II be ration is the of the		
		Measuring annular	ring on an internal	layer		
Measuring annular ring on an external layer						
Figur	Figure G-23. Measurement of Layer-to-Layer Misregistration and Annular Ring					
G.4.5.5.11	•	nickness nickness shall be measured by us .5.1 a) at a magnification of 50 to	-	on prepared		

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0 4 5 5 40				
G.4.5.5.12	Adhesion of cap pla the microsection pr 100X. If there are	lating and Filled Resin ating and filled resin shall be obse epared in paragraph G.4.5.5.1 a) any questionable results, the large imen. Pass/fail shall be determine	at a magnification	n of 50 to hall be used
G.4.5.5.13	•	of Cap Plating of cap plating shall be observed ar red in G.4.5.5.1 a) at a magnificat	•	•
G.4.5.5.14		e observed and measured by using .5.1 a) at a magnification of 25 to	-	n prepared
G.4.5.6	polished to expose th	ess cut vertically near the conductor a e center of the conductor. The sol fication of 200X as a minimum.	•	
G.4.5.7	with its convex side fa the highest point of th The bow and twist sh The percent bow and	ard specimen shall be placed hori: acing upward, and the distance be be printed wiring board shall be me all be calculated as follows. twist shall be calculated by the fo vist = $\frac{H-t}{L} \times 100$ (%)	tween the referent the reference the reference the the term of the reference the term of term	nce plate and



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	-		

G.4.5.10 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 % by volume of isopropyl alcohol and 25 % by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6\Omega$ ·cm. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table G-19 may be used to perform the cleanliness test.

Method	Resistivity (×10 ⁶ Ω·cm)	Equivalent factor	Equivalents of sodium chloride (µg/cm²)
Conductivity bridge	2	1	1.56
Omega Meter ⁽¹⁾	2	1.39	2.2

Table G-19. Equivalent Measuring Method

Note: ⁽¹⁾ Alpha Metals Incorporated, "Omega Meter"

G.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

G.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
- b) Duration: 30 seconds
- c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

G.4.5.11.2 Circuitry

a) Continuity

A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity

b) Circuit shorts

A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

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G.4.5.11.3		ance ween the through hole terminals ent of four-terminal method capa		
	Mechanical Performa			
	The mechanical perfo	ormance tests shall be performed	l as follows.	
G.4.5.12.1	peeled and pulled t at the joining point adherence strength tester shall be inse	be cut with a sharp knife at a mini toward the land, and shall be cut of the conductor and land withou n. Then, a lead wire sufficient in rted in the hole and soldered. Af lering by using a soldering iron sl	off by applying the it degrading the la length for installing ter that, a cycle of	e sharp knife nd g a tensile ^f solder
	b) The lead wire sc) A lead wire shad) The lead wire s	Ill be soldered in to the through h hall be removed from the through Ill be resoldered in to the through hall be removed from the through Ill be resoldered in to the through	h hole (solder rem hole. h hole (solder rem	·
	completely during to resoldering. The sidevelop the tip tem solder iron without wiring board. The completion of e) re room temperature, vertically with the la failure occurs. Bre failure, and a new l	ad shall not be clinched. The lead the solder removal and replaced oldering iron shall be used at 15 operature of 232 to 260°C. The lead bringing its tip into contact with the heating time shall be limited to the soldering, the lead wire shall be i and be pulled at the rate of 50mm and until the pull strength reaches aking off or pulling out the lead wire ead wire shall be soldered and p e following formula.	with a new one wh to 60W and adjust ead wire shall be h he conductor of th he required minimu installed on a tens m per minute forw s the requirement vire shall not be re	nen ted to neated by the e printed um. Upon ile tester at ard and (L) or any garded as a
	$L \geq 1380 \times \frac{\pi \left\{ \left(d_2 \right)^2 - 4 \right\}}{4}$	$\left(\mathbf{d}_{1}\right)^{2}$		
	L = Pull strength (N d ₁ = Hole diameter	•		

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G.4.5.12.2	 Solderability a) Hole solderabil The wetting of s to the inspectio b) Surface soldera After the specin STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. The 25±6mm per se vertical state in 	ity solder shall be inspected using a n n specified in paragraph G.4.5.5.1	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp nto the solder ba econds and raise men shall be kep d. No quick coolir	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of t in the ng shall be
G.4.5.13 I	after the solder Environmental Perfor			
-	The environmental pe	erformance tests shall be performe	ed as follows.	
G.4.5.13.1	 MIL-STD-202. The a) Thermal shock The test shall b temperature sh time for step 2 a heating process as a pre-treatm follows. 1) Heating cond 2) Peak temper 	test shall be performed in accordate following conditions shall apply. (I) (applicable to qualification test) e performed under the test conditi all be -30°C and the number of cy- and 4 shall be within 2 minutes ear is in accordance with JERG-0-043 ent of the printed wiring board. The dition: 200°C min. for 45 seconds re- rature: 230°C min.) on B. However, t cle shall be 1000 ch. Reflow solde shall be performe e heating condition min.	he lowest cycles. The rring of total ed three times
	The test shall	tep 2 and 4 shall be within 2 minut	tion B-3(-65 to +	125℃).

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G.4.5.13.2	cycles, and the during the test.be taken out of evaluated.b) Insulation resis The test shall b	ance s in Test Method 106 of MIL-STD- polarization voltage of 100V±10V Upon completion of step 6 of the the bath and dried immediately by	Y _{DC} shall be applie final cycle, the sp y blowing air at 25 ne test condition E	d to all layers becimen shall 5±5°C and 3, Test
G.4.5.13.3	temperature. After	I be dried at 120±5°C for 2 hours that, the specimen shall be imme cooled to room temperature. This 0 cycles.	ersed in oil or wax	at 260±5°C
G.4.5.13.4	shall be placed on specimen shall the floated in a solder l period of 10 second cooled. After a che inspected for the st accordance with pa probe depth not to Evaluation specime G.3.4.4.12) shall be	I be dried for 2 hours at 121 to 14 a ceramic plate in a desiccator, at n be fluxed in accordance with the path of composition Sn 63±5 % m ds. The specimen shall be placed eck for any defects on the externa tructural integrity using the micros aragraph G.4.5.5.1. Solder temper exceed 50mm from the molten su en of Adhesion of cap plating and e floated in a solder bath for a per and cooling shall be performed th	nd cooled down. e detail specificati aintained at 288± d on a piece of ins l surface, the sam ection prepared in erature shall be m urface of the solde filled resin (parag- iod of 10 seconds	The on and 5°C for a sulator to be ople shall be n easured at a er. yraph
G.4.5.13.5	0.5×10 ⁴ Gy to 1×10 amounts to 1×10 ⁴ G visually to verify that tests of dielectric w performed in accorr respectively. The i	s adiation shall be performed by usi ⁴ Gy per hour to the specimen in o by. After the irradiation, the specin at there is no degradation in any p ithstanding voltage and insulation dance with paragraphs G.4.5.11.1 nsulation resistance shall be mean thstanding voltage test.	pen air, until the t men shall be insp part of the specim resistance shall 1 and G.4.5.13.2 I	otal dose ected en. The be o),

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		APPENDIX H		
		PRINTED WIRING BOARDS		
		FOR HIGH-SPEED SIGNALS		
H.1. General				H-1
•				
H.1.2.1 E	Base Materia	al Code		H-1
H.1.2.2 N	Number of L	ayers		H-1
		s etc		
		nents		
		nents		
-				
		erage		
		aminate, Prepreg and Copper foil		
		ng Materials (Filling Resin)		
		st Ink		
	•			
	-			H-3
-	-	struction		
	-	ng Drawings and Artwork Master (
H.3.3.1 M	Manufacturir H-4 Connector fo	ng Drawings and Artwork Master (or Original Produ	ction Mas H-4
H.3.3.1 M H.3.3.2 (H.3.3.3 I	Manufacturir H-4 Connector fo nterlayer Co	ng Drawings and Artwork Master (or Printed Wiring Boards	or Original Produ	ction Mas H-4 H-4
H.3.3.1 M H.3.3.2 C H.3.3.3 H H.3.3.4 C	Manufacturir H-4 Connector fo nterlayer Co	ng Drawings and Artwork Master (or Original Produ	ction Mas H-4 H-4
H.3.3.1 M H.3.3.2 (H.3.3.3 H H.3.3.4 (H.3.3.5 T	Manufacturir H-4 Connector fo nterlayer Co Connection I Through Hol	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6
H.3.3.1 M H.3.3.2 C H.3.3.3 M H.3.3.4 C H.3.3.5 T H.3.3.6 F	Manufacturir H-4 Connector fo nterlayer Co Connection I Chrough Hol Filling Resin	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6
H.3.3.1 H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole /idth and Thickness	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6 H-6
H.3.3.1 M H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.8 C	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor V Conductor S	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole /idth and Thickness pacing	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6 H-9
H.3.3.1 H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.8 C H.3.3.9 L	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor V Conductor S	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole /idth and Thickness	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6 H-9
H.3.3.1 H.3.3.2 C H.3.3.2 H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W Conductor S Land Diame Pads for BG	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole vidth and Thickness pacing A etc	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6 H-9 H-10 H-11
H.3.3.1 H.3.3.2 C H.3.3.3 H H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F H.3.3.11 H	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W Conductor S Land Diame Pads for BG nternal Laye	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole vidth and Thickness pacing ter A etc	or Original Produ Pads	ction Mas H-4 H-5 H-6 H-6 H-6 H-9 H-10 H-11 H-12
H.3.3.1 H.3.3.2 C H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F H.3.3.11 H H.3.3.12 S	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W Conductor S Land Diame Pads for BG nternal Laye Surface Finis	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole	or Original Produ	ction Mas H-4 H-4 H-5 H-6 H-6 H-10 H-11 H-12 H-14
H.3.3.1 H.3.3.2 C H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F H.3.3.11 H H.3.3.12 S H.3.3.13 S	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W Conductor S Land Diame Pads for BG nternal Laye Surface Finis	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole	or Original Produ	ction Mas H-4 H-4 H-5 H-6 H-6 H-6 H-10 H-11 H-11 H-14 H-14
H.3.3.1 H.3.3.2 C H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F H.3.3.11 H H.3.3.12 S H.3.3.13 S H.3.3.14 F	Manufacturir H-4 Connector fo nterlayer Co Connection I Filling Resin Conductor W Conductor S Land Diamet Pads for BG nternal Laye Surface Finis Solder Resis Plating on O	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole vidth and Thickness pacing ter A etc er Clearance sh Plating st uter Perimieter Sidewall of the Boa	or Original Produ Pads	ction Mas H-4 H-5 H-6 H-6 H-6 H-10 H-11 H-11 H-14 H-14 H-14
H.3.3.1 H.3.3.2 C H.3.3.2 C H.3.3.3 H H.3.3.4 C H.3.3.5 T H.3.3.6 F H.3.3.7 C H.3.3.7 C H.3.3.8 C H.3.3.9 L H.3.3.10 F H.3.3.11 H H.3.3.12 S H.3.3.13 S H.3.3.14 F H.3.3.15 C	Manufacturir H-4 Connector fo nterlayer Co Connection I Fhrough Hol Filling Resin Conductor W Conductor S Land Diame Pads for BG nternal Laye Surface Finis Solder Resis Plating on O Characteristi	ng Drawings and Artwork Master (or Printed Wiring Boards onnection Method for Area Array Packaging e Diameter for Through Hole for Through Hole vidth and Thickness pacing pacing ter A etc sh Plating st uter Perimieter Sidewall of the Boa ic Impedance	or Original Produ Pads	ction Mas H-4 H-4 H-5 H-6 H-6 H-6 H-10 H-11 H-11 H-14 H-14 H-14 H-14
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

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APPENDIX H							
		PRINTED WIRING					
H.1. G	Seneral						
H.1.1	Scope This appendix establishe provisions for the printed transmission loss (herei	d wiring boards for	high-speed sig	nal with reduced			
H.1.2	Part Number						
	The part number of the	printed wiring board	ls is in the follo	owing form.			
	Example: JAXA(¹) 2140	/ <u>H107</u> Individual identification	<u>102</u> Base material code (H.1.2.1)	<u>18(²)</u> Number of layers (H.1.2.2)			
	Notes: (¹) "JAXA" indicates the (²) Number of conductor			nay be abbreviate	ed to "J".		
H.1.2.1	Base Material Code						
	The base material co	de is as specified ir	Table H-1.				
	т	able H-1. Base N	laterial Code				
	Base material code	Insu	lation board ma	terial			
	102	Glass base woven compliant to IPC-41		ther resin,			
H.1.2.2	Number of Layers The maximum numbe	er of layers shall be	specified in ea	ach detail specific	ation.		

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H.2. A	Applicable Documents e	tc.				
H.2.1	Applicable Document	3				
	a) JERG-0-043 S	ents shall be as follows and as spect andards for Surface Mount Soldering Space Application		h 2.1.		
	c) IPC-2152 S	est methods of copper-clad laminate andard for Determining Current Ca pard Design	•	•		
	d) IPC-TM-650 T	est Methods Manual				
H.2.2	Reference Document	3				
	a) JERG-0-054 S	ents shall be as follows and as spec andards for BGA/CGA Soldering P Space Application		ו 2.2.		
	b) JIS C 6012 G	ualification and Performance Speci pards	fication for Rigid	Printed		
H.3. F	Requirements					
H.3.1	Qualification Coverag	e				
	Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs H.3.2 through H.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified sample units are considered qualified to the specified in the detail specification.					
H.3.2	Materials					
	The materials shall be	specified as follows.				
H.3.2.1	 H.3.2.1 Metal-Clad Laminate, Prepreg and Copper foil The copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The copper foil laminated to prepreg on the outermost layer shall be as specified in the drawing. The nominal thickness of the base material shall be no less than 0.05mm. The thickness of the copper foil shall be as specified in Table H-2 and the type of copper foil shall be specified in the detail specification. 					

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Table H-2.	Thickness of Copper Foil (Nominal)
------------	------------------------------------

		Unit: µm
Lover	Classification	Copper foil
Layer	Classification	thickness
External	With SVH	9 minimum
layer	Without SVH	18 minimum
Internal	SVH layer	9 minimum
layer	Any layer other than	18 minimum
	SVH layer or a layer	
	without SVH	

For electrical property of the copper laminate board, dielectric constant shall be 4.0 as a maximum at 1GHz, and dielectric dissipation factor shall be 0.01 as a maximum at 1GHz when the test is performed in accordance with Paragraph 2.5.5.9 of IPC-TM-650.

The standards (including delamination strength) applied to the materials used in the printed wiring boards shall be clearly specified in the detail specification. The detailed information about base materials such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the Application Data Sheet (hereinafter referred to as "ADS").

H.3.2.2 Via Hole Filling Materials (Filling Resin)

The filling materials for SVH and small through hole shall be resin. The detailed information about the filling materials such as type of resin and glass-transition temperature shall be specified in ADS.

H.3.2.3 Solder Resist Ink

The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent.

H.3.2.4 Marking Ink

The marking shall be conducted using epoxy resin base ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

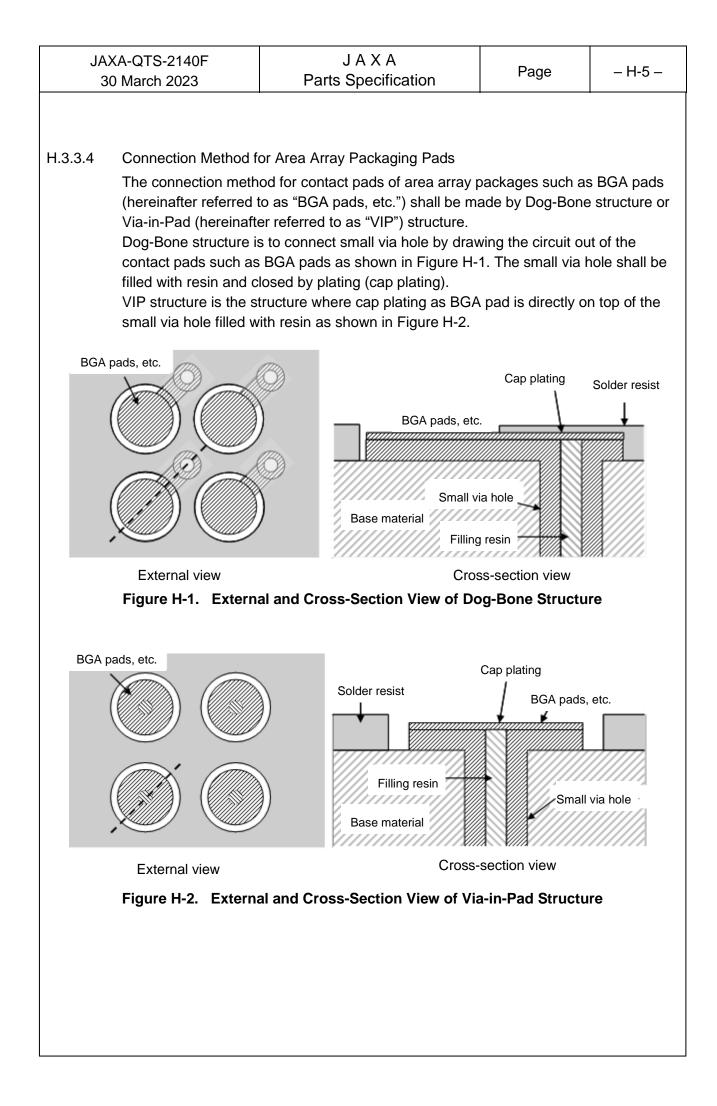
H.3.2.5 Plating

Electroless and electrolysis plating shall be applied to all through holes and for cap plating. Solder coating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.

H.3.2.5.1 Electroless Copper Plating

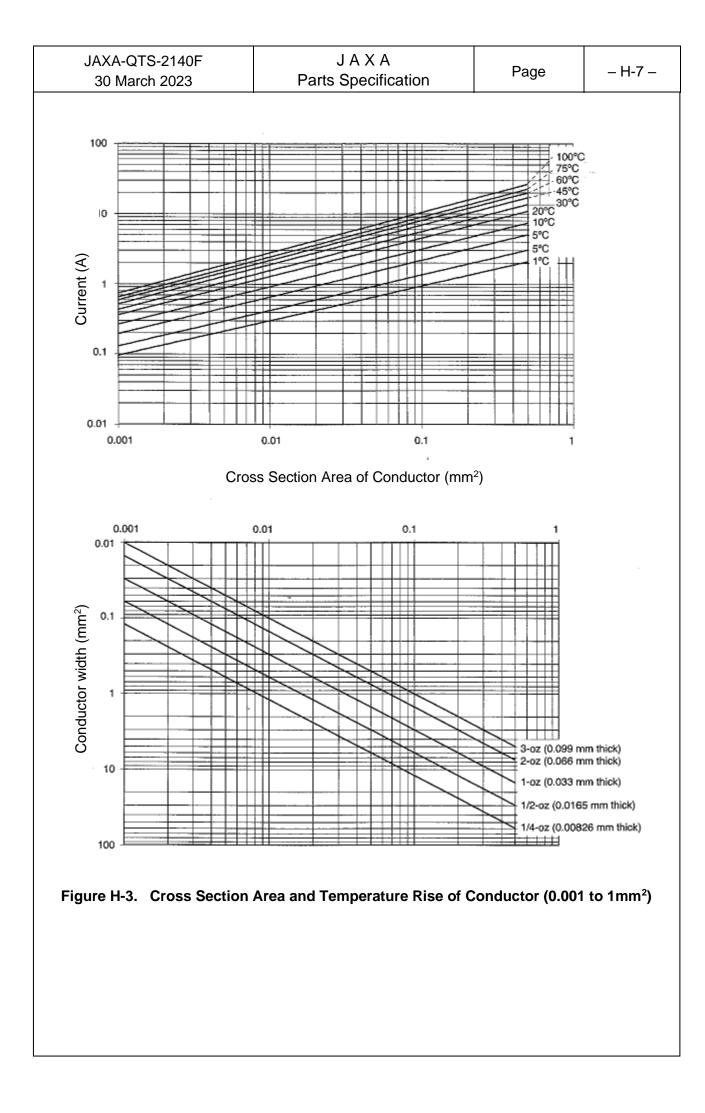
The electroless copper plating shall be applied as a preceding process of electrolytic plating to form a conductive layer over the insulating material.

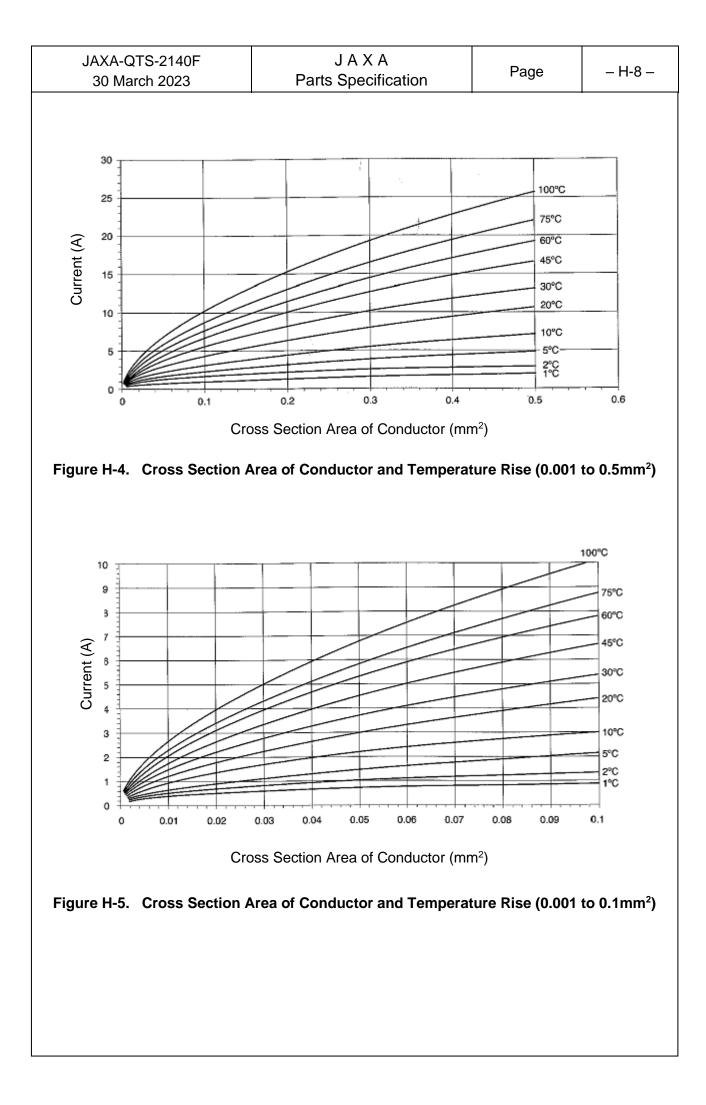
JAXA-QTS-2140F 30 March 2023		Par	J A X A ts Specification	Page	– H-4 –		
H.3.2.5.2 Electrolytic Copper Plating							
The electrolytic copper plating shall have a minimum purity of 99.5 %.							
H.3.2.5.3	Electrolytic Gold Pl	ating					
The electrolytic gold plating shall be as specified in Table H-3. The electrolytic nickel plating specified in paragraph H.3.2.5.4 shall be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 % except for the metal added to increase the hardness.							
	Tab	ole H-3. E	lectrolytic Gold Plating	-			
	Item		Specificatio				
	Purity		Min. 99.7 %	, D			
	KNOOP hard	ness	91 to 129 (inclu	sive)			
H.3.2.5.5	equivalent, and sha Solder Coating The solder used fo		ow stress type. ating shall contain 50 to	70 % tin.			
H.3.3 D	esign and Constructio	n					
H.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master) Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.							
H.3.3.2 Connector for Printed Wiring Boards A direct connector (one-part connector or edge-board connector) shall not be used.							
 H.3.3.3 Interlayer Connection Connection between conductive patterns in different layers of the printed wiring boards shall be provided by small via holes, SVH or through holes. 							

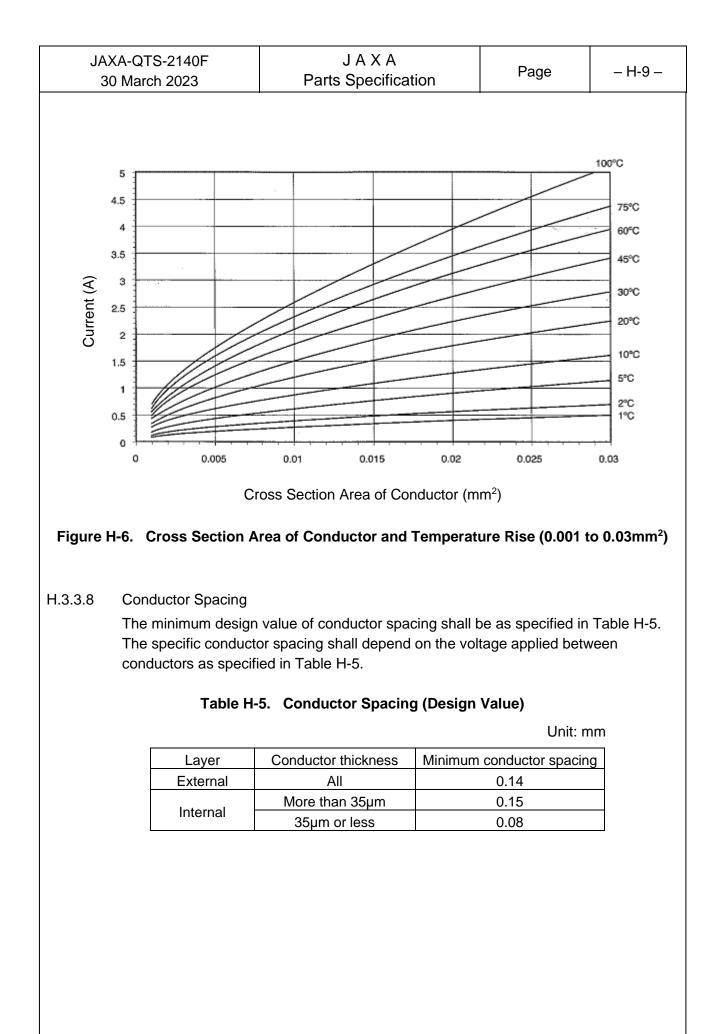


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LI 2 2 5	Three	wah Hala Diama	tor				
H.3.3.5		ough Hole Diame minimum bole d		and SV/H	shall be @0.20m	m as a drill	
	The minimum hole diameter for small via hole and SVH shall be φ 0.20mm as a drill hole. When the land of via hole is used as BGA pads, etc., the drill hole for via hole shall be φ 0.20mm as a maximum.						
H.3.3.6	Fillin	ng Resin for Thro	ough Hole				
	The small via hole to be filled with via filling materials shall be specified in the production drawing. The small via holes and SVH in VIP structure shall be filled with via filling materials.						
H.3.3.7	Conductor Width and Thickness						
	The minimum design value for conductor width shall be as specified in Table H-4. The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor. Figures H-3, H-4, H-5, and H-6 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this will apply to both internal and external layers of the conductor under vacuum and space environmental conditions. The details shall be specified in IPC-2152. When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.						
		Table I	H-4. Conductor Width	(Design V	/alue)		
				_	Unit: mm		
		Layer	Conductor thickness	Minimum	conductor width		
		External	All		0.12		

Layer	Conductor thickness	Minimum conductor width
External	All	0.12
	More than 35µm	0.10
Internal	35µm or less	0.07







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Table H-6. Conductor Spacing for Printed Wiring Boards

Voltage applied between conductors, DC or AC _{p-p} (V)	Minimum conductor spacing		
	External layer	Internal layer	
0 to 50	0.15	0.08	
51 to 100	0.15	0.10	
101 - 300	0.40	0.20	
301 - 500	0.80	0.25	
501 or higher	(0.003xV)	(0.0025xV)	

H.3.3.9 Land Diameter

The minimum design value of land diameter shall be as specified in Table H-7 (see Figure H-7). Non-functional land is not necessary when maintenance of conductor spacing and electrical characteristics requirements are specified.

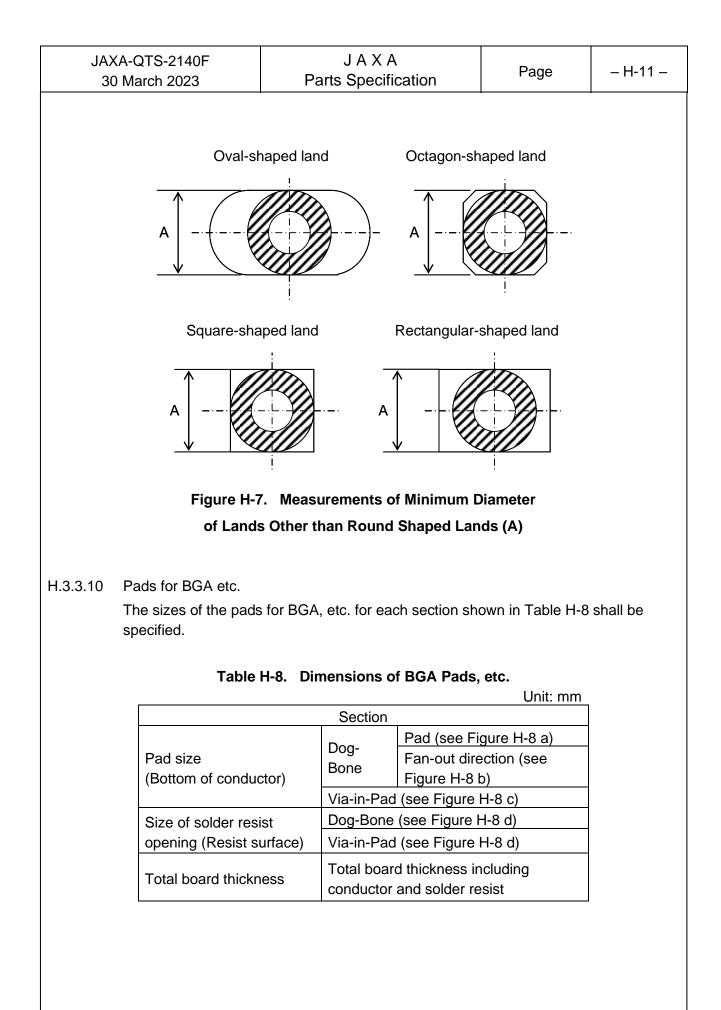
Table H-7. Land Diameter

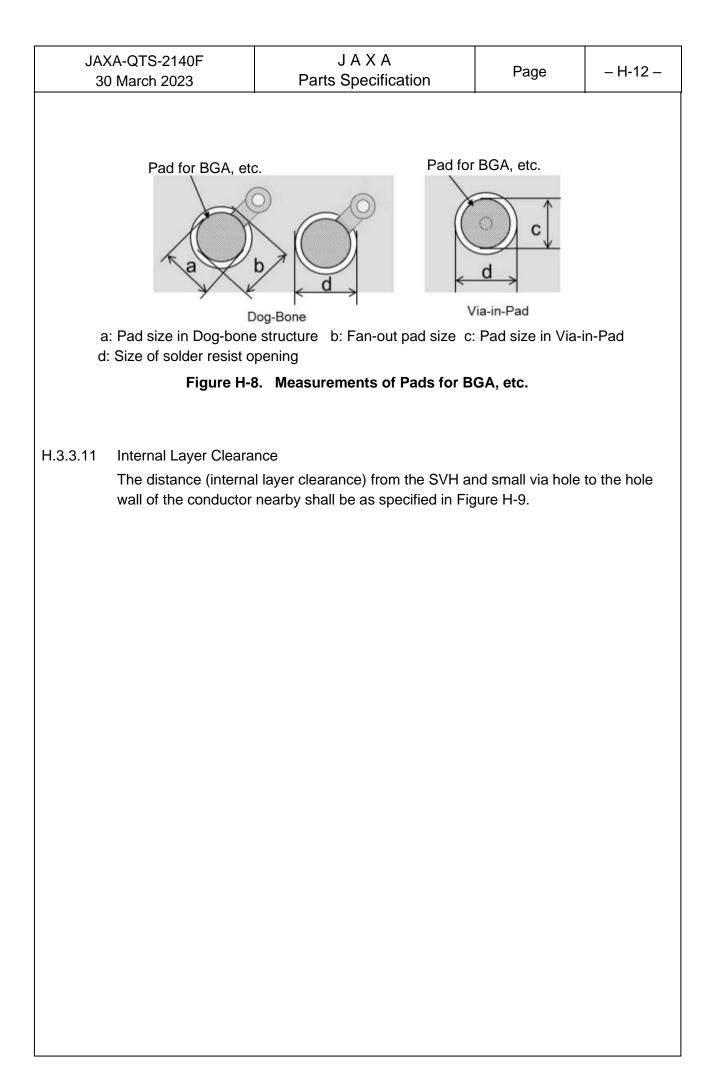
Unit: mm

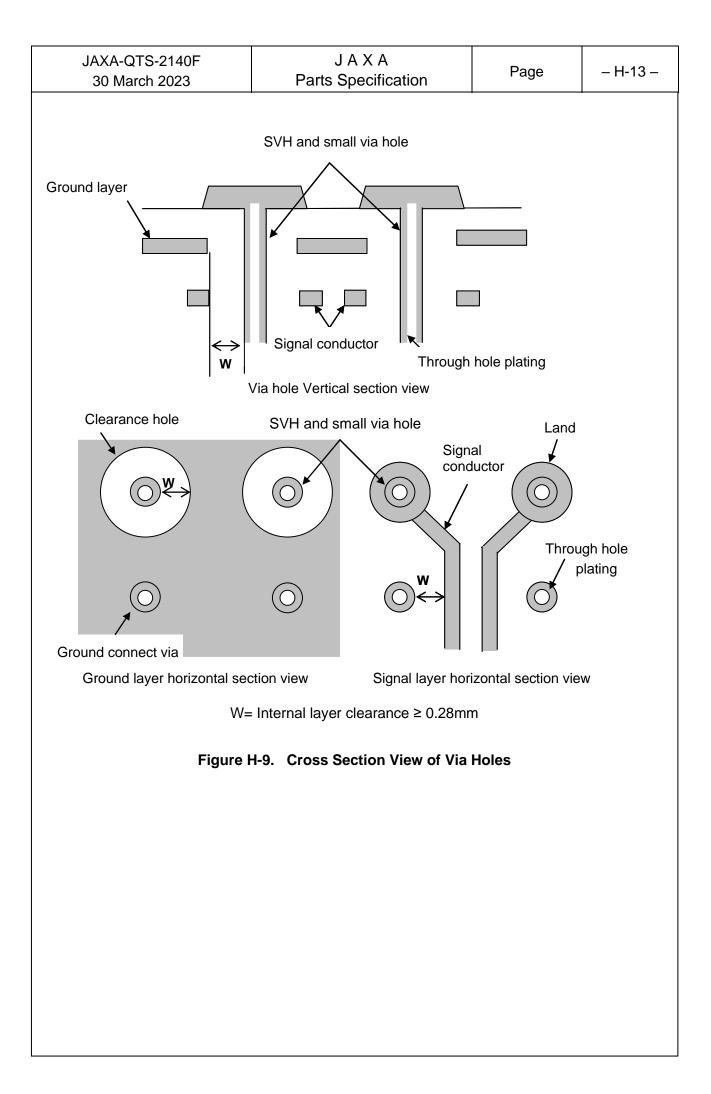
Hole	Minimum land diameter(1)
SVH and small via holes	ϕ (Drill diameter + 0.25)
Plated-through holes except the above	ϕ (Finished hole diameter + 0.5)
Non-plated-through holes	ϕ (Drill diameter + 1.1)

Notes:

(¹) The minimum diameter of lands other than round shaped lands shall be the measure of the length "A" shown in Table H-7.







0					
H.3.3.12	Surface Finish Plating				
	manufacturing drawing Nickel plating shall be	urface finish plating and solder coating specified in the g shall be in accordance with Table H-9. The electroly applied as an undercoat of electrolytic gold plating, a face finish. If more strict requirements than the ones	ytic and shall		
	in Table H-9 are neces manufacturing drawing	ssary, consult with manufacturer and specify on the g.	·		
	Table H-9.	Thickness of Surface Finish Plating			
		Unit: μm	7		
	Plating material	Surface plating thickness	_		
	Electrolytic gold	1.3 to 4.0	_		
	Electrolytic nickel	5 as a minimum	_		
	Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (paragraph H.3.10.2).			
H.3.3.13	Solder Resist				
	The solder resist application shall be specified except for the land, pads (incl. Via-in-				
	Pad), and the small via holes without resin filling. The lands of small via hole and SVH in the dog-bone structure shall be coated with				
	solder resist.				
	Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.				
	The minimum distance	e from the edge of the board to the solder resist shall	l be 0.3m		
H.3.3.14	Plating on Outer Perim	nieter Sidewall of the Board			
	"Sidewall plating") sha	erimeter sidewall of the board (hereinafter referred to Il be specified in the manufacturing drawing if applied the sidewall plating shall be specified in detail specif	d.		
	-				
H.3.3.15	Characteristic Impedance The characteristic impedance of the printed wiring boards shall be specified in the				
	manufacturing drawing		u in the		
	Operating Temperatur	e Range			
H.3.3.16	Operating remperatur	e Range			

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H.3.4.1	Externals of Conduc	tor, Base Material and Solder Resi	st	
H.3.4.1.1	Conductor			
	a) Conductive pa			
		e patterns shall conform to the app inal production master).	roved or provided	1 artwork
	b) Conductor	inal production master).		
	,	s including sidewall plating shall co	ontain no tears, cr	acks, lifting,
	•	Any combination of edge roughne	•	
	-	osing the insulation board shall not		
		of the minimum finished conductor t exceed the design width of the conductor	-	
		ding 0.05mm in width shall not be r		
	-	f 100×100mm on the printed wiring	•	-
		ctor edges shall meet the conducto	r width tolerance	(see Figure
	H-10). The tolerances	s of conductor width and conductor	spacing shall be	as specified
	in Table H-10.		opaoling onali 20	
		pinholes on the ground surface an	,	
	not exceed 1.0	mm in the maximum length and 4	pieces per 625cn	n² in number
			\frown	
			$\left(\bigcirc \right)$	
		Pinhole	(\bigcirc)	
		\mathbb{W}_{1}^{3}		
	<u>↓</u>		₩1 W2	
	\wedge		$\uparrow\uparrow$	
	R	W4 Nick		
	•	um finished conductor width) (Minimum finished conductor width	n)	
		0.80 × Minimum finished conductor		
		nductor width tolerance \ge W5-R	-	
	L = Length	of defect		

Figure H-10. Passing Criteria for Conductor Defects

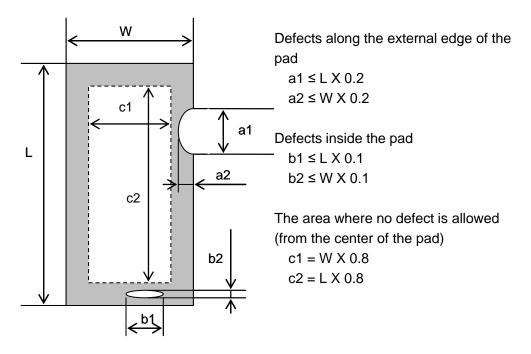
Table H-10.	Tolerance of Conductor Width and Conductor Spacing
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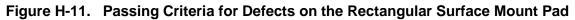
		Unit: mm
	Dimension	Tolerance
	0.07 to lease them 0.40	+0.05
Conductor	0.07 to less than 0.13	-0.03
Conductor	0.13 to less than 0.20	±0.05
width	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
	Less than 0.10	0.05 as a minimum
Conductor	0.10 to less than 0.14	0.06 as a minimum
Conductor	0.14 and more	0.10 as a minimum
spacing	The positive side tolerance is not specified for all design	
value.		

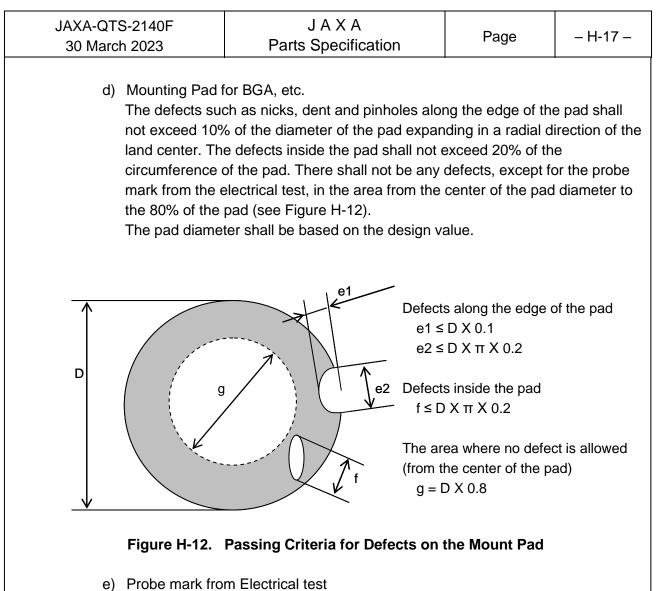
c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure H-11).

The pad length and width shall be based on the design value.







The probe mark from the electrical test

The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

- f) Dielectric layer between conductor layers
 The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.
- g) Solder coating

The solder coating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on sidewall plating side is permitted.

 h) Electrolytic nickel and electrolytic gold plating The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on the conductor side is permitted.

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 H.3.4.1.2 Base Materials a) Edges of printed wiring board Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board. Crazing along the edges of printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller. b) Surface of printed wiring boards The surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall not be permitted. 					
H.3.4.1.3	 b) Significant visu surface, uneve c) Unless otherwi provided that th d) The solder resi e) The application patterns shall n f) Unless otherwi shall not be exp 	er resist shall be free from tackine al damage such as a thin spot, se n color and exposed residual cond se specified, scratches and pinhol ne conductors are covered with sol st shall not encroach onto lands for n range and misalignment of solder neet the provisions of manufacturin se specified on the manufacturing posed in the solder resist opening ne structure, solder resist shall com /H.	paration, roughne luctor shall not be es shall be accep lder resist. or mounting parts r resist and conde ng drawings. drawings, adjace area.	ess on the e permitted. otable, uctive ent conductor	
H.3.4.2	manufacturing drawing	ach part of the printed wiring board ngs. Unless otherwise specified, d ne requirements specified in Table	imensional tolera		

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 Table H-11.
 Dimensional Tolerance

Unit: mm

	Office from	
Item	Dimensional tolerance	
Outline dimensions	± 0.3 for the dimension of 100 or smaller, and additional 0. for every 50 in excess of 100	
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.	
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.	

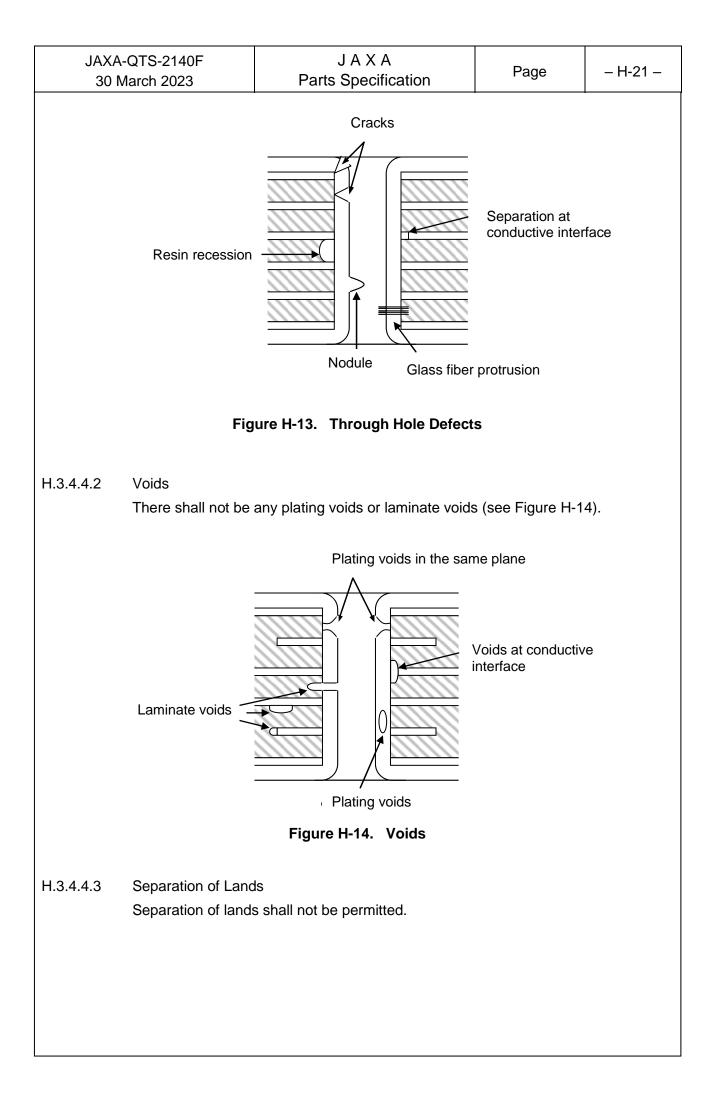
H.3.4.2.1 Dimensions of BGA Pads, etc.

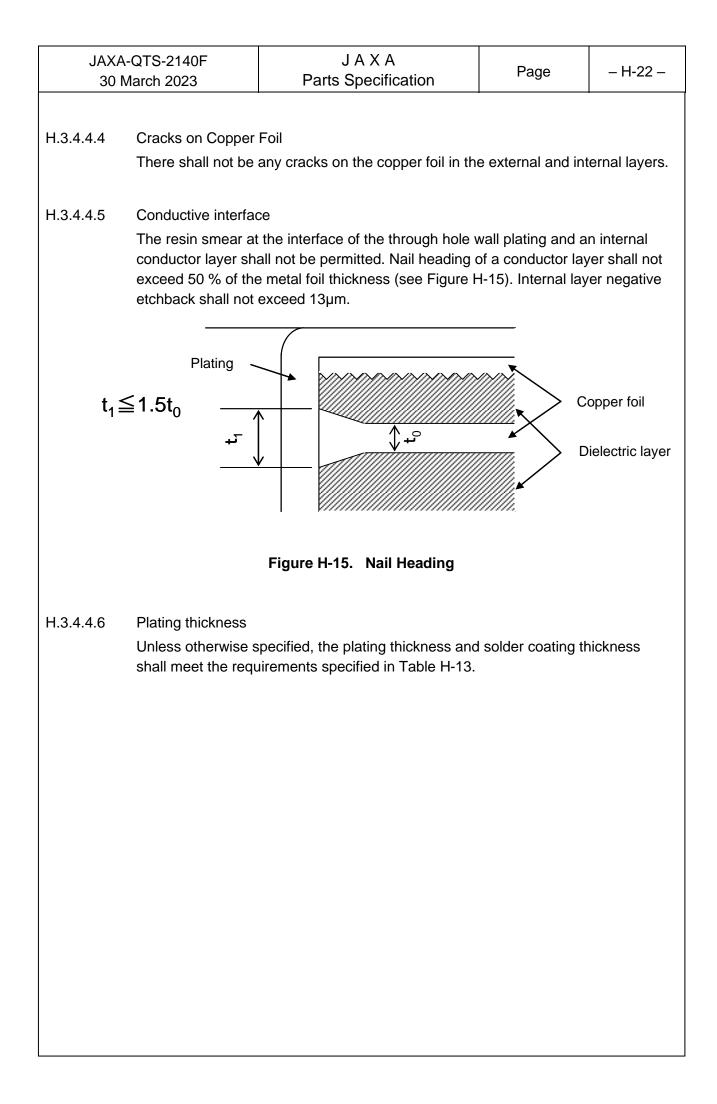
Unless otherwise specified, the dimension tolerance for BGA pads, etc. shall be in accordance with the requirements specified in Table H-12.

			Unit. (mm)
	ltem		
		Pad (Figure H-8 a)	±0.05
Pad size (conductor bottom size)	Dog-Bone	Fan-out direction (Figure H-8 b)	±0.075
	Via-in-Pad (F	Figure H-8 c)	±0.05
Solder resist opening	Dog-Bone (Figure H-8 d)		±0.05
diameter (resist surface)	Via-in-Pad (Figure H-8 d)		±0.05
Accurate alignment	Length of rov	v of BGA pads	±0.05
Pad thickness (conducto	Pad thickness (conductor thickness)		
Total board thickness (incl. solder resist)			±8 %
Co-planarity (flatness): Normal state			0.05mm or less for diagonal diameter of BGA pads

Table H-12. Dimensions for BGA Pads, etc.

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H.3.4.3	Marking					
	 H.3.4.3 Marking The marking shall be produced with the marking inks specified in paragraph H.3.2.4, by copper etching or laser marking. The marking shall remain legible and shall not adversely affect any function, performance or reliability of printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag. a) Part number b) Year and month manufactured c) Manufacturer's name or its identification code d) Product serial number⁽¹⁾ or lot number Note: ⁽¹⁾ Product serial number shall be provided so that the complete manufacturing process can be traced.					
H.3.4.3.1	usable, it shall be o	bard art (equivalent to a single wiring bo clearly marked that the part cannot nod such that it does not easily var	be used. This m	narking shall		
H.3.4.4	Structural Integrity					
H.3.4.4.1						

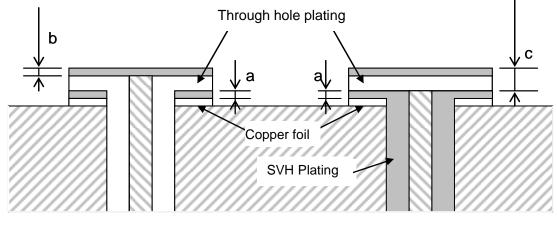




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Table H-13. Thickness of Plating and Solder Coating

			Unit: µm	
Туре	Surface and through hole wall thickness			
Electroless copper	Thic	kness necessary and sufficient for	or electrolytic copper	
plating		plating in the subsequent	process	
		Via hole for part mount	25 as a minimum	
		Small via hole	25 as a minimum	
		SVH	30 as a minimum	
	SVH p	plating on land (Figure H-16 a)	5 as a minimum	
Electrolytic copper		Small via hole	As specified in detail	
plating	Сар	(Figure H-16 b)	specification	
	plating	SVH	As specified in detail	
		(Figure H-16 c)	specification	
		Sidewall plating	25 as a minimum	
Electrolytic gold plating		1.3 to 4.0		
Electrolytic nickel plating	5 as a minimum			
Ostden sesting	Thickness is not specified. However, the requirements of			
Solder coating	S	olderability (paragraph H.3.10.2)	shall be satisfied.	



Small via hole

SVH

a: SVH plating thickness on lands

- b: Cap plating thickness on small via hole
- c: Cap plating on SVH



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H.3.4.4.7	Laminate Cracks Cracks on laminate	e shall not be permitted.		
H.3.4.4.8	Delamination and Blister Delamination and blister shall not be permitted.			
H.3.4.4.9	Layer-to-layer Registraion The layer-to-layer registration error shall not exceed 0.15mm.			
H.3.4.4.10	Annular Ring The minimum annular ring of internal and external layer shall meet the requirements specified in Table H-14.		9	

		Unit: mm
Through hole type	Layer	Annular ring
Through hole	External	0.05
	Internal	0.025
Non-through hole	External	0.38

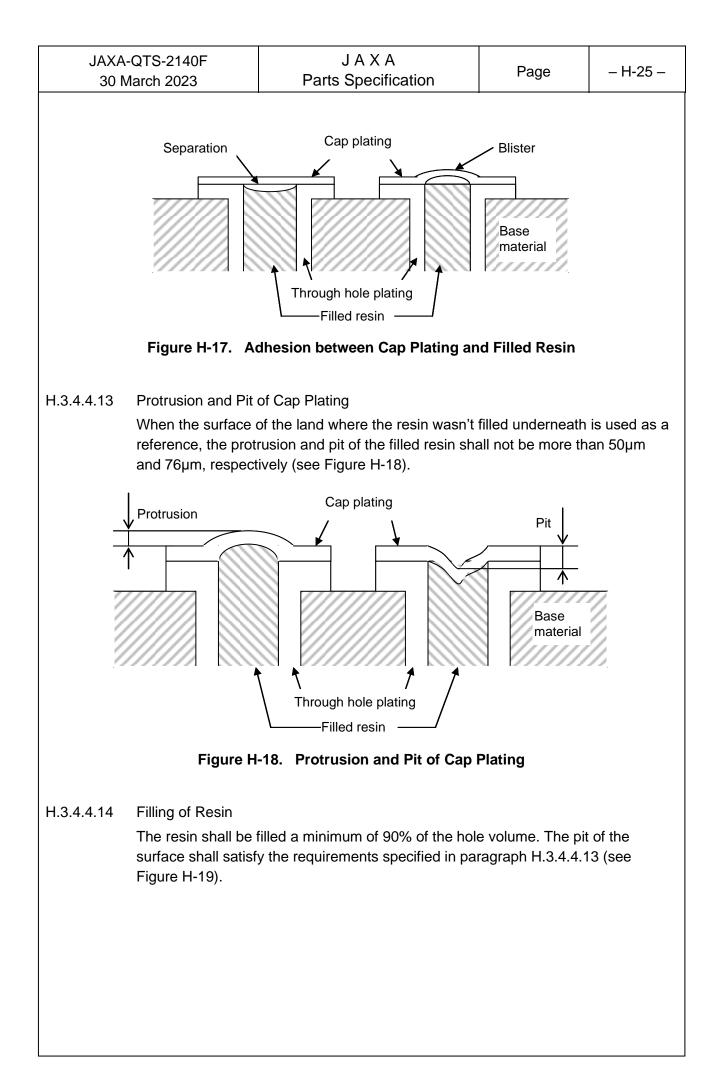
Table H-14. Annular Ring

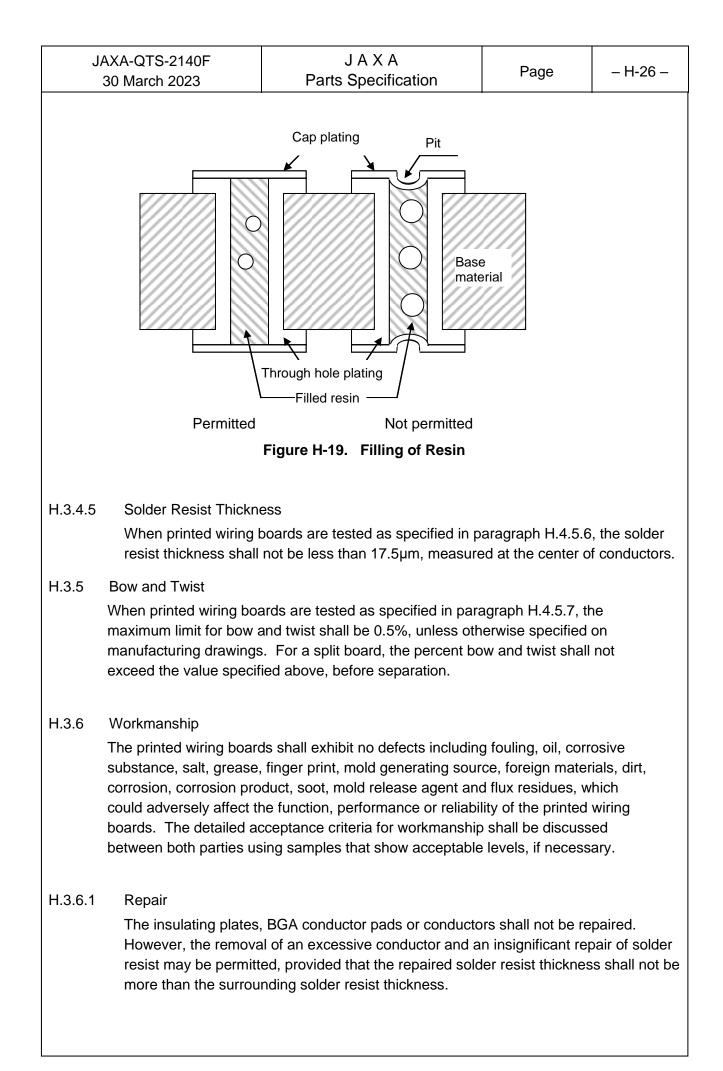
H.3.4.4.11 Dielectric Layer Thickness

The dielectric layer between conductor layers of a multilayer printed wiring board shall not be less than 0.08mm in thickness.

H.3.4.4.12 Adhesion between Cap Plating and Filled Resin

When the cap plating is used as BGA pad, the gap between cap plating and filled resin shall be less than 5μ m. When the cap plating is not used as BGA pad, the requirements specified in paragraph H.3.4.4.13 shall be satisfied (see Figure H-17).





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H.3.7		verhang ards are tested as specified in para ig of plating and conductors, or sliv	•	
H.3.8	Cleanliness When printed wiring boards are tested as specified in paragraph H.4.5.10, the resistivity of the solvent extract shall not be less than $2x10^6\Omega$ cm.			
H.3.9	Electrical Performance Printed wiring board shall meet the following electrical requirements.			
H.3.9.1	Dielectric Withstanding Voltage When tested as specified in paragraph H.4.5.11.1, printed wiring boards shall not exhibit insulation breakdown, flashover or sparkover.			
H.3.9.2	•	ified in paragraph H.4.5.11.2, print short-circuiting between circuit pa	•	shall not
H.3.9.3	resistance between the exceed the value (Ri) connection resistance	boards are tested as specified in p wo lands connecting a circuit on a which is calculated by the formula between all layers can not be me ion resistance shall be repeatedly	Il conductor layers a specified below easured at a time	s shall not . When the , the
	$Ri = 2\rho \frac{I}{W \cdot t} (m\Omega)$			
	p: Volume resistivity a l: Distance between la W: Conductor width (t: Conductor thicknes	mm)	orms the conducto	or (mΩ∙mm)
H.3.9.4	characteristic impeda	ance boards are tested as specified in p nce shall be within the range spec nce is not specified, the impedance	cified in the manu	facturing
H.3.10	Mechanical Performanc	e		

Printed wiring boards shall meet the following mechanical requirements.

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H.3.10.1	 the following requirem a) Bond strength The land shall we smaller. b) Conductor and la When printed with H.4.5.4.1, there are a with the strength of the s	tested as specified in paragraph H.4.5.12.1, printed wiring boards shall meet lowing requirements. This provision shall not apply to SVH or small via holes. Sond strength the land shall withstand a minimum of 89.2N pull or 1380N/cm ² , whichever is maller. Conductor and land When printed wiring boards are inspected visually as specified in paragraph I.4.5.4.1, there shall be no loosening around the through holes. Microsection of through hole When printed wiring boards are microsectioned and inspected in accordance with paragraph H.4.5.5, there shall be no cracks, blistering, measling or		
H.3.10.2	 the following requirem a) Through hole so The through hole solder. This provision b) Surface solderate A minimum of 95 with fresh solder 	lderability e inside wall and land surface shal vision shall not apply to SVH or sr	ll exhibit proper w nall via holes. shall be covered oles, dewetting of	retting of uniformly r small
H.3.10.3	•	ace Conductor ified in paragraph H.4.5.12.2, prin cified in the detail specification.	ted wiring boards	shall meet
-	Environmental Performa Printed wiring boards sh	ance nall meet the following environmer	ntal requirements.	
H.3.11.1	Thermal Shock			
H.3.11.1.1	When printed wirin there shall be no of Printed wiring boar at the completion of	(applicable to qualification test) g boards are tested as specified ir pen circuit, blistering, measling, cr ds shall meet the requirements sp of the test, and the change in conn after the test shall be less than 10	azing or delamin becified in paragra ection resistance	ation. aph H.3.9.2

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 H.3.11.1.2 Thermal Shock (II) (applicable to quality conformance inspection) When printed wiring boards are tested as specified in paragraph H.4.5.13.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph H.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. 				ation. aph H.3.9.2
H.3.11.2	Humidity and Insulation Resistance When printed wiring boards are tested as specified in paragraph H.4.5.13.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be a minimum of $500M\Omega$.			
H.3.11.3	Hot Oil Resistance When printed wiring boards are tested as specified in paragraph H.4.5.13.3, the change in connection resistance between circuits before and after the test shall be less than 10%.			
H.3.11.4	 the following requirer a) Externals There shall be no b) Structural Integr In the vertical most satisfied. 1) Through hole There shall be 2) Laminate vor When the cord When the cord the minimum spacing shale 3) Lifting of lans Lifting of lans Lifting of lans Lifting of lans Cracks on cord There shall be 5) Internal layee There shall be Cracks on cord There shall be 	o measling, cracks, separation of pamination. ity icrosection of through holes, the for- be no corner cracks or barrel crack id onductor spacing on the same plan in conductor spacing specified in the l not exceed 76µm. ds ds after thermal stress test shall be opper foil be no cracks which penetrate throu r connection be no separation between copper for plating. acks rmal stress test, the laminate crack is or on the lands shall not exceed than the ones on the land area sh acent conductors fall below the min	olating and condu llowing requirements. e or between laye e manufacturing of e permitted. ugh the copper fo foil of internal laye ks between the la 80µm, and the la all not cause the	uctors, ents shall be ers satisfies drawings, the il. er and unds of a uminate spacing

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			-

The interface between cap plating and filled resin shall meet the requirements specified in paragraph H.3.4.4.12.

H.3.11.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph H.4.5.13.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall not be less than $500M\Omega$. After the test, the requirements specified in paragraph H.3.9.1 shall be satisfied.

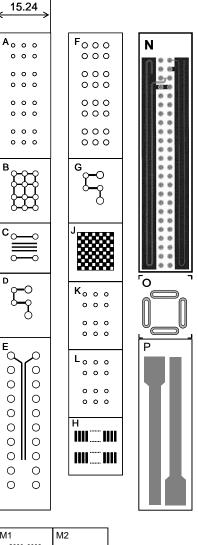
H.4. Quality Assurance Provisions

H.4.1 Test Pattern

The test pattern provided for qualification test and quality conformance inspection shall be in accordance with Figure H-20. The test pattern shall have the same structure as the product produced from the identical work board. A set of the test pattern shall be assigned for each printed wiring board.

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Unit: mm



M1

Е

C

Arrangement of test pattern

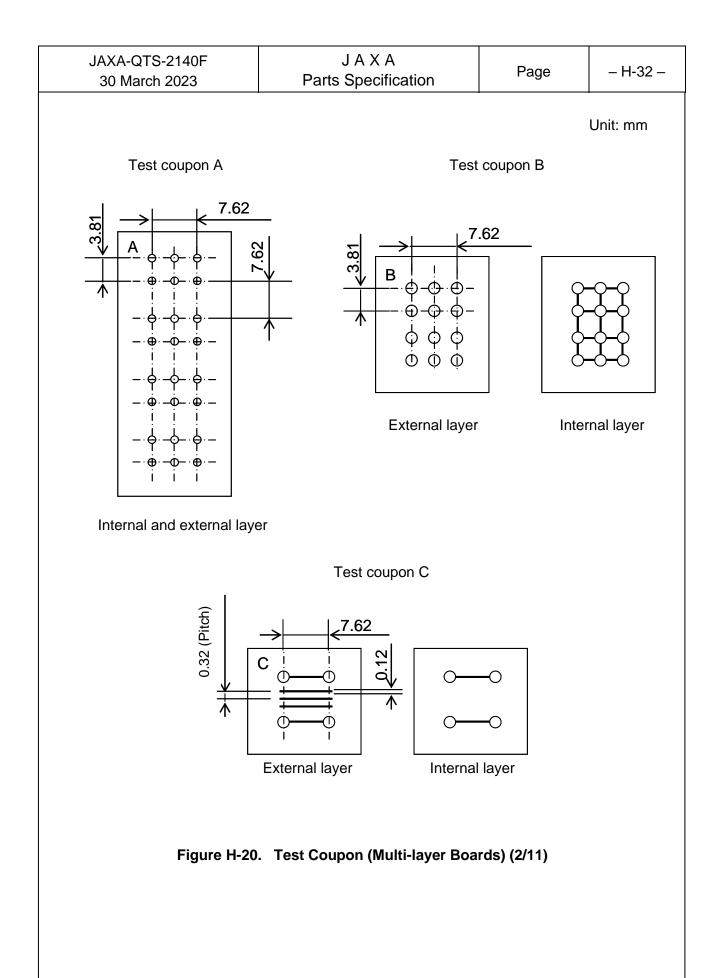
Notes

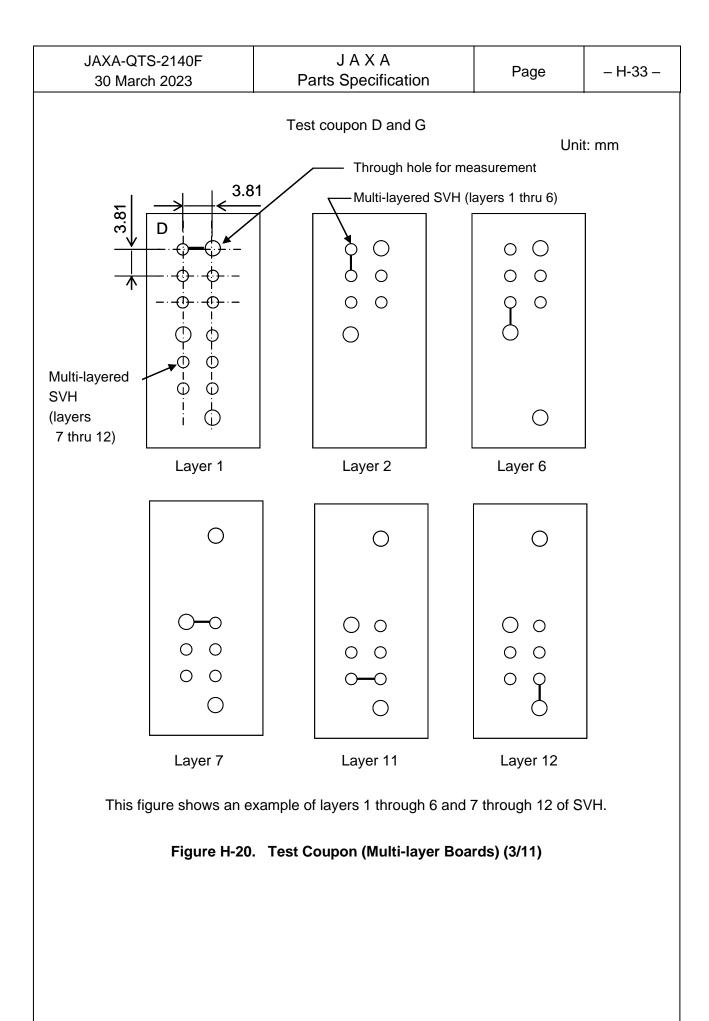
- (1) Unless otherwise specified, the conductor width shall be 0.5±0.1mm.
- (2) Test coupon A indicates the minimum hole diameter of the through hole (incl. small via hole) for the corresponding printed wiring board, and the land diameter shall be the minimum land diameter of the through holes. When applied, small via holes shall be filled with resin. The hole diameter tolerance is not specified.
- (3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes and diameter shall be \$0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.
- (4) The patterns of test coupons D and G vary depending on the number of layers and via hole structure. Each coupon shall be produced so as to form the same number of layers and via hole structure as those of the corresponding product, and to have a circuit continuity through all layers by via holes. The hole and land diameter shall be the minimum diameter for each SVH and small via hole of the corresponding products, and the land shape shall be the typical land shape of the products. On both ends of the printed wiring board, through holes shall be formed to measure the resistance, the diameter of the land and hole shall be \$1.8mm and \$0.8mm, respectively. The hole diameter tolerance is not specified.
- (5) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist shall be the clearance diameter for the corresponding printed wiring board. If the hole diameter for the product is unknown, the land diameter shall be equal to the land diameter + 0.2mm.
- (6) Test coupons K and L shall be prepared only when the corresponding products have SVH. Those coupons vary depending on the number of layers and via hole structure.

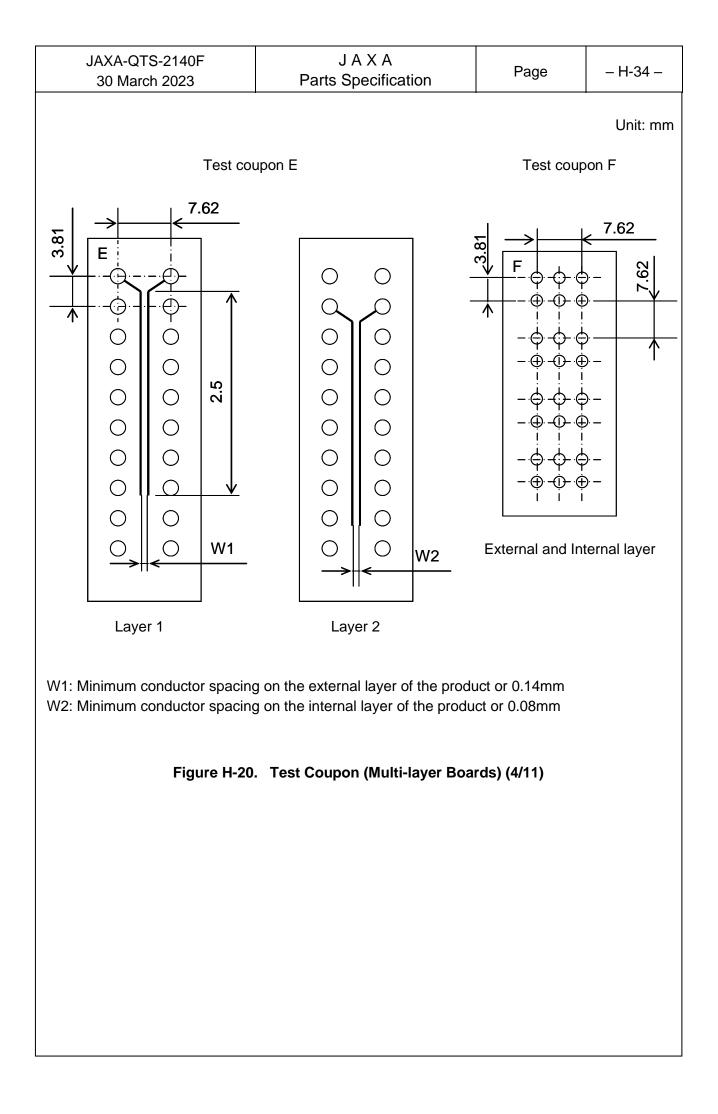
The land shall be formed only on the layers which are connected by SVH.

- (7)Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. The conductors shall be formed on all layers in accordance with this figure.
- (8) The arrangement of test coupons shown in this figure is an example; a different arrangement is also acceptable.
- (9) The symbols of test coupons (A to H and J to M2) shall be used for identification and not for the object of inspection. The marking method is not specified.
- (10) Only when the BGA pads, etc. are required, the test coupon M1 (Dogbone structure) or test coupon M2 (VIP structure) shall be formed in accordance with the pad structure. An example of test coupons M1 and M2 is shown to the left. See detail specification for more detailed information.
- (11) Only when the characteristic impedance is required, the test coupon N shall be formed.
- (12) Only when the outer perimeter sidewall plating is required, the test coupon O shall be formed. An example of test coupons O is shown to the left. See detail specification for more detailed information.
- (13) Only when the structure where copper foil is laminated on the outer layer is required, the test coupon P shall be formed.

Figure H-20. Test Coupon (1/11)







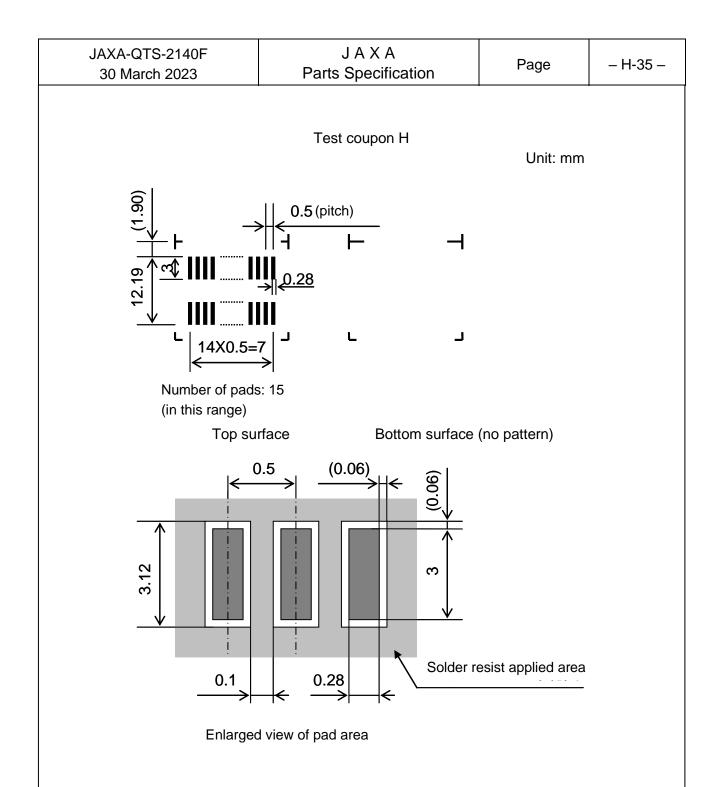
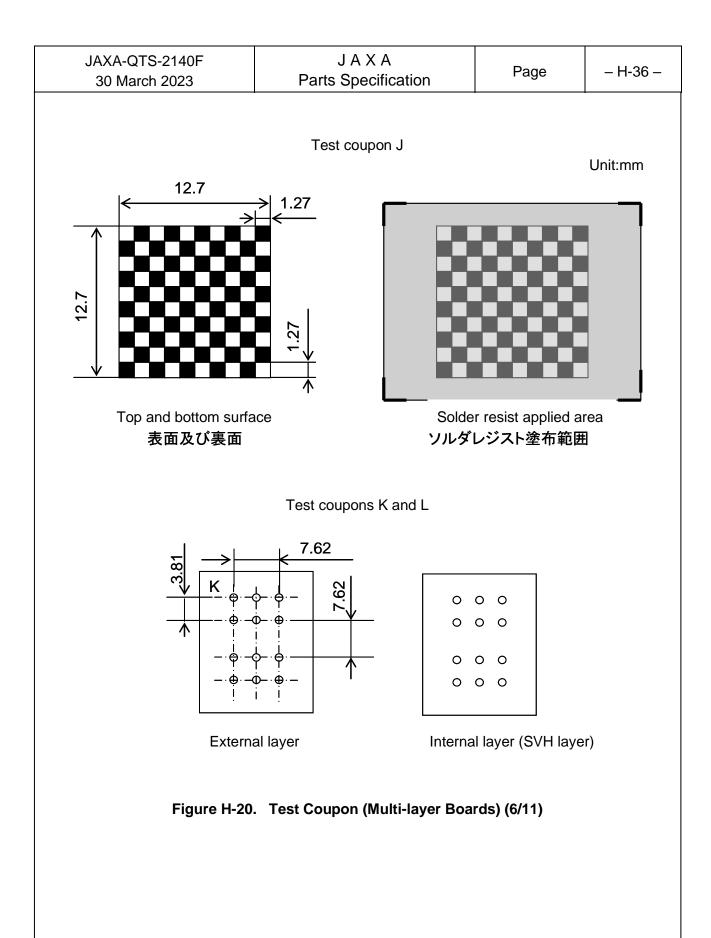


Figure H-20. Test Coupon (Multi-layer Boards) (5/11)



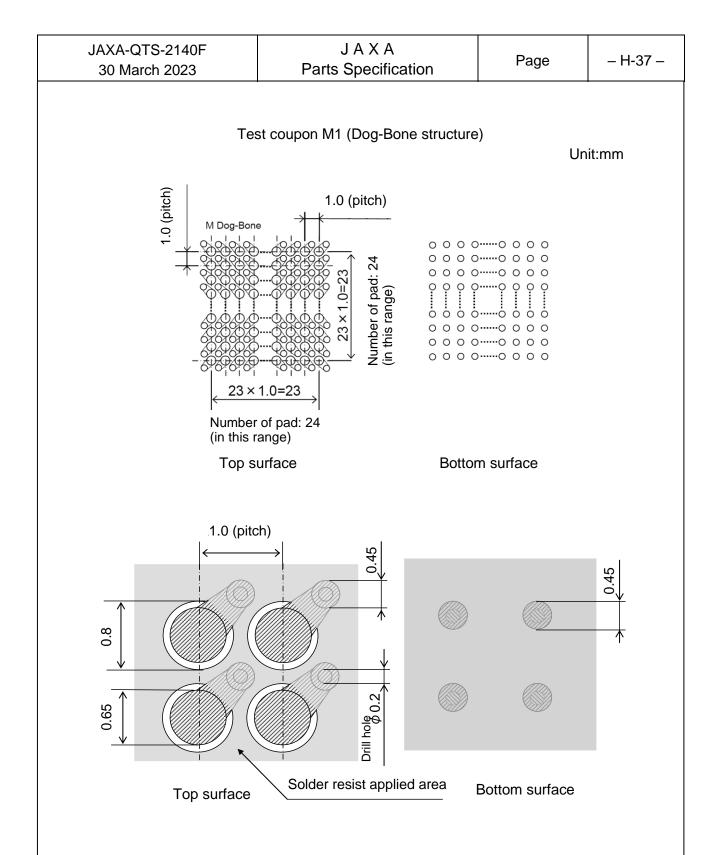
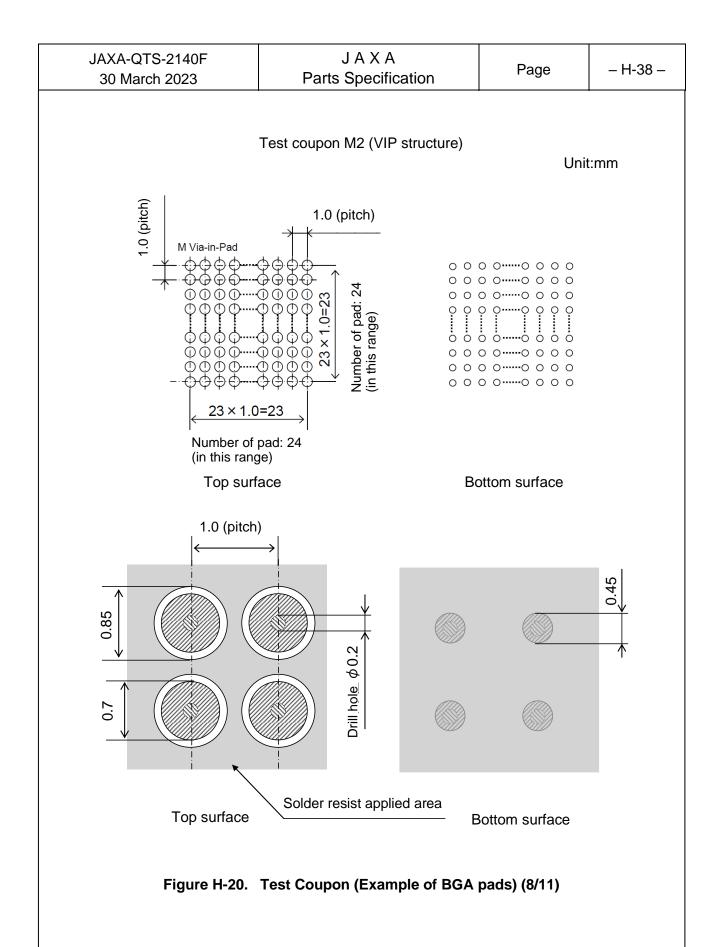
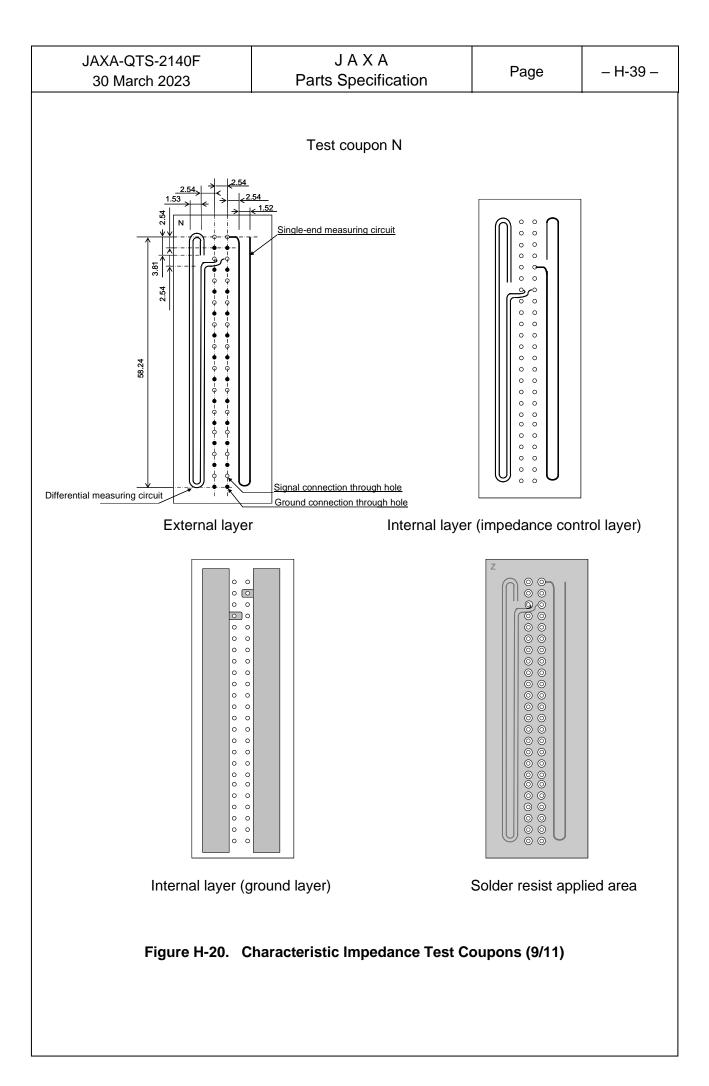


Figure H-20. Test Coupon (Example of BGA pads) (7/11)





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	Testerman		
	Test coupon O		
Fiç	gure H-20. Test Coupons (10/11)	

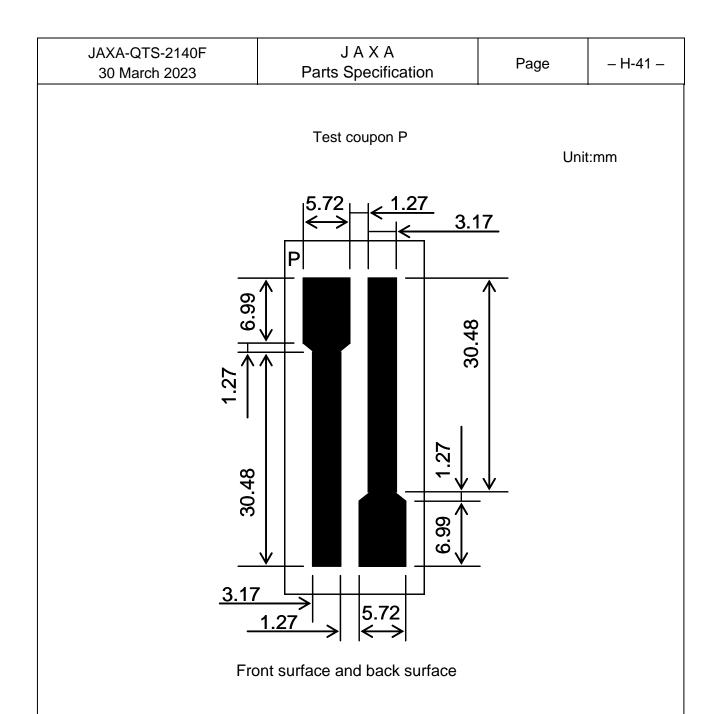


Figure H-20. Peel Strength Test Coupons (11/11)

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H.4.2 In-Process Inspection

The in-process inspection specified in Table H-15 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs H.3.4.1 (Externals of Conductor, Base Material and Solder Resist), H.3.4.2 (Dimensions), H.3.4.3 (Marking), H.3.8 (Cleanliness), and H.3.4.2.1 (Dimensions of BGA Pads, etc)

No.	ltem	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	H.3.4.1 H.3.4.2 H.3.4.3	H.4.5.4.1 H.4.5.4.2 H.4.5.4.3	All	After forming internal circuit and before pre- treating the laminate layer
2	Conductor of external layer Base material of external layer	H.3.4.1.1 H.3.4.1.2	H.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	H.3.8	H.4.5.10	Sampling(1)	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	H.3.4.2.1	H.4.5.4.2	All	After forming solder resist and before solder coating

Table H-15.	In-Process	Inspection
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Note (¹) Sampling inspection shall be performed based on 1.0% of the acceptable quality level (AQL) in "Normal Inspection Level II" specified in JIS Z 9015-1. The lot shall be processed in the same circuit forming process on the same day the sampling inspection was performed and can be subjected to solder resist application.

H.4.3 Qualification Test

H.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole and number of layers sufficient to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation.

H.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table H-16. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table H-16.

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		Table H	<u>I-16. Quali</u>	fication Te			
		Test			Pass	/fail Criteri	а
			Requirement	Test method paragraph	Sample	Quantity	
Group	Order	Test item	paragraph		Production	Test	of
Group	Oldel	restitem	paragraph	paragraph	printed wiring	coupon	allowable
					boards	(1) (2)	defects
		Externals of conductor, base					
		materials, and solder resist	H.3.4.1	H.4.5.4.1		A, B, C,	
	1	Externals, dimensions,				D, E, F,	
I					No. 1 to No. 6	G, H, K,	
I		Dimensions	H.3.4.2	H.4.5.4.2	NO. 1 10 NO. 0	L, M, N,	
		Marking	H.3.4.3	H.4.5.4.3		O and P	
	2	Workmanship	H.3.6	H.4.5.8			
	3	Characteristic impedance	H.3.3.15	H.4.5.11.4		N	
	1	Plating adhesion and	H.3.7	H.4.5.9		С	
II		overhang	-		No. 1 to No. 6	-	
	2	Bow and twist	H.3.5	H.4.5.7		N/A	
	1	Structural integrity	H.3.4.4	H.4.5.5		A, F, K,	-
						M and O	
Ш	2	Terminal pull strength	H.3.10.1	H.4.5.12.1	No. 1	F	
	3	Solder resist thickness	H.3.4.5	H.4.5.6		J	
	4	Peel strength of surface conductor ⁽³⁾	H.3.10.3	H.4.5.12.2		Р	0
	1	Connection resistance	H.3.9.3	H.4.5.11.3			
IV	2	Hot oil resistance	H.3.11.3	H.4.5.13.3	No. 2	D	
	3	Connection resistance	H.3.9.3	H.4.5.11.3			
	1	Circuitry	H.3.9.2	H.4.5.11.2			
	2	Connection resistance	H.3.9.3	H.4.5.11.3		E and	
V	3	Thermal shock (I)	H.3.11.1.1	H.4.5.13.1a)	No. 3	G ⁽⁴⁾	
	4	Circuitry	H.3.9.2	H.4.5.11.2		Ŭ	
	5	Connection resistance	H.3.9.3	H.4.5.11.3			
VI 1 2	Humidity and insulation resistance	H.3.11.2	H.4.5.13.2		_		
	2	Dielectric withstanding voltage	H.3.9.1	H.4.5.11.1	No. 4	E	
1	1	Thermal stress	H.3.11.4	H.4.5.13.4		A, B, L M and O	
VII	2	Solderability	H.3.10.2	H.4.5.12.2	No. 5	B and H ⁽⁵⁾	
VIII	1	Radiation hardness	H.3.11.5	H.4.5.13.5	No.6	N/A	
-	-	Materials	H.3.2	H.4.5.2	N/A		N/A

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

⁽³⁾ This test shall be performed when copper foil laminate structure is under the qualification coverage.

⁽⁴⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽⁵⁾ The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

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H.4.4 Quality C	Conformance In	spection		
H.4.4.1 Quality	/ Conformance	Inspection (Group A)		
H.4.4.1.1 Sam	nple			
proc lot. mar	cess and is mar However, in or ked with rejection	art of a split board fails an inspect ked with rejection, the board may der not to adversely affect the ins on shall not be used as a specime of parts of the same patterns or pa	be included in an pection result, the end of the section result, the end. A "split board	a inspection e part " means a
H.4.4.1.2 Insp	ection Items ar	nd Sample Size		
H-17	7. The inspecti	order of Group A inspection shall ons within each group shall be pe nall be provided for each of Group	erformed in the ord	

		Inspection			P	ass/fail criteria	1
					Quantity of samples		Quantity
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring boards	Test coupon	of allowable defects
	1	Design and construction	H.3.3	H.4.5.3			
I	2	Externals of conductor, base materials, and solder resist Externals, dimensions,	H.3.4.1	H.4.5.4.1		N/A	
·		Dimensions Marking	H.3.4.2	H.4.5.4.2	All		
	3	Workmanship	H.3.4.3 H.3.6	H.4.5.4.3 H.4.5.8			0
	4	Characteristic impedance	H.3.3.15	H.4.5.11.4		N ⁽¹⁾	Ũ
II	1	Bow and twist	H.3.5	H.4.5.7	All	N/A	
III	1	Circuitry	H.3.9.2	H.4.5.11.2	All	N/A	
IV	1	Thermal stress	H.3.11.4	H.4.5.13.4	N/A	A, F, $K^{(2)}$, $M^{(3)}$ and $O^{(4)}$	
V	1	Solderability	H.3.10.2	H.4.5.12.2	N/A	F and H ⁽⁵⁾	

Table H-17. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ Test coupon N shall be inspected when characteristic impedance is required.

⁽²⁾ Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the products is provided with SVH.

⁽³⁾ Test coupon M shall be inspected when the products is provided with BGA pads, etc.

⁽⁴⁾ Test coupon O shall be inspected when the sidewall plating is required.

⁽⁵⁾ Test coupons F and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

H.4.4.2 Quality Conformance Inspection (Group B)

H.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection are manufactured and selected from the lot which passed Group A inspection.

H.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table H-18. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

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		Inspection			Pass/fail	criteria
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
Ι	1	Plating adhesion and overhang	H.3.7	H.4.5.9	С	
П	1	Terminal pull strength	H.3.10.1	H.4.5.12.1	F	
	2	Connection resistance	H.3.9.3	H.4.5.11.3		
III	3	Hot oil resistance	H.3.11.3	H.4.5.13.3	D	
	4	Connection resistance	H.3.9.3	H.4.5.11.3		
	1	Circuitry	H.3.9.2	H.4.5.11.2		
	2	Connection resistance	H.3.9.3	H.4.5.11.3		0
IV	3	Thermal shock (II)	H.3.11.1.2	H.4.5.13.1b)	E and G ⁽¹⁾	
	4	Circuitry	H.3.9.2	H.4.5.11.2		
	5	Connection resistance	H.3.9.3	H.4.5.11.3		
V	1	Humidity and insulation resistance	H.3.11.2	H.4.5.13.2	Е	
v	2	Dielectric withstanding voltage	H.3.9.1	H.4.5.11.1		
VI	1	Peel strength of surface conductor	H.3.10.3	H.4.5.12.2	P ⁽²⁾	

Table H-18. Quality Conformance Inspection (Group B)

Notes:

⁽¹⁾ Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

⁽²⁾ Peel strength of surface conductor is performed when copper foil laminate structure is used. If copper foil laminate structure is in qualification coverage however, group B inspection is performed on a sample without this structure, the inspection shall be performed again on the first lot of the products with this structure.

H.4.5 Methods for Test and Inspection

H.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

H.4.5.2 Materials

The copper clad laminates, prepreg and copper foil shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.

H.4.5.3 Design and Construction

The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.

	(A-QTS-2140F) March 2023	J A X A Parts Specification	Page	– H-47 –
H.4.5.4 H.4.5.4.1		is, Marking and Others uctor, Base Material and Solder Re	esist	
	 a) Conductors For conductive can be used. Painstrument with b) Base Materials Pass or fail shated sufficient accurates c) Solder Resist 	Il be determined by using an optic	ical Inspection ma using an optical n al measuring inst	neasuring
H.4.5.4.2	 accuracy. a) Dimensions of The dimensions measured as for the largest area are the same s detailed measured by 1) Dimension on Each section measured by 2) Position accurace The direction measured with measuring in 3) Height from Each section measured by 4) Total board to For the total 	be measured by using a measuring BGA pads, etc. s of printed wiring boards with BGA pllows. For the board with multiple a shall be selected for measureme ize, any one of the pad shall be selected for measureme ize, any one of the pad shall be selected for measureme is a shall be selected for measureme if BGA pads and solder resist oper of grid corner (outer) of the center of grid corner (outer) of the center of an optical measuring instrument. uracy for BGA pads, etc. no of X and Y axes of circumference ith a 2-dimension end-measuring r astrument sufficient enough for me the base material for BGA pads, etc. of grid corner (outer) and the cent of the focal depth method using a methickness for BGA pads, etc. board thickness including solder con on shall be measured by using a methickness for BGA pads, etc.	A pads, etc. shall BGA pads, the B ent. If all the BGA elected for measu on Figure H-21. Thing diameter er area (inner) sha ce for BGA pads so machine or an eq easurement. etc. (pad thickness oter area (inner) so the allograph. coating and solde	be GA pad with pad areas rement. The all be shall be uivalent s) hall be

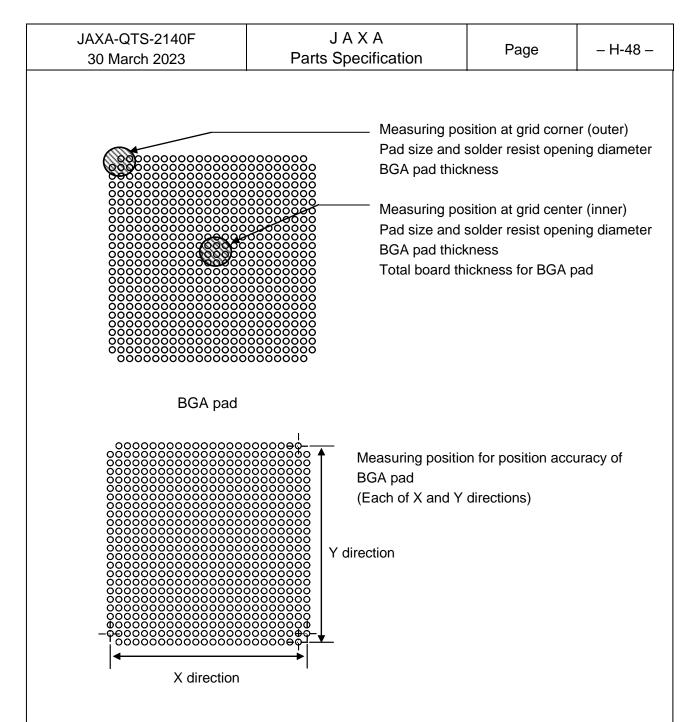


Figure H-21. Measuring Points for BGA Pad

5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure H-22)

	QTS-2140F arch 2023	J A X A Parts Specific	ation	Page	– H-49 –
	Directions of the part 1 2 3 4 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Direction 2	0 ⊢ ↓ Di	olumn 4th row 4th column 6th	
	Figure	e H-22. Measuring			,
H.4.5.4.3	Marking Marking shall be in:	spected visually (nak	ed eyed insp	pection).	
H.4.5.5 Si	center of a hole expose the cent inspected for ea may be prepare measurement of measured shall microsection sh any questionabl specimen. Pass Soft etching to o	ection ng board specimen s . The sample shall b ter of the hole. At lea ach work board. The ed outside of the effect f layer to layer registr be far from the startin all be inspected at a le results, the larger r s/fail shall be determin clarify the borderline of t the observation of in	e encapsula st three plat through hole tive product ation and ar ng point of d magnification nagnification ned at 100X of copper pla	ted in resin and p red-through holes as for the vertical area on the worl nular ring, the h rilling. The vertic n of 50 to 100X. n shall be used to magnification. ating and copper	oolished to shall be microsection board. For ole to be al If there are inspect the foil shall not

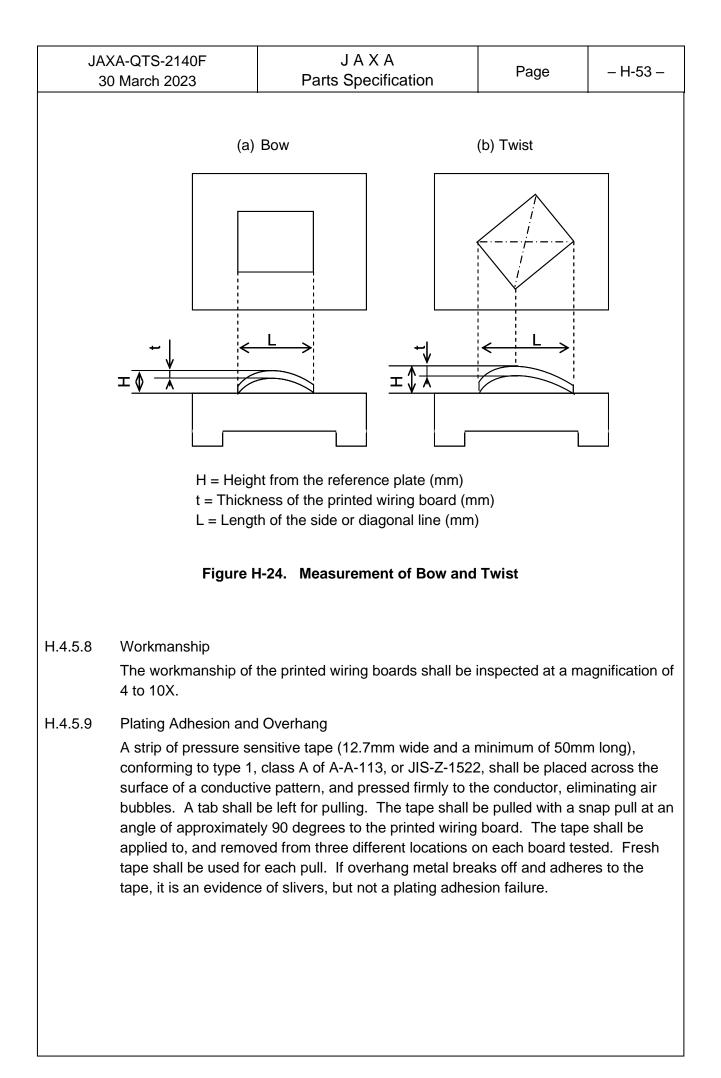
-	A-QTS-2140F March 2023	J A X A Parts Specification	Page	– H-50 –
	 b) Horizontal micro Multilayer board polished. A cor the conductor la horizontal direc are any questio the specimen. F 	·	the parallel directi hole (internal con hification of 50 to ation shall be used 00X magnification	on to expose nection in 100X. If there d to inspect
H.4.5.5.2	void at a magnifica	repared in paragraph H.4.5.5.1 a tion of 50 to 100X. If there are an a shall be used to inspect the spe (magnification.	y questionable res	sults, the
H.4.5.5.3	paragraph H.4.5.5. questionable result	bected for any lifting by using the r 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are an eused to inspect	ny
H.4.5.5.4	paragraph H.4.5.5. questionable result	Foil inspected for any crack by using 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are and an end of the second se	ny
H.4.5.5.5	paragraph H.4.5.5. questionable result	nection ection shall be inspected by using 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are and an end of the second se	ny
H.4.5.5.6	paragraphs H.4.5.5 thickness shall be t hole. If any of the n the value shall not	hall be inspected by using the mic 5.1 a) and b) at a magnification of he average value of three measu neasured value is significantly diff be used for calculating the average iss shall be measured at the thinn	200X as a minimi rements for a plat erent from the oth ge.	um. Plating ed through ner values,
H.4.5.5.7	paragraph H.4.5.5. questionable result	nspected for any crack by using t 1 a) at a magnification of 50 to 10 s, the larger magnification shall b I shall be determined at 100X ma	0X. If there are an e used to inspect	ny

	A-QTS-2140F March 2023	J A X A Parts Specification	Page	– H-51 –
H.4.5.5.8	delamination and b questionable result	Blister prepared in paragraph H.4.5.5. dister at a magnification of 50 s, the larger magnification sha I shall be determined at 100X	o 100X. If there are Il be used to inspect	any
H.4.5.5.9	prepared in paragr misregistration sha board length and th to-layer misregistra board in the directi	stration registration shall be measured aph H.4.5.5.1 a) at a magnifica Il be measured around the hol ne vertical direction. The micro ation shall be prepared by cutti on parallel to the board length r another one hole as a minim	ation of 25 to 100X. e in the direction par sections for inspecti ng the multi-layer pri for at least one hole	The allel to the on of layer- nted wiring and the
H.4.5.5.10	paragraph H.4.5.5. annular ring on an outer edge of the a annular ring on an	nall be measured by using the 1 a) at a magnification of 25 to external layer shall be from the nnular ring on the surface of the internal layer shall be measure the edge of the land (see Figu	100X. The measure surface of the plate the printed wiring boated by the distance from	ement of the ed hole to the ird. The
		Maximum misregistration		
		pos cale dist righ	th land shall be meas ition of the center sha culated. The misregis ance from the center tmost land to the cen nost land.	all be tration is the of the
		Measuring annu	lar ring on an interna	l layer
	easuring annular ring			
Figur	e H-23. Measuremo	ent of Layer-to-Layer Misreg	stration and Annul	ar Ring
H.4.5.5.11		nickness nickness shall be measured by .5.1 a) at a magnification of 50	-	ion prepared

Т

Т

_	A-QTS-2140F March 2023	J A X A Parts Specification	Page	– H-52 –
H.4.5.5.12	-	lating and Filled Resin ating and filled resin shall be obse	rved and measur	ed by using
	the microsection pr 100X. If there are	repared in paragraph H.4.5.5.1 a) any questionable results, the large imen. Pass/fail shall be determine	at a magnification	n of 50 to hall be used
H.4.5.5.13	•	of Cap Plating of cap plating shall be observed ar rred in paragraph H.4.5.5.1 a) at a	•	•
H.4.5.5.14		e observed and measured by using .5.1 a) at a magnification of 25 to s	-	n prepared
H.4.5.6	Solder Resist Thickne	ess		
	polished to expose th	cut vertically near the conductor a e center of the conductor. The sol fication of 200X as a minimum.	•	
H.4.5.7	Bow and Twist			
	with its convex side fa the highest point of th The bow and twist sh The percent bow and	ard specimen shall be placed horizacing upward, and the distance be ne printed wiring board shall be me all be calculated as follows. twist shall be calculated by the for wist = $\frac{H-t}{L} \times 100$ (%)	tween the references the reference the refer	nce plate and



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H.4.5.10 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 % by volume of isopropyl alcohol and 25 % by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6\Omega$ ·cm. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table H-19 may be used to perform the cleanliness test.

Method	Resistivity (×10 ⁶ Ω·cm)	Equivalent factor	Equivalents of sodium chloride (µg/cm²)
Conductivity bridge	2	1	1.56
Omega Meter ⁽¹⁾	2	1.39	2.2

 Table H-19.
 Equivalent Measuring Method

Note: ⁽¹⁾ Alpha Metals Incorporated, "Omega Meter"

H.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

H.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
- b) Duration: 30 seconds
- c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

H.4.5.11.2 Circuitry

a) Continuity

A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity

b) Circuit shorts

A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

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30 1		Faits Specification		
H.4.5.11.3	Connection Resista	ance		
	The resistance bet	ween the through hole terminals s	hall be measured	l by using a
	-	ent of four-terminal method capab	le of measuring a	resistance
	below 0.5 mΩ.			
H.4.5.11.4	Characteristic Impe	edance		
		mpedance shall be measured in a	accordance with F	Paragraph
	2.5.5.7 of IPC-TM-	650.		
H.4.5.12 N	Mechanical Performa	nce		
٦	The mechanical perfo	ormance tests shall be performed	as follows.	
H.4.5.12.1	Terminal Pull Strer	ath		
		be cut with a sharp knife at a minir	num of 6mm from	the land.
		toward the land, and shall be cut of		
	at the joining point	of the conductor and land without	degrading the lar	nd
	•	n. Then, a lead wire sufficient in le	•	•
		rted in the hole and soldered. Aft lering by using a soldering iron sh	•	solder
	Terrioval and Tesoic	iening by using a soluening non sh	all be performed.	
	a) A lead wire sha	Il be soldered in to the through ho	ole.	
	,	hall be removed from the through	,	oval).
	,	Ill be resoldered in to the through		
	,	hall be removed from the through Il be resoldered in to the through	,	oval).
	c) /c			
	•	ad shall not be clinched. The lead		
		he solder removal and replaced v		
	•	oldering iron shall be used at 15 t perature of 232 to 260°C. The le	•	
	• •	bringing its tip into contact with th		•
		heating time shall be limited to the		•
	completion of e) re	soldering, the lead wire shall be ir	nstalled on a tensi	le tester at
	•	and be pulled at the rate of 50mm	•	
		and until the pull strength reaches		
		aking off or pulling out the lead wi ead wire shall be soldered and pu		-
		e following formula.		onger onen
	$L \ge 1380 \times \frac{\pi \left\{ \left(d_2 \right)^2 - 4 \right\}}{4}$	$(\mathbf{d}_1)^2$		
	L = Pull strength (N)		
	$d_1 =$ Hole diameter			
	d_2 = Land diameter	(cm)		

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H.4.5.12.2	The peel strength of Paragraph 2.4.8 of a) Normal state Test condition of b) After Thermal s	of surface conductor is performed FIPC-TM-650 and as follows. A shall be applied.	in accordance wi	th
H.4.5.12.3	 a) Hole solderabil The wetting of s to the inspectio b) Surface soldera After the specir STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. Th 25±6mm per se vertical state in 	solder shall be inspected using a m n specified in paragraph H.4.5.5.1 ability and sidewall plating men is dipped into the flux specifier ux shall be drained for 60 seconds 08 of MIL-STD-202 shall be melted steel paddle. It shall be confirmed 226 and 238°C. The solder slug a he molten solder surface immedia e specimen shall be put vertically i econd, kept in the bath for 4±0.5 se econd. After the pull-up, the specin the air, until the solder is solidified condition of solder on the conduct	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp into the solder ba econds and raise men shall be kep d. No quick coolir	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of d at a rate of t in the ng shall be
H.4.5.13	Environmental Perfor The environmental perfor	mance erformance tests shall be performe	ed as follows.	
H.4.5.13.1	MIL-STD-202. The a) Thermal shock The test shall b temperature sh time for step 2 heating process as a pre-treatm follows. 1) Heating cond	test shall be performed in accordate following conditions shall apply. (I) (applicable to qualification test) be performed under the test conditi all be -30°C and the number of cycl and 4 shall be within 2 minutes ear is in accordance with JERG-0-043 bent of the printed wiring board. The dition: 200°C min. for 45 seconds reature: 230°C min.	on B. However, t cle shall be 1000 ch. Reflow solde shall be performe e heating conditio	he lowest cycles. The ring of total ed three times
	b) Thermal shock	(II) (applicable to quality conformation	ance inspection)	

			r	
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		be performed under the test condi tep 2 and 4 shall be within 2 minut	•	o +125°C).
H.4.5.13.2	cycles, and the during the test. be taken out of evaluated. b) Insulation resis The test shall b	ance s in Test Method 106 of MIL-STD- polarization voltage of 100V±10V Upon completion of step 6 of the the bath and dried immediately by	bc shall be applie final cycle, the sp blowing air at 25 be test condition E	d to all layers becimen shall 5±5°C and 3, Test
H.4.5.13.3	temperature. After	I be dried at 120±5°C for 2 hours a that, the specimen shall be imme cooled to room temperature. This	rsed in oil or wax	at 260±5°C
H.4.5.13.4	shall be placed on specimen shall the floated in a solder l period of 10 secon cooled. After a che inspected for the st accordance with H depth not to excee Evaluation specime H.3.4.4.12) shall be	Il be dried for 2 hours at 121 to 149 a ceramic plate in a desiccator, and n be fluxed in accordance with the bath of composition Sn 63±5 % ma ds. The specimen shall be placed eck for any defects on the external tructural integrity using the microse .4.5.5.1. Solder temperature shall d 50mm from the molten surface of en of Adhesion of cap plating and the e floated in a solder bath for a peri- and cooling shall be performed th	nd cooled down. a detail specificati aintained at 288± on a piece of ins surface, the sam ection prepared in be measured at of the solder. filled resin (paragon)	The on and 5°C for a sulator to be pple shall be n a probe
H.4.5.13.5	0.5×10 ⁴ Gy to 1×10 amounts to 1×10 ⁴ G visually to verify the tests of dielectric w performed in accor respectively. The i	s adiation shall be performed by usir ⁴ Gy per hour to the specimen in op Gy. After the irradiation, the specin at there is no degradation in any p vithstanding voltage and insulation dance with paragraphs H.4.5.11.1 nsulation resistance shall be meas thstanding voltage test.	pen air, until the t nen shall be insp art of the specim resistance shall and H.4.5.13.2 b	otal dose ected en. The be o),

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		APPENDIX J		
		PRINTED WIRING BOARDS,		
		HIGH HEAT RADIATION		
J.1. Genera	I			L-1
	•			
J.1.3.1	Base Materia	al Code		J-3
J.1.3.2	Number of L	ayers		J-3
J.2. Applical		s etc		
		ments		
		ments		
J.3. Require	ments			J-4
J.3.1 Qu	alification Cov	erage		J-4
J.3.2 Ma	terials	-		J-4
J.3.2.1	Copper-Clac	Laminate, Prepreg and Copper fo	oil	J-5
J.3.2.2	High Therma	al Conductive Materials for Build-u	p Layers (Type II	I Printed
	Wiring Board	ds only)		J-5
J.3.2.3	Via Hole Filli	ng Materials (Filling Resin)		J-5
J.3.2.4	Solder Resis	st Ink		J-6
J.3.2.5	Marking Ink.			J-6
J.3.2.6	Plating			J-6
J.3.2.7	Copper Inlay	/		J-7
J.3.3 De	sign and Cons	struction		J-7
J.3.3.1		ng Drawings and Artwork Master (•	
J.3.3.2		or Printed Wiring Boards		
J.3.3.3		onnection		
J.3.3.4	-	Method for Area Array Packaging		
J.3.3.5		er (Type III Printed Wiring Boards		
J.3.3.6		e Diameter	• •	
J.3.3.7	Ų	II Printed Wiring Boards Only)		
J.3.3.8		/ Embedding		
J.3.3.9	••••••	for Through Hole		
J.3.3.10	•	Vidth and Thickness		
J.3.3.11		pacing		
J.3.3.12		ter		
J.3.3.13		A, etc		
J.3.3.14		er Clearance		
J.3.3.15	•	f Through Holes with Embedded C		
J.3.3.16		sh Plating	•••••	
J.3.3.17		st		
J.J.J.J.T/				
J.3.3.17 J.3.3.18	Sideplating of	on Outer Perimeter of the Board		J-19

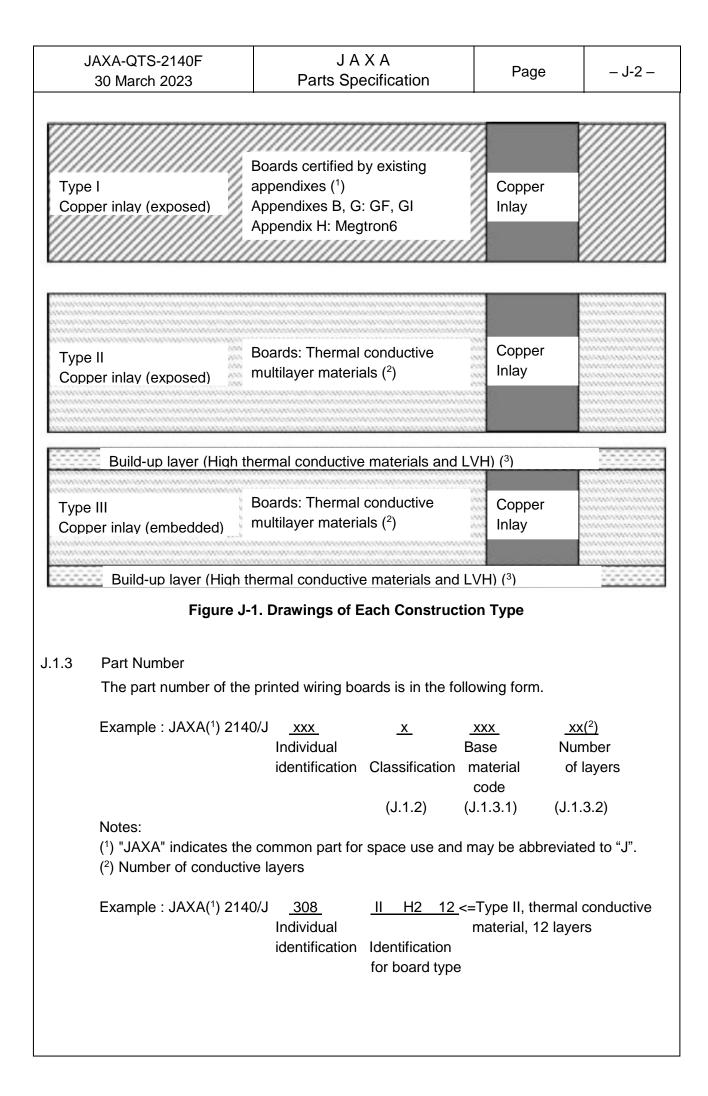
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J.3.3.20	Operating To	emperature Range		J-1
J.3.4 Ext	ternals, Dimer	sions, Marking and Others		J-2
J.3.4.1	Externals of	Conductor, Base Material, Solde	r Resist and Cop	per Inlay
				J-2
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

30 Ma J.1. Genera J.1.1 Scop	QTS-2140F arch 2023 al	J A X A Parts Specification APPENDIX J PRINTED WIRING BOARDS, HIGH HEAT RADIATION	Page	— J-1 —
J.1.1 Scor	al	PRINTED WIRING BOARDS,		
J.1.1 Scor	al	-		
J.1.1 Scor	al			
•				
This	pe			
as "p radia	isions for the printe printed wiring board ation and can radiat	es the general requirements and o d wiring boards, high heat radiatic s"), that applies constructions and e heat by heat conduction from m ostrates defined in other appendix	on (hereinafter ref I materials with hi ounted compone	erred to igh heat
J.1.2 Clas	sification			
cons Base	struction is shown in	wiring boards is shown in Table J Figure J-1. inlay embedding and laminating p	-	
	Table J-1	. Classification of Printed Wiring I	Boards	
Classificatio		Construction		
Туре І	Copper inlay (exposed) / boards (Appendix B, H	, etc.) (¹)	
Type II	Copper inlay (exposed) / boards (Thermal condu	uctive multilayer r	naterials) (²)
Type III		embedded) / boards (Thermal cor ayer (High thermal conductive mat	-	-
(²): The multi (³): Higl only	ilayer materials.		mal conductivity t	han normal



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J.1.3.1	Base Material Code The base material co	de is as specified in Table J-2.		
	1	Table J-2. Base Material Code		
Base material code Insulation board material				
GF		Glass base woven epoxy resin, con JPCA/NASDA-SCL		3

J.1.3.2	Number of Layers
0.1.0.2	Trainbor of Eayord

GI

102

H1

H2

The maximum number of layers of printed wiring boards shall be specified for each classification in detail specification.

Glass base woven polyimide resin, compliant to IPC-

4101, JPCA/NASDA-SCL-01

Glass base woven modified polyphenylene ether resin,

compliant to IPC-4101/102

Thermal conductive materials (less than $1W/m \cdot K$)

Thermal conductive materials (1W/m · K or more)

For type III printed wiring boards, build-up layer, core layer, and the maximum number of layers for each of these types shall be specified in detail specification.

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	30 March 2023	Parts Specification	Tage	- 5-4 -	
J.2.	Applicable Documents et	с.			
J.2.1	Applicable Documents				
J.Z. I	Applicable Documents The applicable documents shall be as follows and as specified in paragraph 2.1 of				
	this specification. a) JERG-0-043 Standards for Surface Mount Soldering Process in Space Application				
	b) JIS C 6481 Test methods of copper-clad laminates for printed wiring boards c) IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design				
	d) IPC-TM-650 Te	st Methods Manual			
J.2.2	Reference Documents				
	this specification. a) JERG-0-054 Sta in 5 b) JIS C 6012 Qu	nts shall be as follows and as spec andards for BGA/CGA Soldering Pr Space Application alification and Performance Specif ards	rocess		
J.3.	Requirements				
J.3.1	Qualification Coverage				
	Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs J.3.2 through J.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test.				
	Qualification tests shall be conducted for each classification. Products with fewer total layers and less thickness than the qualified sample units are considered qualified.				
	using samples with sole be represented by sam qualification coverage r plating. Only solder res	solder coating types, qualification der coating or ENEPIGEG. The qualification ples that have passed the qualification may include electrolytic nickel platin sist inks used for qualification tests qualification coverage shall be spe	ualification covera ation tests and the ng and electrolytic are considered o	age shall e c gold qualified.	
J.3.2	materials for type I prin appendixes, except for	II and III printed wiring boards sha ted wiring boards shall be in accord copper inlay. ed in the detail specification.			

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			-

J.3.2.1 Copper-Clad Laminate, Prepreg and Copper foil

The copper-clad laminate, prepreg and copper foil laminated to prepreg, which are specified in paragraph J.2.1, shall be as specified in the drawing. The nominal thickness of the base material shall be no less than 0.05mm. The thickness of the copper foil shall be as specified in Table J-3 and the type of copper foil shall be specified in the detail specification. (¹)

		Unit: µm
Layer	Classification	Copper foil thickness
	With SVH and LVH	9 minimum
External layer	Without SVH and LVH	18 minimum
	With SVH, IVH and LVH	9 minimum
Internal layer	Without SVH, IVH and LVH	18 minimum

Table J-3. Thickness of Copper Foil (Nominal)

Note (¹): The standards required to materials used in the printed wiring boards shall be specified in the detail specification. The detailed information about base materials (such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the Application Data Sheet (hereinafter referred to as "ADS").

J.3.2.2 High Thermal Conductive Materials for Build-up Layers (Type III Printed Wiring Boards only)

High thermal conductive materials for build-up layers shall be as specified in the drawing.

The copper foil laminated to prepreg on the outermost layer shall be as specified in the drawing.

Thermal conductivity of high thermal conductive materials for build-up layers shall be equal to or more than $1W/m \cdot K$. The detailed information about base materials (such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the ADS.

For directional data, in-plane and out-of-plane directions shall be shown separately. Details shall be specified in the ADS.

J.3.2.3 Via Hole Filling Materials (Filling Resin)

The filling materials for SVH, IVH and small through hole shall be resin. The filling materials for LVH shall be resin or copper-plating.

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J.3.2.4						
	The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent. Thermal conductivity of solder resist shall be specified in the ADS.					
J.3.2.5	Marking Ink The marking shall be conducted using ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or					
	reliability of the printe	d wiring boards.				
J.3.2.6	Plating Electroless and electrolytic copper plating shall be applied to all through holes, LVH and for cap plating. Solder coating or ENEPIGEG plating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.					
J.3.2.6.1	Electroless Copper Plating The electroless copper plating shall be applied as a preceding process of electrolytic copper plating to form a conductive layer over the insulating material.					
J.3.2.6.2	Electrolytic Copper Plating The electrolytic copper plating shall have a minimum purity of 99.5 %.					
J.3.2.6.3	Electrolytic Gold Pl	ating				
	The electrolytic cold r lating The electrolytic gold plating shall be as specified in Table J-4. The electrolytic nickel plating specified in paragraph J.3.2.6.4 shall be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 % except for the metal added to increase the hardness.					
	Table J-4. Electrolytic Gold Plating					
	Item Specification					
	Purity	Min. 99.	7 %			
	KNOOP hard	ness 91 to 129 (in	clusive)			
J.3.2.6.4 Electrolytic Nickel Plating The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent.						

J.3.2.6.5 Solder Coating

The solder used for solder coating shall contain 50 to 70 % tin.

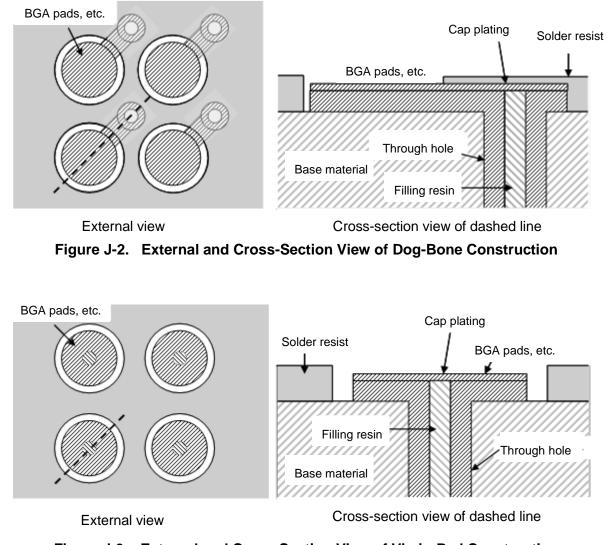
JAXA-QTS-2140F 30 March 2023		J A X A Parts Specification	Page	– J-7 –		
	J.3.2.6.6 ENEPIGEG (Electroless Nickel / Electroless Palladium / Immersion Gold / Electroless Gold)					
For ENEPIGEG plating, electroless nickel plating is applied as an undercoat on the copper circuit, electroless palladium plating is applied on the undercoat, and then electroless gold plating is applied on the electroless palladium plating. (1)						
	Note (¹): Thick palladium / gold plating may cause cracks due to the effects of IMC (intermetallic compound) layer or solidification shrinkage process when mounting insert components or components with large thermal capacities (citing from JERG-1-009).					
J.3.2.7	Copper Inlay					
	99% or more). Detail	s for high heat radiation shall be p s of the copper inlay (standards a be specified in the ADS.	•••	-		
J.3.3	Design and Constructio	n				
	Design and construction for types I, II and III printed wiring boards shall be as follows. Design and construction for type I printed wiring boards shall be in accordance with the applicable appendixes, except for copper inlay embedding.					
J.3.3.1	Manufacturing Drawir	ngs and Artwork Master (or Origina	al Production Ma	ster)		
	this paragraph.	gs of printed wiring boards shall b				
	shall be approved by	awings and artwork masters (or o the purchaser. In the event of cor	nflict between the	,		
	•	gs and artwork masters (or origina gs shall take precedence.	al production mas	sters), the		
J.3.3.2	Connector for Printed	Wiring Boards				
	A direct connector (ca	ard edge connector) shall not be u	sed for printed wi	iring boards.		
J.3.3.3	boards shall be provid through holes includir	conductive patterns in different lay ded by LVH, small via holes, IVH, ng copper inlay are used for signal ed use of the through holes shall b	SVH or through h and other condu	noles. When		

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J.3.3.4	Connection Method f	or Area Array Packaging Pads		

The connection method for contact pads of area array packages such as BGA pads (hereinafter referred to as "BGA pads, etc.") shall be made by Dog-Bone construction or Via-in-Pad (hereinafter referred to as "VIP") construction.

Dog-Bone construction is to connect small via hole by drawing the circuit out of the contact pads such as BGA pads as shown in Figure J-2. The small via hole shall be filled with resin and closed by plating (cap plating). LVH shall be filled with copper plating or filled with resin and closed by cap plating.

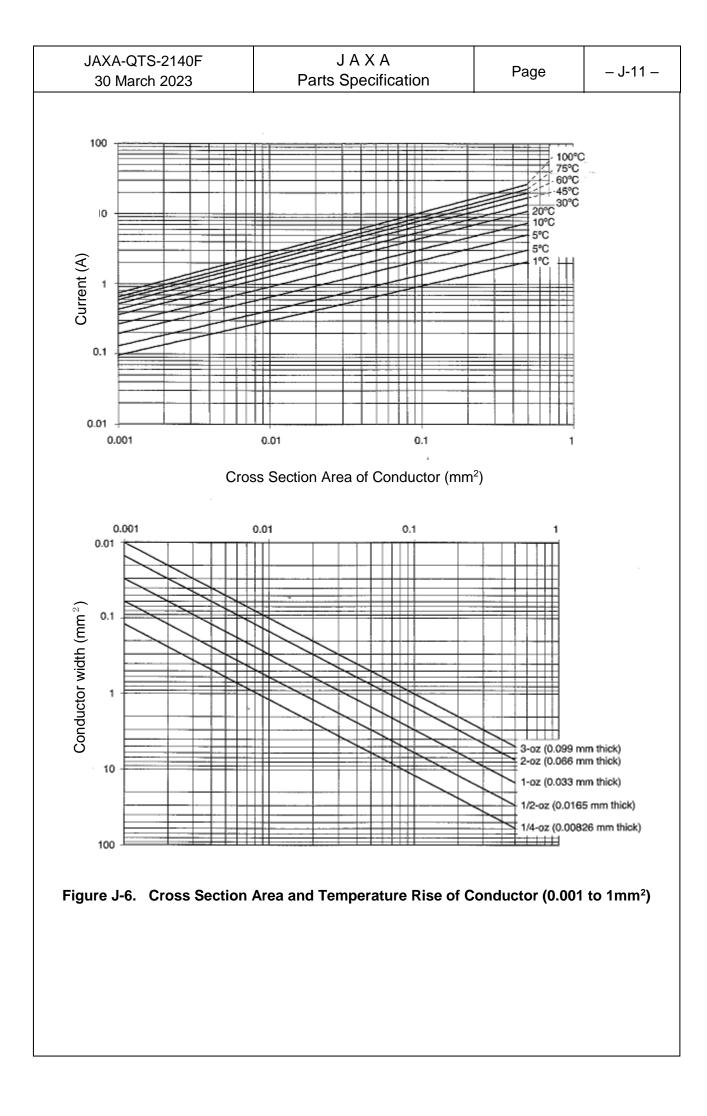
VIP construction is the construction where cap plating as BGA pad is directly on top of the LVH filled with copper plating or resin and closed by cap plating, or SVH or small via hole filled with resin and closed by cap plating as shown in Figure J-3.

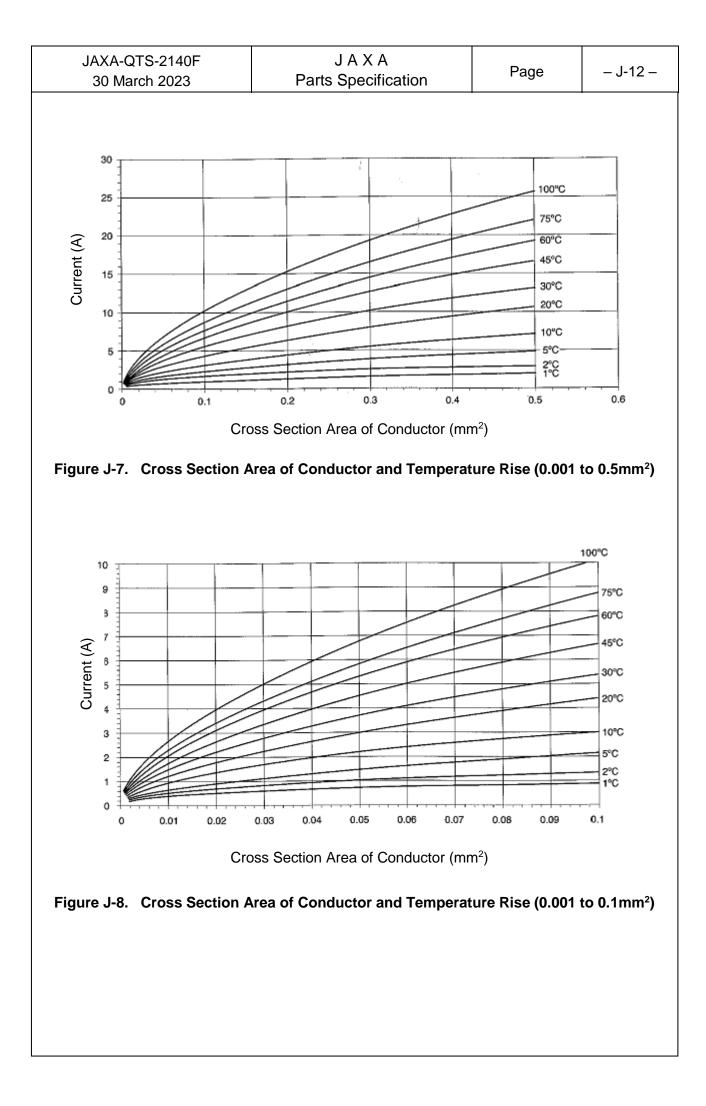


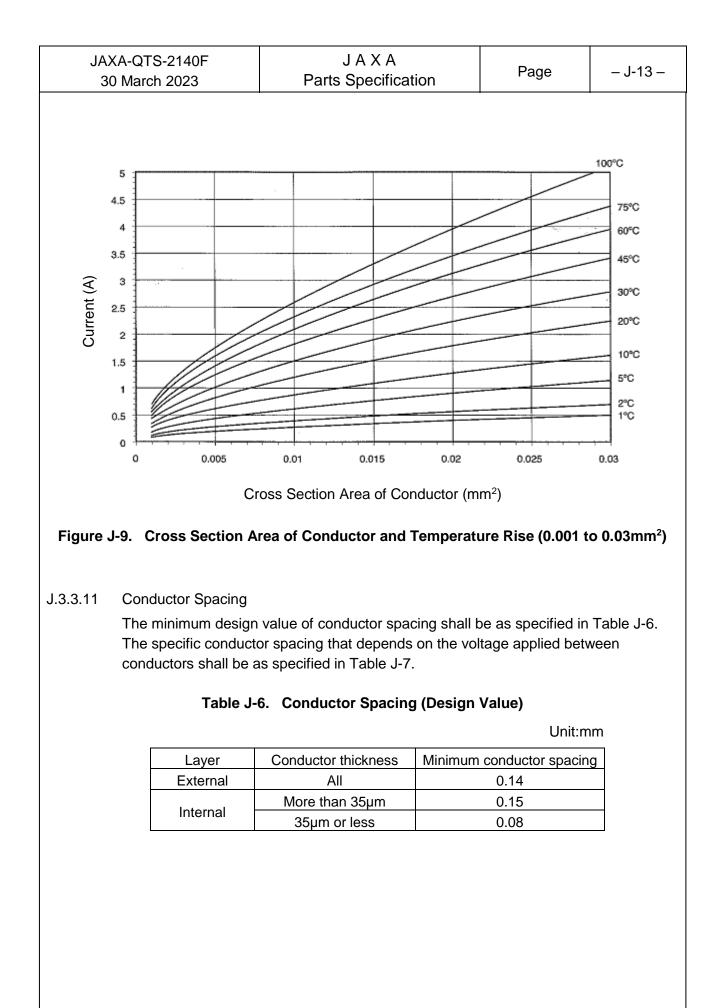


-	XA-QTS-2140F 0 March 2023	J A X A Parts Specification	Page	– J-9 –
J.3.3.5	The number of build- shall be identical. Connection between		hrough staggered	d via or
Stage	-	Stacked Via Co Stacked Construction	The Via Construct	ion
J.3.3.6		ameter for small via hole, IVH and inds of via hole are used as BGA	•	
J.3.3.7	without taper construction conformal mask) shall construction.	Wiring Boards Only) ameter Y for LVH shall be φ0.15m ction and laser processing method I be specified in the detail specific er is specified in paragraph J.3.3.	l (such as direct l ation for a detail	aser and

J.3.3.8	Figure J-5. Cro				
J.3.3.8	-	ss-Section View of LVH	I (Stacked C	Construction)	
J.3.3.8					
		copper inlay is embedded le shapes of the copper	•		•
J.3.3.9	Filling Resin for Thro	ough Hole			
	The small via hole to filled with via filling m	be filled with via filling n naterials shall be specifie SVH and LVH applied to	ed in the man	ufacturing drav	wing.
J.3.3.10	J.3.3.10 Conductor Width and Thickness The minimum design value for conductor width shall be as specified in Table J-5. The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor. Figures J-6, J-7, J-8, and J-9 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this shall apply to conductors on both internal and external layers under vacuum and space environmental conditions. When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.				
	Table .	J-5. Conductor Width	(Design Val	ue)	
				Unit:mm	
	Layer	Conductor thickness		onductor width	
	External Internal	All More than 35µm	0	0.10	
		35µm or less	0	.07	







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Table J-7. Conductor Spacing for Printed Wiring Boards

Voltage applied between	Minimum conductor spacing		
conductors, DC or AC_{p-p} (V)	External layer	Internal layer	
0 to 50	0.14	0.08	
51 to 100	0.14	0.10	
101 - 300	0.40	0.20	
301 - 500	0.80	0.25	
501 or higher	(0.003xV)	(0.0025xV)	

J.3.3.12 Land Diameter

The minimum design value of land diameter shall be as specified in Table J-8 (see Figure J-10). Non-functional land (¹) may not be provided when required to maintain conductor spacing and electrical characteristics.

For through holes with embedded copper inlay, presence/absence of non-functional land shall be specified in the detail specification.

Table J-8. Land Diameter

Unit: mm

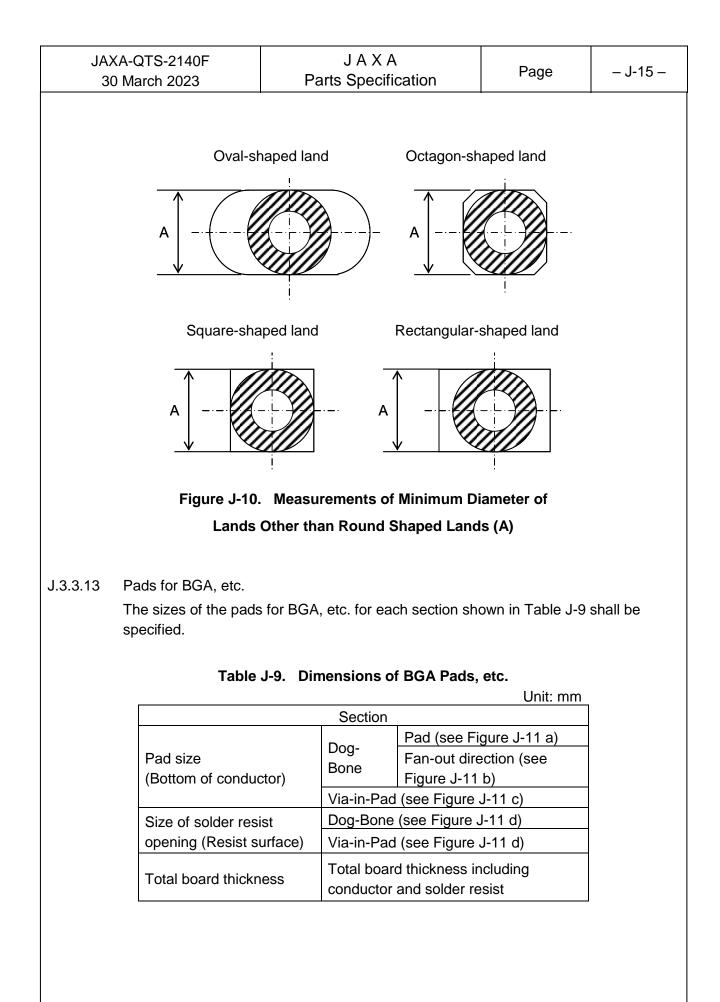
Unit: mm

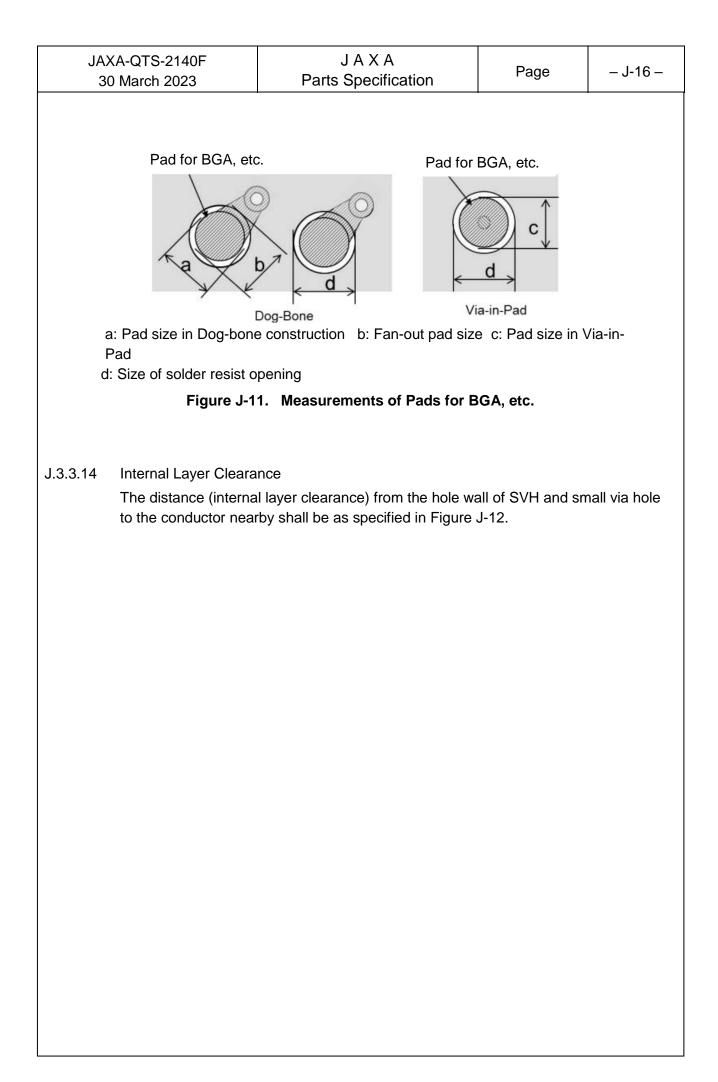
	Ont. Initi	
Hole	Minimum land diameter(2)	
SVH and small via holes	ϕ (Drill diameter + 0.25)	
LVH	Detail specification	
Through holes with embedded copper inlay	Detail specification	
Through holes other than the above	ϕ (Finished hole diameter + 0.5)	
Non-plated through holes	ϕ (Drill diameter + 1.1)	

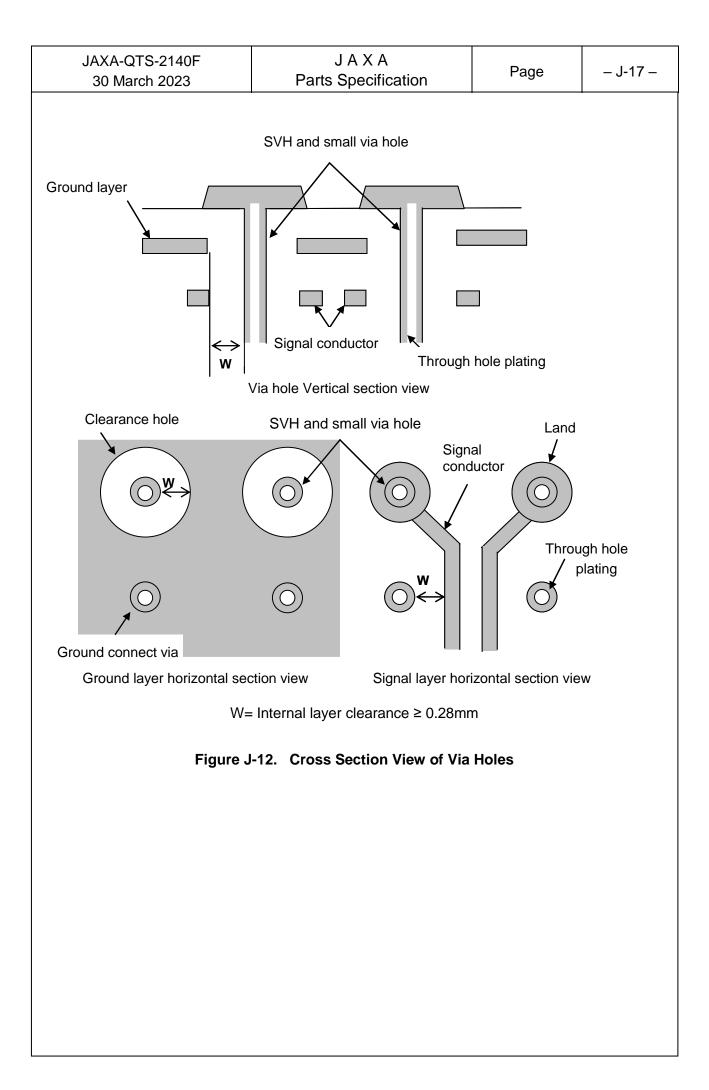
Notes:

(¹) Non-functional land (or inner layer unconnected land) is the land without inner layer connection.

(²) The minimum diameter of lands other than round shaped lands shall be the measure of the length "A" shown in Figure J-10.







-	XA-QTS-2140F 0 March 2023	J A X A Parts Specification	Page	– J-18 –
3(J.3.3.15	Clearance of Through The distances from the the conductor nearby (Figure J-13 b), to the inlay (Figure J-13 c) a be as shown in Figure specification. When these distances these distances for th a: Distance between nearby b: Distance between hole nearby c: Distance between I the another through h	h Holes with Embedded Copper In the hole wall of the through holes w (Figure J-13 a), to the hole wall of the hole wall of the another through and to the edge of the printed wirin the J-13 and these distances shall be s are affected by the size of copper the size of copper inlay shall be spec- hole wall of the through holes with hole wall of the through holes with	lay vith embedded co of the through hole holes with embed og boards (Figure be specified in the er inlay, worst cas ecified. In copper inlay and in copper inlay and in copper inlay and	pper inlay to e nearby Ided copper J-13 d) shall detail se values of conductor through hole wall of
		Copper Inlay		
	Figure J-13. C	ross Section View of Through H	loles in which	
		Copper Inlay is Press-fitted		
J.3.3.16	manufacturing drawin plating shall be applie used for the surface f	surface finish plating and solder can g shall be in accordance with Tab ed as an undercoat of electrolytic g inish. If more strict requirements t sary, consult with manufacturer a	ble J-10. The elec gold plating, and s han the ones spe	trolytic Nickel shall not be

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Table J-10. Thickness of Surface Finish Plating

Unit: µm

Plating material	Surface plating thickness		
Electrolytic gold	1.3 to 4.0		
Electrolytic nickel	Electrolytic nickel 5 as a minimum		
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (J.3.10.2).		
ENEPIGEG(Electroless	EN: Electroless nickel plating (1)	3.00 to 8.00	
Nickel / Electroless	EP: Electroless palladium plating (1)	0.05 to 0.20	
Palladium / Immersion Gold / Electroless Gold)	IG+EG: Immersion gold and electroless gold plating (1)	0.10 to 0.40	

Note (¹): Shall conform to drawings and other specifications. Unless otherwise specified, this table shall apply.

J.3.3.17 Solder Resist

The solder resist application shall be specified except for the land, pads (incl. Via-in-Pad), and the small via holes without resin filling.

The lands of small via hole and SVH in the dog-bone construction shall be coated with solder resist.

Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.

The minimum distance from the edge of the board to the solder resist shall be 0.3mm. Solder resist is basically not applied to the through holes with copper inlay due to thermal design requirements, however solder resist may be formed as necessary for parts mounting and other applications.

J.3.3.18 Sideplating on Outer Perimeter of the Board

The sideplating on outer perimeter of the board (hereinafter referred to as "Sideplating") shall be specified in the manufacturing drawing if applied. The detailed design of the sideplating shall be specified in detail specification.

J.3.3.19 Characteristic Impedance

The characteristic impedance of the printed wiring boards shall be specified in the manufacturing drawing if applied.

J.3.3.20 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph J.3.11.1.2) and within -65 to +125°C.

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- J.3.4 Externals, Dimensions, Marking and Others
- J.3.4.1 Externals of Conductor, Base Material, Solder Resist and Copper Inlay

J.3.4.1.1 Conductor

a) Conductive pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor

The conductors including sideplating shall contain no tears, cracks, lifting, or separation. Any combination of edge roughness, nicks, pinholes or scratches exposing the insulation board shall not reduce the conductor width to less than 80 % of the minimum finished conductor width. The length of any defect shall not exceed the conductor width (design width of the conductor). The number of defects exceeding 0.05mm in width shall not be more than one per conductor or per unit area of 100×100 mm on the printed wiring boards. The roughness at vertical conductor edges shall meet the conductor width tolerance (see Figure J-14).

The tolerances of conductor width and conductor spacing shall be as specified in Table J-11.

The nicks and pinholes on the ground surface and power supply surface shall not exceed 1.0mm in the maximum length and 4 pieces per 625cm² in number.

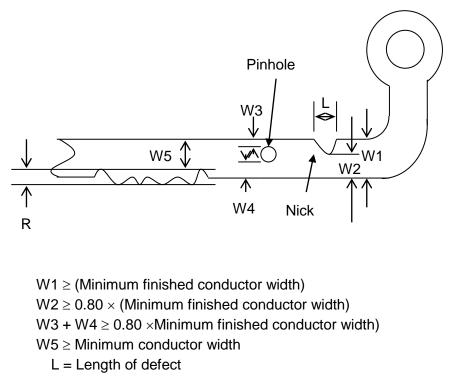


Figure J-14. Acceptance Criteria for Conductor Defects

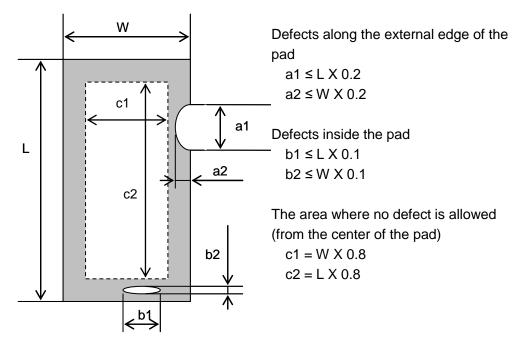
Table J-11.	Tolerance of Conductor Width and Conductor Spacing
-------------	--

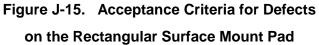
		Unit: mm
Dimension		Tolerance
	0.07 to less than 0.13	+0.05
Conductor		-0.03
Conductor	0.13 to less than 0.20	±0.05
width	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
	Less than 0.10	0.05 as a minimum
Conductor	0.10 to less than 0.14	0.06 as a minimum
Conductor	0.14 or more	0.10 as a minimum
spacing	The positive side tolerance is not specified for all design	
	value.	

c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure J-15).

The pad length and width shall be based on the design value.





The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the ENEPIGEG plating pad section and terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

 f) Between conductors
 The surface of a insulation plate between conductors shall be free from adhesion of any residual conductor or foreign inclusion.

g) Solder coating

The solder coating shall be free from pinholes or pits, and completely cover conductors. However, the copper exposure on sideplating side is permitted.

- h) Electrolytic nickel and electrolytic gold plating
 The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductors surfaces. However, the copper exposure on the conductor side is permitted.

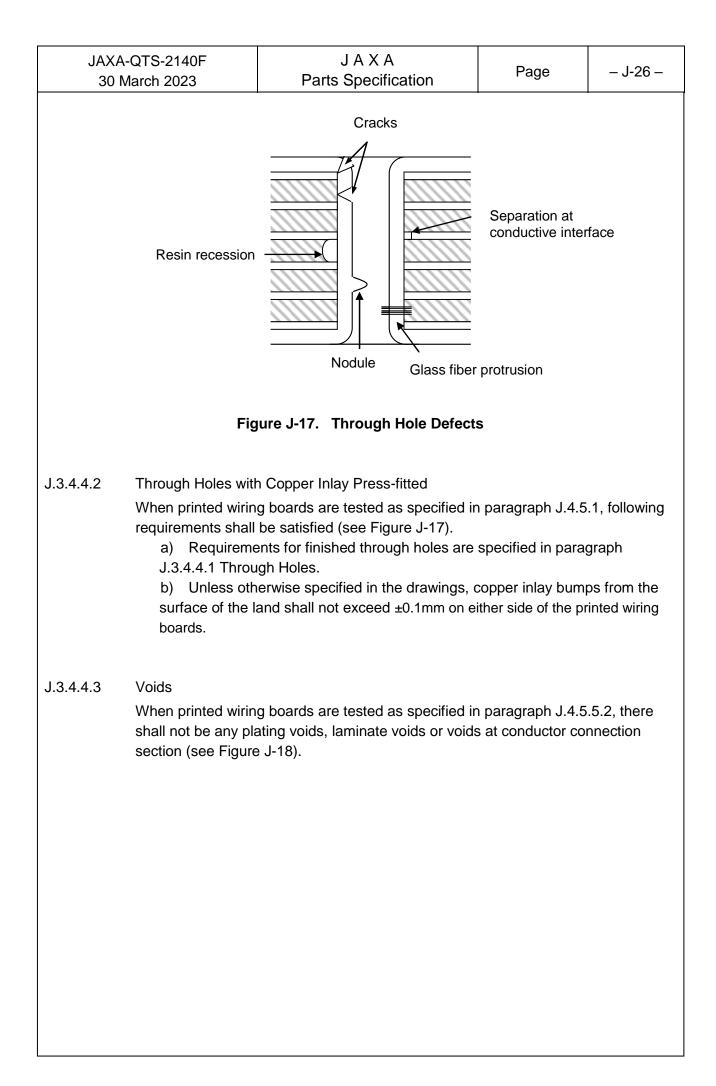
ENEPIGEG shall be free from pinholes or pits, and completely cover conductor surfaces.

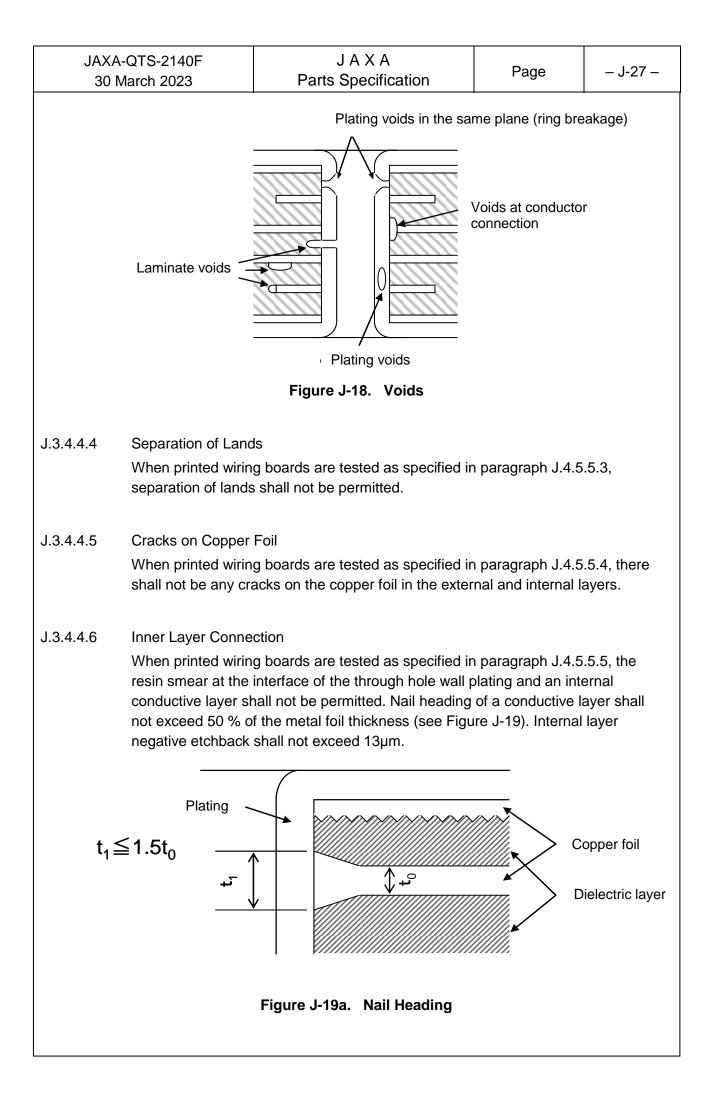
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J.3.4.1.2	Base Materials			•
	Printed wiring b This provision s Crazing and ha when the spacin equal to or great or 1.6mm, whic b) Surface of print The surface of p Each layer and	d wiring board and non-plated thro boards shall not exhibit nicks, crack shall not apply to separate parts of loing along the edges of printed w ng between the crazing or haloing ater than the minimum conductor s hever is smaller. ted wiring boards printed wiring boards shall not exhibit base material shall not exhibit del eath the surface of the board shall	ks or separation a a split board. riring board shall l and an adjacent spacing specified hibit separation ar lamination. Meas	be permitted, conductor is on drawings round holes. sling and
J.3.4.1.3	 b) Significant visu surface, unever c) Unless otherwis provided that th d) The solder resis e) The application patterns shall m f) Unless otherwis shall not be exp 	er resist shall be free from tackine al damage such as a thin spot, se in color and exposed residual cond se specified, scratches and pinhole be conductors are covered with sol st shall not encroach onto lands for in range and misalignment of solder neet the provisions of manufacturing se specified on the manufacturing bosed in the solder resist opening the construction, solder resist shall of and SVH.	paration, roughne luctor shall not be es shall be accep lder resist. or mounting parts r resist and condu- ng drawings. drawings, adjace area.	ess on the e permitted. otable, uctive ent conductor
J.3.4.1.4 a) b) c)	requirements specific Edge of the copper in the copper inlay. Surface of the copper protrudes from the s copper does not pro of the area of the co	f copper inlay shall be acceptable, ied in paragraph J.3.4.2. inlay shall be free from burrs that p er inlay shall be free from scratche surface of the copper inlay. Area o trude from the surface of the copp pper inlay and depths of the scrate ied in paragraph J.3.4.2.	protrude from the es and dents such of the scratches a per inlay shall not	surface of that copper and dents that exceed 5%
	manufacturing drawin	ach part of the printed wiring board ngs. Unless otherwise specified, d e requirements specified in Table	limensional tolera	

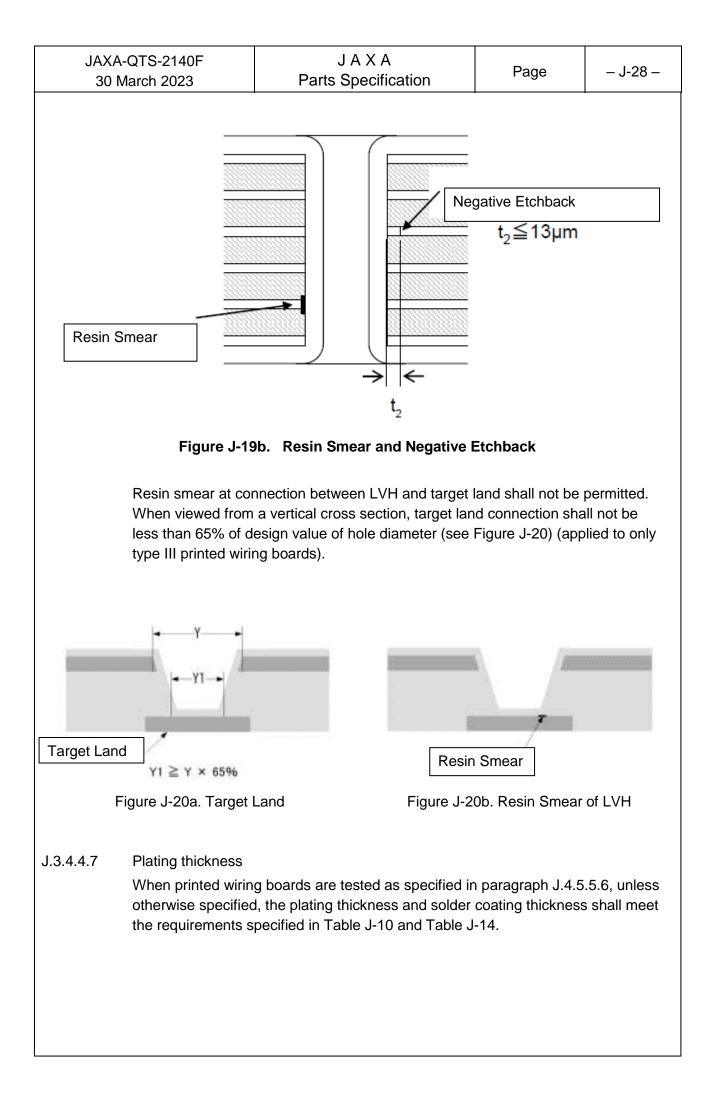
0	IAXA-QTS-2140F 30 March 2023	J A X A Parts Specification	Page	– J-24 –		
	specified. Since tolerances are copper inlay and ma	hole diameter of SVH, IVH, LVH a displayed differently for each type nufacturer-specific criteria for the c on specified in the detail specificatio	of the convexity onvexity toleranc	tolerances of coppe		
	Та	ble J-12. Dimensional Toleranc		mm		
	Item	Dimensional tolera	Dimensional tolerance			
	Outline dimensions		±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100			
	Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH, IVH, LVH and small via holes is not specified.				
	Undercut	Undercut at each edge of conductor total thickness of the copper foil				
	Unevenness of copper inlay	Unevenness of copper inlay shall no flatness, based on the lands of the copper inlay will be en	rough holes in whic			
3.4.2.	1 Dimensions of BG	A Pads, etc.				
	Unless otherwise	specified, the dimension tolerance he requirements specified in Table	-	c. shall be i		
	Table	J-13. Dimensions for BGA Pads	s, etc.			
			U	nit. (mm)		

			Unit. (mm)
	Item		Tolerance
		Pad (Figure J-11 a)	±0.05
Pad size (conductor bottom size)	Dog-Bone	Fan-out direction (Figure J-11 b)	±0.075
	Via-in-Pad (Figure J-11 c)		±0.05
Solder resist opening	Dog-Bone (Figure J-11 d)		±0.05
diameter (resist surface)	Via-in-Pad (F	Figure J-11 d)	±0.05
Accurate alignment	Length of rov	w of BGA pads	±0.05
Pad thickness (conducto	r thickness)		±0.01
Total board thickness (incl. solder resist)		±8 %	
Co-planarity (flatness): N	lormal state		0.05mm or less for diagonal diameter of BGA pads

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		· · · · · ·	L	l
J.3.4.3	 paragraph J.3.2.5, by adversely affect any f Unless otherwise spector board. If marking on placed on a tag. a) Part number b) Year and month c) Manufacturer's n 	produced with the marking inks or copper etching. The marking sha function, performance or reliability ecified, the following shall be marked the printed wiring boards is impose manufactured name or its identification code umber ⁽¹⁾ or lot number	all remain legible of printed wiring ed on each printe	and shall not boards. d wiring
	Note: ⁽¹⁾ Product seria process can	I number shall be provided so that be traced.	t the complete ma	anufacturing
J.3.4.3.1	usable, it shall be c	bard Irt (equivalent to a single wiring bo clearly marked that the part cannot nod such that it does not easily var	be used. This n	narking shall
J.3.4.4	Structural Integrity			
J.3.4.4.1	following requirement inlay), small via hol Figure J-17). a) Plating sha fiber protrusion b) Protrusion diameter in thr drawings. c) Partial pits specified in pa d) Resin rece through hole s from the surface resin recession of the cumulat thickness bein evaluated. Re e) The pits of provided that t	g boards are tested as specified in ents for through holes (including th les, sideplating, SVH, IVH and LVH all not exhibit cracks, conductive in n, and shall be continuously smoor of plating caused by burr and nod rough holes below its lower limit sp of plating shall not exceed 10% or ragraph J.3.4.4.7. ssion at the boundary section betw hall be permitted, provided the ma ce of the plated-through holes doe n on any side of the plated-through ive base material thickness (sum of g evaluated) on the side of the plates plating caused by negative etchback he negative etchback satisfies the .4.4.6. This requirement is not app	Arough holes with H shall be satisfie aterface separation th from the land. ules shall not red becified on manuf f the plating thick ween hole wall ar aximum depth as as not exceed 80µ h hole does not e of the dielectric la ated-through hole permitted. ack shall be perm arequirements sp	copper ed (see on or glass luce the hole facturing ness nd plated- measured um, and the xceed 40 % over being nitted,







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Table J-14.	Thickness	of Plating	and Other
-------------	-----------	------------	-----------

			Unit: µm	
Туре		Surface and through hole wa	all thickness	
Electroless copper	Thickne	ess necessary and sufficient for	for electrolytic copper	
plating		plating in the subsequent	t process	
		Component hole	25 as a minimum	
		Small via hole	25 as a minimum	
		SVH and IVH	25 as a minimum	
		Filled via (at the corner of	As specified in detail	
	LVH	the capture land)	specification	
		Resin-filled via	As specified in detail specification	
Electrolytic copper	Through holes with copper inlay press- fitted		25 as a minimum	
plating	SVH pla	ting on land (Figure J-21 a)	5 as a minimum	
		Small via hole	As specified in detail	
		(Figure J-21 b)	specification	
	Сар	SVH	As specified in detail	
	plating	(Figure J-21 c)	specification	
		LVH	As specified in detail	
		(Figure J-21 d)	specification	
	Sideplating		25 as a minimum	
Electrolytic gold plating				
Electrolytic nickel plating				
Solder coating	Shown in Table J-10			
ENEPIGEG (Electroless				
Nickel / Electroless				
Palladium / Immersion				
Gold / Electroless Gold)				

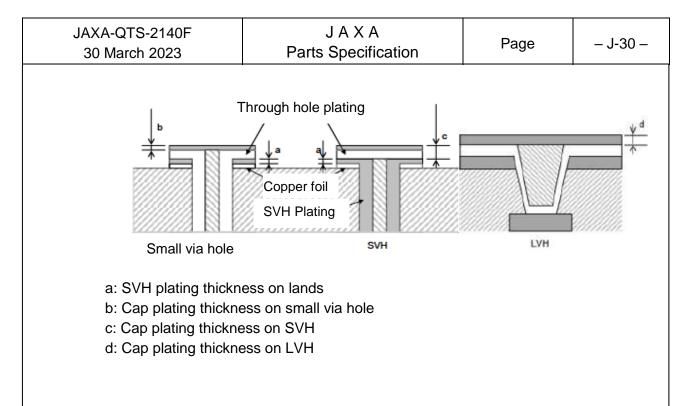
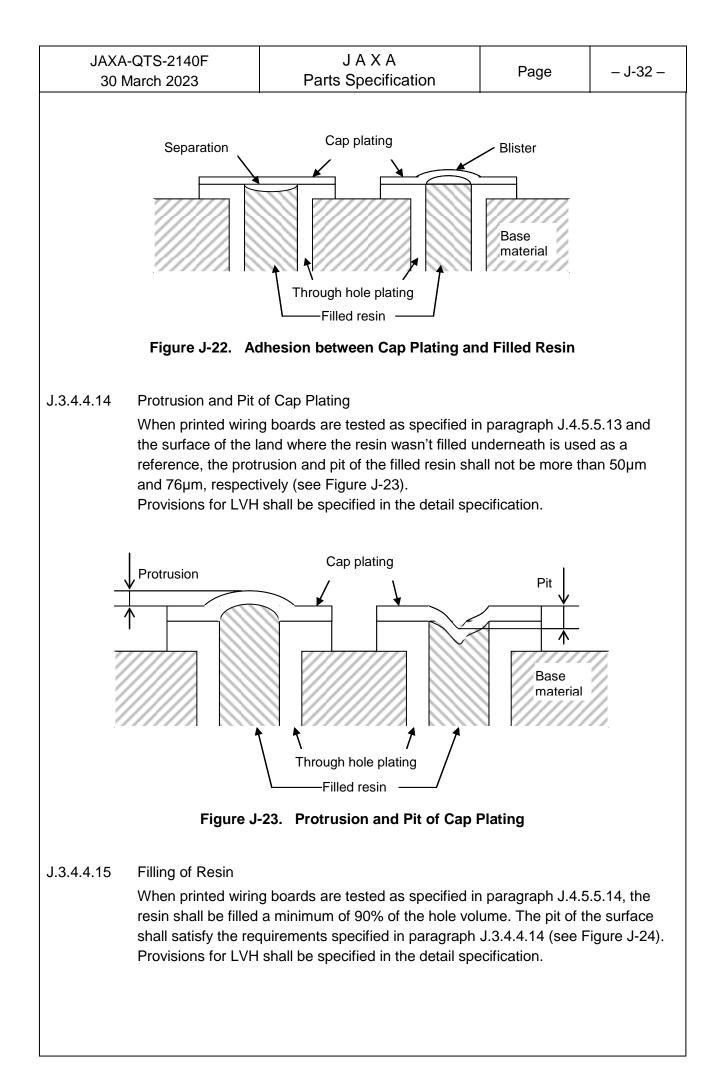
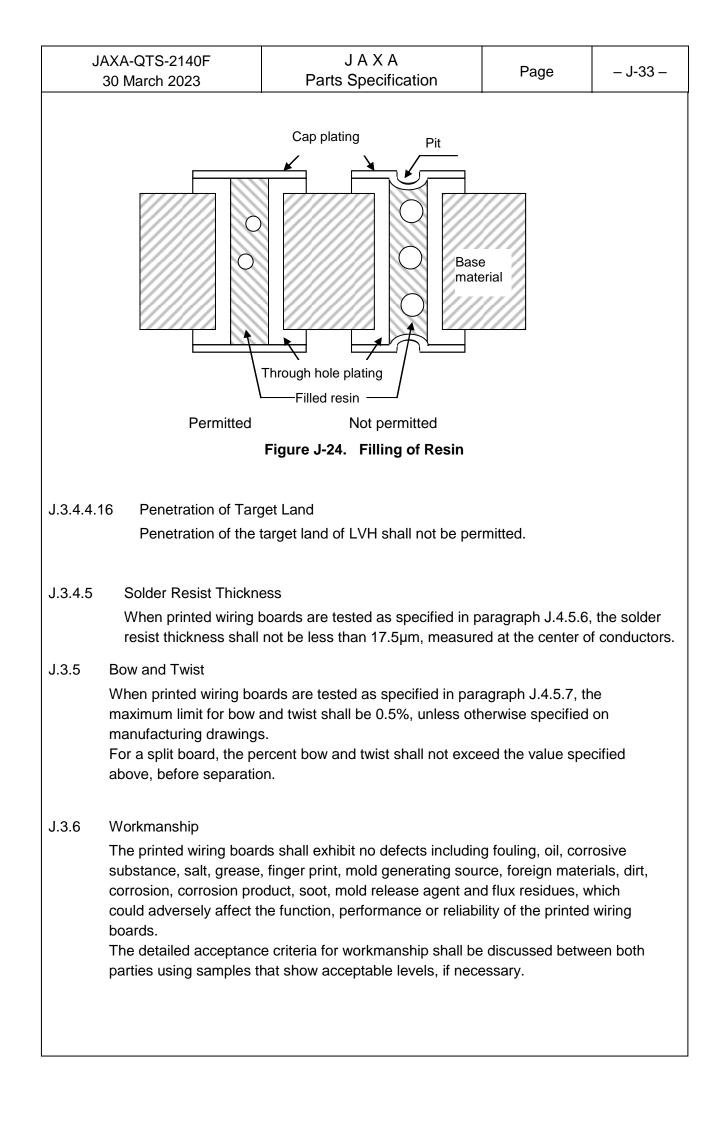


Figure J-21. Cap Plating Thickness

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30 1	March 2023	Parts S	Specifica	tion	Tage	- 5-51 -
J.3.4.4.8	Laminate Cracks					
	When printed wiring on laminate shall n			specified in	paragraph J.4.	5.5.7, cracks
J.3.4.4.9	Delamination and E	Blister				
	When printed wiring delamination and b	-		•	paragraph J.4.	5.5.8,
J.3.4.4.10	Layer-to-layer Reg	straion				
	When printed wirin layer-to-layer regis			•		5.5.9, the
J.3.4.4.11	Conductor Width of	Land (Annula	r Ring)			
	When printed wiring minimum conducto than the values spe	g boards are te r width of land	ested as of intern	•		
	Tabl	e J-15. Cond	luctor W	idth of Lar	nd	
					Init: mm	
	Through	nole type	Layer	Conducto		
	Through h		xternal	of lar		
	Through h		nternal	0.03		
	Non-plated		xternal	0.38		
	LVH	Ex	ternal(1)	No hole br	eakage	
			ternal(2)	No hole br	eakage	
	Notes (¹) External: (²) Internal: T	•				
J.3.4.4.12	Dielectric Layer Th	ckness				
	When printed wirin dielectric layer thic board shall not be l	kness between	n conduct	•		-
J.3.4.4.13	Adhesion between	Cap Plating ar	nd Filled	Resin		
	When printed wiring the cap plating is u shall be less than 5 requirements speci The above-mentior	sed as BGA pa um. When the fied in paragra	ad, the ga e cap plat aph J.3.4.	ap between ing is not u .4.14 shall l	cap plating and sed as BGA page	d filled resin d, the





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	30 March 2023	Parts Specification		
J.3.6.1	However, the remova resist may be permitt	, BGA conductor pads or conductor al of an excessive conductor and a ed, provided that the repaired solo nding solder resist thickness.	in insignificant rep	bair of solder
J.3.7		overhang ards are tested as specified in par ng of plating and conductors, or sli	•	
J.3.8		ards are tested as specified in par extract shall not be less than 2x1	•	the
J.3.9	Electrical Performance Printed wiring board sha	all meet the following electrical rec	quirements.	
J.3.9.1		ng Voltage poards are tested as specified in p shall not exhibit insulation breakd	•	
J.3.9.2		poards are tested as specified in p shall not exhibit open circuit or sh	•	
J.3.9.3	resistance between to exceed the value (Ri) When the connection the unmeasured conn all connection resista	boards are tested as specified in p wo lands connecting a circuit on a which is calculated by the formula resistance between all layers car nection resistance shall be repeated	Il conductive laye a specified below not be measured edly measured se	rs shall not d at a time,
		mm)	orms the conducto	or (mΩ∙mm)

-	4XA-QTS-2140F 30 March 2023	J A X A Parts Specification	Page	– J-35 –
J.3.9.3.1	Connection resista J.4.5.11.3.1. Test	ance of Copper Inlay nce of copper inlay shall be teste results shall be evaluated using t conducted as initial values.	• •	• .
J.3.9.4	are tested as specifie within the range spec	ance mpedance is specified in the drav d in paragraph J.4.5.11.4, the ch ified in the manufacturing drawin nce shall be within ±10% of the s	aracteristic impeda g. If the tolerance	ance shall be
J.3.10	Mechanical Performance Printed wiring boards sh	e nall meet the following mechanica	al requirements.	
J.3.10.1	 printed wiring boards only to component ho a) Bond strength The land shall wind smaller. b) Conductor and late When printed wind J.4.5.4.1, there is c) Microsection of the When printed wind wind the printed wind the	boards are tested as specified in shall meet the following requirent les. thstand a minimum of 89.2N pull and ring boards are inspected visually hall be no loosening around the f	or 1380N/cm ² , wh v as specified in pathrough holes. nd inspected as sp	on shall apply hichever is aragraph becified in
J.3.10.2	 When printed wiring boards printed wiring boards a) Through hole sol The through hole solder. This provised b) Surface conducted A minimum of 95 with fresh solder 	inside wall and land surface sha vision shall apply to only compon	all exhibit proper w ent holes. a shall be covered noles, dewetting or	etting of uniformly small
J.3.10.3	When printed wiring b	ace Conductor boards are tested as specified in shall meet the requirements spe		

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Whe J.4.8	• • •	•		•
	nmental Performa d wiring boards sh	ance nall meet the following environmen	tal requirements.	
J.3.11.1 The	rmal Shock			
W th Pr at	/hen printed wiring lere shall be no op rinted wiring boar the completion o	applicable to qualification test) g boards are tested as specified in pen circuit, blistering, measling, cra ds shall meet the requirements sp f the test, and the change in conne after the test shall be less than 10	azing or delamina ecified in paragra ection resistance	ation. iph J.3.9.2
W th Pi at	/hen printed wiring lere shall be no op rinted wiring boar the completion o	(Applied to Quality Conformance I g boards are tested as specified in pen circuit, blistering, measling, cra ds shall meet the requirements sp f the test, and the change in conne after the test shall be less than 10	a paragraph J.4.5 azing or delamina ecified in paragra ection resistance	ation. Iph J.3.9.2
At J.	4.5.13.1 b), samp	Thermal Shock boards are tested as specified in les prepared according to paragra fied in paragraph J.3.11.4 b).	•	•
Whe shal	I be no blistering,	on Resistance boards are tested as specified in p measling or delamination. The ins minimum of 500MΩ.	•	
Whe		poards are tested as specified in participation of the resistance between circuits before	• •	
Whe	ted wiring boards Externals	poards are tested as specified in possible of the following requirements of measling, cracks, separation of point mination.	ents.	

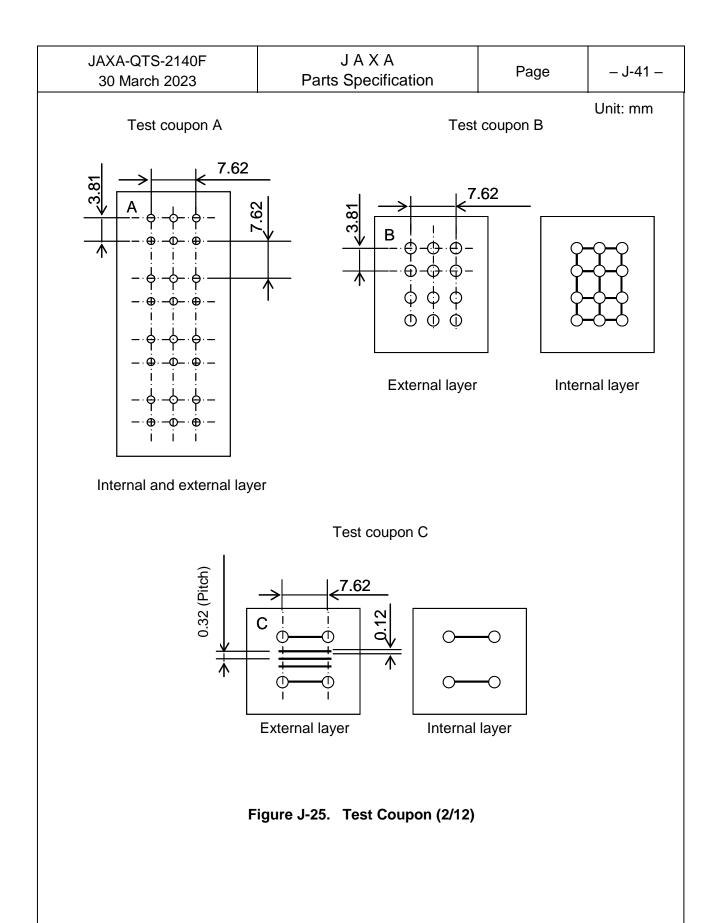
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				<u> </u>
	b) Structural Integri	ity		
	In the vertical mi	icrosection of through holes, the fo	llowing requirem	ents shall be
	satisfied.			
	1) Through hole	e		
	There shall b	be no corner cracks or barrel crack	KS.	
	Laminate voi			
		nductor spacing on the same plan	-	
		n conductor spacing specified in th	e manufacturing	drawings, the
		l not exceed 76µm.		
	 Lifting of land 	ds after thermal stress test shall be	a permitted	
	4) Cracks on co		e permited.	
	,	be no cracks which penetrate throu	ugh the copper fo	il.
	5) Internal laye	•	-9	
	•	be no separation between copper f	foil of internal laye	er and
	through hole	plating, and between target land a	and LVH plating.	
	6) Laminate Cra	acks		
		rmal stress test, the laminate crac		
	-	s or on the lands shall not exceed		
		than the ones on the land area sh		
	-	acent conductors fall below the mi	nimum conductor	spacing.
	7) Delamination	be no delamination and blisters.		
		cap plating and filled resin		
	,	e between cap plating and filled re	sin shall meet the	à
		s specified in paragraph J.3.4.4.13		
	Plating and F			•
	9) For through	holes with copper inlay embedded	, unevenness of	the copper
	inlay shall m	eet the requirements specified in p	baragraph J.3.4.2	
	Note: If there are any	description conflicting with above	requirements, qu	uality shall be
	•	d by satisfying quality requiremen	• • •	•
	specification.			
J.3.11.5	Radiation Hardness			
		boards are tested as specified in p	•	
		uch as measling, delamination or v		
		conductors shall not be less than 5 ed in paragraph J.3.9.1 shall be sa		
		sa in purugruph 0.0.0.1 shali be sa		
J.3.11.6	Vibration			
	When printed wiring I	boards are tested as specified in p	aragraph J.4.5.1	3.6, the
	printed wiring boards	shall meet the requirements spec	ified in paragraph	n J.3.9.2 at

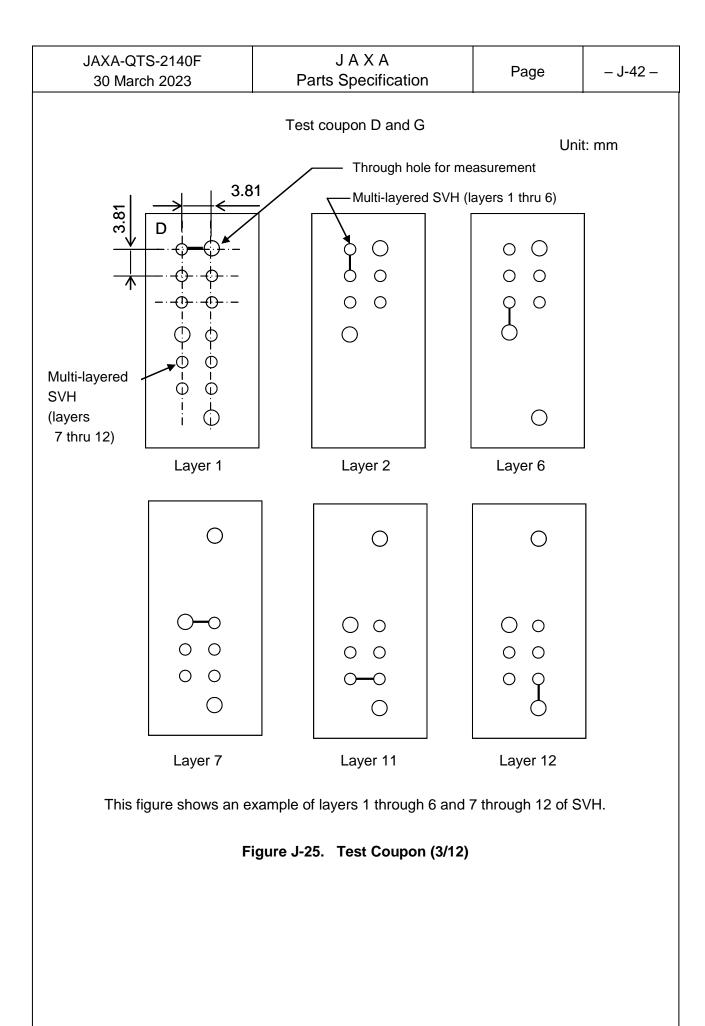
the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. Furthermore, the printed wiring

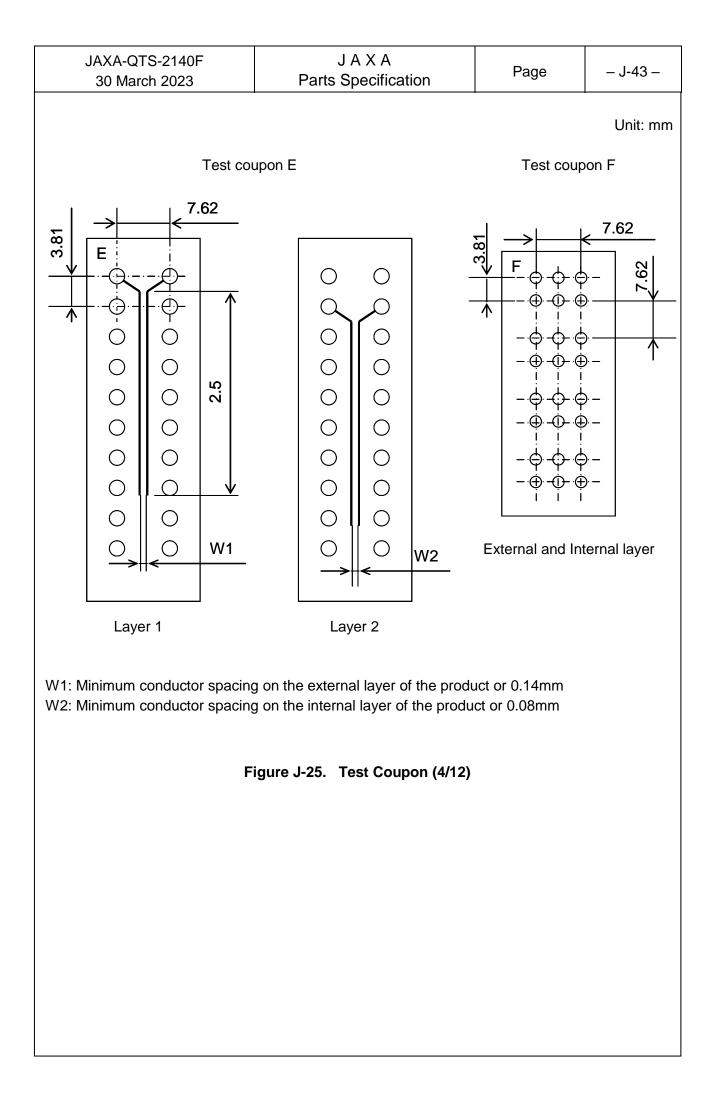
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		e requirements specified in paragra ne copper inlay shall meet the requ	•	
J.3.11.7	printed wiring boards the completion of the before and after the to boards shall meet the	boards are tested as specified in p shall meet the requirements spec test, and the change in connectio est shall be less than 10%. Furthe requirements specified in paragra te copper inlay shall meet the requ	ified in paragraph n resistance betw ermore, the printe aphs J.3.4.1.2 b)	n J.3.9.2 at veen circuits ed wiring and J.3.4.1.4
	Optional Tests This paragraph specifie specified in this specific qualified items. Optiona however, the test metho	s the tests that are out of the scop ation and that are not used for par al tests can be conducted addition od and handling of test results, etc ne part manufacturer in advance.	ss/fail decisions f ally at the user's	or request,
J.3.12.1	paragraph J.4.5.14.1,	ess Test) ser, printed wiring boards shall be and meet the requirements speci able to copper inlay section.	-	
J.3.12.2	• •	ser, printed wiring boards shall be and meet the requirements speci	-	
J.4. Qu	uality Assurance Provisi	ons		
-	shall be in accordance construction as the proc	ed for qualification test and quality with Figure J-25. The test coupon duct produced from the identical w coupon shall be assigned for eac	shall have the sa ork board.	•

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	 Parts Specification Arrangement of test coupons Notes Unless otherwise specified, the cond Test coupon A indicates the minimum hole (incl. small via hole) for the corr and the land diameter shall be the m through holes. When applied, small The hole diameter tolerance is not s For test coupons B, C, E and F, the 1.8±0.13mm, and the land shape sh products. All holes shall be through \o0.8mm. The hole diameter tolerance corresponding printed wiring board. The patterns of test coupons D and of layers and via hole (including LVH be produced so as to form the same construction as those of the correspi- circuit continuity through all layers by be included. The hole and land diam diameter for each SVH, IVH, LVH ar corresponding products, and the lan shape of the products. On both ends through holes shall be formed to me of the land and hole shall be \o1.8mm hole diameter tolerance is not specif Solder resist shall apply to the test of solder resist shall apply to the test of solder resist shall apply to the test of solder resist shall be the clearan printed wiring board. If the hole diam the land diameter shall be equal to tti (6) Test coupons K and L shall be prepa products have SVH, IVH and LVH. T the number of layers and via hole cort shall be formed on all layers in acco 30.1 The arrangement of test coupons (A to H identification and not for the object of is not specified. (10) Only when the BGA pads, etc. are n bone construction) or test coupon M formed in accordance with the pad of coupons M1 and M2 is shown to the more detailed information. (11) Only when the characteristic imped: N shall be formed. If the characteristic other test coupon may be used. (12) Only when the construction where of outer layer is required, the test coupon formed in accordance with the pad of coupon M1 and M2 is shown to the more detailed information. (12) Only when the construction where of outer layer is required, the test coupon <!--</th--><th>ductor width shall be m hole diameter of t responding printed v inimum land diame via holes shall be fi pecified. land diameter shall all be the typical lan holes and diameter re shall be the tolera G vary depending o d) construction. Eac number of layers a onding product, and y via holes. Copper neter shall be the m nd small via hole of d shape shall be the s of the printed wirin asure the resistance n and ϕ0.8mm, resp ied. oupons E, H, and J ucts. The clearance ce diameter for the neter for the product he land diameter + 0 ared only when the of hose coupons vary onstruction. a layers which are co and in this figure is able. I and J to M2) shall f inspection. The ma- construction. An exa left. See detail spec- ance is required, the stic impedance are a olating is required are a olating is requi</th><th>e 0.5±0.1mm. he through viring board, ter of the lled with resin. be d shape of the shall be ance for the n the number h coupon shall nd via hole to have a inlay may not inimum the e typical land g board, e, the diameter ectively. The , only when spacing for corresponding is unknown, 0.2mm. corresponding depending on connected by conductors, ne conductors re. an example; a be used for arking method upon M1 (Dog- shall be mple of test cification for e test coupon tessured, the he test coupon tessured, the he test coupon tessured, the ted on the</th>	ductor width shall be m hole diameter of t responding printed v inimum land diame via holes shall be fi pecified. land diameter shall all be the typical lan holes and diameter re shall be the tolera G vary depending o d) construction. Eac number of layers a onding product, and y via holes. Copper neter shall be the m nd small via hole of d shape shall be the s of the printed wirin asure the resistance n and ϕ 0.8mm, resp ied. oupons E, H, and J ucts. The clearance ce diameter for the neter for the product he land diameter + 0 ared only when the of hose coupons vary onstruction. a layers which are co and in this figure is able. I and J to M2) shall f inspection. The ma- construction. An exa left. See detail spec- ance is required, the stic impedance are a olating is required are a olating is requi	e 0.5±0.1mm. he through viring board, ter of the lled with resin. be d shape of the shall be ance for the n the number h coupon shall nd via hole to have a inlay may not inimum the e typical land g board, e, the diameter ectively. The , only when spacing for corresponding is unknown, 0.2mm. corresponding depending on connected by conductors, ne conductors re. an example; a be used for arking method upon M1 (Dog- shall be mple of test cification for e test coupon tessured, the he test coupon tessured, the he test coupon tessured, the ted on the

Copper Inlay (14) For type I and II printed wiring boards, test coupon R shall be formed. Number of copper inlay shall be two. (15) For type III printed wiring boards, test coupon S shall be formed in order to evaluate continuity between copper inlay and LVH and insulation between copper inlay and adjacent conductors. Details of test coupon S shall be as specified in the detail specification. (16) When specified in the drawings or other documentation, IST test coupon shall be formed.	JAXA-QTS-2140F 30 March 2023	J A X A Parts Specification	Page	– J-40 –
Figure J-25. Test Coupon (1/12) (Continued)		Number of copper inlay shall be two 15) For type III printed wiring boards, te order to evaluate continuity between insulation between copper inlay and test coupon S shall be as specified 16) When specified in the drawings or c coupon shall be formed.	b. st coupon S shall b n copper inlay and L adjacent conducto in the detail specific other documentation	e formed in LVH and rs. Details of ation.







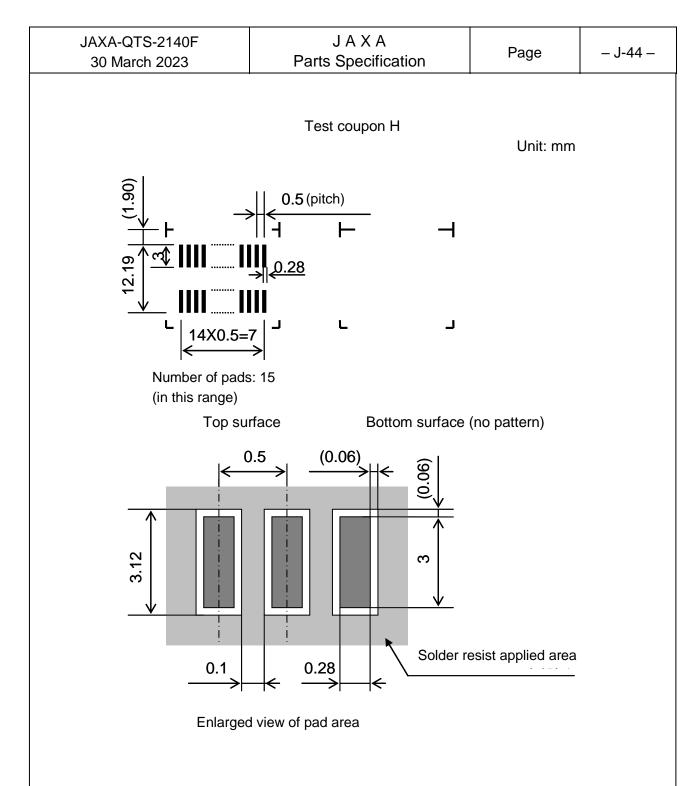
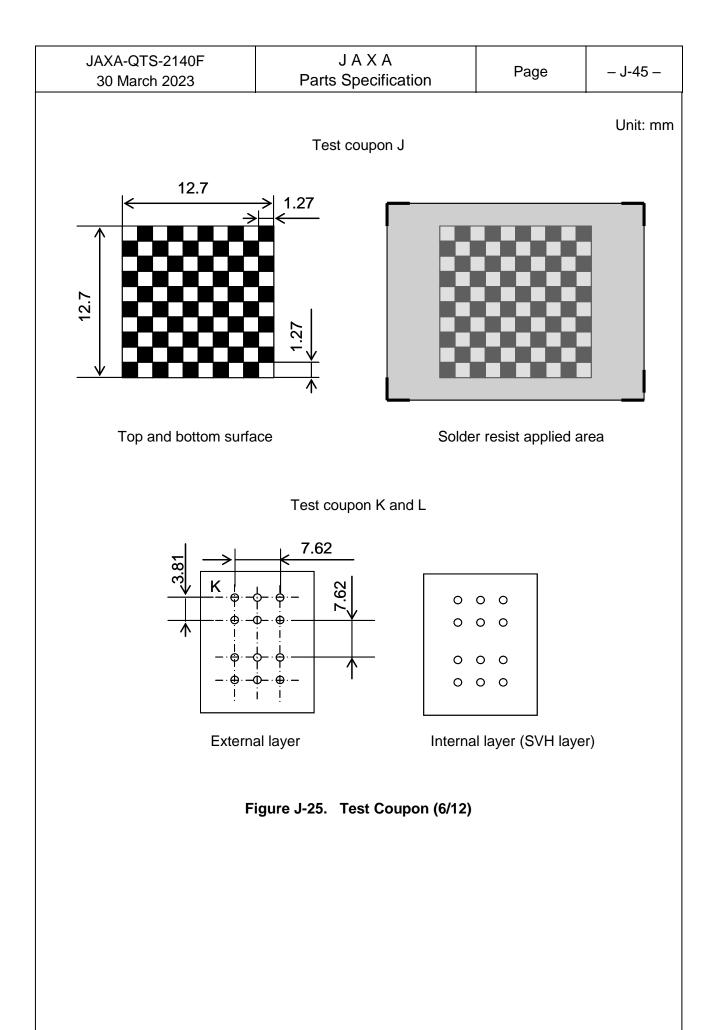


Figure J-25. Test Coupon (5/12)



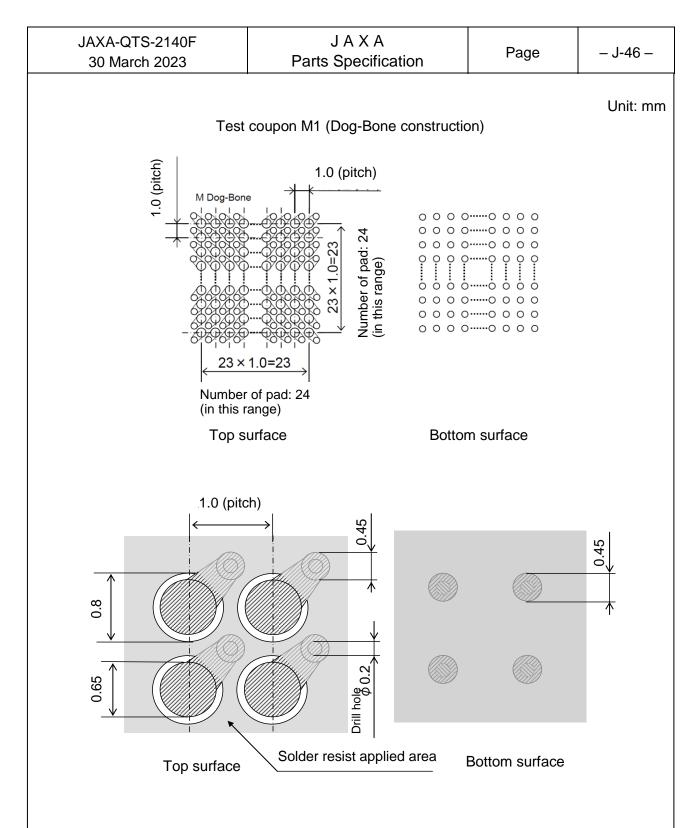


Figure J-25. Test Coupon (Example of BGA pads) (7/12)

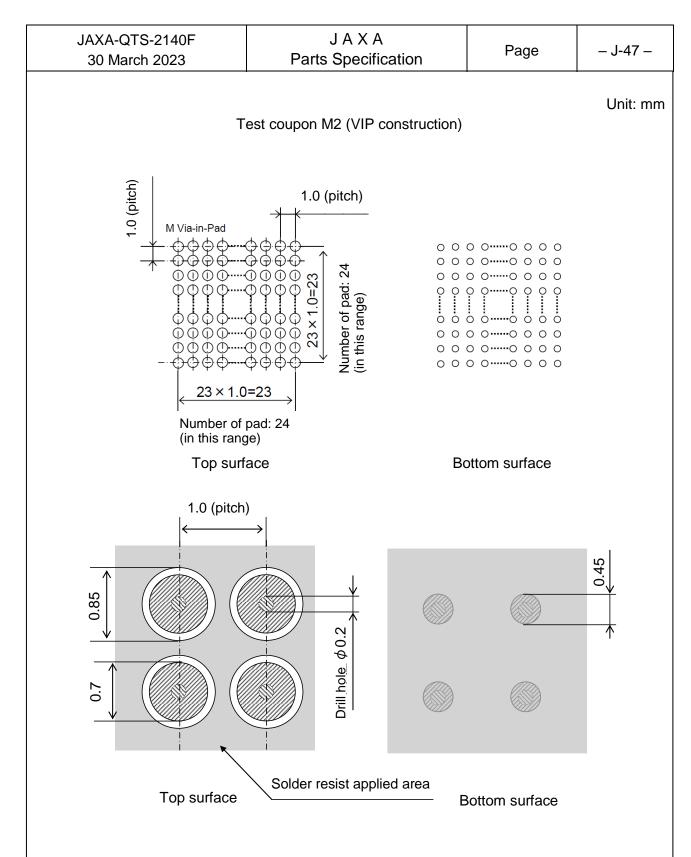
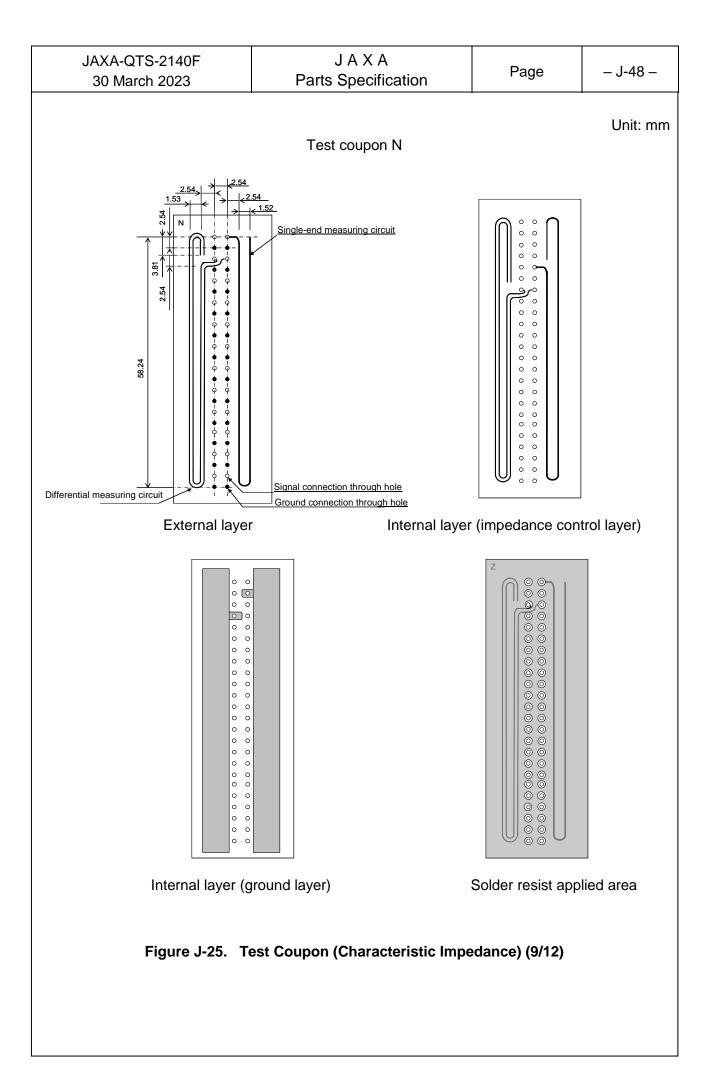


Figure J-25. Test Coupon (Example of BGA pads) (8/12)



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	Test coupon O		
	U		
I			

Figure J-25. Test Coupon (Outer Perimeter Sideplating) (10/12)

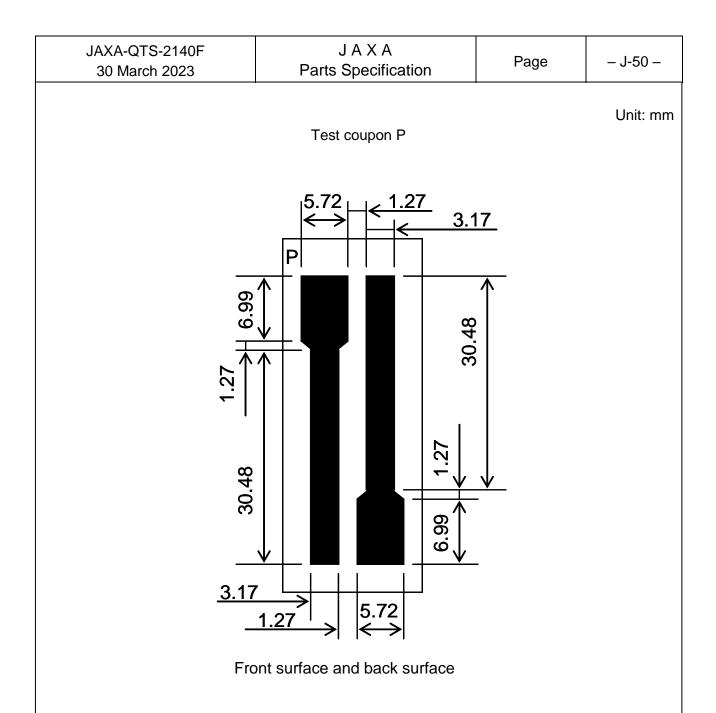


Figure J-25. Test Coupon (Peel Strength) (11/12)

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	Test Coupon R		
External layer Through hole for measurement (Copper inlay connection) Internal layer connected with copper	(Co	ough hole for meas pper inlay connecti ough hole for meas acent conductor co	ion) urement
inlay Through hole plating Internal layer not connected with copper inlay		er inlay – conductor num value on the prir	
Vertical cross-section (6 layers)			
_	st Coupon (Extrusion Strength o		

Continuity and Insulation) (12/12)

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J.4.2 In-Process Inspection

The in-process inspection specified in Table J-16 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs J.3.4.1 (Externals of Conductor, Base Material, Solder Resist and Copper Inlay), J.3.4.2 (Dimensions), J.3.4.3 (Marking), J.3.8 (Cleanliness), and J.3.4.2.1 (Dimensions of BGA Pads, etc).

No.	Item	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	J.3.4.1 J.3.4.2 J.3.4.3	J.4.5.4.1 J.4.5.4.2 J.4.5.4.3	All	After forming internal circuit and before pre-treating the laminate layer
2	Conductor of external layer Base material of external layer	J.3.4.1.1 J.3.4.1.2	J.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	J.3.8	J.4.5.10	AQL 1.0%	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	J.3.4.2.1	J.4.5.4.2	All	After forming solder resist and before solder coating
5	Externals of copper inlay section	J.3.4.1.4	J.4.5.4.1 d)	All	After forming circuit on copper inlay press-fit layer

J.4.3 Qualification Test

J.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole, copper inlay, number of layers and construction sufficient enough to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board.

In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include at least one of deep-hole-shape slit, V-groove cut and continuous perforation.

J.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table J-17. Upon completion of Group I and II tests, Group III through IX tests shall be performed using specimens allocated to the appropriate group tests. Group III through IX tests may be performed in any order regardless of group number. However, tests in each of Group III through IX shall be performed in the order listed.

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Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table J-17.

		Test				/fail Criter	ia
		Requirement	Test method	Sample size		Number of	
Group	Order	Test item	paragraph	paragraph	Production printed wiring boards	Test coupon (1) (2)	defectives
. 1	1	Externals of conductor, base materials, and solder resist Externals, dimensions,	J.3.4.1	J.4.5.4.1	No. 1 to No. 6	A, B, C, D, E, F, G, H, K,	
I		Dimensions Marking	J.3.4.2 J.3.4.3	J.4.5.4.2 J.4.5.4.3		L, M, N, O, P, R and S	
	2	Workmanship	J.3.6	J.4.5.8			
Ш	1	Plating adhesion and overhang	J.3.7	J.4.5.9	No. 1 to No. 6	С	
	2	Bow and twist	J.3.5	J.4.5.7		N/A	
	1	Structural integrity	J.3.4.4	J.4.5.5		A, F, K, M and O	
	2	Through hole pull strength	J.3.10.1	J.4.5.12.1		F	
Ш	3	Solder resist thickness	J.3.4.5	J.4.5.6	No. 1	J	-
	4	Peel strength of surface conductor ⁽³⁾	J.3.10.3	J.4.5.12.2		Р	-
	5	Extrusion strength of copper inlay ⁽⁴⁾	J.3.10.4	J.4.5.12.4		R	
	1	Connection resistance	J.3.9.3	J.4.5.11.3	No. 2	D, R and	0
IV	2	Hot oil resistance	J.3.11.3	J.4.5.13.3		S ⁽⁵⁾	
	3	Connection resistance	J.3.9.3	J.4.5.11.3		-	
	1	Circuitry	J.3.9.2	J.4.5.11.2			
	2	Connection resistance	H.3.9.3	J.4.5.11.3			
	3	Thermal shock (I)	J.3.11.1.1	J.4.5.13.1a)		E, G, R	
V	4	Circuitry	J.3.9.2	J.4.5.11.2	No. 3	and S ⁽⁶⁾	
	5 6	Connection resistance Cross-section after thermal shock	J.3.9.3 J.3.11.1.3	J.4.5.11.3 J.4.5.5.1			
	1	Humidity and insulation resistance	J.3.11.2	J.4.5.13.2		E, R and	
VI	2	Dielectric withstanding voltage	J.3.9.1	J.4.5.11.1	No. 4	S ⁽⁵⁾	
VII	1	Thermal stress	J.3.11.4	J.4.5.13.4	No. 5	A, B, L M, O, R and S	
	2	Solderability	J.3.10.2	J.4.5.12.3		B and H ⁽⁷⁾	
VIII	1	Radiation hardness	J.3.11.5	J.4.5.13.5	No.6 N/A		1
	1	Vibration	J.3.11.6	J.4.5.13.6	As specified in J.4.5.13.6 h) and J.4.5.13.7 h).		
IX	2	Shock	J.3.11.7	J.4.5.13.7			0
-	-	Materials	J.3.2	J.4.5.2	N/A	,	N/A

Table J-17.	Qualification	Test
	a a a a a a a a a a a a a a a a a a a	

Notes:

⁽¹⁾ The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through IX tests. For Group II through IX tests, one test coupon shall be provided for each coupon

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type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

- ⁽²⁾ Test coupons and sample product shall be fabricated simultaneously. For Group III through IX tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.
- ⁽³⁾ This test shall be performed when copper foil laminate construction is under the qualification coverage.
- ⁽⁴⁾ Applied to type I and II printed wiring boards.
- ⁽⁵⁾ The test coupon R shall be tested for type I and II printed wiring boards and the test coupon S shall be tested for type III printed wiring boards.
- ⁽⁶⁾ Under the circuitry test, the test coupon G shall be subjected to the continuity test, test coupon E shall be subjected to the circuit shorts test, test coupon R shall be subjected to the continuity test and circuit shorts test for copper inlay of type I and II printed wiring boards, and test coupon S shall be subjected to the continuity test and circuit shorts test for copper inlay of type I and II printed wiring boards, and test coupon S shall be subjected to the continuity test and circuit shorts test for copper inlay including type III LVH.
- ⁽⁷⁾ The test coupon B shall have been subjected to thermal stress test prior to this test. The test coupons B and H shall be subjected to the tests for through hole solderability and surface conductor solderability, respectively.

J.4.4 Quality Conformance Inspection

J.4.4.1 Quality Conformance Inspection (Group A)

J.4.4.1.1 Sample

The quality conformance inspection shall be performed with the sample products and the test coupons. The test coupons and sample product shall be manufactured simultaneously.

Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen.

A "split board" means a board constructed of parts of the same patterns or parts of different patterns.

J.4.4.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table J-18. The inspections within each group shall be performed in the order listed. One test coupon shall be provided for each of Group IV and V test.

		Inspection			F	Pass/fail criteri	а
				Samp			
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Production printed wiring boards	Test coupon	Number of defectives permitted
	1	Design and construction	J.3.3	J.4.5.3			
I	2	Externals of conductor, base materials, and solder resist	J.3.4.1	J.4.5.4.1	100%	N/A	
		Dimensions Marking	J.3.4.2 J.3.4.3	J.4.5.4.2 J.4.5.4.3			
	3	Workmanship	J.3.6	J.4.5.8			0
	4	Characteristic impedance	J.3.3.19	J.4.5.11.4	100%	N ⁽¹⁾	
Ш	1	Bow and twist	J.3.5	J.4.5.7	100%	N/A	
III	1	Circuitry	J.3.9.2	J.4.5.11.2	100%	N/A	
IV	1	Thermal stress	J.3.11.4	J.4.5.13.4	N/A	A, F, K ⁽²⁾ , M ⁽³⁾ , O ⁽⁴⁾ , R and S ⁽⁵⁾	
V	1	Solderability	J.3.10.2	J.4.5.12.3	N/A	F and H ⁽⁶⁾	

Table J-18. Quality Conformance Inspection (Group A)

Notes:

⁽¹⁾ Test coupon N shall be inspected when characteristic impedance is required.

⁽²⁾ Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the product is provided with SVH.

⁽³⁾ Test coupon M shall be inspected when the products is provided with pads such as BGA pads.

⁽⁴⁾ Test coupon O shall be inspected when the sideplating is required.

⁽⁵⁾ Test coupon R shall be inspected for type I and II printed wiring boards and the test coupon S shall be inspected for type III printed wiring boards.

⁽⁶⁾ Test coupons F and H shall be subjected to the tests for through hole solderability and surface conductor solderability, respectively.

J.4.4.2 Quality Conformance Inspection (Group B)

J.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection and selected from the lot which passed Group A inspection.

J.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table J-19. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

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	-	Inspection			Pass/fail criteria	
Group	Order	Inspection item	Requirement paragraph	Test method paragraph	Test coupon	Quantity of allowable defects
-	1	Plating adhesion and overhang	J.3.7	J.4.5.9	С	
П	1	Through hole pull strength	J.3.10.1	J.4.5.12.1	F	
	1	Connection resistance	J.3.9.3	J.4.5.11.3		
111	2	Hot oil resistance	J.3.11.3	J.4.5.13.3	D, R and S ⁽¹⁾	
	3	Connection resistance	J.3.9.3	J.4.5.11.3		
	1	Circuitry	J.3.9.2	J.4.5.11.2		0
	2	Connection resistance	J.3.9.3	J.4.5.11.3		
IV	3	Thermal shock (II)	J.3.11.1.2	J.4.5.13.1b)	E, G, R and	
IV	4	Circuitry	J.3.9.2	J.4.5.11.2	S ⁽²⁾	
	5	Connection resistance	J.3.9.3	J.4.5.11.3		
	6	Cross-section after thermal shock	J.3.11.1.3	J.4.5.5.1		
V	1	Humidity and insulation resistance	J.3.11.2	J.4.5.13.2	E, R and S ⁽¹⁾	
v	2	Dielectric withstanding voltage	J.3.9.1	J.4.5.11.1	$rac{1}{2}$, r and $3^{(1)}$	
	1	Peel strength of surface conductor	J.3.10.3	J.4.5.12.2	P ⁽³⁾]
VI	2	Extrusion strength of copper inlay ⁽⁴⁾	J.3.10.4	J.4.5.12.4	R	

Notes:

⁽¹⁾ Test coupon R shall be inspected for type I and II printed wiring boards and the test coupon S shall be inspected for type III printed wiring boards.

- ⁽²⁾ Under the circuitry test, the test coupon G shall be subjected to the continuity test, test coupon E shall be subjected to the circuit shorts test, test coupon R shall be subjected to the continuity and circuit shorts test of copper inlay of type I and II printed wiring boards and test coupon S shall be subjected to the continuity and circuit shorts test of copper inlay including LVH of type III printed wiring boards.
- ⁽³⁾ Peel strength of surface conductor is performed when copper foil laminate construction is used. If copper foil laminate construction is in qualification coverage and group B inspection is performed on a sample without this construction, the inspection shall be performed again on the first lot of the products with this construction.

⁽⁴⁾ Applied to type I and II printed wiring boards.

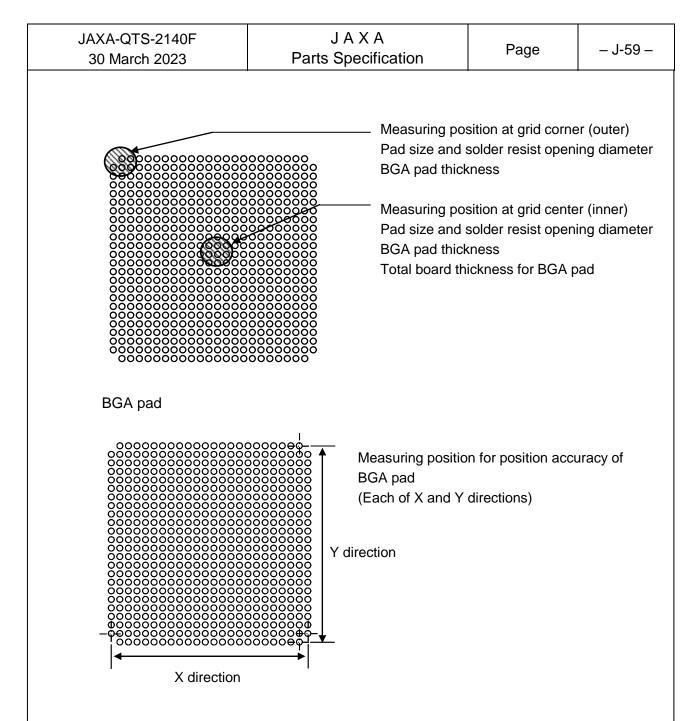
J.4.5 Methods for Test and Inspection

J.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

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J.4.5.2	J.4.5.2 Materials The copper clad laminates, prepreg and copper foil shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.					
J.4.5.3	Design and Construction The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.					
J.4.5.4	Externals, Dimension	s, Marking and Others				
J.4.5.4.1	 External inspection a) Conductors For conductive can be used. Paris instrument with b) Base Materials Pass or fail shate sufficient accurate c) Solder Resist Pass or fail shate d) Copper Inlay Second 	Il be determined by using 10X ma	X magnifier. tical Inspection ma using an optical n cal measuring inst	achine (AOI) neasuring		
J.4.5.4.2	accuracy. a) Dimension The dimensions as follows. For area shall be se size, any one of measurement s 1) Dimension of Each section measured by 2) Position accu The direction measured wi measuring in	e measured by using a measuring s of BGA pads, etc. s of printed wiring boards with BG the board with multiple BGA pads elected for measurement. If all the f the pad shall be selected for mea- ections shall be shown in Figure of pads such as BGA pads. and so of grid corner (outer) and the cer an optical measuring instrument. uracy for pads such as BGA pads s of X and Y axes of circumference th a 2-dimension end-measuring in strument sufficient enough for mea- he base material for pads such as	A pads, etc. shall , the BGA pad wite BGA pad areas a asurement. The d J-26. Ider resist openin ter area (inner) st ce for BGA pads s machine or an eque	be measured th the largest are the same etailed g diameter hall be shall be uivalent		

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 Each section of grid corner (outer) and the center area (inner) of BGA pad shall be measured by the focal depth method using a metallograph or by an optical measuring instrument. 4) Total board thickness for pads such as BGA pads. For the total board thickness including solder coating and solder resist, the center section of BGA pad shall be measured by using a micrometer. 								

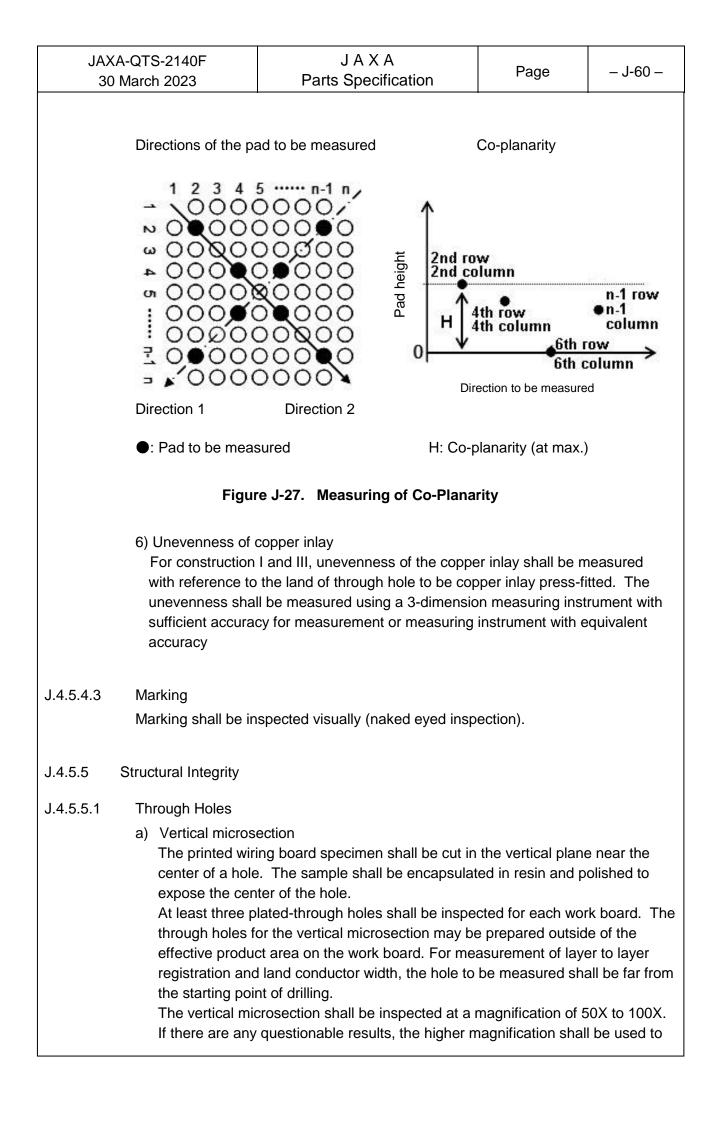




5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

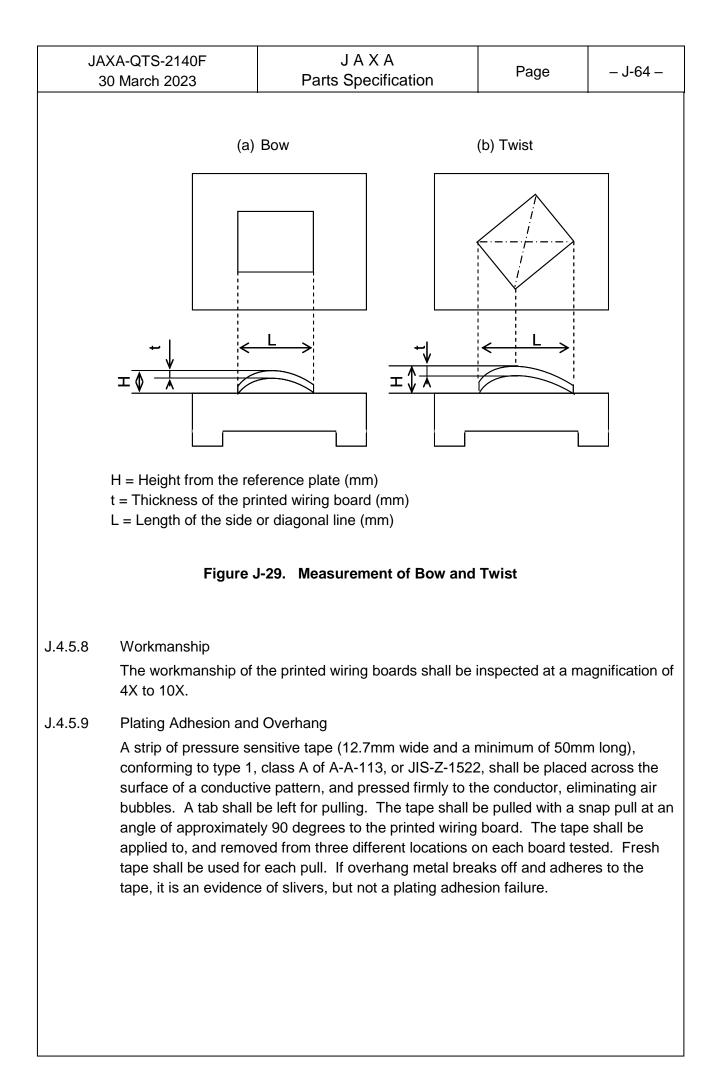
Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure J-27)



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 inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching to clarify the borderline of copper plating and copper foil shall not be conducted at the observation of internal connection and resin smear. b) Horizontal microsection b) Multilayer boards with through holes shall be encapsulated in resin and polished. A conductive layer shall be polished in the parallel direction to expose the conductive layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the higher magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching shall not be conducted on the microsection surface. 					
J.4.5.5.2	Voids				
	The microsection prepared in paragraph J.4.5.5.1 a) shall be inspected for any void at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.				
J.4.5.5.3	Lifting of Lands				
	Lands shall be inspected for any lifting by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.				
J.4.5.5.4	Cracks on Copper	Foil			
	Copper foil shall be inspected for any crack by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.				
J.4.5.5.5	Internal Layer Con	nection			
	paragraphs J.4.5.5 questionable result	ection shall be inspected by using .1 a) and b) at a magnification of 5 s, the larger magnification shall be I shall be determined at 100X mag	50X to 100X. If the used to inspect	ere are any	
J.4.5.5.6	paragraph J.4.5.5. shall be the averag any of the measure value shall not be u	hall be inspected by using the mic 1 a) at a magnification of 200X as he value of three measurements for ed value is significantly different froused for calculating the average. here shall be measured at the thinne	a minimum. Plati r a plated throug om the other valu	ng thickness h hole. If es, the	

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J.4.5.5.7	 4.5.5.7 Laminate Cracks Laminate shall be inspected for any crack by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification. 					
J.4.5.5.8	Delamination and Blister The microsection prepared in paragraph J.4.5.5.1 a) shall be inspected for any delamination and blister at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.					
J.4.5.5.9	Layer-to-layer registration The layer-to-layer registration shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 25X to 100X. The misregistration shall be measured around the hole in the direction parallel to the board length and the vertical direction. The microsections for inspection of layer- to-layer misregistration shall be prepared by cutting the multi-layer printed wiring board in the direction parallel to the board length for at least one hole and the vertical direction for another one hole as a minimum. (See Figure J-28)					
J.4.5.5.10	Land Conductor Width (Annular ring) The land conductor width (annular ring) shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 25X to 100X. The measurement of the annular ring on an external layer shall be from the surface of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure J-28).					
	→¦-	Maximum misregistration				
Each land shall be measured and the position of the center shall be calculated. The misregistration is the distance from the center of the rightmost land to the center of the leftmost land. Measuring annular ring on an internal layer						
Measuring annular ring on an external layer Figure J-28. Measurement of Layer-to-Layer Misregistration and Annular Ring						

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J.4.5.5.11	5.11 Insulation Layer Thickness Insulation Layer Thickness shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X.						
J.4.5.5.12	Adhesion of cap pla the microsection pr 100X. If there are	Adhesion of Cap Plating and Filled Resin Adhesion of cap plating and filled resin shall be observed and measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.					
J.4.5.5.13	Protrusion and Pit of Cap Plating Protrusion and pit of cap plating shall be observed and measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X as a minimum.						
J.4.5.5.14		e observed and measured by using 5.1 a) at a magnification of 25X to	-	n prepared			
J.4.5.6	polished to expose th	ess cut vertically near the conductor a e center of the conductor. The sol fication of 200X as a minimum.					
J.4.5.7	with its convex side fa the highest point of th percent bow and twis	ard specimen shall be placed horizacing upward, and the distance be be printed wiring board shall be me t shall be calculated by the following wist = $\frac{H-t}{L} \times 100$ (%)	tween the references asured (see Figure 1) the tween the references as the tween the references as the tween the twe	nce plate and			



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J.4.5.10	wiring board shall be volume of isopropyl a The wash solution sh solution shall be pour 100ml of the wash so both sides of the boa of one minute. The re measured with a cone accuracy.	te shall be positioned over an elect suspended within the funnel. A w lcohol and 25 % by volume of dist all have a resistivity not less than red onto both sides of the printed v lution is collected from each board rd). The time required for the was esistivity of the collected wash sol ductivity bridge or other instrumen	rash solution of 7 tilled water shall to $6x10^{6}\Omega \cdot cm$. The wiring board from d surface of 6.5cr th activity shall be ution in the beake t of equivalent ra	5 % by be prepared. wash the top until m ² (including a minimum er shall be nge and
_	Table .	J-20. Equivalent Measuring Me	thod	

Method	Resistivity (×10⁰Ω·cm)	Equivalent factor	Equivalents of sodium chloride (µg/cm²)
Conductivity bridge	2	1	1.56
Omega Meter ⁽¹⁾	2	1.39	2.2

Note: ⁽¹⁾ Alpha Metals Incorporated, "Omega Meter"

J.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

J.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

- a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
- b) Duration: 30 seconds
- c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

J.4.5.11.2 Circuitry

a) Continuity

A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity

b) Circuit shorts

A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

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J.4.5.11.3		ance ween the through hole terminals s ent of four-terminal method capab			
J.4.5.11.3.1					
Without Plat	ting after Press-fitting	B B C C C C C C C C C C C C C C C C C C	ection (Example: 6	S Layers)	
With Platin	g after Press-fitting of	f Copper Inlay: Vertical Microsect	ion (Example: 6 L	ayers)	
	Figure J-	30. Measuring Points for Copp	er Inlay		
J.4.5.11.4	Characteristic Impe The characteristic i 2.5.5.7 of IPC-TM-	mpedance shall be measured in a	accordance with p	paragraph	
	Mechanical Performa				

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J.4.5.12.1	Through Hole Pull Strength					
	A conductor shall be cut with a sharp knife at a minimum of 6mm from the land, peeled and pulled toward the land, and shall be cut off by applying the sharp knife at the joining point of the conductor and land without degrading the land adherence strength. Then, a lead wire sufficient in length for installing a tensile tester shall be inserted in the hole and soldered. After that, a cycle of solder removal and resoldering by using a soldering iron shall be performed.					
	 a) A lead wire shall be soldered in to the through hole. b) The lead wire shall be removed from the through hole (solder removal). c) A lead wire shall be resoldered in to the through hole. 					
	d) The lead wire shall be removed from the through hole (solder removal).					
	e) A lead wire shall be resoldered in to the through hole. The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the required minimum. Upon completion of e) resoldering, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Breaking off or pulling out the lead wire shall not be regarded as a failure, and a new lead wire shall be soldered and pulled. The pull strength shall be calculated by the following formula. $L \ge 1380 \times \frac{\pi\left\{ \left(d_2 \right)^2 \cdot \left(d_1 \right)^2 \right\}}{4}$					
	L = Pull strength (N) d ₁ = Hole diameter (cm) d ₂ = Land diameter (cm)					

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J.4.5.12.2	J.4.5.12.2 Peel Strength of Surface Conductor						
	 The peel strength of surface conductor is performed in accordance with Paragraph 2.4.8 of IPC-TM-650 and as follows. a) Normal state Test condition A shall be applied. b) After Thermal stress Test condition B shall be applied. 						
J.4.5.12.3	to the inspectio b) Surface conduc After the specin STD-202, the fl Test Method 20 clean stainless range between removed from t immersion. The 25±6mm per se vertical state in	solder shall be inspected using a m n specified in paragraph J.4.5.5.1. ctor solderability and sideplating nen is dipped into the flux specifier ux shall be drained for 60 seconds 08 of MIL-STD-202 shall be melted steel paddle. It shall be confirmed 226 and 238°C. The solder slug a he molten solder surface immedia e specimen shall be put vertically i econd, kept in the bath for 4±0.5 se econd. After the pull-up, the specin the air, until the solder is solidified condition of solder on the conduct	d in Test Method s. Solder complia d in a bath and sti d that the tempera and burnt flux sha tely before the sp nto the solder ba econds and raise men shall be kep d. No quick coolir	208 of MIL- ant with the rred with a ature is in the all be becimen th at a rate of d at a rate of t in the ng shall be			
J.4.5.12.4	Extrusion Strength The test methods f detail specification	or extrusion strength of copper inla	ay shall be specif	ied in the			
J.4.5.13	Environmental Perfor	mance erformance tests shall be performe	ed as follows.				
J.4.5.13.1	MIL-STD-202. The a) Thermal shock The test shall b temperature sh time for steps 2 Reflow solderin be performed th	test shall be performed in accordate following conditions shall apply. (I) (applicable to qualification test) e performed under the test conditi all be -30°C and the number of cy and 4 shall be within 2 minutes ea of total heating process in according of total heating process in according the measured and recorded befor) on B. However, t cle shall be 1200 ach. dance with JERG ie printed wiring b	he lowest cycles. The 6-0-043 shall board. The			

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	 to confirm there is no effect by the reflow. The heating condition shall be as follows. 1) Heating condition: 200°C min. for 45 seconds min. 2) Peak temperature: 230°C min. b) Thermal shock (II) (applicable to quality conformance inspection) The test shall be performed under the test condition B-3 (-65°C to +125°C). The time for step 2 and 4 shall be within 2 minutes each. 					
J.4.5.13.2	cycles, and the during the test. be taken out of evaluated. b) Insulation resis The test shall b	ance s in Test Method 106 of MIL-STD- polarization voltage of 100V±10Vr Upon completion of step 6 of the the bath and dried immediately by	bc shall be applie final cycle, the sp blowing air at 25 e test condition E	d to all layers becimen shall 5±5°C and 3, Test		
J.4.5.13.3	Hot Oil Resistance The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. This Immersion and cooling shall be performed for 10 cycles.					
J.4.5.13.4	Thermal Stress The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 % maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for the structural integrity using the microsection prepared in accordance with paragraph J.4.5.5.1. Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder. Evaluation specimen of Adhesion of cap plating and filled resin (paragraph J.3.4.4.13) shall be floated in a solder bath for a period of 10 seconds and cooled down. This floating and cooling shall be performed three times.					
J.4.5.13.5	0.5×10 ⁴ Gy to 1×10 amounts to 1×10 ⁴ G visually to verify the	s adiation shall be performed by usir ⁴ Gy per hour to the specimen in op Gy. After the irradiation, the specin at there is no degradation in any p rithstanding voltage and insulation	ben air, until the t nen shall be insp art of the specim	otal dose ected en. The		

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	respectively. The i	dance with paragraphs J.4.5.11.1 nsulation resistance shall be meas thstanding voltage test.	,	
J.4.5.13.6	Vibration			
	Vibration test shall Following condition a) Mounting metho Printed wiring b lifting height: (1) test axis with sp b) Measurement b Interrupted or s J.4.5.11.2 and t paragraph J.4.5 accordance with c) Test condition: Frequency range Total RMS acce d) Vibration direct e) Number of tests Each vibration t minutes for 3 di f) Measurement a Interrupted or s J.4.5.11.2 and t paragraph J.4.5 accordance with g) Visual inspection Printed wiring b h) Design of test b Design of test b - External dime ϕ 3.5mmx4P, b - Copper inlay s	ooard shall be secured to the jig (m Omm to 20mm) / rigid studs are ac becified torque. before test horted circuits shall be checked in the connection resistance shall be 5.11.3. Unevenness of copper inla h paragraph J.4.5.4.2 b). II-H ge: 50Hz to 2,000Hz eleration: 34.02 Grms ion: Three-direction is and duration test duration shall be 15 minutes of rections. after test horted circuits shall be checked in the connection resistance shall be 5.11.3. Unevenness of copper inla h paragraph J.4.5.4.2 b).	tests. nounting section: cceptable) on the accordance with measured in acc ay shall be measu once per direction accordance with measured in acc ay shall be measu hification of 4X to lows. 0mm, mounting h e board (Size of c	 (φ 6mm), appropriate paragraph ordance with ared in ; total of 45 paragraph ordance with ared in 10X.
J.4.5.13.7	 Following condition a) Mounting method Printed wiring b lifting height: (1) test axis with sp b) Measurement b 	oard shall be secured to the jig (m 0mm to 2mm) / rigid studs are acc becified torque.	tests. nounting section: ceptable) on the a	(φ6mm), appropriate
	•	the connection resistance shall be		

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 accordance with c) Test condition: d) Shock test directions e) Number of tests Number of shock directions. f) Measurement at Interrupted or state J.4.5.11.2 and the paragraph J.4.5 accordance with g) Visual inspection Printed wiring b h) Design of test b Design of test b External diments \$\phi\$ 3.5mmx4P, b Copper inlay s 	n paragraph J.4.5.4.2 b). F (1500G, 0.5m/s, half-sine wave ction: Three-direction s test shall be 3 times per direction for test horted circuits shall be checked in he connection resistance shall be 5.11.3. Unevenness of copper inli- n paragraph J.4.5.4.2 b). on after test oard shall be inspected at a mag board for evaluation loard for evaluation sions: 100mm, mounting pitch: S oard thickness: 1.6mm	e) on; total of 9 times n accordance with e measured in acc ay shall be measu nification of 4X to llows. 90mm, mounting h	s for 3 a paragraph cordance with ured in 10X. nole diameter:	
Optional Tests				
IST is performed to evaluation) of patte in the detail specifie	IST (Interconnect Stress Test) IST is performed to evaluate connection reliability (acceleration correlation evaluation) of pattern wirings and through holes. Test methods shall be specified in the detail specification. When the IST cannot be performed, the reason shall be specified in the detail			
shear test and ball specification. When the pad strer	pull test. Test methods shall be any shall be any shall be any test cannot be performed, the state of the sta	specified in the de	etail	
	March 2023 paragraph J.4.5 accordance with c) Test condition: d) Shock test direct e) Number of tests Number of shood directions. f) Measurement a Interrupted or s J.4.5.11.2 and t paragraph J.4.5 accordance with g) Visual inspection Printed wiring b h) Design of test b Design of test b - External diment ϕ 3.5mmx4P, b - Copper inlay s shall be the mat Optional Tests IST (Interconnect S IST is performed to evaluation) of patter in the detail specific When the IST cannot specification. Pad Strength Test For the pads requirt shear test and ball specification. When the pad strer	 March 2023 Parts Specification paragraph J.4.5.11.3. Unevenness of copper inlaccordance with paragraph J.4.5.4.2 b). c) Test condition: F (1500G, 0.5m/s, half-sine waved) Shock test direction: Three-direction e) Number of tests Number of shock test shall be 3 times per directidirections. f) Measurement after test Interrupted or shorted circuits shall be checked in J.4.5.11.2 and the connection resistance shall be paragraph J.4.5.11.3. Unevenness of copper inlaccordance with paragraph J.4.5.4.2 b). g) Visual inspection after test Printed wiring board shall be inspected at a mag h) Design of test board for evaluation Design of test board for evaluation Design of test board for evaluation shall be as for External dimensions: 100mm, mounting pitch: § φ 3.5mmx4P, board thickness: 1.6mm Copper inlay shall be located at the center of the shall be the maximum size in the qualification random of pattern wirings and through holes. Test in the detail specification. When the IST cannot be performed, the reason shall specification. Pad Strength Test For the pads requiring strength verification, pad stre shear test and ball pull test. Test methods shall be a specification. 	March 2023 Parts Specification Page paragraph J.4.5.11.3. Unevenness of copper inlay shall be measu accordance with paragraph J.4.5.4.2 b). c) Test condition: F (1500G, 0.5m/s, half-sine wave) d) Shock test direction: Three-direction e) Number of tests Number of shock test shall be 3 times per direction; total of 9 times directions. f) Measurement after test f) Measurement after test Interrupted or shorted circuits shall be checked in accordance with J.4.5.11.2 and the connection resistance shall be measured in acc paragraph J.4.5.11.3. Unevenness of copper inlay shall be measu accordance with paragraph J.4.5.4.2 b). g) Visual inspection after test Printed wiring board shall be inspected at a magnification of 4X to h) Design of test board for evaluation Design of test board for evaluation shall be as follows. e External dimensions: 100mm, mounting pitch: 90mm, mounting f ϕ 3.5mmx4P, board thickness: 1.6mm Copper inlay shall be located at the center of the board (Size of of shall be the maximum size in the qualification range) Optional Tests IST (Interconnect Stress Test) IST is performed to evaluate connection reliability (acceleration correl evaluation) of pattern wirings and through holes. Test methods shall b in the detail specification. When the IST cannot be performed, the reason shall be specified in th specification. Pad Strength Test For the pads requiring strength verification, pad strength test is perfor	