Registration No.1265

JAXA-QTS-2140F
30 March 2023

Superseding
JAXA-QTS-2140E
Cancelled
30 March 2023

PRINTED WIRING BOARDS, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

JAXA
JAPAN AEROSPACE EXPLORATION AGENCY

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

Revision Log		
Revision	Date	Description
NC	25 Dec. 2001	Original
A	31 March 2004	(1) Revised to reflect the organizational change from NASDA to JAXA. (2) Clarified the contents of the provisions.
B	17 Nov. 2008	(1) Revised to reflect the revision of JAXA-QTS-2000 from revision B to revision C • Changed “NASDA***” to “JAXA***” in the part number definition. • Specified the part number for the transition to the QML certification system. (2) Appendix C Added the provision regarding lead-free surface finish (3) Other changes to clarify the requirements and to correct inconsistency. • Paragraph 2.2: Reflected the change of document identification for JAXA Design Standard for Printed Wiring Boards and Assemblies NASDA-HDBK-8 → JERG-0-042 Reflected the change of document identification for JAXA Parts Application Handbook. NASDA-HDBK-4 → JERG-0-035
C	9 July 2009	(1) Added Printed wiring boards, CIC controlled thermal expansion, glass base woven polyimide resin base material (Appendix F). (2) Changes associated with the addition of Appendix F. (3) Other changes to correct errors.
D	14 Jan. 2014	(1) Added Printed wiring boards, Area array packaging (Appendix G) and some changes accompanied with the addition. (2) Others: Corrected errors.
E	2 April 2015	(1) Added Printed wiring boards for High Speed Signals (Appendix H) and some changes accompanies with the addition (main document). (2) Clarified the test method of Terminal Pull Strength (Appendixes A through F) (3) Others; Corrected errors, etc.
F	30 March 2023	(1) Added Printed wiring boards, high heat radiation (Appendix J).
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Appendix A
Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material

Appendix B
Fine Pitch Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material

Appendix C
Discrete Wiring Boards, Glass Base Woven Epoxy Resin Base Material

Appendix D
Printed Wiring Boards, Flexible, Polyimide Film Base Material

Appendix E
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Appendix F
Printed Wiring Boards, CIC Controlled Thermal Expansion, Glass Base Woven Polyimide Resin Base Material

Appendix G
Printed Wiring Boards, Area Array Packaging

Appendix H
Printed Wiring Boards for High Speed Signals

Appendix J
Printed Wiring Boards, High Heat Radiation

PRINTED WIRING BOARDS, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the general requirements and quality assurance provisions for space use high reliability, printed wiring boards (hereinafter referred to as "printed wiring boards") used for electronic equipment installed on spacecraft. This specification complies with JAXA-QTS-2000 (Common Parts/Materials, Space Use, General Specification for) which was recently established to transition to the qualified manufacturing line system and replaces the following specifications.

a) NASDA-QTS-1046A	Printed Wiring Boards, High Reliability, Space Use, General Specification for
b) NASDA-QTS-1047	Fine Pitch Printed Wiring Boards, High Reliability, Space Use, General Specification for
c) NASDA-QTS-1051	Discrete Wiring Boards, High Reliability, Space Use, General Specification for
d) NASDA-QTS-1026A	Flexible Printed Wiring Boards, High Reliability, Space Use, General Specification for
e) NASDA-QTS-1066	Rigid-Flex Printed Wiring Boards, High Reliability, Space Use, General Specification for

1.2 Terms and Definitions

The definitions for terms used herein are as follows and as specified in JIS C 5603. The terminology shall be provided in paragraph 6.3.

a) Outgassing
The gas released from a printed wiring board or its substance, which is measured by the methods specified in ASTM E 595.

b) Workmanship
The appearance and conditions of finished products.

1.3 Classification

Products covered by this specification are classified into the types specified in Table 1.

Table 1. Classification

Classification	Appendix	Previous QPL specification
Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	A	NASDA-QTS-1046A
Fine Pitch Printed Wiring Boards, Glass Base Woven Polyimide Resin or Glass Base Woven Epoxy Resin Base Material	B	NASDA-QTS-1047
Discrete Wiring Boards, Glass Base Woven Epoxy Resin Base Material	C	NASDA-QTS-1051
Printed Wiring Boards, Flexible, Polyimide Film Base Material	D	NASDA-QTS-1026A
Rigid-Flex Printed Wiring Boards	E	NASDA-QTS-1066
Printed Wiring Boards, CIC Controlled Thermal Expansion, Glass Base Woven Polyimide Resin Base Material	F	–
Printed Wiring Boards, Area Array Packaging	G	–
Printed Wiring Boards for High Speed Signals	H	–
Printed Wiring Boards,High Heat Radiation	J	

1.4 Part Number

The part number shall be in accordance with paragraph A.3.1.4 of JAXA-QTS-2000. The details shall be in accordance with the detail specification.

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents

The documents listed below form a part of this specification as specified herein. These documents are the latest issues available at the time of contract award or application. If it is necessary to designate an issue, the issue shall be specified in the detail specification.

a) JAXA-QTS-2000	Common Parts/Materials, Space Use, General Specification for
b) JIS C 5603	Terms and Definitions for Printed Circuits
c) MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
d) IPC-4101	Specifications for Base Materials for Rigid and Multilayer Printed Boards
e) IPC-SM-840	Qualification and Performance of Permanent Solder Mask
f) A-A-113	Tape, Pressure-Sensitive Adhesive
g) ASTM E595	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment
h) SAE-AMS-QQ-N-290	Nickel Plating (Electrodeposited)
i) JIS C 5012	Test Methods for Printed Wiring Boards
j) JIS Z 9015-1	Sampling Procedures for Inspection by Attributes - Part 1: Sampling Plans Indexed by Acceptable Quality Level (AQL) for Lot-by-Lot Inspection

k) JIS Z 1522 Pressure Sensitive Adhesive Cellophane Tapes
l) JPCA/NASDA-SCL01 Printed Wiring Boards, High Reliability, Space Use, Common Materials for, Detail Specification for
m) IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
n) IPC-4204 Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry

2.2 Reference Documents

Following documents are reference documents.

a) JERG-0-0042 JAXA Design Standard for Printed Wiring Boards and Assemblies
b) JERG-0-0035 JAXA Parts Application Handbook
c) IPC-2221 Generic Standard on Printed Board Design
d) IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards
e) IPC-2223 Sectional Design Standard for Flexible Printed Boards
f) IPC J-STD-004 Requirements for Soldering Fluxes
g) IPC J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.3 Order of Precedence

In the event of a conflict between the text of this specification and the applicable documents, the following order of precedence shall be applied.

a) Detail specification
b) This specification
c) JAXA-QTS-2000
d) Applicable documents of this specification (paragraph 2.1, except for JAXA-QTS-2000)

2.4 Detail Specification

Detailed requirements for the type and performance of printed wiring boards are specified in each detail specification.
The detail specification shall be prepared and implemented by a manufacturer in accordance with paragraph A.4 of JAXA-QTS-2000. The detailed specification shall also be registered and issued to the Japan Aerospace Exploration Agency (hereinafter referred to as 'JAXA').

2.4.1 Detail Specification Number

The detail specification number shall be indicated in the following form in accordance with paragraph A.2.2.2 of JAXA-QTS-2000. The individual identification shall be a three digits number and the first digit represents the QML manufacturer and the remaining two digits are a series number.

Example: JAXA-QTS-2140 / A 101 A

This specification number	Appendix letter	Individual identification	Revision letter

2.4.2 Revision Letter of the Detail Specification

A revision letter in the detail specification number shall be assigned in accordance with paragraph A.2.2.2.4 of JAXA-QTS-2000.

2.4.3 Independency of Detail Specification

The detail specification shall be a stand-alone document with a unique number in accordance with paragraph 2.4.1.

2.4.4 Format of Detail Specification

The detail specification format shall be in accordance with paragraph A.6 b) of JAXA-QTS-2000 and shall specify each requirement in accordance with paragraph A.4 of JAXA-QTS-2000.

3. REQUIREMENTS

3.1 Certification

3.1.1 Qualification Coverage

Qualification coverage shall be as specified in the appendixes and the detail specifications.

3.1.2 Initial Qualification

To acquire certification of the printed wiring board in compliance with this specification, a manufacturer shall establish a quality assurance program in accordance with paragraph 3.2.1 of JAXA-QTS-2000, perform the qualification tests specified in paragraph 4.4 of this specification, and acquire a certification status from JAXA as specified in paragraph 3.4.1 of JAXA-QTS-2000. The manufacturer shall be listed on the Qualified Manufacturer List of the Japan Aerospace Exploration Agency (JAXA QML).

3.1.3 Retention of Qualification

To continue supplying printed wiring boards in accordance with this specification, a manufacturer must apply for retention of certification in accordance with paragraph 3.4.2.1 of JAXA-QTS-2000 commencing between 30 and 60 days prior to the expiration date of the certification period (paragraph 3.1.4).
If products were not shipped during the effective period of certification and a quality conformance inspection was not conducted, the manufacturer may apply for retention of certification without conducting the quality conformance inspection.

3.1.4 Effective Period of Certification

The effective period of certification granted in compliance with this specification shall be three (3) years.

3.1.5 Change of Qualification Coverage

To change the qualification coverage, the manufacturer shall perform procedures for re-qualification in accordance with paragraph 3.4.3 of JAXA-QTS-2000.

3.2 Quality Assurance Program

3.2.1 Establishment of a Quality Assurance Program

To acquire certification in compliance with this specification, the manufacturer shall be responsible for establishing a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall generate a quality assurance program plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to JAXA for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.

3.2.2 TRB Formation

To acquire a certification status in compliance with this specification, the manufacturer shall form and operate the Technical Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.

3.3 Materials

Materials used in the printed wiring boards shall be as specified herein. When definite materials are not specified in this specification, materials shall be used which meet the requirements of this specification and shall be specified in the document defining the manufacturing conditions of the quality assurance program.

3.3.1 Outgassing

The outgassing test shall be performed in accordance with ASTM E 595 as part of the qualification test or when the materials are changed. The following outgassing data shall be specified in the application data sheet (ADS).

a) Total Mass Loss (TML)
b) Collected Volatile Condensable Materials (CVCM)

3.4 Design and Construction

The design and construction shall be as specified in appendixes. The detail requirements such as circuit dimensions and layer structure shall be specified in the detail specification.

3.5 Externals, Dimensions, Marking and Others

The externals, dimensions, marking and others shall be as specified in appendixes.

3.6 Workmanship

The workmanship of the printed wiring boards shall be as specified in the appendixes.

3.7 Electrical Performance

Requirements on the electrical performance shall be as specified in the appendixes.

3.8 Mechanical Performance

Requirements on the mechanical performance shall be as specified in the appendixes.

3.9 Environmental Performance

Requirements on the environmental performance shall be as specified in the appendixes.

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The manufacturer shall be responsible for implementing the quality assurance program specified in paragraph 3.2 of this specification and operating the TRB.

4.2 Classification of Tests and Inspections

The tests and inspections shall be classified into the following three categories in accordance with paragraph 4.3 of JAXA-QTS-2000.

a) In-process inspection
b) Qualification test
c) Quality conformance inspection

4.3 In-Process Inspection

The manufacturer shall perform the following in-process inspections during the manufacturing process to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize properties which cannot be measured using the finished products. The manufacturing flowchart in the quality assurance program plan shall define the inspection process.

a) Internal visual inspection of semi-finished products (100% or sampled inspection for non-destructive inspection)
b) Physical and chemical inspection of semi-finished products (destructive or non-destructive, 100% or sampled inspection)
c) Characterization of semi-finished products (100% or sampled inspection for non-destructive inspection)

4.4 Qualification Test

4.4.1 Sample

Samples shall be manufactured in accordance with the manufacturing specification, the process and control as specified in the quality assurance programs and shall also typify the qualification coverage. The details shall be in accordance with the appendixes.

4.4.2 Manufacturing Records

The manufacturer, which intends to acquire certification status, shall archive material certification, receiving inspection data or test data of materials used, work records related to sample preparation, and in-process inspection data. These records shall be readily available upon request.

4.4.3 Test Items and Sample Size

Test items, order of tests and number of samples shall be as specified in the appendixes.

4.4.4 Criteria for Pass/Fail

A failure of any test specified in the appendixes shall constitute failure of the qualification tests. If the failure mode of the defectives is catastrophic such as open or short circuit where the function of the printed wiring board might be lost, the printed wiring board fails the qualification test.

4.4.5 Disposition after Tests

The samples used in the qualification test shall not be delivered. The products in the same inspection lot that have passed the qualification test may be delivered if they passed the Group A quality conformance inspections. If a sample fails to pass the qualification test, the manufacturer shall review applicable materials and/or manufacturing processes and take corrective actions on them. After the corrective action has been taken, the qualification tests specified in each appendix shall be repeated. In this case, JAXA has the authority to determine whether all or partial test items shall be performed.

4.5 Quality Conformance Inspection

4.5.1 Quality Conformance Inspection (Group A)

All products shall be subjected to the Group A inspections at the time of production.

4.5.1.1 Sample

The test coupons submitted for the Group A inspection shall be as specified in the appendixes.

4.5.1.2 Inspection Items and Sample Size

The inspection items, number of samples and test order shall be in accordance with the appendixes.

4.5.1.3 Criteria for Pass/Fail

A failure of any test in the Group A inspections specified in the appendixes shall constitute failure of the Group A inspections. If the failure mode of the defectives is catastrophic such as open or short circuit where the function of the printed wiring board might be lost, the printed wiring board fails the Group A inspections. The details shall be in accordance with the appendixes.

4.5.1.4 Disposition after Inspections

The lots rejected in the Group A inspection shall not be delivered.

4.5.2 Quality Conformance Inspection (Group B)

Group B inspection shall be performed for the first products manufactured within the certification period. When no products were manufactured during the effective

certification period and the recertification was obtained without conducting the quality conformance inspection, it shall be performed at the time of resuming production.

4.5.2.1 Sample

The test coupons submitted for the Group B inspection shall be as specified in the appendixes. Inspection lots for the Group B inspection shall consist of samples that have passed the Group A inspections.

4.5.2.2 Inspection Items and Sample Size

Items, sample size and order of the Group B inspection shall be as specified in the appendixes.

4.5.2.3 Criteria for Pass/Fail

A failure of any test in the Group B inspections specified in the appendixes shall constitute failure of the Group B inspections. If the failure mode of the defectives is catastrophic such as open or short circuit where the function of the printed wiring board might be lost, the printed wiring board fails the Group B inspections.

4.5.2.4 Disposition after Inspections

The samples used for the Group B inspections shall not be delivered. If the samples fail in the Group B inspections, the QML manufacturer shall conduct a failure analysis on the defectives and take corrective actions on applicable materials and/or manufacturing processes. Delivery of the products shall be suspended until JAXA confirms the outcome of corrective actions.

4.6 Method for Test or Inspection

4.6.1 Externals, Dimensions, Marking and Others

The externals, dimensions, marking and others shall be tested in accordance with the appendixes.

4.6.2 Workmanship

The workmanship of the printed wiring boards shall be tested in accordance with the appendixes.

4.6.3 Electrical Performance

The electrical performances of the printed wiring boards shall be tested in accordance with the appendixes.

4.6.4 Mechanical Performance

The mechanical performances of the printed wiring boards shall be tested in accordance with the appendixes.

4.6.5 Environmental Performance

The environmental performances of the printed wiring boards shall be tested in accordance with the appendixes.

4.7 Long-Term Storage

This provision shall not apply.

4.8 Change of Tests and Inspections

Any change in the in-process inspection or quality conformance inspection specified in this specification shall be made in accordance with paragraphs 4.4 and 6.1 of JAXA-QTS-2000.

5. PREPARATION FOR DELIVERY

Preparation for delivery shall be as follows and as specified in paragraph 5 of JAXA-QTS-2000.

5.1 Packaging

The printed wiring boards shall be packaged with a material that will not affect the insulating plate and conductors. The packaging shall be performed in an appropriate manner to protect the products from any damage during handling and transportation.

5.2 Marking on Package

The following shall be marked on the packages.

a) Part name
b) Part numbers those defined in this specification and by the purchaser
c) Applicable specification number
d) Year and month manufactured, and production serial number or lot identification code
e) Purchaser's name
f) Manufacturer's name
g) Quantity of packages
h) Date of inspection
i) Inspection result

6. NOTES

6.1 Notes for Manufacturer

6.1.1 Preparation and Registration of Application Data Sheet

The manufacturer shall prepare the application data sheet in accordance with Appendix G of JAXA-QTS-2000 and register it with JAXA.

6.2 Notes for Purchasers

Refer to the application data sheet for the detailed data of the products and notes.

6.2.1 Items to be Specified for Procurement

To purchase printed wiring boards manufactured in compliance with this specification, the purchaser shall provide the following information.

a) Part number those defined in this specification and by the purchaser.
b) This specification number.
c) Detail specification number

d) Indication of test data or source inspection results to be submitted for delivery
e) Others

As mentioned in e), requirements other than those defined in this specification may be specified for special applications. However, if the requirements conflict with the existing requirements in this specification, the purchaser shall not request the manufacturer to indicate that the printed wiring board complies with this specification.

6.3 Terminology

The definitions for terms used in this specification shall be as follows.

a) Artwork
An original production master of photos for circuits, solder mask, symbol print and part drawing. Or drawings to produce the original production master of photos.

b) Artwork master
An original drawing of the specified accuracy which is used to produce an original production master.

c) Interstitial Via Hole (IVH)
A through hole connecting internal circuit layers of a multilayer printed wiring board, but not extending fully through all layers (see Figure 1).

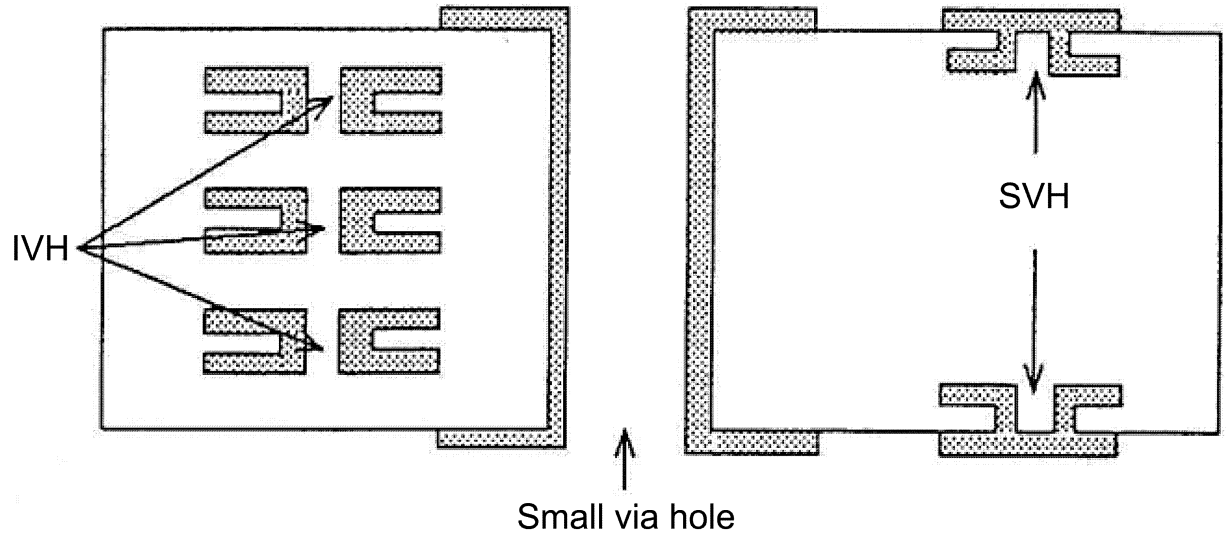

Figure 1. Cross Section of Multilayer Printed Wiring Board with Small Via Hole, IVH and SVH

d) Outer type
A type of rigid-flex printed wiring board, where a flexible section is formed on one side of an external layer. The flexible section contains a single conductor layer.

e) Undercut
The reduction of conductor cross-section on a printed circuit board, caused by etching (see Figure 2).

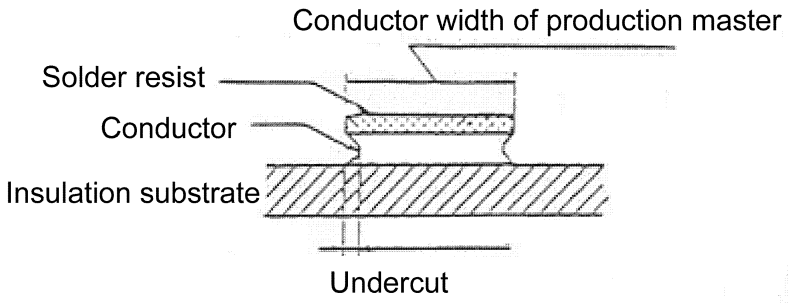

Figure 2. Undercut

f) Inner type
A type of rigid-flex printed wiring board, where a flexible section is formed on internal layers. The flexible section is constructed of one or more conductor layers.

g) Weave texture
A surface condition of base material in which a weave pattern of glass cloth is apparent.

h) Surface Via Hole (SVH)
A through hole connecting an external circuit layer and internal circuit layers of a multilayer printed wiring board, but not extending through all layers (see Figure 1).

i) Etchback
A process to remove the resin smear and further remove the insulator on the surface of the hole wall to the specific depth in order to expose the internal layer conductor.

j) Area Array Packaging
A large Scale Integrated (LSI) package for surface mounting, in which grid-like terminals are formed underneath the package as external connecting terminals.

k) Overhang
Increase in conductor width and the surface plating at the land or conductor edge is formed in an eaves shape.

l) Crazing
Continuous line of white spots in measling along a glass fiber.

m) Sub land
An auxiliary land to increase the reliability of connection between a conductor and land.

n) Small via holes
A through hole drilled with a maximum drill diameter of 0.5mm in general. This is used to provide an electrical interconnection between all layers, but in which there is no intention to insert a component lead. The small via holes make it possible to realize high density wiring (see Figure 1).

o) Sparkover
An insulation breakdown which results from air discharge.

p) Sliver
A thin strip of metal torn off from the overhang portion at a land or conductor edge.

q) Through hole
A hole drilled fully through the printed wiring board and formed by deposition of metal on its inside surface. This is used to provide an electrical interconnection between conductive patterns in different layers. Through holes include IVH, SVH and small via hole.

r) Original production master
An original master with a 1:1 scale pattern which is used to produce the production master.

s) Manufacturing drawing
A drawing which defines specifications and characteristics of printed wiring boards, such as a style, conductive pattern arrangement, hole structure, etching and finishing.

t) Solder resist
Coating ink applied to the surface of a printed wiring board where solder is not desired. This is intended to prevent bridges between patterns during soldering.

u) Dewetting
A condition which occurs when molten solder has coated a metal surface and then recedes before hardening, leaving irregularly shaped globules or granules of solder and a thin solder film.

v) Delamination
A separation between layers within the base material.

w) Copper-invar-copper (CIC)
A clad laminate of three metals; copper, invar (Fe_{64} Ni_{36} alloy) and copper.

x) Conductor
Circuitry formed by etching or plating. The conductor does not include a wire, unless specified.

y) Nail heading
The flared condition of copper on internal conductor layers of a multilayer printed wiring board, caused by hole drilling. This is formed in a nail head shape.

z) Negative Etchback
A etchback process to recess the conductor material of internal layer more than the insulation material around the hole.

aa) Nodule
A projection of plating which is formed inside a through hole during deposition.

ab) Non-plated-through hole
A hole drilled through the printed wiring board, which contains no plating on the hole wall. This hole is used as a mounting hole for inserting a screw and does not provide an electrical interconnection.

ac) Via hole
A through hole drilled with a drill diameter of 0.35mm to 0.5mm, used for higher density wiring (inner type). This is used to provide an electrical interconnection between all layers, but in which there is no intention to insert a component lead. The via holes make it possible to realize high density wiring.

ad) Non-functional land
A land which is not electrically interconnected to the conductive pattern on the same layer.

ae) Fusing
Homogeneous alloying process performed by heating a solder layer, after solder plating is applied as an etching resist for circuit forming.

af) Three patterns between basic grids
A design achieving a circuit density of three patterns of 0.13mm conductor width in 2.54mm spacing between basic grids (see Figure 3).

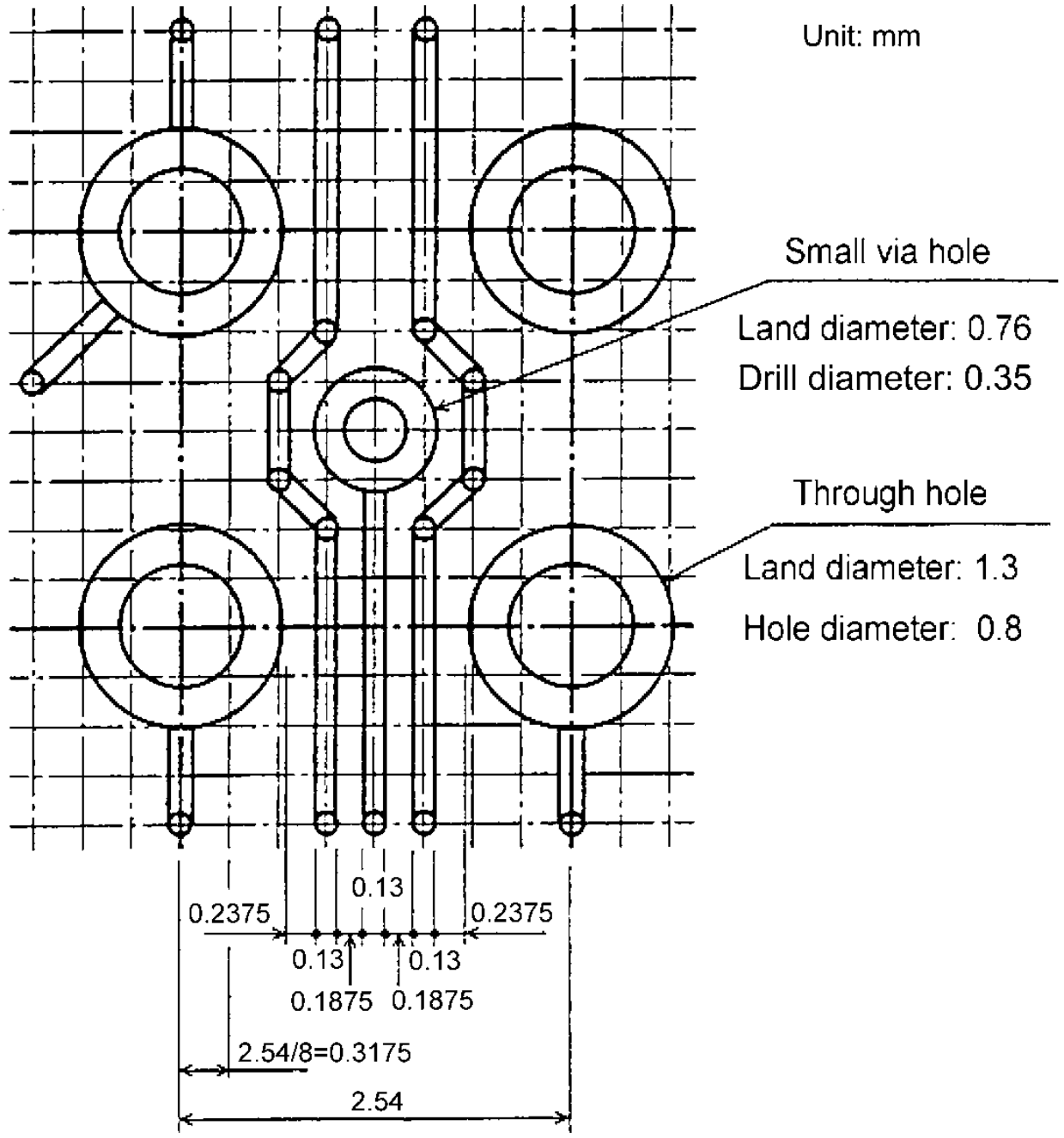

Figure 3. Three Patterns between Basic Grids

ag) Fine pitch printed wiring board
A printed wiring board which has a circuit density of three patterns (maximum) between basic grids. This enables surface mounting of QFP with 0.5mm lead pitch.

ah) Flashover
An insulation breakdown caused by a surface creepage. A discharge resulted from a short between electrodes is generally called all-path breakdown. Flashover is a type of all-path breakdown which occurs in gas, liquid or solid. Flashover is also called sparkover.

ai) Blister
A localized swelling and separation on the material surface caused by the pressure of air or gas entrapped within the laminate.

aj) Printed wiring board connectors
A component mounted on an edge of a printed wiring board, which is used to provide electrical connection with external equipment. The printed wiring board connectors are classified into two types, an indirect connector and a direct connector. An indirect connector (e.g. male connector) is attached on a printed wiring board and connected to a circuit of the board. This type is intended to provide connect mating with another connector (see Figure 4). A direct connector (one-part connector or edge-board connector) is intended for mating and interconnecting with edge board contacts on an edge of a printed wiring board (see Figure 5).

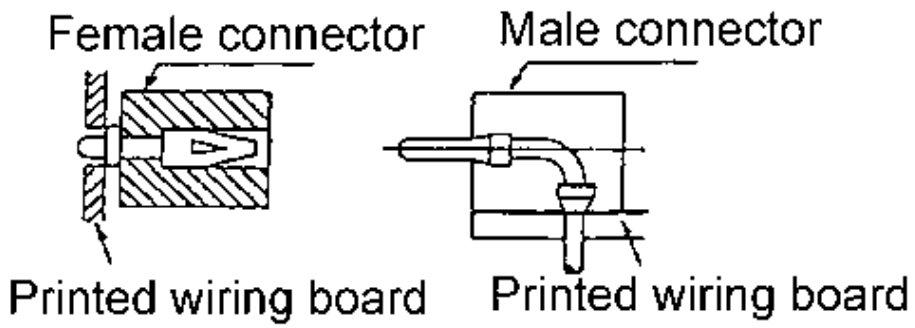

Figure 4. Indirect Connector

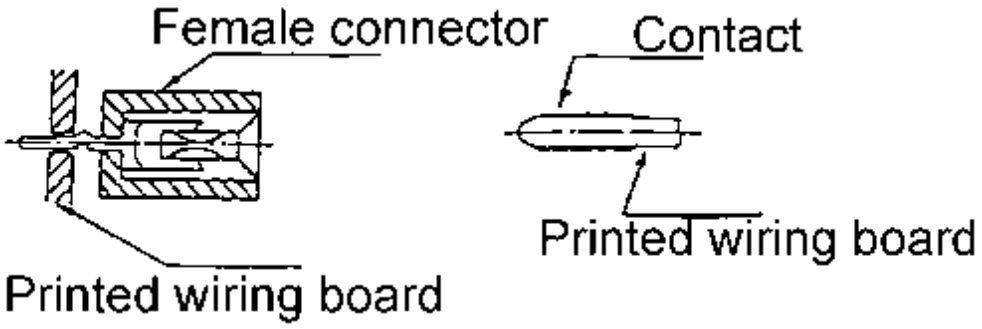

Figure 5. Direct Connector

ak) Rigid-flex printed wiring board
A printed wiring board using both rigid and flexible base materials.

al) Measling
Discrete white spots underneath the surface of the base material, which are caused by separation of glass fibers and resin material of a printed wiring board laminate.

am) Effective bonded conductor width
The width of a conductor adjacent to an insulating plate.

an) Work board
A board containing one or more printed wiring boards and test coupons, which is used for manufacturing products.

ao) Split board
The printed wiring board which can be divided into two or more after mounting or soldering. For easy division, the board has a deep-hole-shape slit, V-groove cut, continuous perforation or a combination of them.

ap) Land
A portion of a conductive pattern used for connecting a plated-through hole and a surface circuit or internal circuit.

aq) Resin smear
Resin transferred from the base material onto the wall of a through hole or portion used for connection. This is caused by softening or melting the base material due to the frictional heat during drilling.

ar) Resin recession
A void between the barrel of a plated-through hole and the wall of the hole, which is detected by microsectioning the printed wiring board.

APPENDIX A

**PRINTED WIRING BOARDS,
GLASS BASE WOVEN POLYIMIDE RESIN OR
GLASS BASE WOVEN EPOXY RESIN
BASE MATERIAL**

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX A

PRINTED WIRING BOARDS, GLASS BASE WOVEN POLYIMIDE RESIN OR GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL

A.1. General

A.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards which use glass base woven polyimide resin (GI) or glass base woven epoxy resin (GF) as a base material (hereinafter referred to as "printed wiring boards").

A.1.2 Classification

Products covered by this specification shall be classified as specified in Table A-1.

Table A-1. Classification

Base material	Construction	Remarks
Glass base woven epoxy resin	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
	Double-sided printed wiring board	
	Multilayer printed wiring board	
Glass base woven polyimide resin	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
	Double-sided printed wiring board	
	Multilayer printed wiring board	

A.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA(1) 2140/A 101 GF III 6(2)

101	GF	III	6(2)
Individual identification	Base material code (see A.1.3.1)	Processing code (see A.1.3.2)	Number of layers (see A.1.3.3)

Notes:

(1) "JAXA" indicates the part is for space use and may be abbreviated “J”.

(2) Number of conductor layers

A.1.3.1 Base Material Code

The base material code is as specified in Table A-2.

Table A-2. Base Material Code

Base material code(1)	Base material
GF	Glass base woven epoxy resin, compliant to IPC-4101 or JPCA/NASDA-SCL01
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

Note: (1) Applicable standards for GF and GI types are as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), shall be specified in the Application Data Sheet (ADS).

A.1.3.2 Processing Code

The processing code is as specified in Table A-3.

Table A-3. Processing Code

Processing code	Construction	Remarks
I	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
II	Double-sided printed wiring board	
III	Multilayer printed wiring board	

A.1.3.3 Number of Layers

The maximum number of layers shall be specified in each detail specification.

A.2. Applicable Documents

A.2.1 Reference Documents

The following documents are reference documents.

NHB 5300.4(3I) Requirements for Printed Wiring Boards

NHB 5300.4 (3K) Design Requirements for Rigid Printed Wiring Boards and Assemblies

A.3. Requirements

A.3.1 Qualification Coverage

Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs A.3.2 to A.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are

considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

A.3.2 Materials

The materials shall be specified as follows and as specified in paragraph 3.3.

A.3.2.1 Metal-Clad Laminate and Prepreg

The metal-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on the drawings. The base material shall be epoxy resin or polyimide resin (paragraph A.1.3.1). The nominal thickness of the base material shall be not less than 0.05mm. The metal foil for the outermost layer shall have a nominal thickness of a minimum of 18μm, and the metal foil for an internal layer shall have 35μm as a minimum. The applicable standards for the material used in the printed wiring boards shall be specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

A.3.2.2 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

A.3.2.3 Solder Resist

The solder resist applied on the printed wiring boards shall conform to IPC-SM-840 Class H or the equivalent.

A.3.2.4 Plating

As a rule, surface plating shall be electrolytic solder plating. If plating other than electrolytic solder plating is applied, the plating shall be selected from the types specified in this appendix. If plating other than electrolytic solder plating is partially required on the surface to be covered with electrolytic solder plating, the other plating shall be applied, followed by the electrolytic solder plating, in order to minimize the overlap of the two platings. All through holes shall be covered with copper plating and the same type surface plating as the plating applied on lands.

A.3.2.4.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

A.3.2.4.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

A.3.2.4.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table A-4. The electrolytic nickel plating specified in paragraph A.3.2.4.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.

Table A-4. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 percent
KNOOP hardness	91 to 129 (inclusive)

A.3.2.4.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.

A.3.2.4.5 Electrolytic Solder Plating

The electrolytic solder plating shall contain 50 to 70 percent tin and shall have the thickness specified in paragraph A.3.3.6 as a minimum before fusing. The fusing process shall be performed in the final stage of the manufacturing process of printed wiring boards.

A.3.2.5 Marking Ink

The marking shall be produced using epoxy resin base inks that do not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.

A.3.3 Design and Construction

A.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

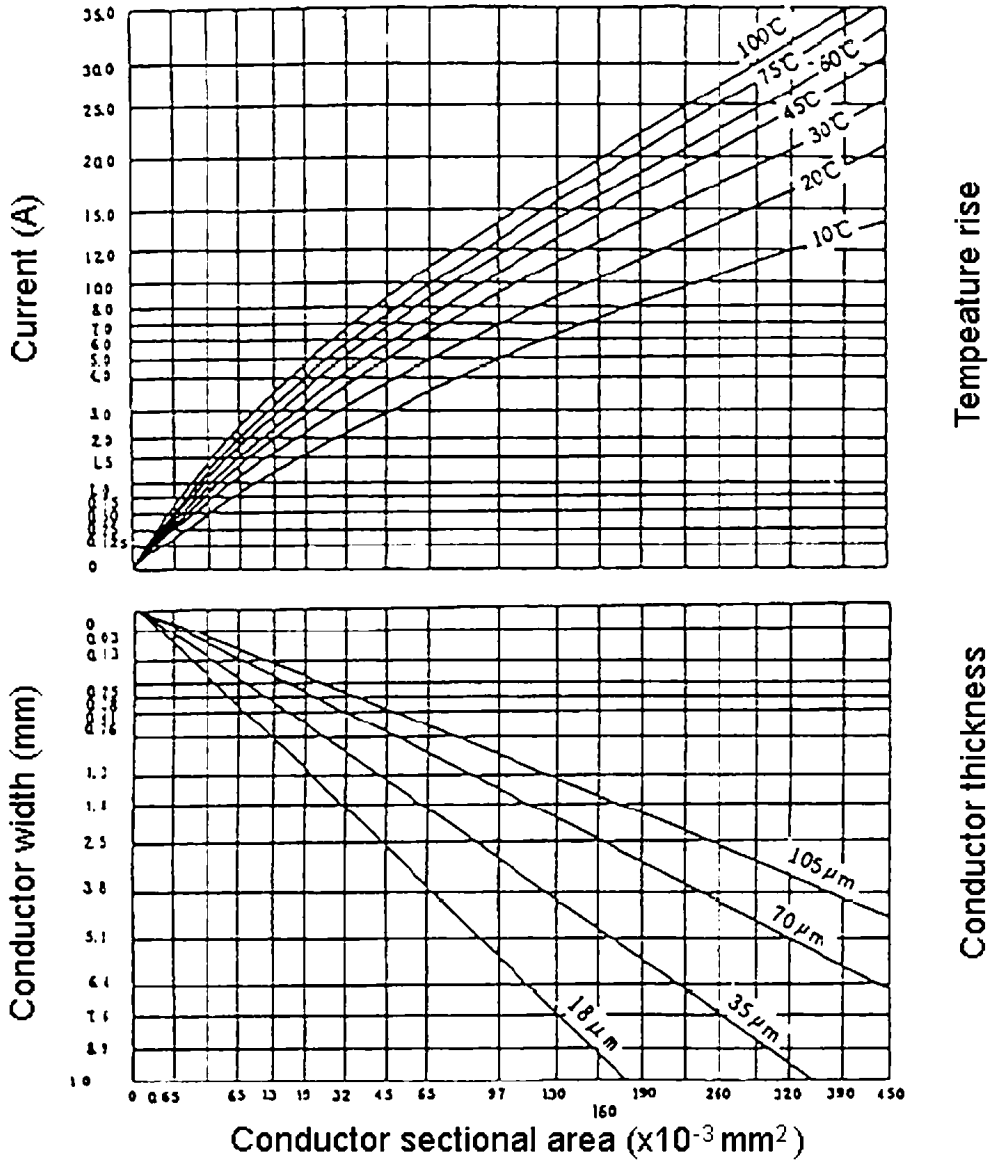
Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

A.3.3.2 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes.

A.3.3.3 Conductor Width

The design width of the conductor shall be not less than 0.20mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures A-1 and A-2.



Remarks:

(1) This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations due to etching techniques, conductor thickness and width and cross-sectional areas.

(2) Additional derating of 15 percent for the allowable current is suggested under the following conditions:
   a) Where dielectric layer thickness is less than 0.8mm.
   b) Where conductor thickness is greater than 105μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.

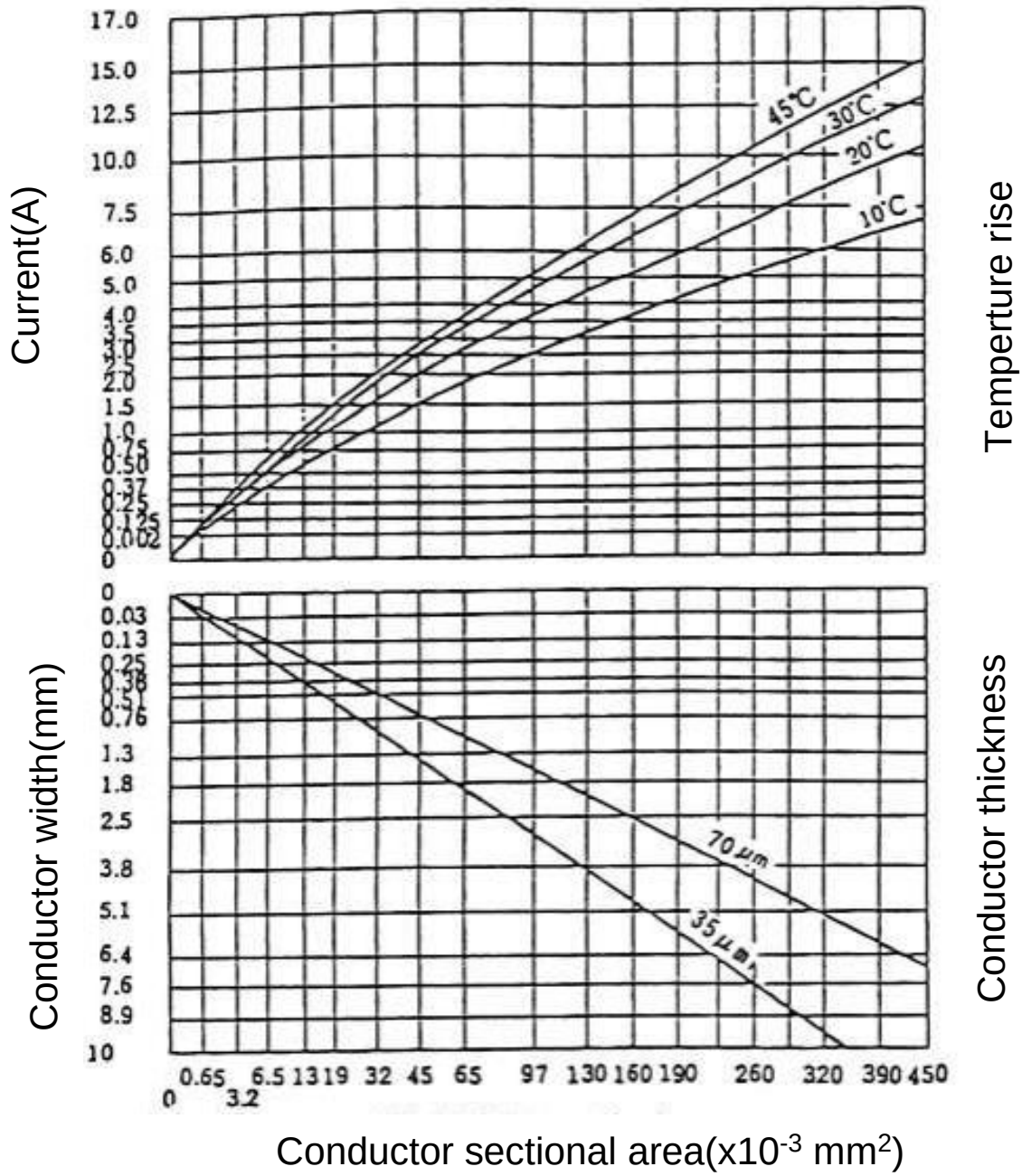
(4) For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperature rises.

(5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.

(6) The effect of heating due to heat generating parts is not considered.

(7) The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure A-1. Conductor Width (External Layer)



Remark: (1) Remarks (1) through (7) of Figure A-1 shall apply to this figure.

Figure A-2. Conductor Width (Internal Layer)

A.3.3.4 Conductor Spacing

The conductor spacing in design shall be not less than 0.20mm. The specific conductor spacing shall depend on the applied voltage as specified in Table A-5.

Table A-5. Conductor Spacing

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	
	External layer	Internal layer
0 - 100	0.20	0.20
101 - 300	0.48	0.30
301 - 500	0.86	0.35
501 or higher	(0.003xV)+0.1	(0.003xV)+0.1

A.3.3.5 Annular Ring

The design value for the annular ring of a plated-through hole shall be not less than 0.325mm at the conductor connecting area of an external layer and 0.3mm on an internal layer. The design value of the annular ring of a non-plated-through hole shall be a minimum of 0.55mm.

A.3.3.6 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table A-6.

Table A-6. Plating or Coating Thickness

Unit: μm

Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 25
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	Min. 5
Electrolytic solder	Min. 8 on surface Min. 4 inside a through hole
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.

A.3.3.7 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph A.3.10.2) and as specified in Table A-7.

Table A-7. Operating Temperature Range

Unit: °C

Base material	Temperature range
GF	-65 to +125
GI	-65 to +170

A.3.4 Externals, Dimensions, Marking and Others

A.3.4.1 Externals and Construction

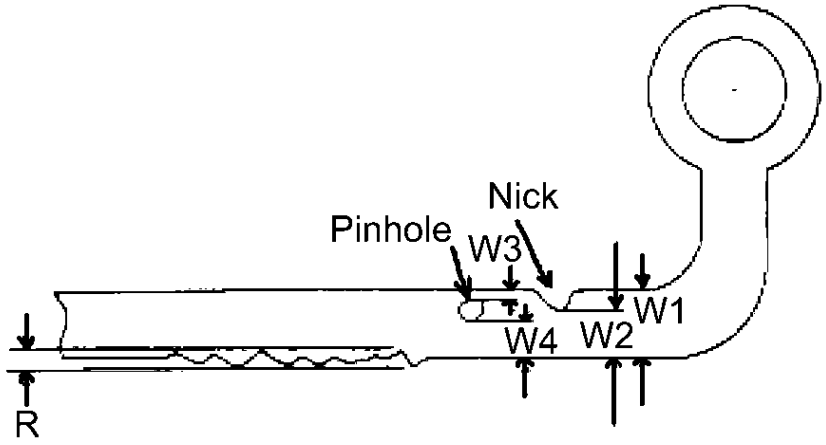
A.3.4.1.1 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

A.3.4.1.2 Conductor

a) All conductors of the printed wiring boards shall be formed by etching the metal foil or composed from etching and plating on a metal foil.

b) The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.1mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.13mm in the difference between the convex and concave portions in any range of 13mm in length (see Figure A-3).



Unit: mm

W1 ≥ (Minimum finished conductor width) ≥ 0.1
W2 ≥ 0.80×(Minimum finished conductor width) ≥ 0.1
W3+W4 ≥ 0.80×(Minimum finished conductor width) ≥ 0.1
R ≤ 0.13 in any range of 13 in length

Figure A-3. Conductor Defects

A.3.4.1.3 Minimum Annular Ring

When measured in accordance with paragraph A.4.4.2.2 f), the annular ring of a plated-through hole shall be not less than 0.13mm on an external layer and 0.05mm on an internal layer. The annular ring of a non-plated-through hole shall be not less than 0.38mm and contain no defects.

A.3.4.1.4 Electrolytic Solder Plating

The electrolytic solder plating shall be uniform, free from pinholes or pits, and completely cover conductive patterns after fusing. This provision shall not apply to vertical conductor edges.

A.3.4.1.5 Solder Coating

The solder coating shall be uniform, free from pinholes or pits, and completely cover conductive patterns. This provision shall not apply to vertical conductor edges.

A.3.4.1.6 Edges of Printed Wiring Board

There shall be no nicks, cracks or peeling at edges of the printed wiring boards.

A.3.4.1.7 Surface of Printed Wiring Board

On the surface of the printed wiring boards, there shall be no cracks or peeling from the portions around holes.

A.3.4.1.8 Measling, Crazing and Delamination

The printed wiring boards shall exhibit no delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board and the spacing between conductors which have no electrical continuity is not reduced exceeding 25 percent. Crazing along edges of the printed wiring boards shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

A.3.4.1.9 Solder Resist

The solder resist shall completely cover the range of conductors specified on drawings. Visual damage such as significant thin spots or uneven color shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the manufacturing drawings.

A.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table A-8.

Table A-8. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	$^{+0.10}_{-0.15}$ for any hole diameter
Conductor width	±0.10 for any conductor width
Conductor spacing	-0.10 for any conductor spacing. The positive side tolerance is not specified. The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

A.3.4.3 Marking

The marking shall be produced with the marking ink specified in paragraph A.3.2.5 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.
All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

A.3.4.4 Through Holes

When printed wiring boards are tested as specified in paragraph A.4.4.2.2, the plating inside through holes shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall be acceptable, provided that the hole diameter is not reduced below its lower limit specified on drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 80μm and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure A-4).

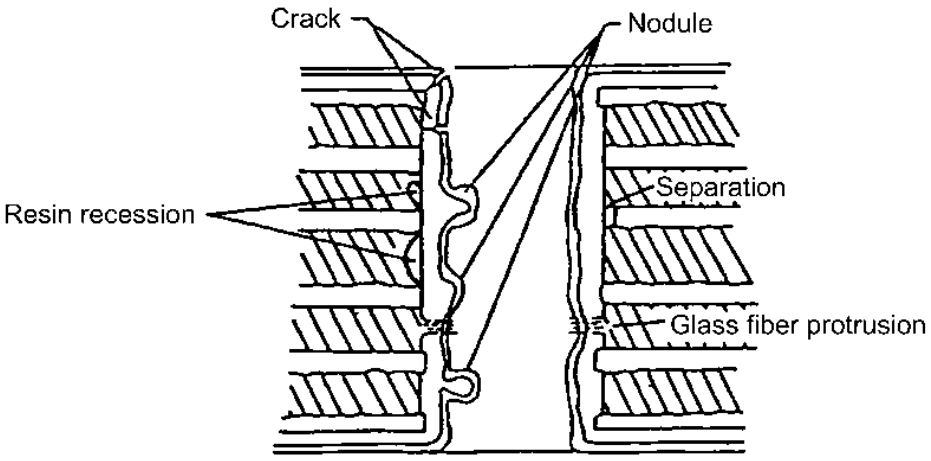


Figure A-4. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure A-5).

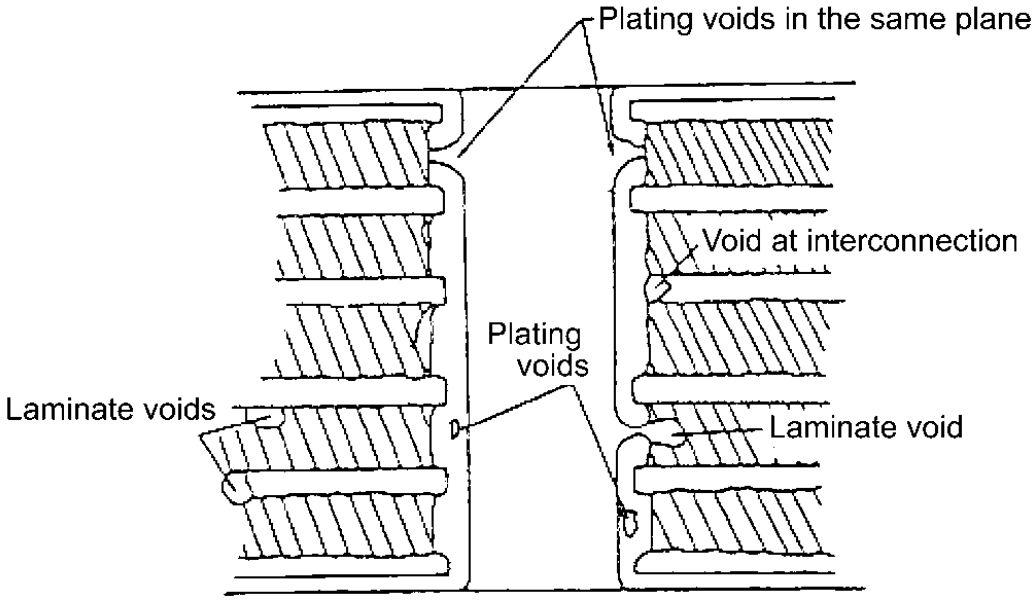


Figure A-5. Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure A-6).

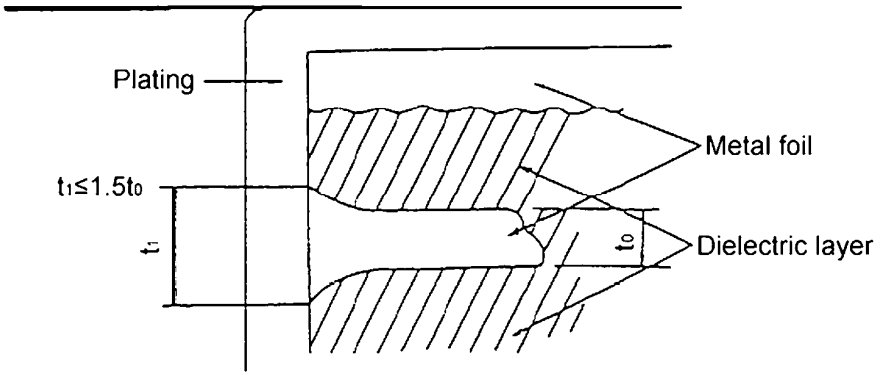


Figure A-6. Nail Heading

c) Layer-to-layer registration
The layer-to-layer registration error shall not exceed 0.35mm.

d) Dielectric layer thickness
The dielectric layer between conductor layers of a multilayer printed wiring board shall be not less than 0.08mm in thickness.

e) Plating thickness
The plating thickness shall meet the requirements specified in paragraph A.3.3.6.

f) Annular ring
The annular ring shall meet the requirements specified in paragraph A.3.4.1.3.

A.3.5 Workmanship

Printed wiring boards shall not exhibit defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could adversely affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

A.3.5.1 Bow and Twist

When printed wiring boards are tested as specified in paragraph A.4.4.3.1, the maximum limit for bow and twist shall be 1.5 percent, unless otherwise specified on manufacturing drawings.

A.3.5.2 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.

A.3.6 Plating Adhesion and Overhang

When printed wiring boards are tested as specified in paragraph A.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

A.3.7 Cleanliness

When printed wiring boards are tested as specified in paragraph A.4.4.5, there shall be no ionic contamination. The resistivity of the solvent extract shall be not less than $2\times10^{6}\Omega\cdot cm$.

A.3.8 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

A.3.8.1 Dielectric Withstanding Voltage

When printed wiring boards are tested as specified in paragraph A.4.4.6.1, there shall be no insulation breakdown, flashover or sparkover.

A.3.8.2 Circuitry

A.3.8.2.1 Continuity

When printed wiring boards are tested as specified in paragraph A.4.4.6.2 a), there shall be no open circuits between circuit patterns.

A.3.8.2.2 Circuit Shorts

When printed wiring boards are tested as specified in paragraph A.4.4.6.2 b), there shall be no circuit shorts between circuit patterns.

A.3.8.3 Connection Resistance

When printed wiring boards are tested as specified in paragraph A.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \cdot t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)

l: Distance between lands (mm)

W: Conductor width (mm)

t: Conductor thickness (mm)

A.3.9 Mechanical Performance

Printed wiring board shall meet the following mechanical requirements.

A.3.9.1 Terminal Pull Strength

When tested as specified in paragraph A.4.4.7.1, printed wiring boards shall meet the following requirements.

a) Bond strength
The land shall withstand 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph A.4.4.2.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with paragraph A.4.4.2.2 a), there shall be no cracks, blistering, measling or delamination.

A.3.9.2 Solderability

A.3.9.2.1 Hole Solderability

When printed wiring boards are tested as specified in paragraph A.4.4.7.2 a), the through hole inside wall and land surface shall exhibit proper wetting of solder.

A.3.9.2.2 Surface Solderability

When printed wiring boards are tested as specified in paragraph A.4.4.7.2 b), a minimum 95 percent of the surface conductor area shall be covered uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated at a point.

A.3.10 Environmental Performance

Printed wiring board shall meet the following environmental requirements.

A.3.10.1 Thermal Shock

A.3.10.1.1 Thermal Shock (I) (applicable to qualification test)

When printed wiring boards are tested as specified in paragraph A.4.4.8.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph A.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

A.3.10.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed wiring boards are tested as specified in paragraph A.4.4.8.1 b), there shall be no open circuits, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph A.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

A.3.10.2 Humidity and Insulation Resistance

When printed wiring boards are tested as specified in paragraph A.4.4.8.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be not less than 500MΩ.

A.3.10.3 Hot Oil Resistance

When printed wiring boards are tested as specified in paragraph A.4.4.8.3, the change in connection resistance between circuits before and after the test shall be less than 10 percent.

A.3.10.4 Thermal Stress

When tested as specified in paragraph A.4.4.8.4, printed wiring boards shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Copper foil
There shall be no cracks in internal copper foils in the vertical microsection of through holes.

c) Laminate voids
Laminate voids with the longest dimension of a maximum of 76μm shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings.

A.3.10.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph A.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph A.3.8.1 shall be satisfied.

A.4. Quality Assurance Provisions

A.4.1 In-Process Inspection

The in-process inspection shall be as specified in Table A-9.

Table A-9. In-Process Inspection

No.	Inspection item	Requirement paragraph	Test method paragraph	Quantity of samples	
				Production printed wiring board	Test coupon
1	Externals, construction and dimensions of internal layers		A.4.4.2.1	100%	100%
	Metal-clad laminate and prepreg	A.3.2.1			
	Conductor spacing	A.3.3.4			
	Annular ring	A.3.3.5			
	Conductive pattern	A.3.4.1.1			
	Conductor	A.3.4.1.2			
	Surface of printed wiring board	A.3.4.1.7			
	Dimensions	A.3.4.2			
	Workmanship(1)	A.3.5			
2	Cleanliness(2)	A.3.7	A.4.4.5	2(3)	—

Notes:
(1) The requirements specified in paragraph A.3.5.1 are not applied.
(2) The cleanliness inspection shall be performed for the production printed wiring boards which are to be coated with solder resist, immediately before the application of solder resist.
(3) Two production printed wiring boards shall be selected from the lot which is to be coated with solder resist at the same time.

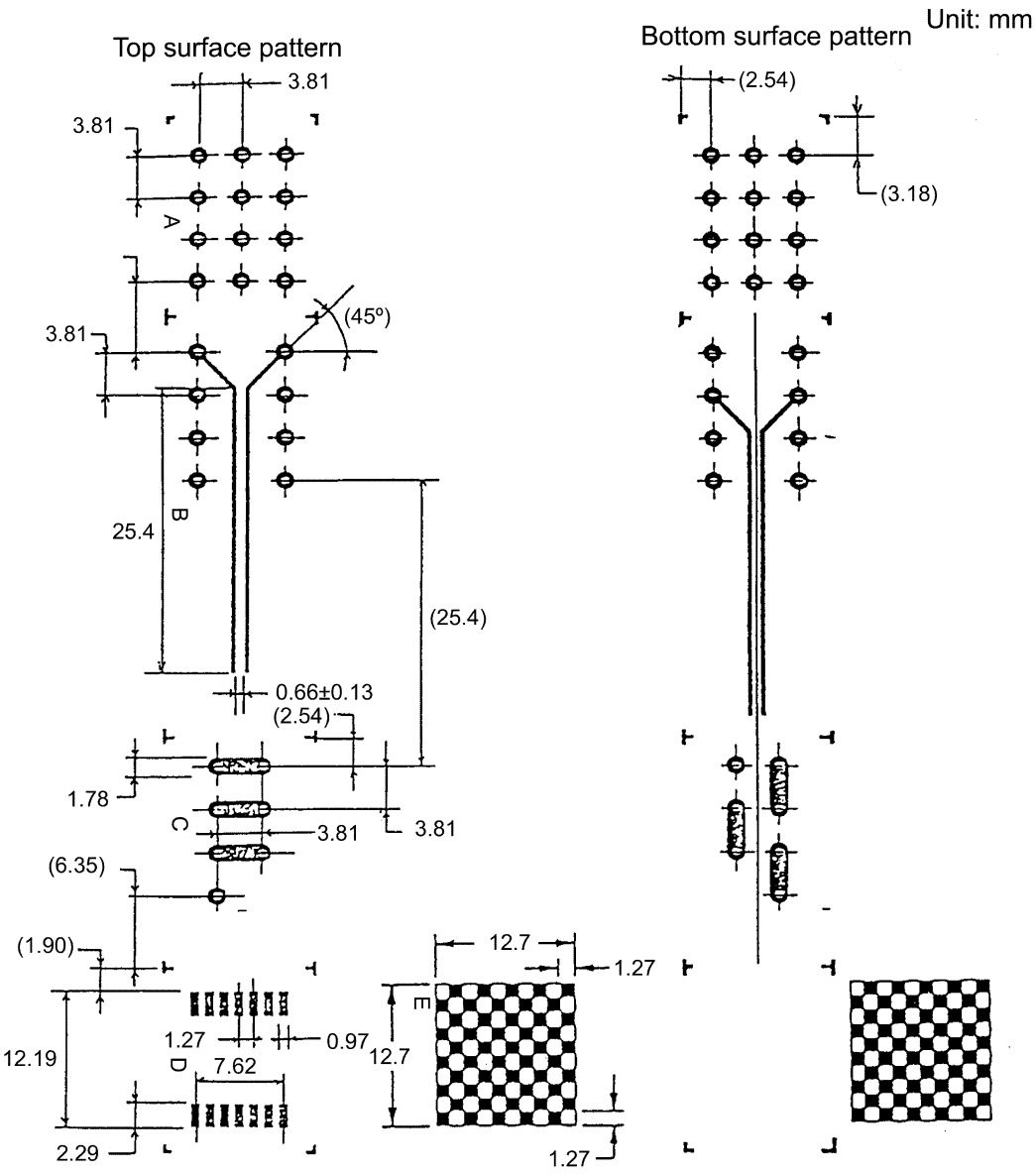
A.4.2 Qualification Test

A.4.2.1 Sample

Samples shall be approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure A-7 for single-sided or double-sided printed wiring boards and Figure A-8 for multilayer printed wiring boards.

A.4.2.2 Test Items and Number of Samples

Tests of each group shall be performed in the order listed in Table A-10. Upon completion of Group I and II tests, Group III through VIII tests shall be performed as specified in Table A-10, using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order shown in Table A-10. The sample shall include six production printed wiring boards and one for each test coupon.



Notes:

(1) For the test coupons except for coupon A, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter shall be the minimum hole diameter of the corresponding printed wiring board. For the test coupon A, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land.
All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

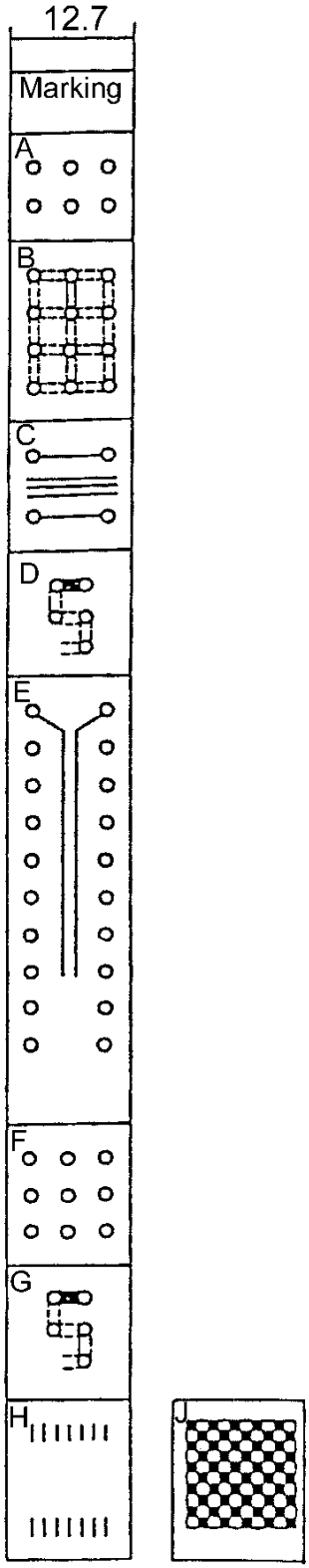
(2) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(3) The dimensions in the parentheses are reference dimensions.

(4) Solder resist shall apply to both sides of the test coupon E, only when solder resist is required for the products.

Figure A-7. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board)

Arrangement of Test Coupons



Unit: mm

Notes:

(1) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(2) For the test coupons of A and B, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the hole diameter shall be the maximum hole diameter of the corresponding minimum lands.
For the test coupons of B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(3) The test coupons of D, E and G are different in the number of conductors, depending on the number and construction of layers. Therefore, the conductors shall be formed on all layers in accordance with this figure.

(4) The arrangement of test coupons shown in this appendix is an example; a different arrangement is also acceptable.

(5) The symbols of test coupons (A to H and J) shall be used for identification and not for the object of inspection. The marking method is not specified.

(6) Solder resist shall apply to only the test coupon J.

Figure A-8. Test Coupons (for Multilayer Printed Wiring Board) (1/3)

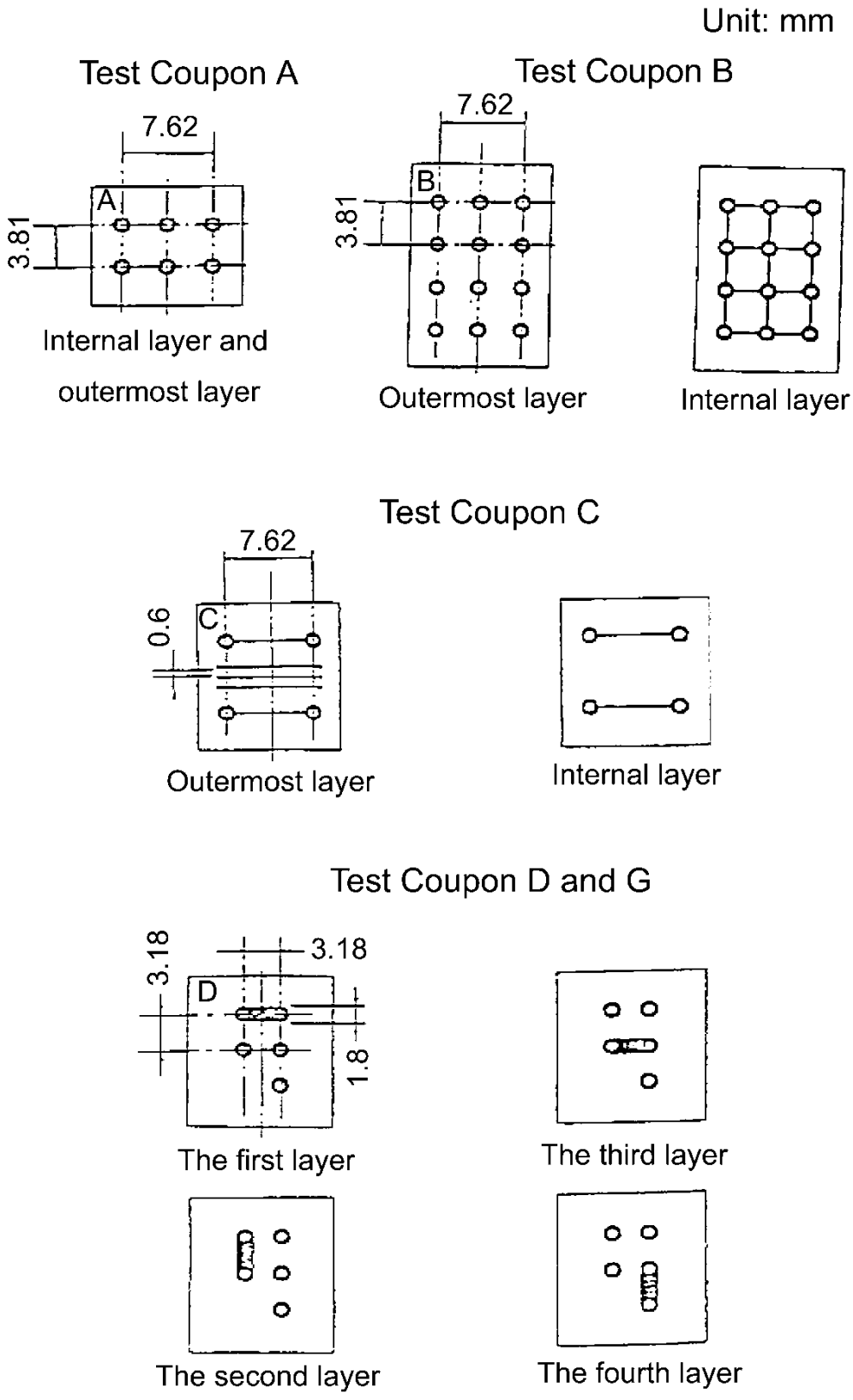
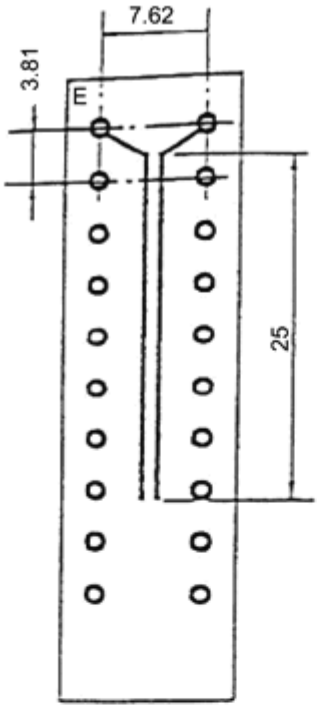


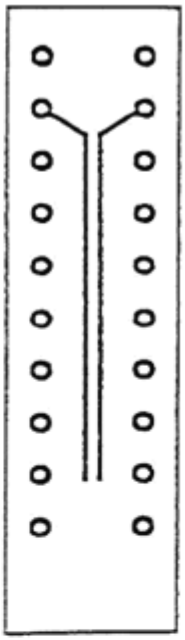
Figure A-8. Test Coupons (for Multilayer Printed Wiring Board) (2/3)

Unit: mm

Test Coupon E

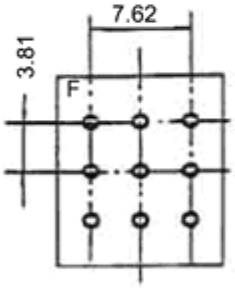


Outermost layer



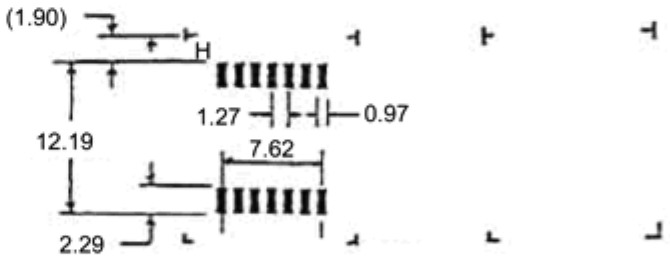
Internal layer

Test Coupon F



Internal layer and outermost layer

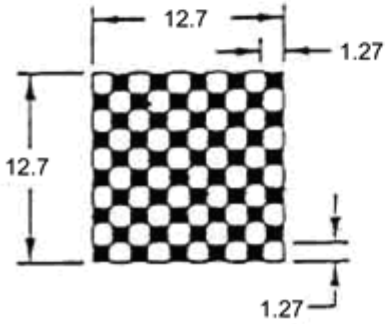
Test Coupon H



Top surface

Bottom surface

Test Coupon J



Top surface and bottom surface

Figure A-8. Test Coupons (for Multilayer Printed Wiring Board) (3/3)

Table A-10. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail		
					Samples[1]		Quantity of allowable defects
Group	Order	Test item			Production printed wiring boards	Test coupon[2]	
I	1	Design and construction Interlayer connection Conductor width Conductor spacing Annular ring	 A.3.3.2 A.3.3.3 A.3.3.4 A.3.3.5	A.4.4.2	No. 1 to No. 6	A, B, C, D, E, F, G H,Kand L[3]	0
	2	Externals, dimensions, marking and others Design and construction Dimensions Marking	 A.3.4.1 A.3.4.2 A.3.4.3	A.4.4.2.1			
	3	Workmanship[4]	A.3.5	A.4.4.3			
II	1	Plating adhesion and overhang	A.3.6	A.4.4.4	No. 1 to No. 6	C	
	2	Bow and twist	A.3.5.1	A.4.4.3.1		N/A	
III	1	Through holes	A.3.4.4	A.4.4.2.2	No. 1	A or F	
	2	Terminal pull strength	A.3.9.1	A.4.4.7.1		A or F	
IV	1	Connection resistance	A.3.8.3	A.4.4.6.3	No. 2	D	
	2	Hot oil resistance	A.3.10.3	A.4.4.8.3			
	3	Connection resistance	A.3.8.3	A.4.4.6.3			
V	1	Circuitry Continuity Circuit shorts	 A.3.8.2.1 A.3.8.2.2	 A.4.4.6.2 a) A.4.4.6.2 b)	No. 3	 G E	
	2	Connection resistance	A.3.8.3	A.4.4.6.3		G	
	3	Thermal shock (I)	A.3.10.1.1	A.4.4.8.1 a)		E and G	
	4	Circuitry Continuity Circuit shorts	 A.3.8.2.1 A.3.8.2.2	 A.4.4.6.2 a) A.4.4.6.2 b)		 G E	
	5	Connection resistance	A.3.8.3	A.4.4.6.3		G	
VI	1	Humidity and insulation resistance	A.3.10.2	A.4.4.8.2	No. 4	E	
	2	Dielectric withstanding voltage	A.3.8.1	A.4.4.6.1			
VII	1	Thermal stress	A.3.10.4	A.4.4.8.4	No. 5	B	
	2	Solderability Hole solderability Surface solderability	 A.3.9.2.1 A.3.9.2.2	 A.4.4.7.2 a) A.4.4.7.2 b)		 B[3] H	
VIII	1	Radiation hardness	A.3.10.5	A.4.4.8.5	No.6	-	
-	1	Materials	A.3.2	N/A	[5]		N/A

Notes:

[1] The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above.

[2] Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

[3] The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

[4] Bow and twist (paragraph A.3.5.1) of the samples shall be tested during the second test of Group II tests.

[5] Data to certify compliance with design specifications shall be submitted.

A.4.3 Quality Conformance Inspection

A.4.3.1 Quality Conformance Inspection (Group A)

A.4.3.1.1 Sample

The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be manufactured simultaneously and one test coupon is subjected to each of Group IV and V tests.

A.4.3.1.2 Inspection Items and Sample Size

The items and test order of Group A inspection shall be in accordance with Table A-11. The inspections within each group shall be performed in the order listed.

Table A-11. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail		
					Quantity of samples(1)		
Group	Order	Inspection item			Production printed wiring boards	Test coupon(1)	Quantity of allowable defects
I	1	Externals, dimensions, marking and others Design and construction Dimensions Marking	A.3.4.1 A.3.4.2 A.3.4.3	A.4.4.2.1	All	N/A	0
	2	Workmanship(2)	A.3.5	A.4.4.3			
II	1	Bow and twist	A.3.5.1	A.4.4.3.1	All	N/A	
III	1	Circuitry	A.3.8.2	A.4.4.6.2	All	N/A	
IV	1	Thermal stress	A.3.10.4	A.4.4.8.4	N/A	B (A)	
	2	Through hole Conductive interface Plating thickness	A.3.4.4 b) A.3.4.4 e)	A.4.4.2.2	N/A	B (A)	
V	1	Solderability Hole solderability Surface solderability	A.3.9.2.1 A.3.9.2.2	A.4.4.7.2 a) A.4.4.7.2 b)	N/A	B (A) H (D)	

Notes:

(1) A letter in the parentheses indicates the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

(2) Bow and twist (paragraph A.3.5.1) of the samples shall be tested during the first test of Group II tests.

A.4.3.2 Quality Conformance Inspection (Group B)

A.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

A.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table A-12. The inspections within each group shall be performed in the order listed. Test coupons and products shall be manufactured simultaneously and one test coupon shall be subjected to each of Group I and IV tests and two test coupons shall be subjected to each of Group II and III tests.

Table A-12. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	A.3.6	A.4.4.4	C	0
II	1	Terminal pull strength	A.3.9.1	A.4.4.7.1	F	
	2	Connection resistance	A.3.8.3	A.4.4.6.3	D	
	3	Hot oil resistance	A.3.10.3	A.4.4.8.3		
	4	Connection resistance	A.3.8.3	A.4.4.6.3		
III	1	Connection resistance	A.3.8.3	A.4.4.6.3	G	
	2	Thermal shock (II)	A.3.10.1.2	A.4.4.8.1 b)	E and G	
	3	Circuitry				
		Continuity	A.3.8.2.1	A.4.4.6.2 a)	G	
		Circuit shorts	A.3.8.2.2	A.4.4.6.2 b)	E	
	4	Connection resistance	A.3.8.3	A.4.4.6.3	G	
IV	1	Humidity and insulation resistance	A.3.10.2	A.4.4.8.2	E	
	2	Dielectric withstanding voltage	A.3.8.1	A.4.4.6.1		

A.4.4 Methods for Test and Inspection

A.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 20% to 80%, and a luminance of 750 lx as a minimum.

A.4.4.2 Externals, Dimensions, Marking and Others

A.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of printed wiring boards shall be tested. External surfaces shall be inspected visually.

a) Conductive patterns and edges
Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument with a sufficient accuracy.

b) Annular ring
Annular rings on the external layer shall be measured from the internal surface

(within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular rings shall be measured using an optical measuring instrument of a sufficient accuracy.

A.4.4.2.2 Through Holes

a) Vertical microsection
The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, base material thickness and plating thickness) at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned in parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board's length direction.

b) Horizontal microsection
Only multilayer boards shall be subjected to the horizontal microsection inspection. Multilayer boards with through holes shall be encapsulated and polished. A conductor layer shall be polished in the parallel direction. The microsection is prepared to expose the conductor layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X.

c) Plating thickness
The plating thickness shall be measured using microsections prepared in accordance with paragraph A 4.4.2.2 a) at a magnification of minimum 200X. Measurements shall be averaged from three determinations for a plated-through hole. Isolated thick or thin sections shall not be used for averaging.

d) Layer-to-layer registration
The layer-to-layer registration shall be measured at a magnification of 25 to 100X using microsections prepared in accordance with paragraph A.4.4.2.2 a). The misregistration shall be inspected around the hole in the direction parallel to the board length and the vertical direction (see Figure A-9).

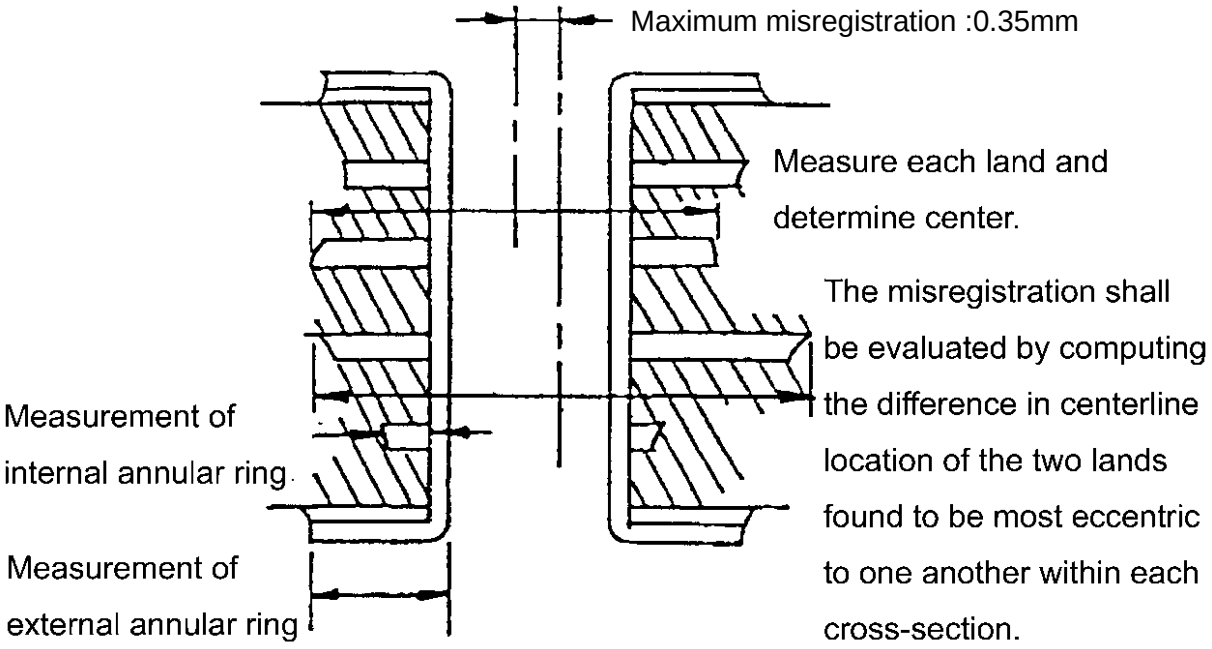


Figure A-9. Measurement of Layer-to-Layer Registration and Annular Ring

e) Dielectric layer thickness

The dielectric layer thickness shall be measured using microsections prepared in accordance with paragraph A.4.4.2.2 a).

f) Annular ring

The annular ring shall be measured using microsections prepared in accordance with paragraph A.4.4.2.2 a). The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure A-9).

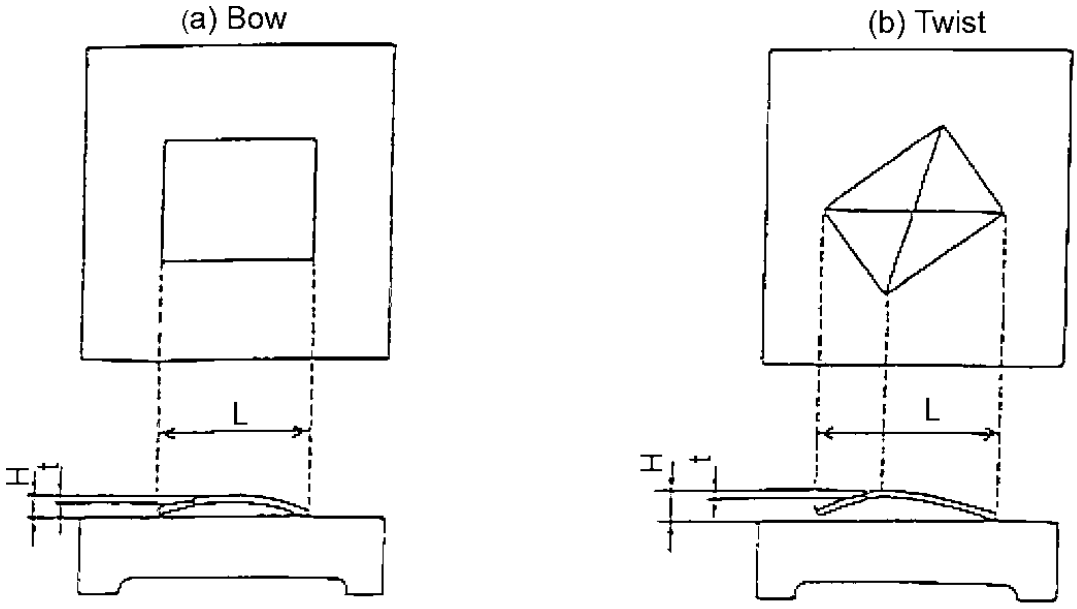
A.4.4.3 Workmanship

The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

A.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure A-10). The percent bow and twist shall be calculated by the following formula.

$$\text{Percent bow and twist} = \frac{H\text{-}t}{L} \times 100\ (\%)$$



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure A-10. Measurement of Bow and Twist

A.4.4.4 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and minimum 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

A.4.4.5 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 percent by volume of isopropyl alcohol and 25 percent by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6 \Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table A-13 may be used to perform the cleanliness test.

Table A-13. Equivalent Factors

Method	Resistivity ($\times 10^6 \Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.20
Ionograph(2)	2	2.01	3.10
Ion Chaser(3)	2	3.25	3.81

Notes:
(1) Alpha Metals Incorporated, “Omega Meter”
(2) Alpha Metals Incorporated, “Ionograph”
(3) E. I. Dupont Company, Incorporated, “Ion Chaser”

A.4.4.6 Electrical Performance

The electrical performance tests shall be performed as follows.

A.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $1000V_{AC}$ peak or $1000V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

A.4.4.6.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity.
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

A.4.4.6.3 Connection Resistance

The resistance between the through hole terminals shall be measured using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5mΩ.

A.4.4.7 Mechanical Performance

The mechanical performance tests shall be performed as follows.

A.4.4.7.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.
Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

A.4.4.7.2 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph A.4.4.8.4.
b) Surface solderability
After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of

25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

A.4.4.8 Environmental Performance

The environmental performance tests shall be performed as follows.

A.4.4.8.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
   1) For GF base material
      The test shall be performed under the test condition B. The low temperature shall be -30°C and the high temperature shall be +125°C. The time for step 2 and 4 shall be within 2 minutes each, and the number of cycles shall be 1000.
   2) For GI base material
      The test shall be performed under the test condition F. The low temperature shall be -30°C and the high temperature shall be +150°C. The time for step 2 and 4 shall be within 2 minutes each, and the number of cycles shall be 1000.
b) Thermal shock (II) (applicable to quality conformance inspection)
   1) For GF base material
      The test shall be performed under the test condition B-3. The time for step 2 and 4 shall be within 2 minutes each.
   2) For GI base material
      The test shall be performed under the test condition F-3. The high temperature shall be +170°C, and the time for step 2 and 4 shall be within 2 minutes each.

A.4.4.8.2 Humidity and Insulation Resistance

The tests shall be performed in the following order.

a) Humidity resistance
   The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed in 10 cycles. The polarization voltage shall not be applied. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.
b) Insulation resistance
   The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

A.4.4.8.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C

for 5 seconds and cooled to room temperature. Immersion and cooling shall be performed for 10 cycles.

A.4.4.8.4 Thermal Stress

The specimen shall be conditioned by drying for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 percent maintained at 288±5°C for a period of 10 seconds. After thermal stressing, the specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for cracks on the internal copper foil and laminate voids using the microsection prepared in accordance with A.4.4.2.2 a). Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

A.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with A.4.4.6.1 and A.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

APPENDIX B

**FINE PITCH PRINTED WIRING BOARDS,
GLASS BASE WOVEN POLYIMIDE RESIN OR
GLASS BASE WOVEN EPOXY RESIN
BASE MATERIAL**

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX B

**FINE PITCH PRINTED WIRING BOARDS,
GLASS BASE WOVEN POLYIMIDE RESIN OR
GLASS BASE WOVEN EPOXY RESIN
BASE MATERIAL**

B.1. General

B.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the fine pitch printed wiring boards which use glass base woven polyimide resin (GI) or glass base woven epoxy resin (GF) as a base material (hereinafter referred to as "printed wiring boards").

B.1.2 Classification

Products covered by this specification shall be classified as specified in Table B-1.

Table B-1. Classification

	Base material	Construction	Remarks
Classification	Glass base woven epoxy resin	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
		Double-sided printed wiring board	
		Multilayer printed wiring board	
	Glass base woven polyimide resin	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
		Double-sided printed wiring board	
		Multilayer printed wiring board	

B.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA(1) 2140/B <u>101</u> <u>GF</u> <u>III</u> <u>4</u>(2) <u>Y</u>

Individual identification	Base material code (B.1.3.1)	Processing code (B.1.3.2)	Number of layers (B.1.3.3)	Heat resistance (B.1.3.4)

Notes:
(1) "JAXA" indicates the part is for space use and may be abbreviated “J”.
(2) Number of conductor layers

B.1.3.1 Base Material Code

The base material code is as specified in Table B-2.

Table B-2. Base Material Code

Base material code(1)	Base material
GF	Glass base woven epoxy resin, compliant to IPC-4101 or JPCA/NASDA-SCL01
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

Note: (1) Applicable standards for GF and GI types are as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), are as specified in the Application Data Sheet (ADS).

B.1.3.2 Processing Code

The processing code is as specified in Table B-3.

Table B-3. Processing Code

Processing code	Construction	Remarks
I	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
II	Double-sided printed wiring board	
III	Multilayer printed wiring board	

B.1.3.3 Number of Layers

The maximum number of layers shall be specified in each detail specification.

B.1.3.4 Heat Resistance

Classification of printed wiring boards by heat resistance shall be specified in Table B-4.

Table B-4. Heat Resistance and Thermal Shock

Base material code	Heat resistance	Thermal shock	
		Temperature range (°C)	Number of cycles
GF	No code	-30 to +125	1,000
	Y(1)	-30 to +125	800
		-30 to +100	1,000
GI	No code	-30 to +150	1,000
	Y(1)	-30 to +150	800
		-30 to +125	1,000

Note: (1) The printed wiring boards shall meet two test conditions for heat resistance.

B.2. Applicable Documents

B.2.1 Reference Documents

The reference documents shall be as specified in paragraph 2.2.

B.3. Requirements

B.3.1 Qualification Coverage

Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs B.3.2 to B.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. Test data taken using samples with the same base and the same metal foil may be used as test data for samples with a different number of layers except for the thermal shock test. In this case the sample shall have more layers than the samples for qualification test. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

B.3.2 Materials

The materials shall be specified as follows and as specified in paragraph 3.3.

B.3.2.1 Metal-Clad Laminate and Prepreg

The metal-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The base material shall be epoxy resin or polyimide resin (paragraph B.1.3.1). The nominal thickness of the base material shall be not less than 0.05mm. The metal foil shall be copper regardless of the base material type. The copper foil for the outermost layer shall have a thickness of 18μm (nominal) as a minimum in consideration of additional conductor thickness for plating. Only when printed wiring boards have surface via holes (SVH), the copper foil for the outermost layer shall have an additional thickness of 9μm (nominal) as a minimum. The copper foil for an internal layer shall have a nominal thickness of 35μm as a minimum. However, it shall be a minimum of 18μm (nominal) in consideration of additional conductor thickness for plating, only when interstitial vial holes (IVH) and SVH are provided. The applicable standards for the material used in the printed wiring boards shall be specified in each detail specification. Details of GI base material, including type and the glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

B.3.2.2 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

B.3.2.3 Solder Resist

The solder resist applied on the printed wiring boards shall conform to IPC-SM-840 Class H or the equivalent. The application shall be in accordance with manufacturing drawings.

B.3.2.4 Marking Ink

The marking shall be produced using epoxy resin base ink that does not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

B.3.2.5 Plating

Unless otherwise specified the solder coating specified in paragraph B.3.2.2 shall be applied to all through holes (excluding IVH, SVH and small via holes), lands and surface conductive patterns, except for where solder resist is applied. All through holes except IVH and SVH shall be coated with copper plating and subsequently with the same type surface plating as the plating applied on lands. When plating other than the plating applied on lands is partially required in through holes except for the fine pith patterns, electrolytic gold plating may be applied.

B.3.2.5.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

B.3.2.5.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

B.3.2.5.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table B-5. The electrolytic nickel plating specified in paragraph B.3.2.5.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.

B.3.2.5.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.

Table B-5. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 percent
KNOOP hardness	91 to 129 (inclusive)

B.3.3 Design and Construction

B.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

B.3.3.2 Connector for Printed Wiring Boards

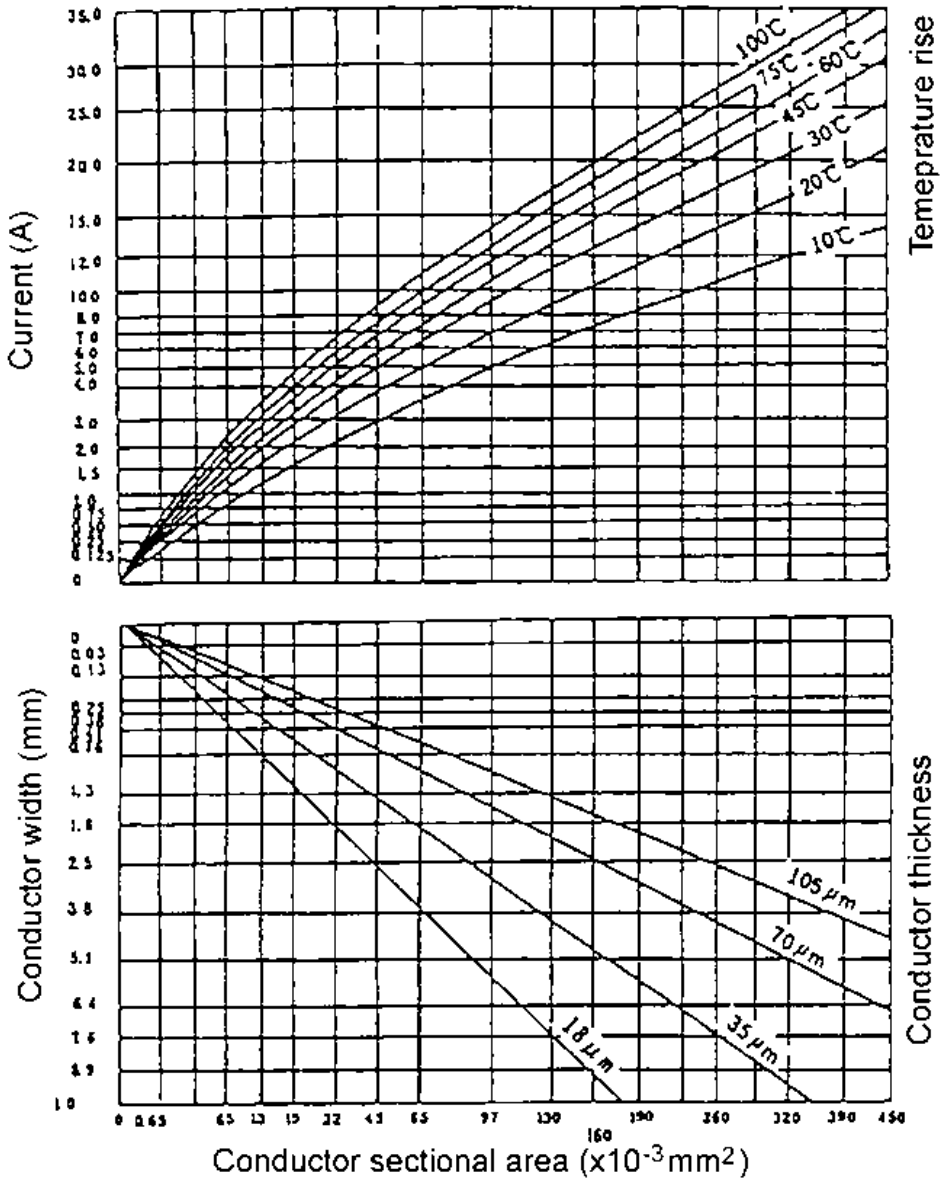
A direct connector (one-part connector or edge-board connector) shall not be used.

B.3.3.3 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes including small via holes, IVH and SVH. The small via holes shall be a minimum of 0.35mm in its drill diameter. The IVH and SVH shall have a minimum of 0.2mm in their drill diameters.

B.3.3.4 Conductor Width

The design width of the conductor shall be not less than 0.13mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures B-1 and B-2.



Remarks:

(1) This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations due to etching techniques, conductor thickness and width and cross-sectional areas.

(2) Additional derating of 15 percent for the allowable current is suggested under the following conditions:
   a) Where dielectric layer thickness is less than 0.8mm.
   b) Where conductor thickness is greater than 105μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.

(4) For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperature rises.

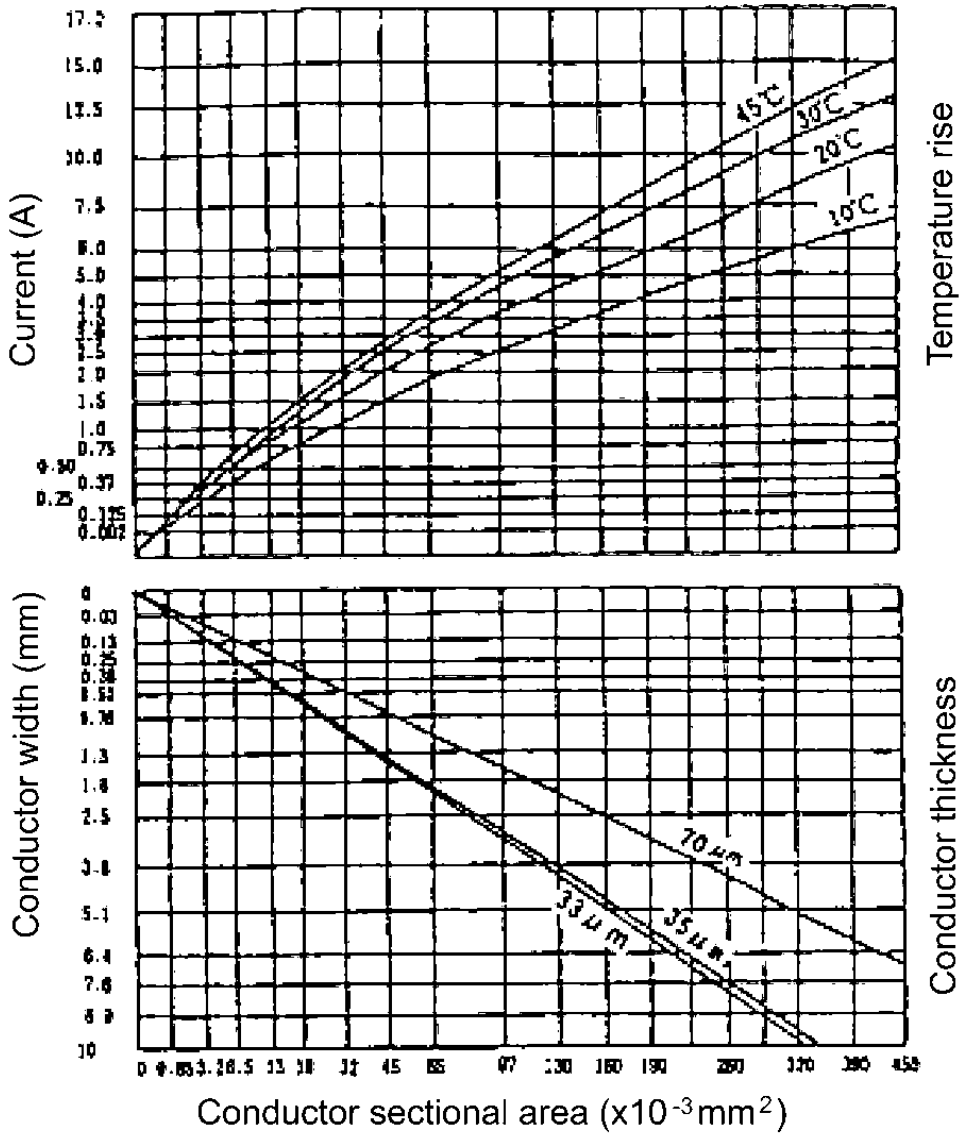
(5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.

(6) The effect of heating due to heat generating parts is not considered.

(7) The final conductor thickness in the chart does not include plating thickness of metals other than copper.

(8) The 54μm line shall apply to an external layer with SVH.

Figure B-1. Conductor Width (External Layer)



Remarks:

(1) Remarks (1) through (7) of Figure B-1 shall apply to this figure.

(2) The 33μm line shall apply to internal layers with SVH and IVH.

Figure B-2. Conductor Width (Internal Layer)

B.3.3.5 Conductor Spacing

The conductor spacing in design shall be not less than 0.18mm. The specific conductor spacing shall depend on the voltage applied between conductors as specified in Table B-6.

Table B-6. Conductor Spacing for Coated Printed Wiring Board

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	
	External layer	Internal layer
0 - 100	0.18	0.18
101 - 300	0.48	0.30
301 - 500	0.86	0.35
501 or higher	(0.003xV)+0.1	(0.003xV)+0.1

B.3.3.6 Land Diameter

The minimum design value of land diameter shall be as specified in Table B-7 (see Figure B-3).

Table B-7. Land Diameter

Unit: mm

Hole	Minimum land diameter(1)
IVH, SVH and small via holes	Drill diameter + 0.4(2)
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

Notes:

(1) The minimum diameter of lands other than round shaped lands shall be measured as the length “A”, as shown in Figure B-3.

(2) The minimum diameter of the land provided with a small via hole shall be 0.76mm.

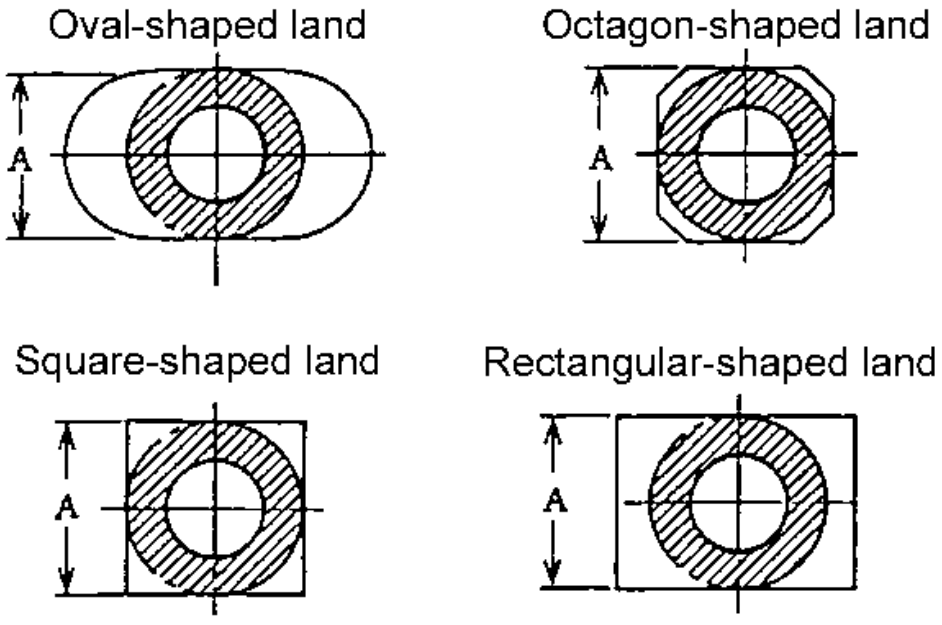


Figure B-3. Measurement of Minimum Diameter of Lands Other than Round Shaped Lands

B.3.3.7 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table B-8.

Table B-8. Plating or Coating Thickness

Unit: μm

Plating material	Surface and through hole plating thickness	
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating	
Electrolytic copper	Component hole	Min. 25
	Small via hole	Min. 30
	IVH and SVH	Min. 15
Electrolytic gold	1.3 to 4.0	
Electrolytic nickel	Min. 5	
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.	

B.3.3.8 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph B.3.10.1.2) and as specified in Table B-9.

Table B-9. Operating Temperature Range

Unit: °C

Base material	Temperature range
GF	-65 to +125
GI	-65 to +170

B.3.4 Externals, Dimensions, Marking and Others

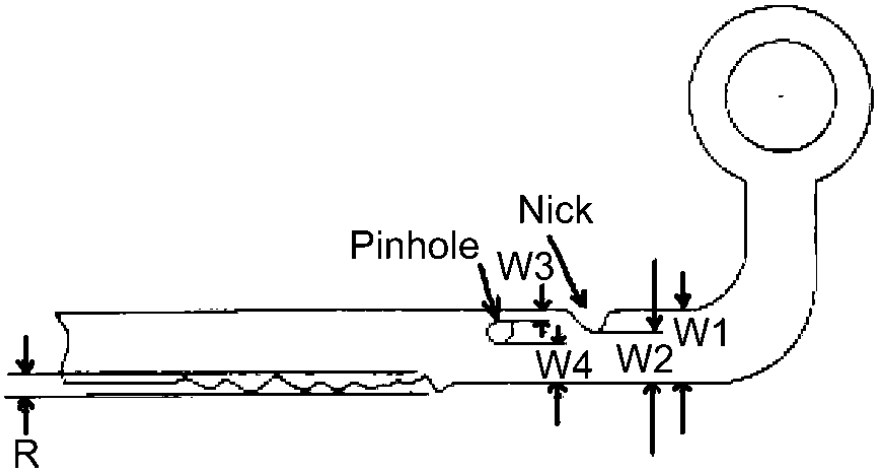
B.3.4.1 Externals and Construction

B.3.4.1.1 Externals of Conductive Pattern, Base Material and Solder Resist

a) Conductive pattern
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor
The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The

length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is not less than 0.2mm, the roughness shall be maximum 0.13mm (see Figure B-4).



Unit: mm

W1 ≥ (Minimum finished conductor width) ≥ 0.08
W2 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
W3+W4 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
R in any range of 13 in length
R ≤ 0.08, when the design width of the conductor is less than 0.2
R ≤ 0.13, when the design width of the conductor is 0.2 or more

Figure B-4. Conductor Defects

c) Annular ring
When the annular ring on the internal and external layers are measured in accordance with paragraph B.4.4.2.2 f), the annular ring of a plated-through hole shall be not less than 0.05mm. The annular ring of a non-plated-through hole shall be not less than 0.38mm and shall not contain any defect. When the annular ring for plated-through hole on an external layer shall be a minimum of 0.13mm in diameter, a sub-land or other equivalent alternative shall be provided.

d) Dielectric layer between conductor layers
The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.

e) Electrolytic solder plating and solder coating
The electrolytic solder plating and solder coating shall be free from pinholes or pits, and completely cover conductive patterns.

f) Edges of printed wiring board
Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board.

g) Surface of printed wiring board
Surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board, and the spacing between conductors is not reduced exceeding 25 percent. Crazing along edges of the printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

h) Solder resist
The cured solder resist shall be free from tackiness, blistering and delamination. Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the provisions of manufacturing drawings.

B.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table B-10.

Table B-10. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of IVH, SVH and small via holes is not specified.
Conductor width	0.13 or more and less than 0.20: ±0.05 0.20 or more and less than 0.50: ±0.10 0.50 or more: ±20 percent of circuit width
Conductor spacing	For the design of three patterns between basic grids, the tolerance of conductor spacing shall be -0.08. (The positive side tolerance is not specified.) For the design of maximum two patterns between basic grids, the tolerance of conductor spacing shall be -0.10. (The positive side tolerance is not specified.) The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

B.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph B.3.2.4 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.

All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

B.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

B.3.4.4 Through Holes

When printed circuit boards are tested as specified in paragraph B.4.4.2.2, the plating of small via holes, IVH and SVH shall not exhibit cracks, conductive interface

separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80μm, and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure B-5).

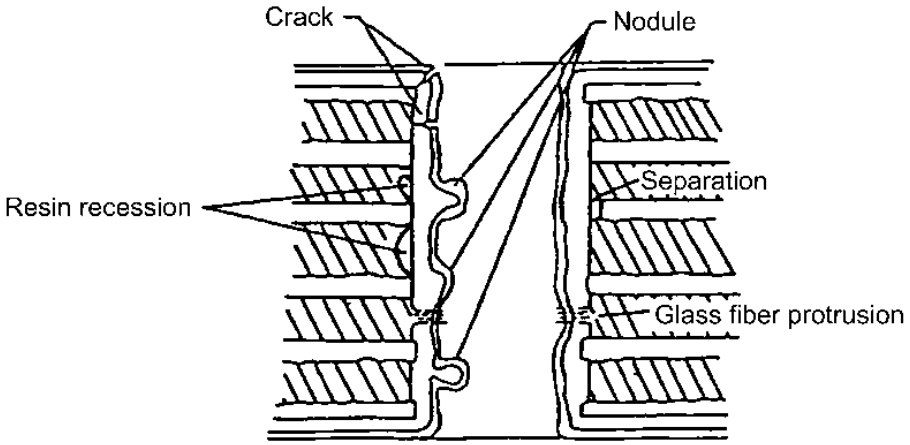


Figure B-5. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure B-6).

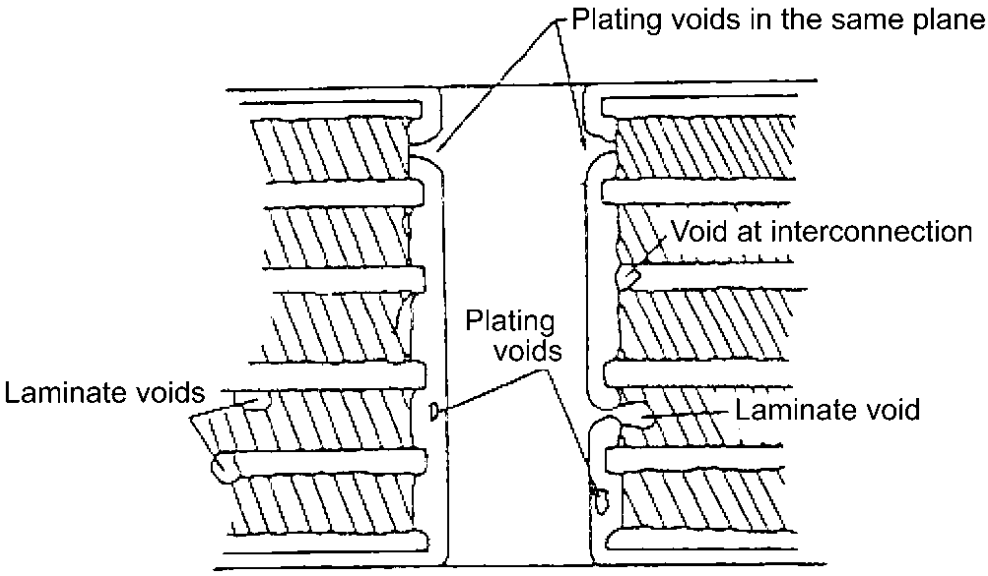


Figure B-6. Voids

b) Conductive interface
The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure B-7).

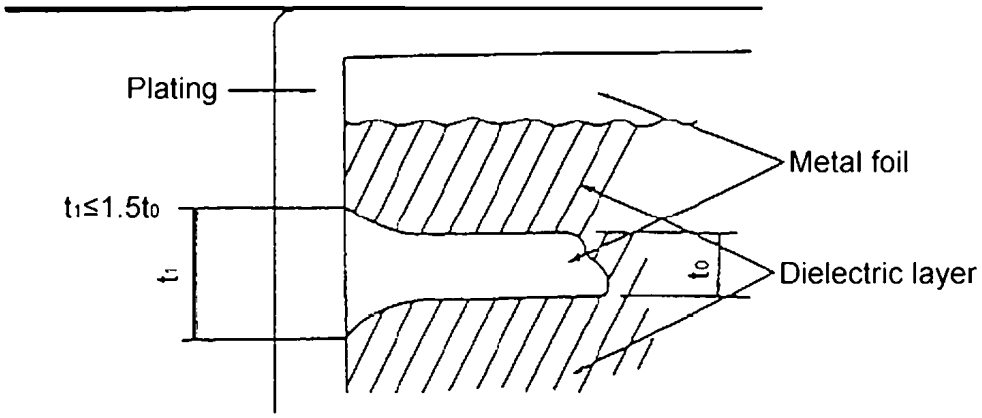


Figure B-7. Nail Heading

c) Layer-to-layer registration
The layer-to-layer registration error shall not exceed 0.20mm.

d) Dielectric layer thickness
The dielectric layer between conductor layers of a multilayer printed wiring board shall be not less than 0.08mm in thickness.

e) Plating thickness
The plating thickness shall meet the requirements specified in paragraph B.3.3.7.

f) Annular ring
The annular ring shall meet the requirements specified in paragraph B.3.4.1.1 c).

B.3.4.5 Solder Resist Thickness

When printed circuit boards are tested as specified in paragraph B.4.4.2.3, the solder resist thickness shall be not less than 17.5μm, measured at the center of conductors.

B.3.5 Workmanship

The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

B.3.5.1 Bow and Twist

When printed circuit boards are tested as specified in paragraph B.4.4.3.1, the maximum limit for bow and twist shall be 0.8 percent, unless otherwise specified on

manufacturing drawings. For a split board, the percent bow and twist shall not exceed the value specified above, before separation.

B.3.5.2 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.

B.3.6 Plating Adhesion and Overhang

When printed circuit boards are tested as specified in paragraph B.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

B.3.7 Cleanliness

The printed wiring boards shall exhibit no fouling including dirt, oil, corrosion, corrosion product, salt, soot, grease, finger print, mold release agent, foreign inclusion and flux residues, or ionic contamination. When printed circuit boards are tested as specified in paragraph B.4.4.5, the resistivity of the solvent extract shall be not less than $2x10^6 \Omega \cdot cm$.

B.3.8 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

B.3.8.1 Dielectric Withstanding Voltage

When tested as specified in paragraph B.4.4.6.1, printed circuit boards shall not exhibit insulation breakdown, flashover or sparkover.

B.3.8.2 Circuitry

When tested as specified in paragraph B.4.4.6.2, printed circuit boards shall not exhibit open circuit or short-circuiting between circuit patterns.

B.3.8.3 Connection Resistance

When printed circuit boards are tested as specified in paragraph B.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \bullet t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

B.3.9 Mechanical Performance

Printed wiring boards shall meet the following mechanical requirements.

B.3.9.1 Terminal Pull Strength

When tested as specified in paragraph B.4.4.7.1, printed wiring boards shall meet the following requirements. This provision shall not apply to IVH, SVH or small via holes.

a) Bond strength
The land shall withstand 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph B.4.4.2.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with paragraph B.4.4.2.2, there shall be no cracks, blistering, measling or delamination.

B.3.9.2 Solderability

When tested as specified in paragraph B.4.4.7.2, printed wiring boards shall meet the following requirements.

a) Hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to IVH, SVH or small via holes.

b) Surface solderability
A minimum of 95 percent of the surface conductor area shall be covered uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area.

B.3.10 Environmental Performance

Printed wiring boards shall meet the following environmental requirements.

B.3.10.1 Thermal Shock

B.3.10.1.1 Thermal Shock (I) (applicable to qualification test)

When printed circuit boards are tested as specified in paragraph B.4.4.8.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph B.4.4.6.2, and connection resistance shall be measured in accordance with paragraph B.4.4.6.3. Printed wiring boards shall meet the requirements specified in paragraph B.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

B.3.10.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed circuit boards are tested as specified in paragraph B.4.4.8.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph B.4.4.6.2, and connection resistance shall be measured in accordance with paragraph B.4.4.6.3. Printed wiring boards shall meet the requirements specified in paragraph B.3.8.2 after the test, and the

change in connection resistance between circuits before and after the test shall be less than 10 percent.

B.3.10.2 Humidity and Insulation Resistance

When printed circuit boards are tested as specified in paragraph B.4.4.8.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be not less than 500MΩ.

B.3.10.3 Hot Oil Resistance

When printed circuit boards are tested as specified in paragraph B.4.4.8.3, the change in connection resistance between circuits before and after the test shall be less than 10 percent.

B.3.10.4 Thermal Stress

When tested as specified in paragraph B.4.4.8.4, printed wiring boards shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Copper foil
There shall be no cracks in internal copper foils in the vertical microsection of through holes.

c) Laminate voids
Laminate voids with the longest dimension of 76μm as a maximum shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings.

B.3.10.5 Radiation Hardness

When printed circuit boards are tested as specified in paragraph B.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph B.3.8.1 shall be satisfied.

B.4. Quality Assurance Provisions

B.4.1 In-Process Inspection

The in-process inspection specified below shall be performed, and printed wiring boards shall meet the requirements of paragraphs B.3.4.1, B.3.4.2, B.3.4.3 and B.3.7.

a) Visual inspection of internal layers, construction and dimensions (100 percent)
b) Cleanliness (sampling)

B.4.2 Qualification Test

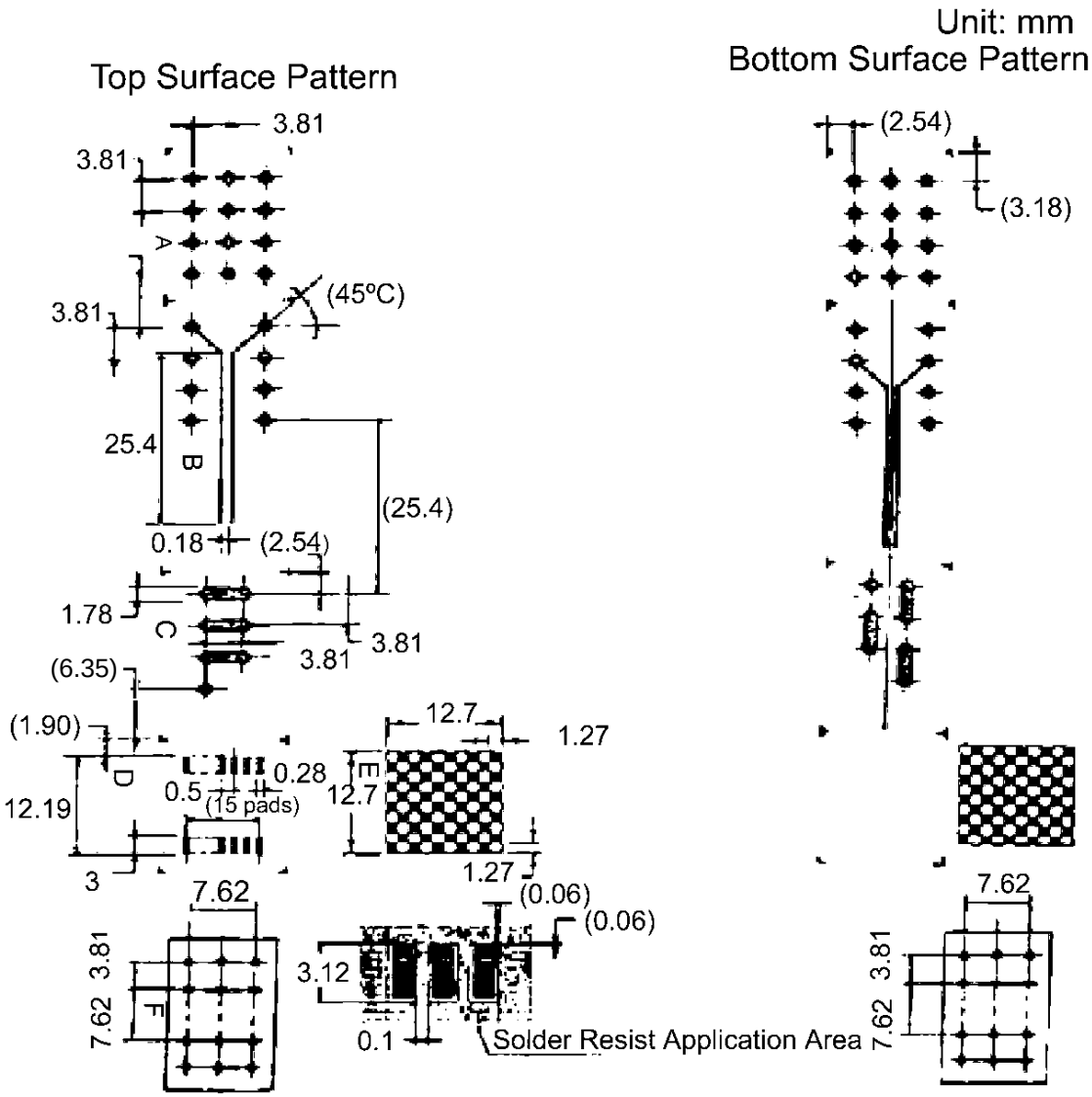
B.4.2.1 Sample

Samples shall be approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure B-8 for single-sided or double-sided printed wiring boards and Figure B-9 for multilayer printed wiring boards. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board.

B.4.2.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table B-11. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Three combined conditions of temperature range and number of cycles shall apply to each base material type, as specified in Table B-4. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table B-11.

Unit: mm



Notes:

(1) For the test coupons A and B, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter shall be 0.8mm. For the test coupons C and F, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land. The test coupon F shall be prepared, only when the corresponding product has small via holes. All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

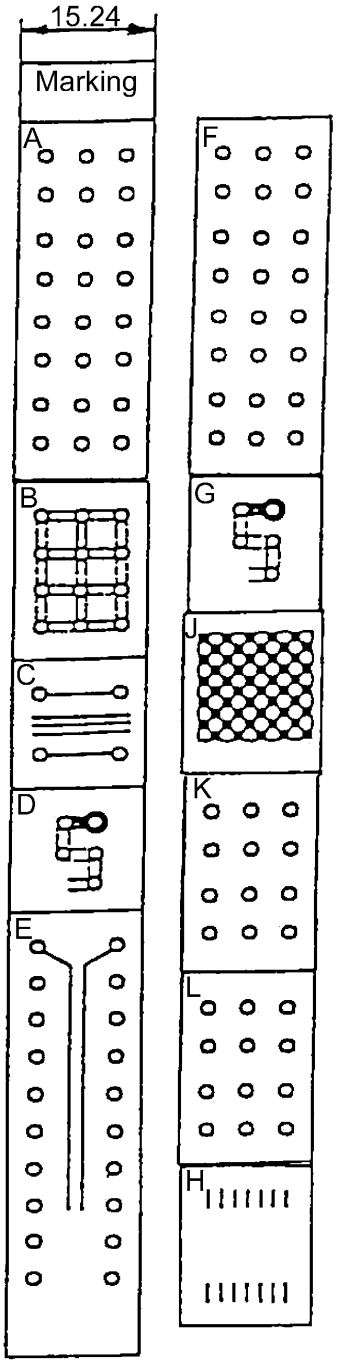
(2) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(3) The dimensions in the parentheses are reference dimensions.

(4) Solder resist shall apply to the test coupons B, D, and E, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon B shall be the land diameter increased by 0.2mm. For coupon E, the solder resist shall apply to the entire layer.

Figure B-8. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board)

Arrangement of Test Coupons



Unit: mm

Notes:

(1) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(2) For test coupon A, the land diameter shall be the minimum land diameter of small via holes for the corresponding printed wiring board. The hole diameter shall be the maximum hole diameter among the minimum lands. All holes shall be through holes. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes. The hole diameter shall be 0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(4) Test coupons D and G are different in the number of layers and via hole structure. Each coupon shall be produced so as to form the same number of layers and via hole structure as those of the corresponding product, and to have a circuit continuity through all layers by via holes.
The land diameter shall be that of each IVH, SVH and small via hole of the corresponding products. The land shape shall be the typical land shape of the products.
The hole diameter shall be the maximum hole diameter among the minimum lands. On both ends of the printed wiring board, through holes shall be formed to measure the resistance. The land diameter shall be 1.8mm and hole diameter shall be 0.8mm. All holes shall be through holes. The hole diameter tolerance is not specified.

(5) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon E shall be equal to the land diameter +0.2mm.

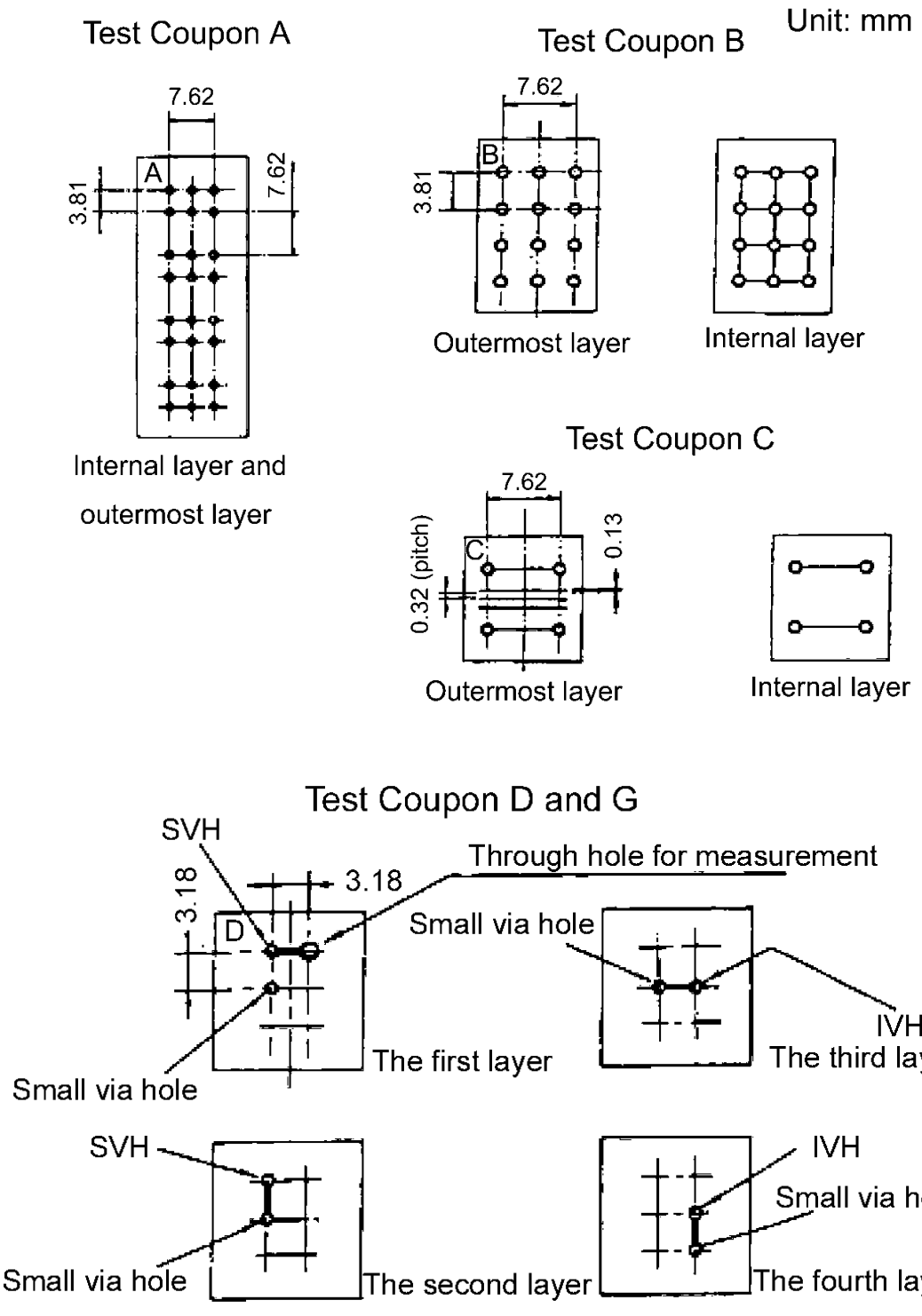
(6) Test coupons K and L shall be prepared, when the corresponding products have an IVH or SVH. Those coupons are different in the number of layers and via hole structure.
The land shall be formed only on the layers which are connected by an IVH or SVH.
The land diameter shall be equal to the minimum land diameter of each IVH or SVH of the corresponding products. The hole diameter shall be the maximum hole diameter among the minimum lands. On the outermost layer, the land, of which diameter is the same as the diameter of the land on an IVH layer, shall be formed whether a SVH is provided or not.

(7) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. Therefore, the conductors shall be formed on all layers in accordance with this figure.

(8) The arrangement of test coupons shown in this appendix is an example; a different arrangement is also acceptable.

(9) The symbols of test coupons (A to H and J to L) shall be used for identification and not for the object of inspection. The marking method is not specified.

Figure B-9. Test Coupons (for Multilayer Printed Wiring Board) (1/4)



In this figure, the first and the second layers are connected by a SVH, and the third and fourth layers are connected by an IVH.

Figure B-9. Test Coupons (for Multilayer Printed Wiring Board) (2/4)

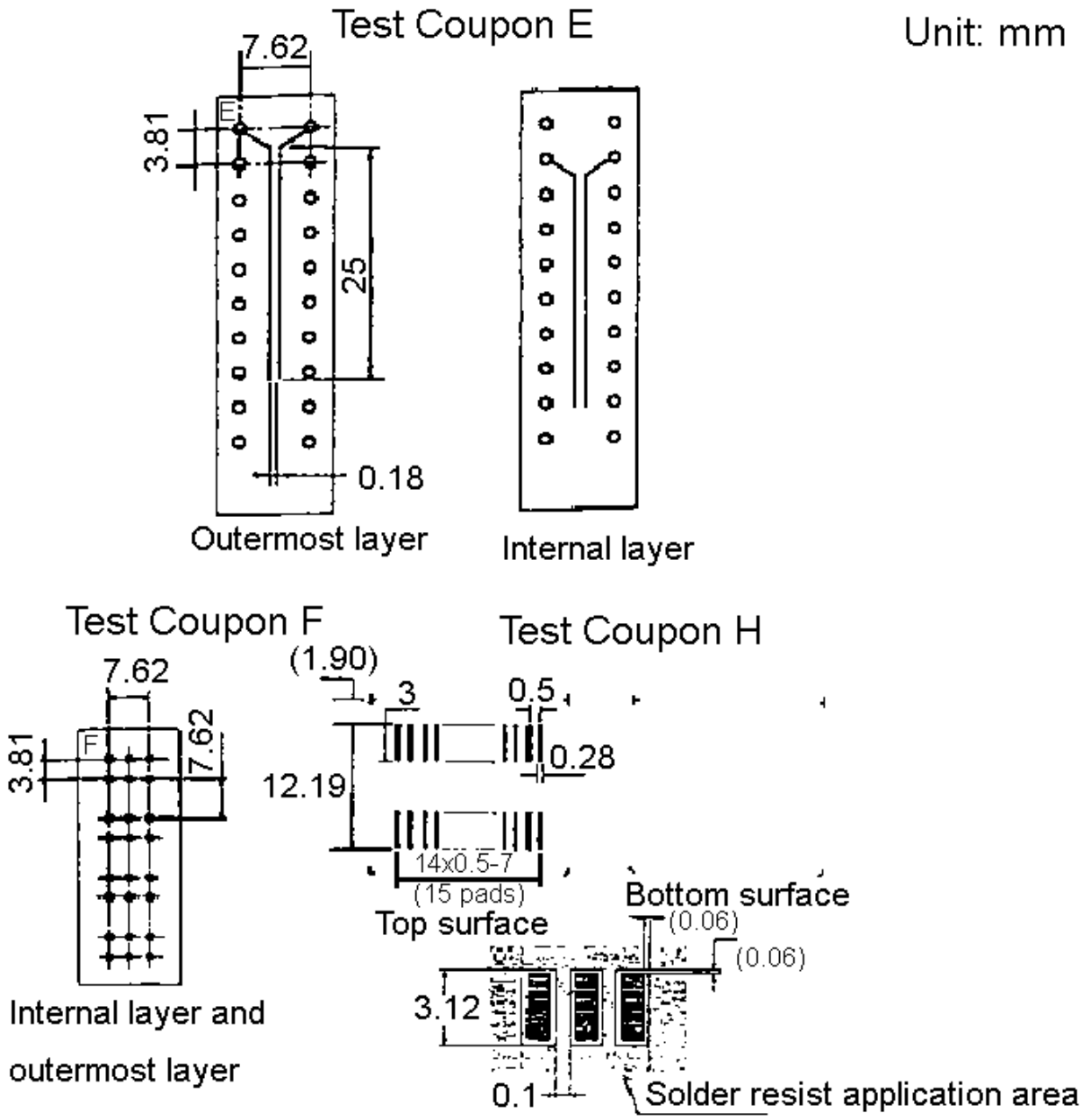
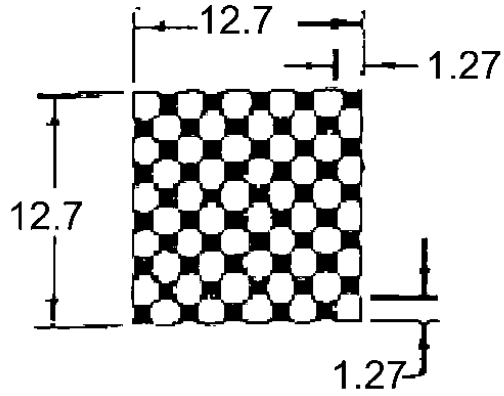


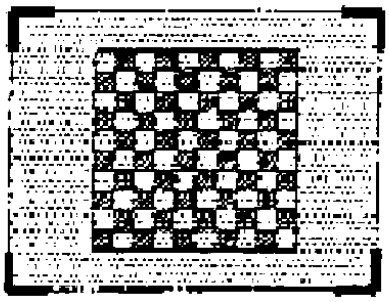
Figure B-9. Test Coupons (for Multilayer Printed Wiring Board) (3/4)

Unit: mm

Test Coupon J

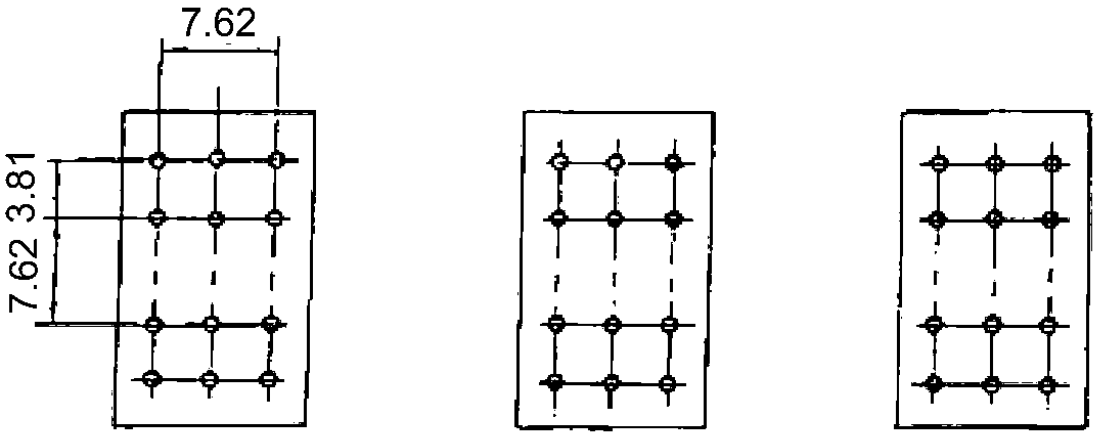


Top surface and bottom surface



Solder resist application area

Test Coupon K and L



Outermost layer

Internal layer with SVH

Internal layer with IVH

Figure B-9. Test Coupons (for Multilayer Printed Wiring Board) (4/4)

Table B-11. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail		
					Samples(1)		Quantity of allowable defects
Group	Order	Test item			Production printed wiring boards	Test coupon (2)	
I	1	Design and construction	B.3.3	B.4.4.2	No. 1 to No. 6	A, B, C, D, E, F, G, H, K and L(4)	0
	2	Externals, dimensions, marking and others Externals and construction Dimensions Marking	B.3.4.1 B.3.4.2 B.3.4.3	B.4.4.2.1			
	3	Workmanship(3)	B.3.5	B.4.4.3			
II	1	Plating adhesion and overhang	B.3.6	B.4.4.4	No. 1 to No. 6	C	
	2	Bow and twist	B.3.5.1	B.4.4.3.1		N/A	
III	1	Through holes	B.3.4.4	B.4.4.2.2	No. 1	A, F and K	
	2	Terminal pull strength	B.3.9.1	B.4.4.7.1		F	
	3	Solder resist thickness	B.3.4.5	B.4.4.2.3		J	
IV	1	Connection resistance	B.3.8.3	B.4.4.6.3	No. 2	D	
	2	Hot oil resistance	B.3.10.3	B.4.4.8.3			
	3	Connection resistance	B.3.8.3	B.4.4.6.3			
V	1	Circuitry	B.3.8.2	B.4.4.6.2	No. 3	E and G(5)	
	2	Connection resistance	B.3.8.3	B.4.4.6.3			
	3	Thermal shock (I)	B.3.10.1.1	B.4.4.8.1 a)			
	4	Circuitry	B.3.8.2	B.4.4.6.2			
	5	Connection resistance	B.3.8.3	B.4.4.6.3			
VI	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	No. 4	E	
	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1			
VII	1	Thermal stress	B.3.10.4	B.4.4.8.4	No. 5	A, B and L	
	2	Solderability	B.3.9.2	B.4.4.7.2		B and H(6)	
VIII	1	Radiation hardness	B.3.10.5	B.4.4.8.5	No.6	N/A	
-	1	Materials	B.3.2	N/A	(7)		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. In order to qualify split boards, split board specimens shall be submitted as the production samples.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the second test of Group II tests.

(4) Group I test shall be performed on the test coupons which are to be provided for Group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(5) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(6) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

(7) Data to certify compliance with design specifications shall be submitted.

B.4.3 Quality Conformance Inspection

B.4.3.1 Quality Conformance Inspection (Group A)

B.4.3.1.1 Sample

The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be manufactured simultaneously.
Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen. A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

B.4.3.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table B-12. The inspections within each group shall be performed in the order listed.
For Group IV and V tests, one test coupon shall be provided for each coupon type specified in Table B-12.

Table B-12. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail		
					Quantity of samples		
Group	Order	Inspection item			Production printed wiring boards	Test coupon(1)	Quantity of allowable defects
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	B.3.4.1 B.3.4.2 B.3.4.3	B.4.4.2.1	All	N/A	0
	2	Workmanship(2)	B.3.5	B.4.4.3			
II	1	Bow and twist	B.3.5.1	B.4.4.3.1	All	N/A	
III	1	Circuitry	B.3.8.2	B.4.4.6.2	All	N/A	
IV	1	Thermal stress	B.3.10.4	B.4.4.8.4	N/A	A, F and K (A, B and F)(3), (4)	
	2	Through holes Conductive interface Plating thickness	B.3.4.4 b) e)	B.4.4.2.2 a) and d) c)		A, B and L (A and F)(3), (4)	
V	1	Solderability	B.3.9.2	B.4.4.7.2	N/A	B and H (A and D)(5)	

Notes:

(1) A letter inside the parentheses shows the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

(2) Bow and twist (paragraph B.3.5.1) of the samples shall be tested during the first test of Group II tests.

(3) For a multilayer printed wiring board, test coupon A shall be inspected, when the corresponding product is provided with small via holes. Test coupons K and L shall be inspected when the corresponding products have IVH or SVH.

(4) For a single-sided or double-sided printed wiring board, test coupon F shall be inspected, only when the corresponding product is provided with small via holes.

(5) Test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.

B.4.3.2 Quality Conformance Inspection (Group B)

B.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

B.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table B-13. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

Table B-13. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	B.3.6	B.4.4.4	C	0
II	1	Terminal pull strength	B.3.9.1	B.4.4.7.1	F	
	2	Connection resistance	B.3.8.3	B.4.4.6.3	D	
	3	Hot oil resistance	B.3.10.3	B.4.4.8.3		
	4	Connection resistance	B.3.8.3	B.4.4.6.3		
III	1	Circuitry	B.3.8.2	B.4.4.6.2	E and G(1)	
	2	Connection resistance	B.3.8.3	B.4.4.6.3		
	3	Thermal shock (II)	B.3.10.1.2	B.4.4.8.1 b)		
	4	Circuitry	B.3.8.2	B.4.4.6.2		
	5	Connection resistance	B.3.8.3	B.4.4.6.3		
IV	1	Humidity and insulation resistance	B.3.10.2	B.4.4.8.2	E	
	2	Dielectric withstanding voltage	B.3.8.1	B.4.4.6.1		

Note: (1) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

B.4.4 Methods for Test and Inspection

B.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

B.4.4.2 Externals, Dimensions, Marking and Others

B.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of the printed wiring board shall be tested.

a) Conductive patterns and edges
Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument which has sufficient accuracy.

b) Annular ring
The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular ring shall be measured using an optical measuring instrument which has sufficient accuracy.

B.4.4.2.2 Through Holes

a) Vertical microsection
The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the solder resist thickness and plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, base material thickness and plating thickness) at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board's length direction.

b) Horizontal microsection
Only multilayer boards shall be subjected to the horizontal microsection inspection. Multilayer boards with through holes shall be encapsulated and polished. A conductor layer shall be polished in the parallel direction. The microsection is prepared to expose the conductor layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X.

c) Plating thickness
The plating thickness shall be measured using microsections prepared in accordance with paragraph B 4.4.2.2 a) at a magnification of minimum 200X. Measurements shall be averaged from three determinations for a plated-through hole. Isolated thick or thin sections shall not be used for averaging.

d) Layer-to-layer registration
The layer-to-layer registration shall be measured at a magnification of 25 to 100X using microsections prepared in accordance with paragraph B.4.4.2.2 a). The misregistration shall be inspected around the hole in the direction parallel

to the board length and the vertical direction. This provision shall not apply to IVH or SVH. (See Figure B-10.)

e) Dielectric layer thickness
The dielectric layer thickness shall be measured using microsections prepared in accordance with paragraph B.4.4.2.2 a).

f) Annular ring
The annular ring shall be measured using microsections prepared in accordance with paragraph B.4.4.2.2 a). The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure B-10). The IVH and SVH shall not be subjected to the cross-sectional observation. However, they shall be inspected for the annular ring in accordance with paragraph B.4.4.2.1 b).

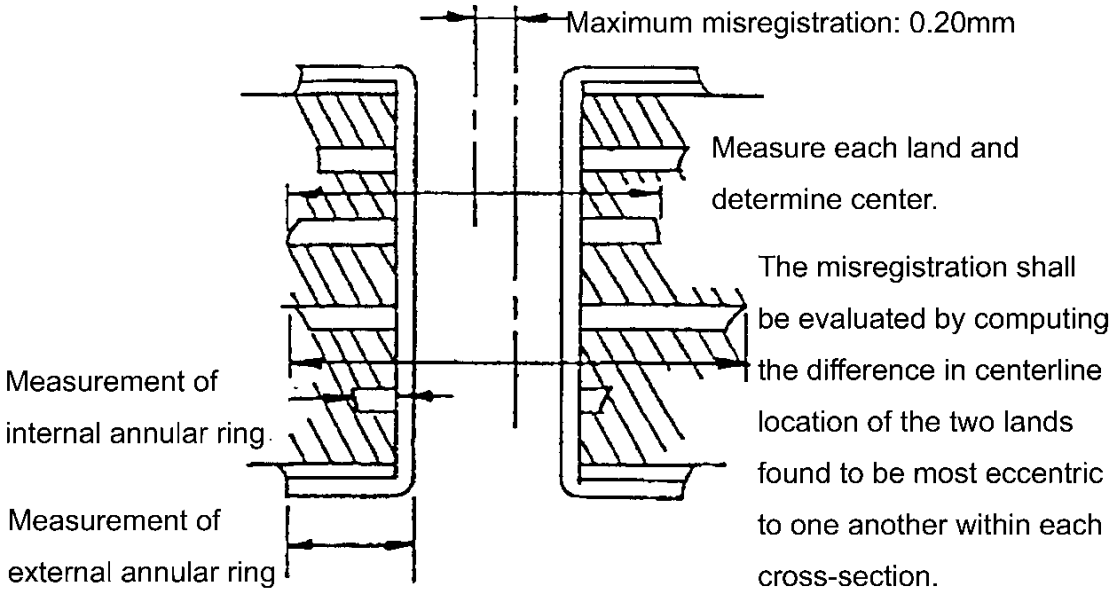


Figure B-10. Measurement of Layer-to-Layer Registration and Annular Ring

B.4.4.2.3 Solder Resist Thickness

The solder resist thickness shall be measured using a microsection prepared in accordance with paragraph B.4.4.2.2 a) at a magnification of minimum 200X.

B.4.4.3 Workmanship

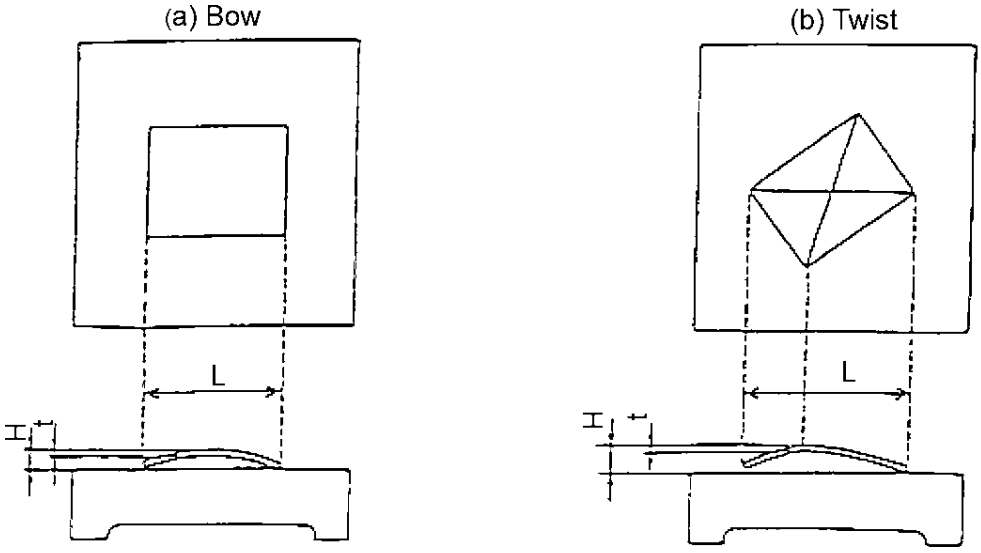
The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

B.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see

Figure B-11). The percent bow and twist shall be calculated by the following formula.

Percent bow and twist = $\frac{H\text{-}t}{L} \times 100$ (%)



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure B-11. Measurement of Bow and Twist

B.4.4.4 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and minimum 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

B.4.4.5 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 percent by volume of isopropyl alcohol and 25 percent by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6 \Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range

and accuracy. The alternate test methods specified in Table B-14 may be used to perform the cleanliness test.

Table B-14. Equivalent Factors

Method	Resistivity ($\times 10^6 \Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.20

Note: (1) Alpha Metals Incorporated, “Omega Meter”

B.4.4.6 Electrical Performance

The electrical performance tests shall be performed as follows.

B.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $1000V_{AC}$ peak or $1000V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

B.4.4.6.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

B.4.4.6.3 Connection Resistance

The resistance between the through hole terminals shall be measured using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5 mΩ.

B.4.4.7 Mechanical Performance

The mechanical performance tests shall be performed as follows.

B.4.4.7.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.

Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

B.4.4.7.2 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph B.4.4.8.4.

b) Surface solderability
After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be

permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

B.4.4.8 Environmental Performance

The environmental performance tests shall be performed as follows.

B.4.4.8.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
The temperature range and number of cycles shall be as specified in Table B-4. The time for step 2 and 4 shall be within 2 minutes each.

b) Thermal shock (II) (applicable to quality conformance inspection)
   1) For GF base material
   The test shall be performed under the test condition B-3. The time for step 2 and 4 shall be within 2 minutes each.
   2) For GI base material
   The test shall be performed under the test condition F-3. The high temperature shall be +170°C, and the time for step 2 and 4 shall be within 2 minutes each.

B.4.4.8.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

B.4.4.8.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. Immersion and cooling shall be performed for 10 cycles.

B.4.4.8.4 Thermal Stress

The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 percent maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for any crack on the internal copper foil and laminate voids using the microsection prepared in accordance with B.4.4.2.2 a). Solder

temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

B.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph B.4.4.6.1 and B.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

APPENDIX C

DISCRETE WIRING BOARDS,
GLASS BASE WOVEN EPOXY RESIN
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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX C

DISCRETE WIRING BOARDS, GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL

C.1. General

C.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the discrete wiring boards (hereinafter referred to as "printed wiring boards"). The printed wiring boards provide three types of structure; the general-purpose structure without a metal core, high heat-radiation structure with copper plates, and high heat-radiation and low-thermal expansion structure with copper-invar-copper (hereinafter referred to as “CIC”).

C.1.2 Classification

Products covered by this specification shall be classified as specified in Table C-1. The structure of each type is as shown in Figure C-1.

Table C-1. Classification

Type	Structure	Metal core for heat radiation
I	General-purpose	No metal core
II	High heat-radiation	Copper
III	High heat-radiation and low-thermal expansion	CIC

C.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA(1) 2140/C <u>501</u> <u>GF</u> <u>N</u> <u>4</u>

501	GF	N	4
Individual identification	Base material code (see C.1.3.1)	Metal core code (see C.1.3.2)	Number of internal circuit layers

Note: (1) "JAXA" indicates the part is for space use and may be abbreviated “J”.

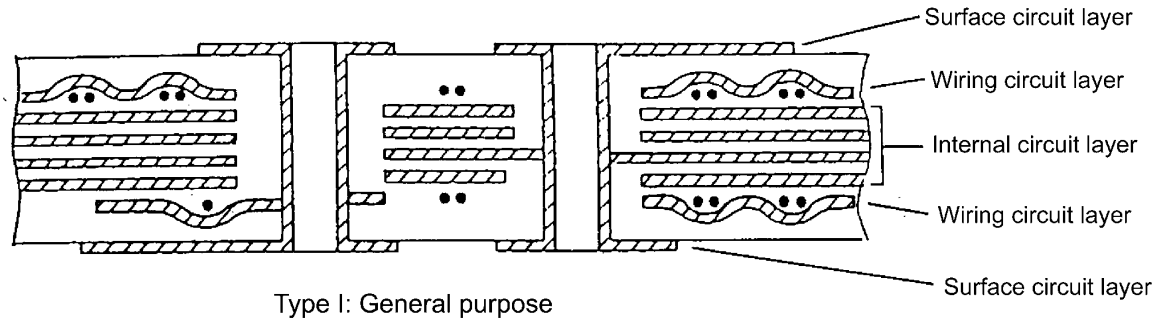
C.1.3.1 Base Material Code

The base material code is as shown in Table C-2.

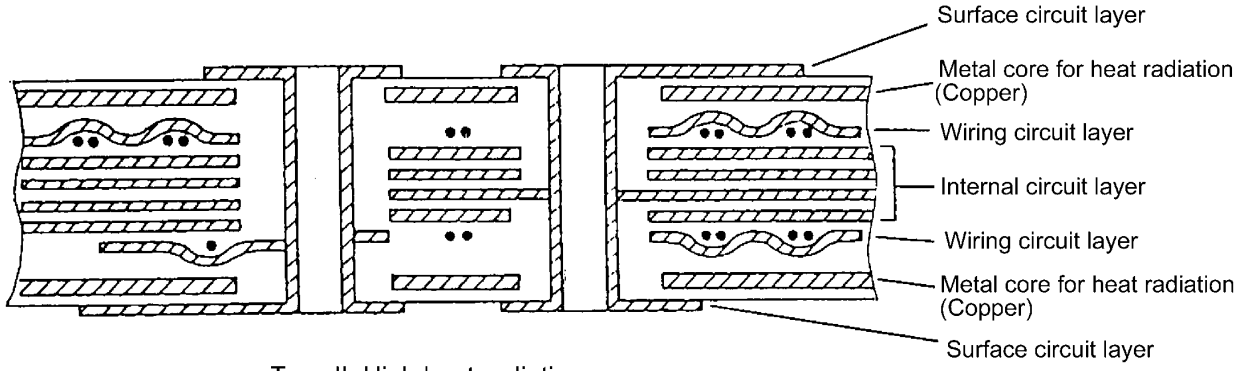
Table C-2. Base Material Code

Base material code(1)	Base material
GF	Glass base woven epoxy resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

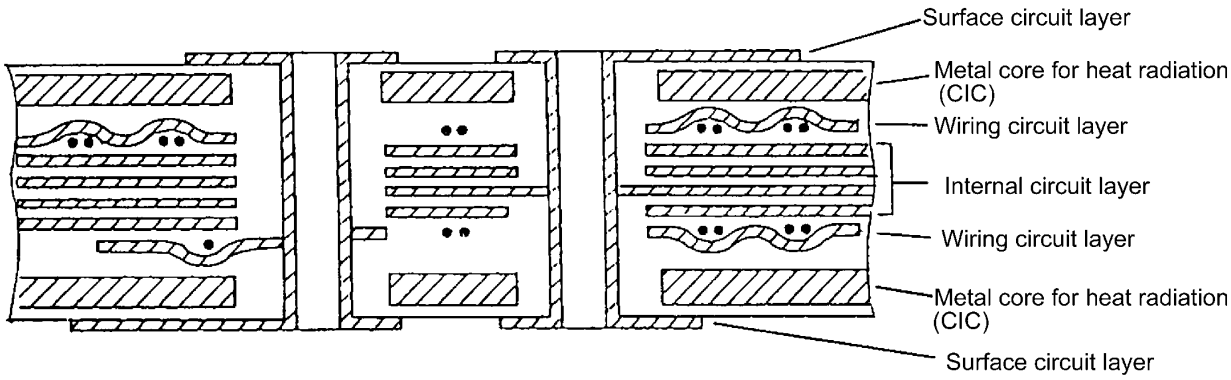
Note: (1) Applicable standards for GF type are as specified in the detail specification.



Type I: General purpose



Type II: High heat-radiation



Type III: High heat-radiation and low-thermal expansion

Figure C-1. Basic Cross-Section of Printed Wiring Boards

C.1.3.2 Classification of Metal Cores for Heat Radiation

The metal core for heat radiation is identified by a single capital letter symbol as shown in Table C-3.

Table C-3. Classification of Metal Cores for Heat Radiation

Symbol	Metal core for heat radiation
N	No metal core
C	Copper
I	CIC

C.2. Applicable Documents

C.2.1 Reference Documents

The following documents are reference documents of this appendix.

a) MIL-PRF-55110 Printed Wiring Board, Rigid, General Specification for
b) IPC-DW425 Design and End Product Requirements for Discrete Wiring Boards

C.3. Requirements

C.3.1 Qualification Coverage

Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs C.3.2 to C.3.10. Products shall have metal core for heat radiation listed in Table C-4. Products with fewer layers than the qualified sample units are considered qualified. All surface plating types specified in paragraph C.3.2.4 is considered qualified if any one of those plating types is qualified. Only solder resist inks used for qualification tests are considered qualified. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. The maximum thickness shall be specified in the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

Table C-4. Qualification Coverage

Type	Metal core for heat radiation	Number of layers of metal core for heat radiation	Number of surface circuit layers	Number of wiring circuit layers	Number of maximum internal circuit layers
I	No metal core	0	2	2	4
II	Copper	2	2	2	4
III	CIC	2	2	2	4

C.3.2 Materials

The materials shall be specified as follows and as specified in paragraph 3.3.

C.3.2.1 Copper-Clad Laminate and Prepreg

The copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The nominal thickness of a dielectric layer shall be not less than 0.08mm, and a prepreg shall have a nominal thickness of 0.05mm. The metal foil shall be copper regardless of the base material type. The metal foil for the outermost layer shall have a nominal thickness of 18μm as a minimum, and the metal foil for an internal layer shall have a minimum thickness of 35μm. The applicable standards for the material used in the printed wiring boards shall be specified in each detail specification.

C.3.2.2 Wires and Adhesive Sheets

The wires shall be insulated mainly with polyimide resin, and have an adhesive coating of phenoxy-epoxy resin over the insulating coating. The nominal diameter of copper wire shall be not less than 0.10mm. The nominal thickness of the insulating coating shall be a minimum of 0.01mm. The adhesive sheets for the wires shall have phenoxy-epoxy resin as a main component.

C.3.2.3 Metal Core for Heat Radiation

The metal cores for heat radiation for the type II and III of the printed wiring boards shall meet the following requirements.

a) The metal core of the type II structure (high heat-radiation type) shall be constructed of copper. The copper purity shall be a minimum of 99.8 percent, and the nominal thickness of the core shall be not more than 0.15mm.
b) The metal core of the type III structure (high heat-radiation and low-thermal expansion type) shall be constructed of CIC. The nominal thickness of the core shall be not more than 0.15mm.

C.3.2.4 Plating

The plating type shall be selected from the types specified in this appendix. All through holes shall be covered with copper plating. Plating thickness shall conform to the requirements of this specification. Surface plating may be applied, if necessary. The surface plating type and the application area shall be as defined on drawings which are approved by purchasers. Lands and through holes shall be covered with the same surface plating.

C.3.2.4.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

C.3.2.4.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

C.3.2.4.3 ENEPIGEG (Electroless Ni, Electroless Pd, Immersion Au, Electroless Au plating)

EN (Electroless Nickel)/EP (Electroless Palladium)/IG (Immersion Gold)/EG (Electroless Gold) plating is conditioned by EN plated on the copper circuit pattern as an undercoat which are plated with EP and then coated with IG and EG plating on top of it.
EN plating is a nickel/phosphorus type, EP plating is pure palladium type, EG plating is cyan-free type and IG plating is cyan type.
The purity of both EP and EG plating shall be 99.9% as a minimum.

C.3.2.5 Solder Resist

The solder resist applied on the printed wiring boards shall conform to IPC-SM-840 Class H or the equivalent.

C.3.2.6 Marking Ink

The marking shall be produced by using epoxy resin base inks that do not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

C.3.3 Design and Construction

C.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points, and the grid spacing shall be 1.27mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings, artwork masters (or original production masters) and net lists shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

C.3.3.2 Structure of Printed Wiring Board

Printed wiring board shall be basically constructed of two or four internal circuit layers with etched patterns, two wiring circuit layers which sandwich the internal circuit layers, and two surface circuit layers with etched patterns on both sides of the printed wiring board. A metal core for heat radiation shall be formed between a surface circuit layer and wiring circuit layer. The structure of the printed wiring board shall be as shown in Figure C-1. In this figure, the printed wiring board has four power/ground planes.

C.3.3.3 Conductive Pattern

The circuit patterns on internal and surface layers shall conform to the approved artwork master (or original production master). The signal patterns of the wiring shall meet the approved wiring patterns.

C.3.3.4 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. The dimensional tolerance shall be in accordance with the requirements specified in Table C-5, unless otherwise specified.

Table C-5. Dimensional Tolerance

Unit: mm

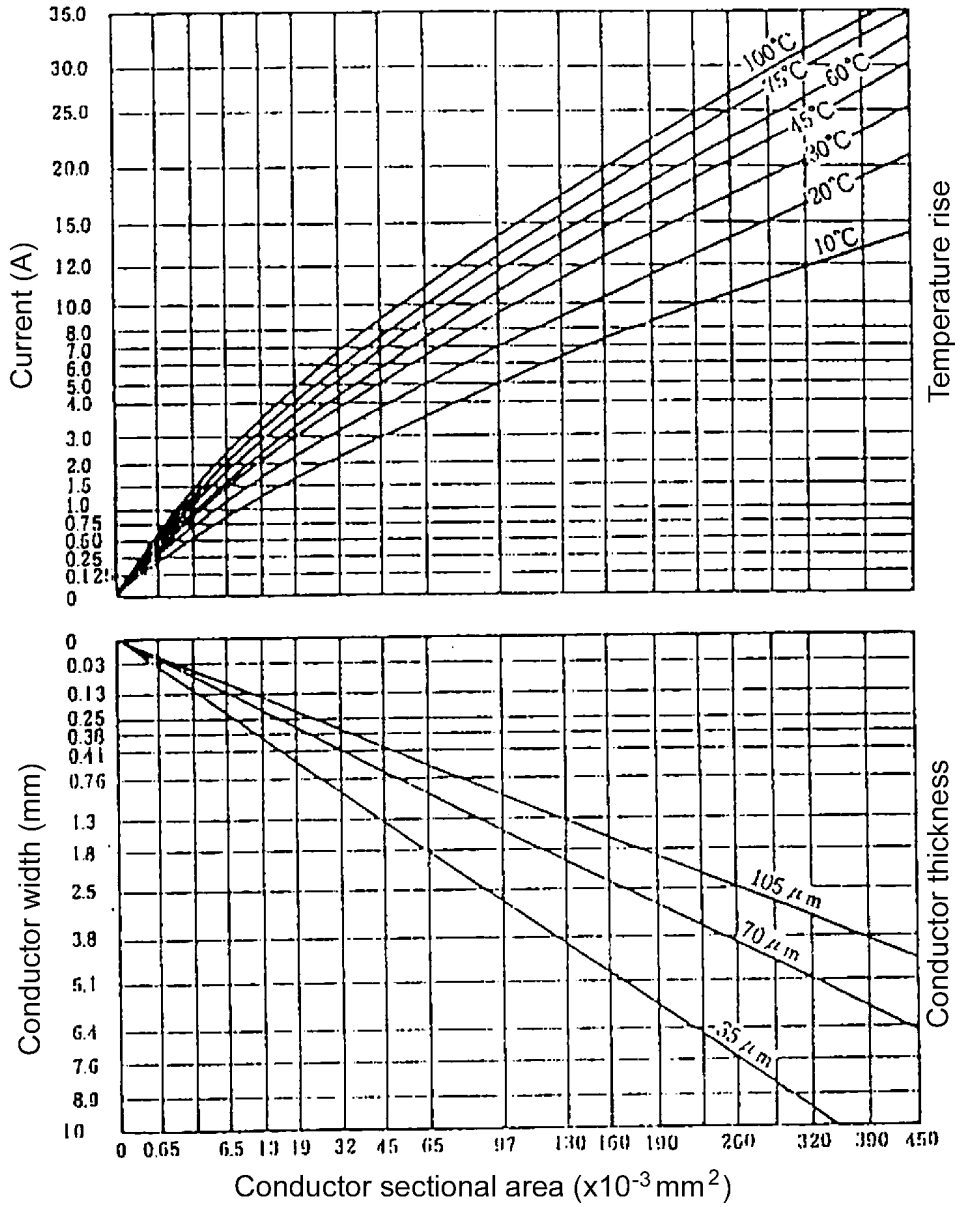
Item	Dimensional tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$.
Conductor width	±0.10 for any conductor width. The minimum tolerance of the finished conductor width shall be 0.08.
Conductor spacing	-0.10 for any conductor spacing. The positive side tolerance is not specified. The minimum tolerance of finished conductor spacing on an external layer shall be 0.13.

C.3.3.5 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes.

C.3.3.6 Conductor Width

The design width of the conductor shall be not less than 0.13mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures C-2 and C-3.



Remarks:

(1) This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. It is assumed that the conductor surface area is relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations in etching techniques, conductor thickness and width and cross-sectional areas.

(2) Additional derating of 15 percent for the allowable current is suggested under the following conditions:
   a) Where dielectric layer thickness is less than 0.8mm.
   b) Where conductor thickness is not less than 105μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.

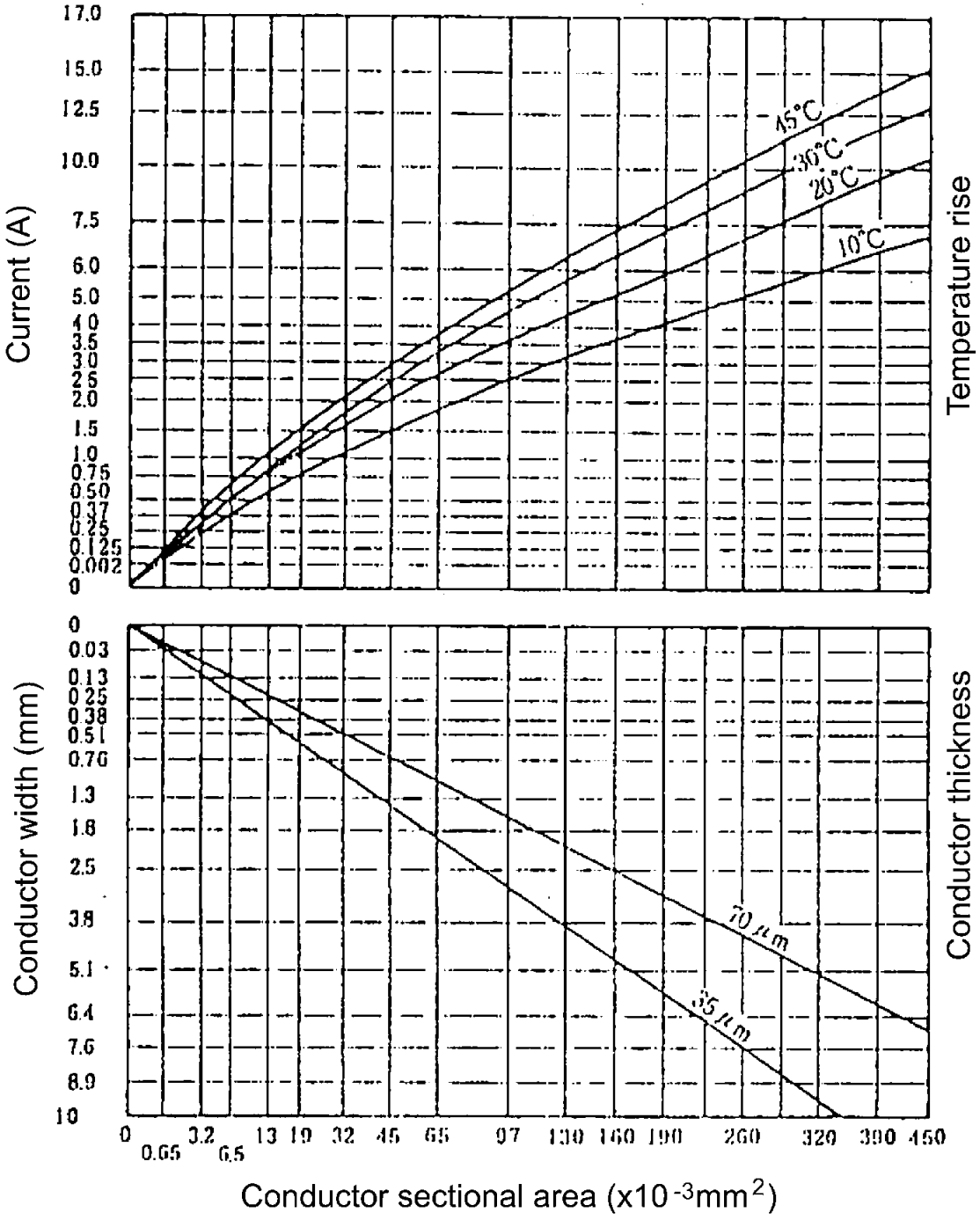
(4) For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperatures rises.

(5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current. The equivalent cross section is equal to the sum of the cross sections of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.

(6) The effect of heating due to heat generating parts is not considered.

(7) The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure C-2. Conductor Width (External Layer)



Remark: (1) Remarks (1) through (7) of Figure C-2 shall apply to this figure.

Figure C-3. Conductor Width (Internal Layer)

C.3.3.7 Annular Ring

When a plated-through hole provides an electrical connection, but is not used for inserting a lead, the design value of the annular ring shall be not less than 0.25mm. When a plated-through hole is used for inserting a lead, the design value of the annular ring shall be a minimum of 0.30mm. The design value of an annular ring of a non-plated-through hole shall be not less than 0.55mm.

C.3.3.8 Wire Spacing and Conductor Spacing

C.3.3.8.1 Wire Spacing

The design value of spacing between wires in parallel shall be not less than 0.3mm. The spacing where wires are crossed is not specified.

C.3.3.8.2 Conductor Spacing

The design conductor spacing on a circuitry layer shall be not less than 0.20mm. The specific conductor spacing shall be as specified in Table C-6.

Table C-6. Conductor Spacing and Wire Spacing (Design Value)

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	Minimum spacing between wires in parallel
0 - 15	0.20	0.3 {12 mil}
16 - 30	0.25	
31 - 50	0.38	
51 - 100	0.51	
101 - 300	0.76	
301 - 500	1.52	
501 or higher	(0.003xV)+0.1	

C.3.3.9 Operating Temperature Range

The printed wiring boards shall operate within the temperature range of -65°C to +125°C.

C.3.4 Externals, Dimensions, Marking and Others

C.3.4.1 Externals and Construction

C.3.4.1.1 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

C.3.4.1.2 Externals

Printed wiring boards shall not exhibit cracks nor separation around holes. There shall be no delamination on each layer or base material. Measling and crazing

underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board and the spacing between conductors shall not be reduced by a maximum of 25 percent. Crazing along edges of the printed wiring boards shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the smaller of the minimum conductor spacing specified on drawings or 1.6mm. The cured solder resist shall be free from tackiness, blistering and delamination. Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the provisions of manufacturing drawings.

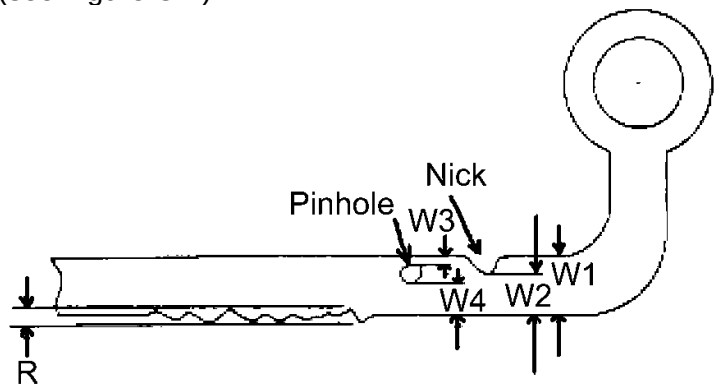
C.3.4.2 Dimensions

C.3.4.2.1 Externals

The external dimensions, finished hole diameter and conductor spacing shall be in accordance with the requirements of Table C-5.

C.3.4.2.2 Conductor

The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.13mm in the difference between the convex and concave portions in any range of 13mm in length (see Figure C-4).



W1 ≥ (Minimum finished conductor width) ≥ 0.08 (mm)
W2 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08 (mm)
W3+W4 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08 (mm)
R ≤ 0.13 (mm) in any range of 13 mm in length

Figure C-4. Conductor Defects

C.3.4.3 Marking

When tested in accordance with paragraphs C.4.4.2.1 and C.4.4.2.3, printed wiring boards shall meet the requirements specified in a) to d) and e), respectively.

a) Unless otherwise specified, printed wiring boards shall be marked with the part number, year and month manufactured, manufacturer's name or its identification code, and production serial number or lot number. The production serial number shall be provided so that the complete manufacturing process can be traced.
b) The marking shall not encroach on a hole for inserting a lead or land for surface mounting.
c) The marking shall be produced by the same process used in producing conductive patterns, by the use of marking ink specified in paragraph C.3.2.6, or by laser marking. The marking shall not affect any function, performance or reliability of the printed wiring boards.
d) If marking on the printed wiring boards is impossible, the marking may be placed on a tag.
e) All marking shall remain legible.

C.3.4.4 Through Holes

When printed circuit boards are tested as specified in paragraph C.4.4.2.2, the plating inside through holes shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall be acceptable, provided that the hole diameter is not reduced below its lower limit specified on drawings. Resin recession at the outer surface of the plated-through hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 80μm and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure C-5).

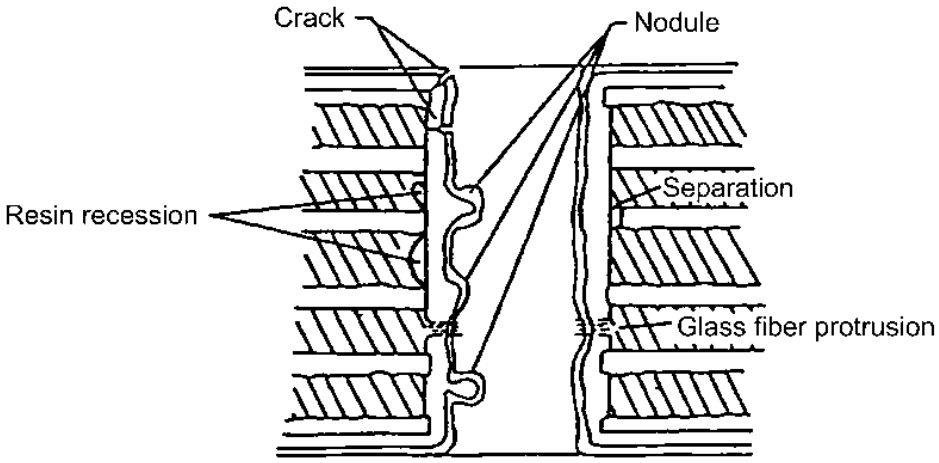


Figure C-5. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through

hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane, or at a wire connection (see Figure C-6).

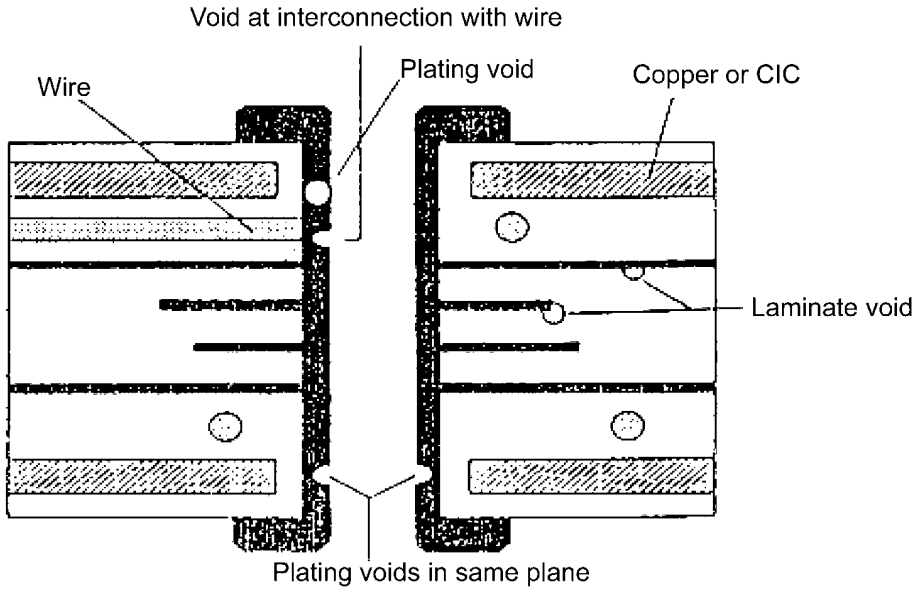


Figure C-6. Plating Voids and Laminate Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the interface circumference in horizontal microsection, and shall not exceed 50 percent of the interface in the same plane in vertical microsection. The resin smear at the interface of through hole plating and a wire shall be a maximum of 50 percent of the wire diameter in the same plane. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness. Nail heading at the interface with a wire is not specified (see Figure C-7).

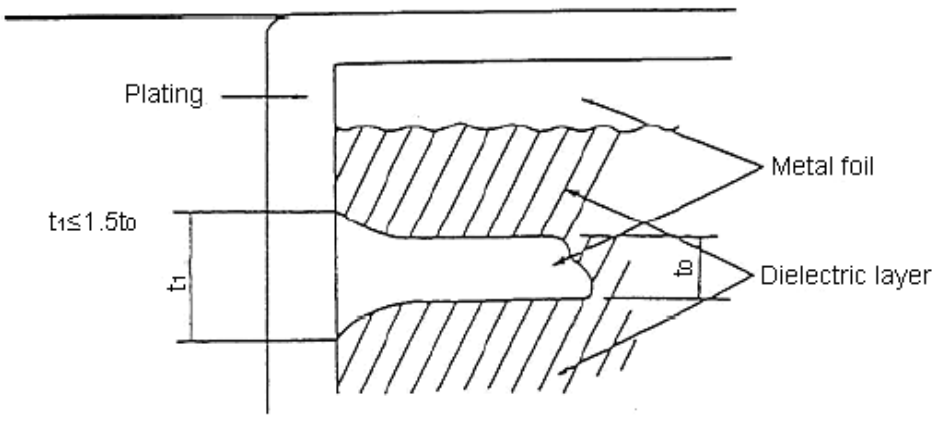


Figure C-7. Nail Heading

c) Plating thickness and others
The thickness of plating and solder coating shall be as specified in Table C-7.

Table C-7. Plating or Coating Thickness

Unit: μm

Plating material	Surface and through hole plating thickness
Electroless copper	Min. 30 in design value
Electrolytic copper	Min. 30 in design value The finished thickness of electroless and electrolytic copper plating shall be minimum 45μm in total.
EN : Electroless nickel(1)	3.00 to 8.00
EP : Electroless palladium(1)	0.05 to 0.36
IG + EG : Immersion gold + Electroless gold plating(1)	0.10 to 0.40

Note: (1) The thickness shall meet the requirements specified in drawings. If not specified in the drawings, it shall be as specified here.

d) Layer-to-layer registration
The layer-to-layer registration error shall not exceed 0.35mm, except for wiring layers.

e) Dielectric layer thickness
The dielectric layer between conductor layers shall be no less than 0.08mm in thickness. The thickness of a dielectric layer where wires are crossed is not specified.

f) Annular ring
When the annular rings of internal and external layers are measured in accordance with C.4.4.2.2 f), the annular ring of a plated-through hole shall be a minimum of 45μm in diameter. The annular ring of a non-plated-through hole shall be not less than 0.38mm in diameter and contain no defects.

g) Undercut
The undercut along a conductor edge shall not exceed the total thickness of the copper foil and plated copper.

h) Spacing between hole wall plating and internal conductor
The spacing between the hole wall plating and an internal conductor shall be not less than 0.20mm.

C.3.5 Workmanship

Printed wiring boards shall not exhibit defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

C.3.5.1 Bow and Twist

When printed wiring boards are tested as specified in paragraph C.4.4.3.1, the maximum limit for bow and twist shall be 1.5 percent, unless otherwise specified on manufacturing drawings.

C.3.5.2 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.

C.3.6 Plating Adhesion and Overhang

When printed wiring boards are tested as specified in paragraph C.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

C.3.7 Cleanliness

When tested as specified in paragraph C.4.4.5, printed wiring boards shall meet the following requirements.

a) The printed wiring boards shall exhibit no ionic contamination and fouling including dirt, oil, corrosion, corrosion product, salt, soot, grease, finger print, mold release agent, foreign material and flux residues.
b) The resistivity of the solvent extract shall be not less than $2\times10^{6}\Omega\cdot$cm.

C.3.8 Electrical Performance

The printed wiring board shall meet the following electrical requirements.

C.3.8.1 Dielectric Withstanding Voltage

When printed wiring boards are tested as specified in paragraph C.4.4.6.1, there shall be no insulation breakdown, flashover or sparkover.

C.3.8.2 Insulation Resistance

When tested as specified in paragraph C.4.4.6.3, the insulation resistance shall be not less than 500MΩ where wires are crossed, between wires in parallel, at the surface and internal circuit layers or at metal core for heat radiation.

C.3.8.3 Circuitry

When printed wiring boards are tested as specified in paragraph C.4.4.6.4, there shall be no open circuit or short-circuiting between circuit patterns or wiring.

C.3.8.4 Connection Resistance

a) Production Printed Wiring Boards (No.1 to No.6)
When printed wiring boards are tested as specified in paragraph C.4.4.6.2, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers cannot be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri=2\rho\frac{l}{W \bullet t}(m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

b) Test pattern G
When tested as specified in paragraph C.4.4.6.2, the connection resistance shall not exceed 1Ω.

C.3.9 Mechanical Performance

Printed wiring board shall meet the following mechanical requirements.

C.3.9.1 Terminal Pull Strength

When tested as specified in paragraph C.4.4.7.1, printed wiring board shall meet the following requirements.

a) Terminal pull
Min. 1380N/cm^2
b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph C.4.4.2.1, there shall be no loosening around the through holes.
c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with C.4.4.2.2 a), there shall be no cracks, blistering, measling or delamination.

C.3.9.2 Solderability

When tested as specified in paragraph C.4.4.7.2, printed wiring boards shall meet the following requirements.

a) Hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder.
b) Surface solderability
A minimum of 95 percent of the surface conductor area shall be covered

uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they shall not be concentrated at a point.

C.3.10 Environmental Performance

Printed wiring board shall meet the following environmental requirements.

C.3.10.1 Thermal Shock

C.3.10.1.1 Thermal Shock (I) (applicable to qualification test)

When printed wiring boards are tested as specified in paragraph C.4.4.8.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph C.3.8.3 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

C.3.10.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed wiring boards are tested as specified in paragraph C.4.4.8.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph C.3.8.3 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

C.3.10.2 Hot Oil Resistance

When printed wiring boards are tested as specified in paragraph C.4.4.8.3, there shall be no open circuit, blistering, measling, crazing or delamination. The printed wiring boards shall meet the requirements specified in paragraph C.3.8.3 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

C.3.10.3 Thermal Stress

When tested as specified in paragraph C.4.4.8.4, printed wiring boards shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Copper foil, wires, metal cores for heat radiation
There shall be no cracks in the vertical microsection of through holes in internal copper foils, wires or metal cores for heat radiation.

c) Laminate voids
Laminate voids with the longest dimension of 76μm as a maximum shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings.

C.3.10.4 Humidity Resistance

When tested as specified in paragraph C.4.4.8.2, printed wiring boards shall meet the following requirements.

a) Bow and twist
The maximum limit for bow and twist shall be 1.5 percent.

b) Dielectric withstanding voltage
There shall be no insulation breakdown, flashover or sparkover.

c) Insulation resistance
The insulation resistance shall be not less than 500MΩ where wires are crossed, between wires in parallel, at the surface and internal circuit layers or at metal core layer for heat radiation.

d) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

C.3.10.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph C.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph C.3.8.1 shall be satisfied.

C.4. Quality Assurance Provisions

C.4.1 In-Process Inspection

The in-process inspection shall be as specified in Table C-8.

Table C-8. In-Process Inspection

No.	Inspection item	Requirement paragraph	Test method paragraph	Quantity of samples	
				Production printed wiring board	Test coupon
1	Externals, construction and dimensions of internal layers Externals and construction Dimensions Marking Workmanship(1)	 C.3.4.1 C.3.4.2 C.3.4.3 C.3.5	C.4.4.2.1 C.4.4.3	100%	100%
2	Cleanliness(2)	C.3.7	C.4.4.5	2(3)	-

Notes:

(1) The requirements specified in paragraph C.3.5.1 are not applied.

(2) The cleanliness inspection shall be performed for the production printed wiring boards which are to be coated with solder resist, immediately before the application of solder resist.

(3) Two production printed wiring boards shall be selected from the lot to be coated with solder resist at the same time.

C.4.2 Qualification Test

C.4.2.1 Sample

Samples shall be production printed wiring boards approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons specified in Table C-8 shall also be submitted. The samples shall consist of the test coupons and sample products manufactured simultaneously.

C.4.2.2 Test Items and Number of Samples

The tests within each group shall be performed in the order listed in Table C-9. Upon completion of Group I through IV tests, Group V through X tests shall be performed using specimens allocated to the appropriate group tests. Group V through X tests may be performed in any order regardless of group number. However, the tests within each group of V through X shall be performed in the specified order. The number of samples submitted for each test shall be as specified in Table C-9.

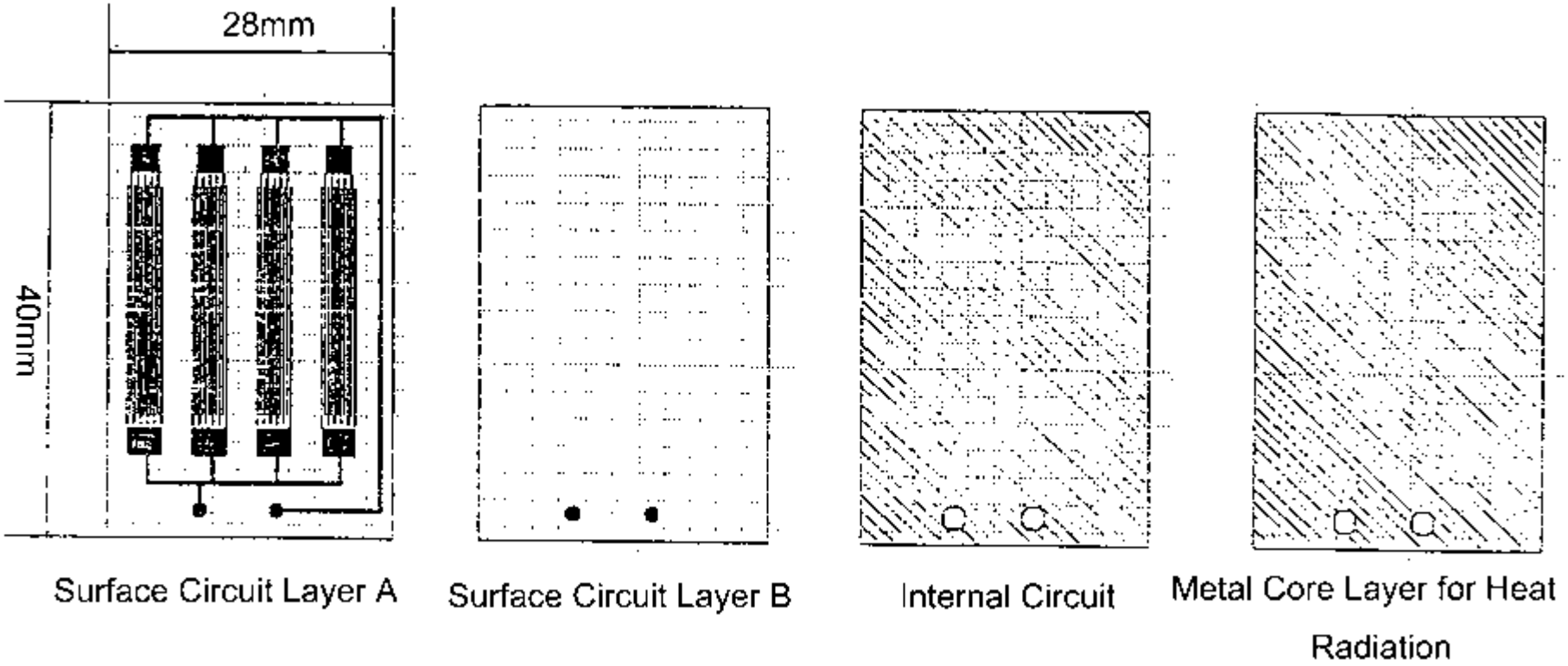
Table C-9. Qualification Test

Test			Requirement paragraph	Test method paragraph	Samples		Quantity of allowable defects
Group	Order	Test item			No.(1)	Test coupon	
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	C.3.4.1 C.3.4.2 C.3.4.3	C.4.4.2.1	No. 1 to No. 6	A to G	0
	2	Workmanship	C.3.5	C.4.4.3			
II	1	Circuitry	C.3.8.3	C.4.4.6.4	No. 1 to No. 6	A to E, G	
III	1	Connection resistance	C.3.8.4	C.4.4.6.2	No. 1 to No. 6	G	
IV	1	Dielectric withstanding voltage	C.3.8.1	C.4.4.6.1	No. 1 to No. 6	A to E	
	2	Insulation resistance	C.3.8.2	C.4.4.6.3	No. 1 to No. 6	A to E	
V	1	Through holes	C.3.4.4	C.4.4.2.2	No. 1	A, E, G	
VI	1	Plating adhesion and overhang	C.3.6	C.4.4.4	No. 2	F	
	2	Marking	C.3.4.3	C.4.4.2.3	No. 2	-	
VII	1	Thermal stress	C.3.10.3	C.4.4.8.4	No. 3	E	
	2	Solderability	C.3.9.2	C.4.4.7.2	No. 3	B, E	
VIII	1	Terminal pull strength	C.3.9.1	C.4.4.7.1	No. 4	F	
	2	Hot oil resistance	C.3.10.2	C.4.4.8.3	No. 4	A to E, G	
IX	1	Thermal shock (I)	C.3.10.1.1	C.4.4.8.1 a)	No. 5	A to E, G	
	2	Radiation hardness	C.3.10.5	C.4.4.8.5	No. 5	A to E, G	
X	1	Humidity resistance	C.3.10.4	C.4.4.8.2	No. 6	A to E, G	
-		Materials	C.3.2	N/A	(2)	-	N/A

Notes:

(1) Six production printed wiring boards shall be prepared for each structure type of the printed wiring board.

(2) Data to certify compliance with design specifications shall be submitted.



Land width: 0.13mm
Conductor spacing: 0.2mm

Figure C-8. Test Coupon

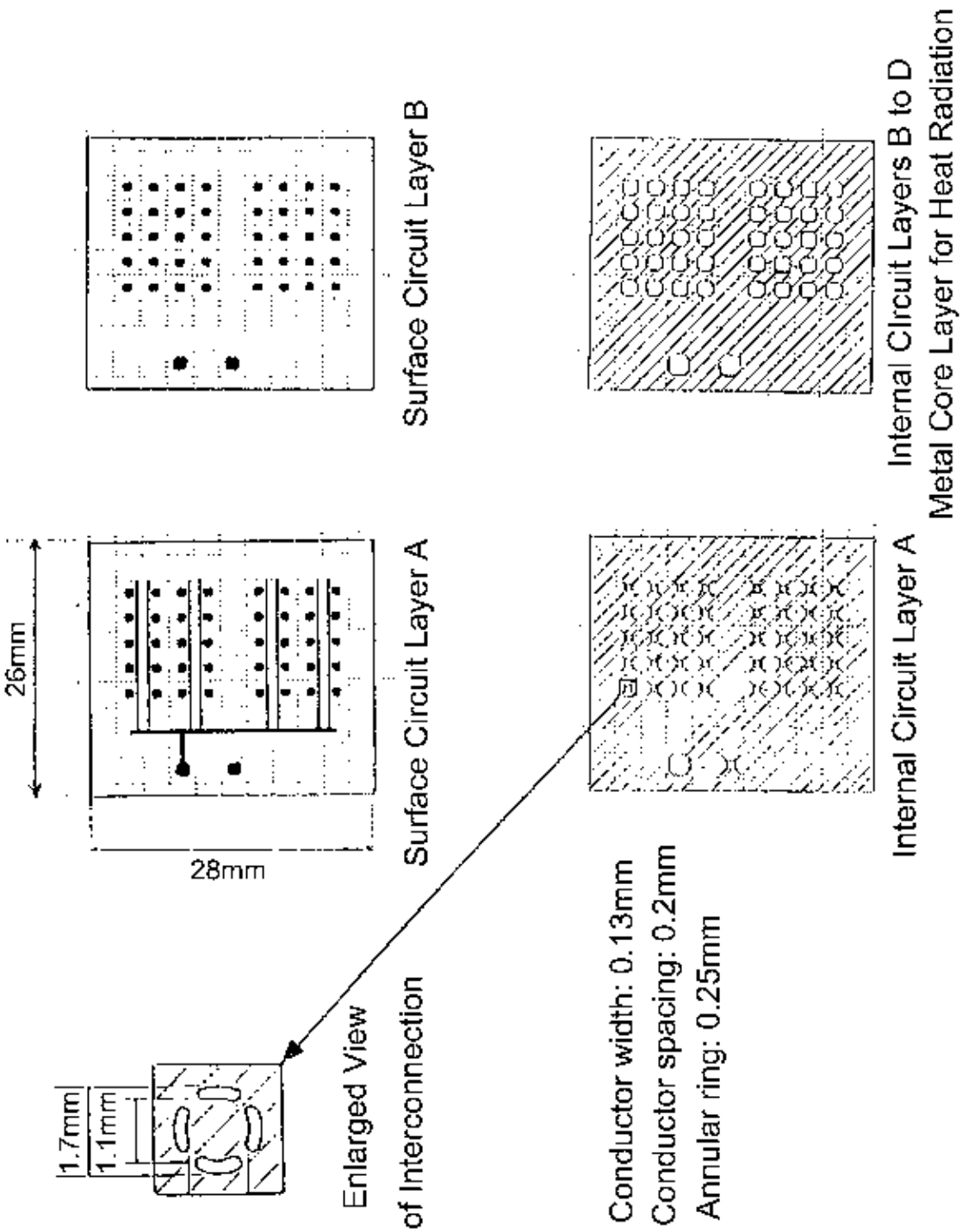


Figure C-8. Test Coupon B

Diameter of wire core: 0.1mm

Figure C-8. Test Coupon C

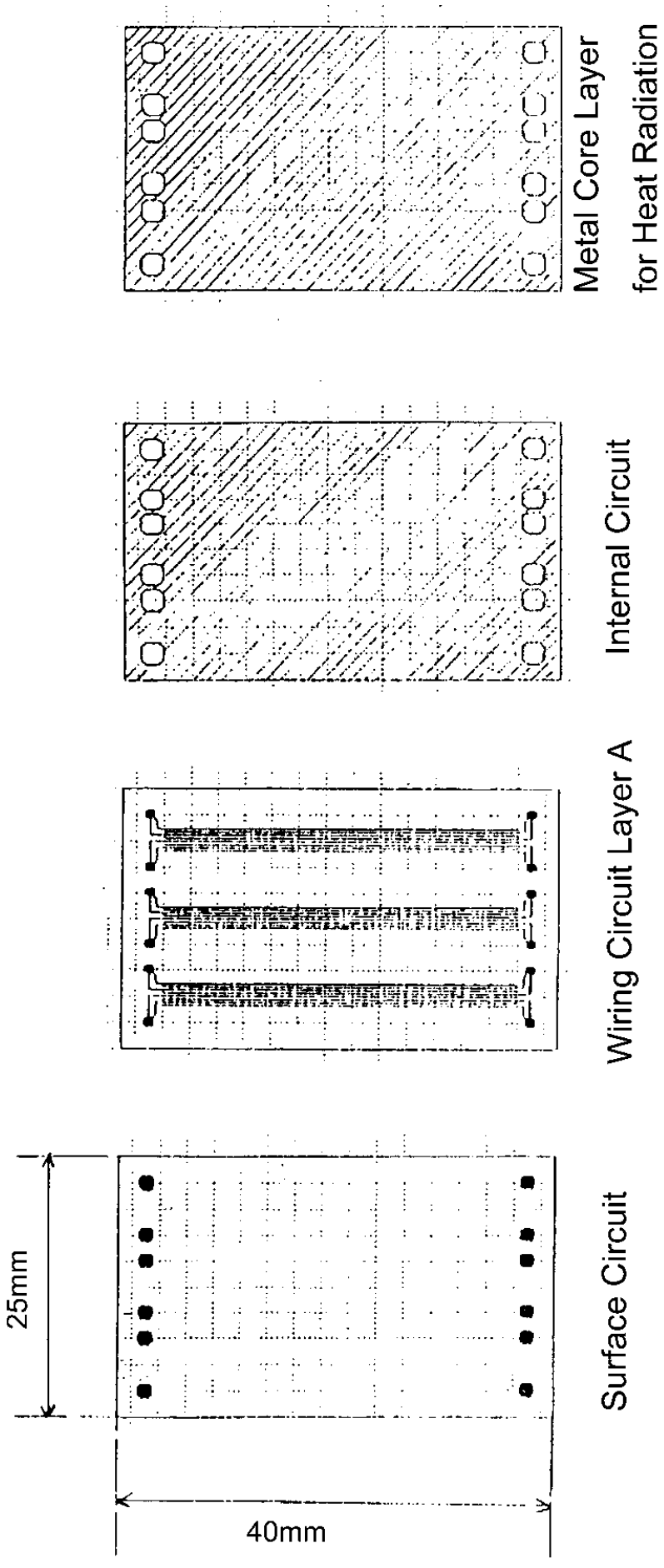


Figure C-8. Test Coupon D

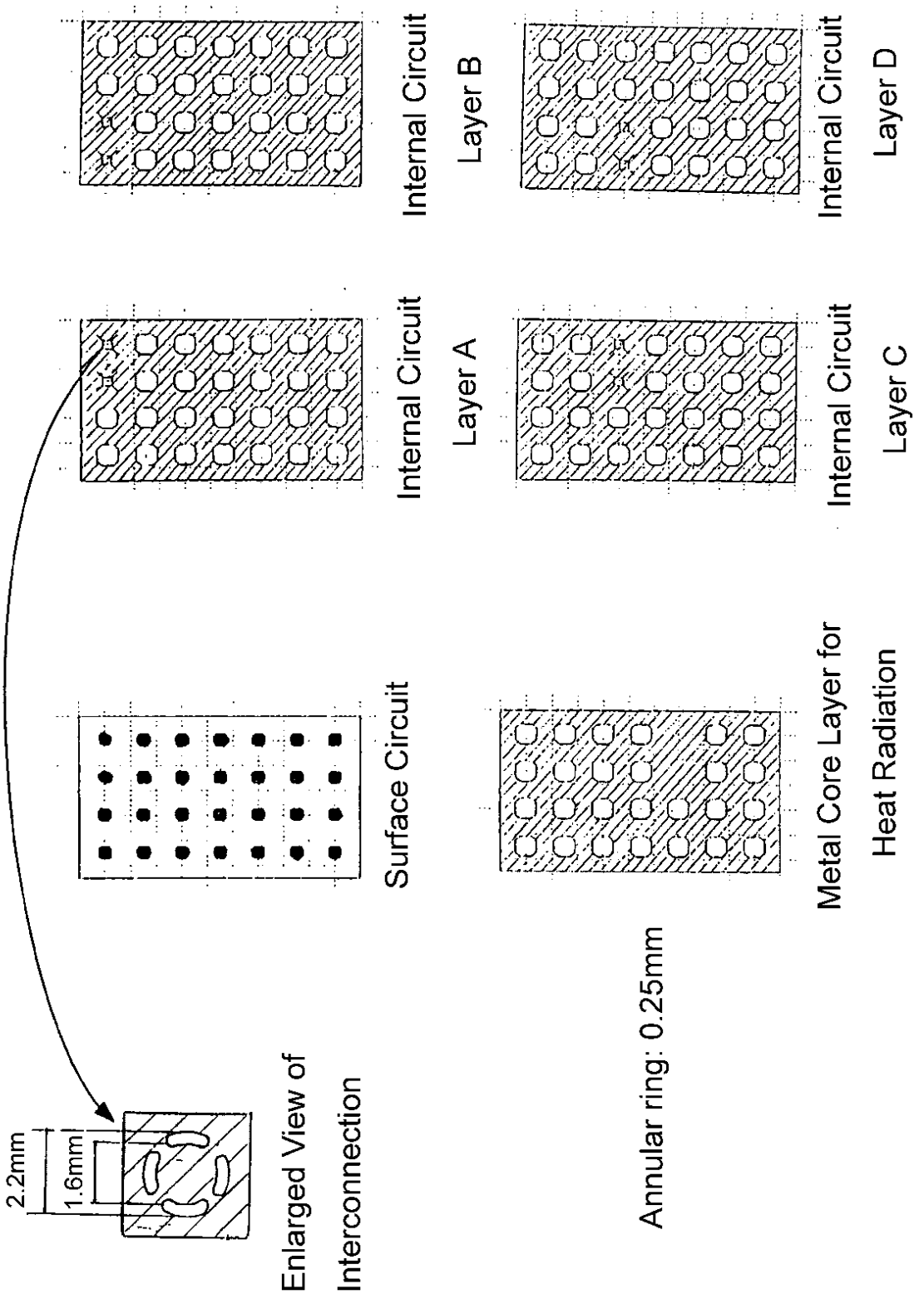
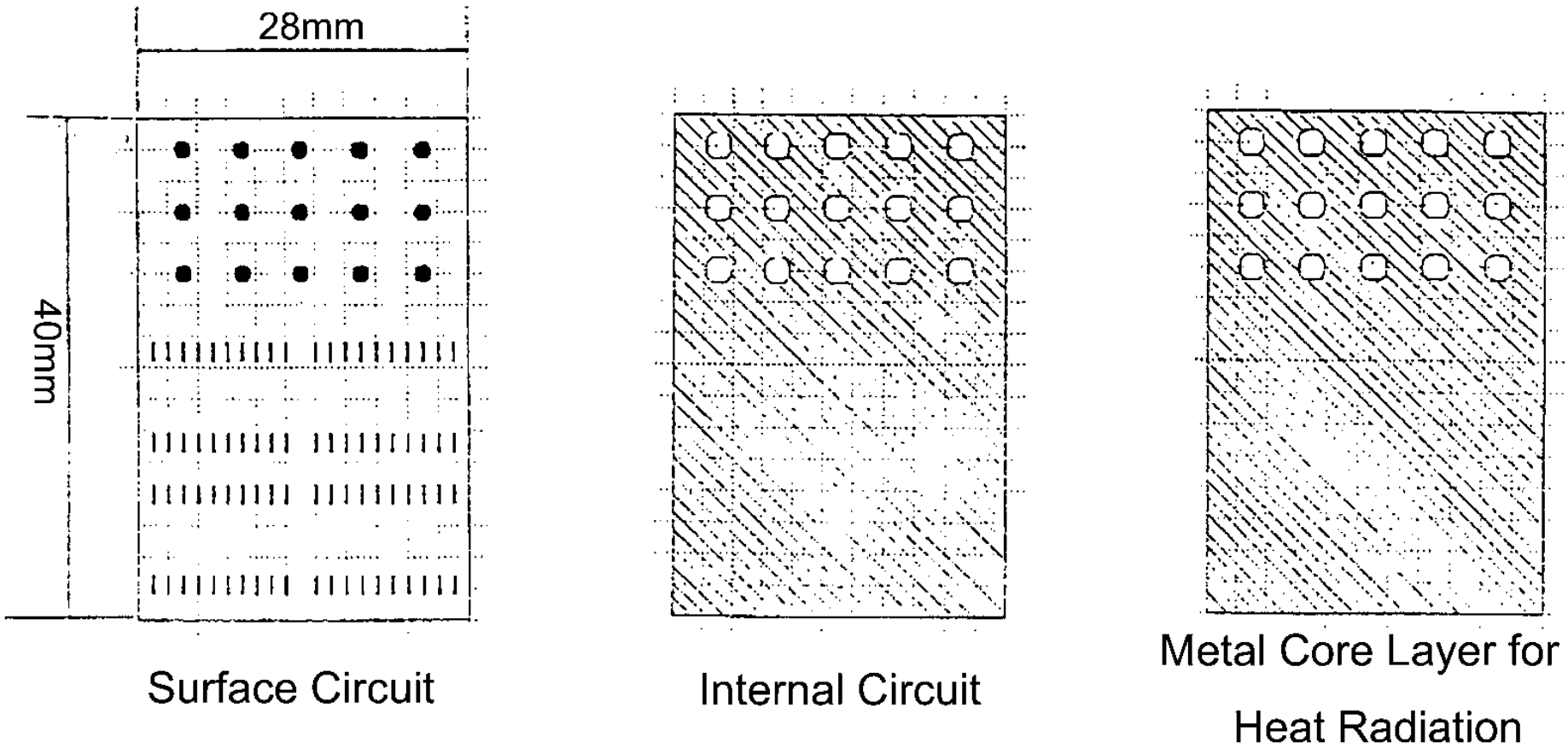


Figure C-8. Test Coupon E



Annular ring: 0.25mm

Figure C-8. Test Coupon F

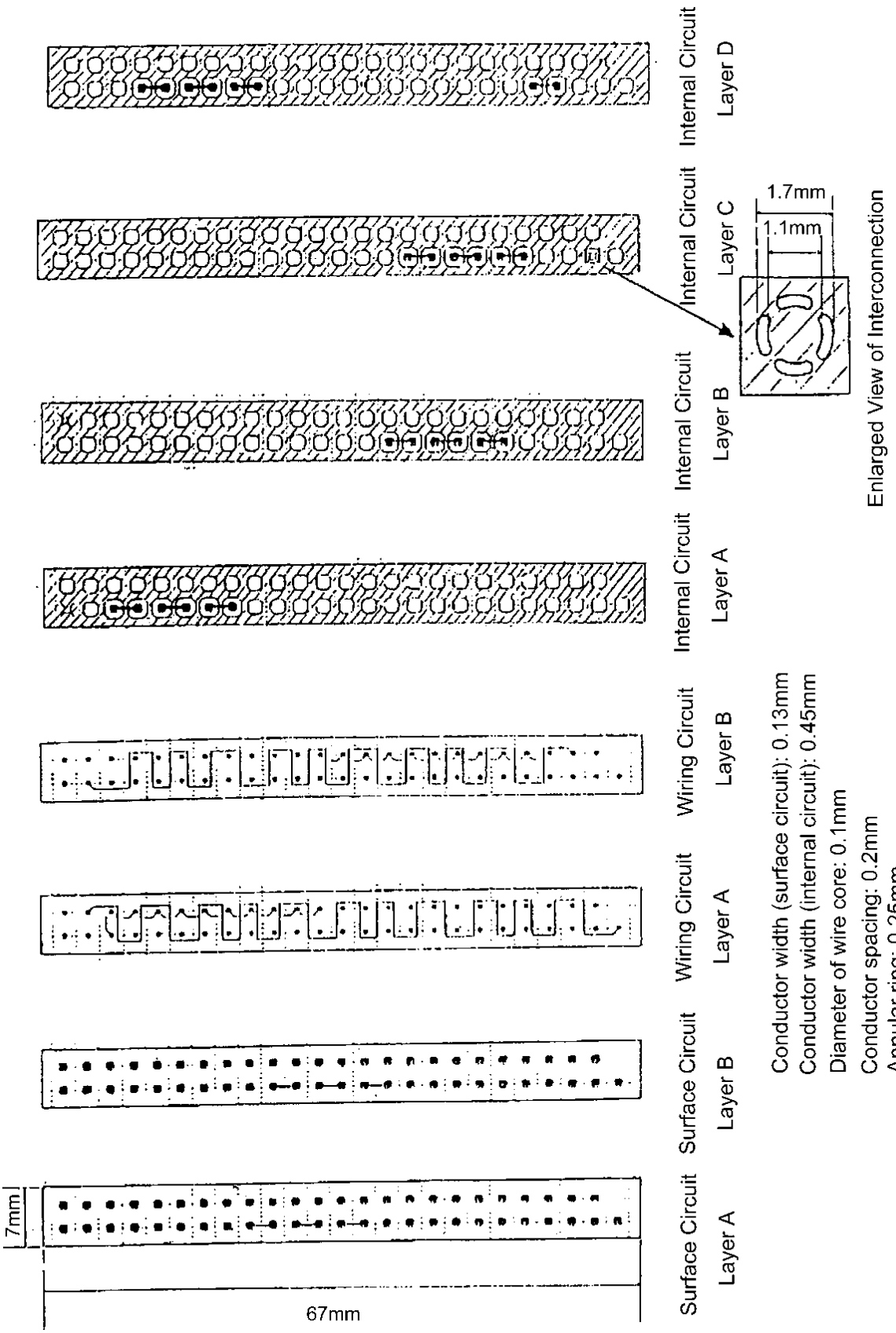


Figure C-8. Test Coupon G

C.4.3 Quality Conformance Inspection

C.4.3.1 Quality Conformance Inspection (Group A)

C.4.3.1.1 Sample

The quality conformance inspection shall be performed on all products. Test coupons and sample products shall be manufactured simultaneously.

C.4.3.1.2 Inspection Items and Sample Size

The items and test order of Group A inspection shall be in accordance with Table C-10. The inspections within each group shall be performed in the order listed.

Table C-10. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Samples	
Group	Order	Inspection item			Production printed wiring board	Test coupon
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	 C.3.4.1 C.3.4.2(1) C.3.4.3	C.4.4.2.1	All	A to G
	2	Workmanship	C.3.5	C.4.4.3		
II	1	Circuitry	C.3.8.3	C.4.4.6.4	All	-
III	1	Connection resistance	C.3.8.4	C.4.4.6.2	-	G(2)
IV	1	Dielectric withstanding voltage	C.3.8.1	C.4.4.6.1	All	-
	2	Insulation resistance	C.3.8.2	C.4.4.6.3	-	A to E(2)
V	1	Through holes	C.3.4.4	C.4.4.2.2	-	G(2)
VI	1	Plating adhesion and overhang	C.3.6	C.4.4.4	Sampling(2)	-
VII	1	Thermal stress	C.3.10.3	C.4.4.8.4	-	E(2)
	2	Solderability	C.3.9.2	C.4.4.7.2	-	B, E(2)
VIII	1	Hot oil resistance	C.3.10.2	C.4.4.8.3	-	G(2)

Notes:

(1) Sampling inspection shall be performed and the AQL shall be 2.5%.

(2) Sampling inspection shall be performed and the “Inspection Level II” of JIS Z 9015-1 and the AQL of 2.5% shall be applied.

C.4.3.2 Quality Conformance Inspection (Group B)

C.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

C.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table C-11. The inspections within each group shall be performed in the order listed.

Table C-11. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Samples	
Group	Order	Inspection item			Production printed wiring board	Test coupon
I	1	Terminal pull strength	C.3.9.1	C.4.4.7.1	-	F(1)
II	1	Thermal shock (II)	C.3.10.1.2	C.4.4.8.1 b)	-	A to E, G(1)
III	1	Humidity resistance	C.3.10.4	C.4.4.8.2	-	A to E, G(1)

Note: (1) Sampling inspection shall be performed and the “Inspection Level II” of JIS Z 9015-1 and the AQL of 2.5% shall be applied.

C.4.4 Methods for Test and Inspection

C.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 20% to 80%, and a luminance of 750 lx as a minimum.

C.4.4.2 Externals, Dimensions, Marking and Others

C.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of printed wiring boards shall be tested. The externals shall be inspected visually.

a) Conductive patterns and edges
Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument with a sufficient accuracy.

b) Annular ring
The annular ring on an external layer shall be measured from the internal surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular ring shall be measured using an optical measuring instrument with a sufficient accuracy.

C.4.4.2.2 Through Holes

a) Vertical microsection
The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, base material thickness and plating thickness) at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board’s length direction.

b) Horizontal microsection

The printed wiring board specimen shall be cut in a direction parallel to a wire to observe the interface of the wire and plating inside the through hole. The interface between the internal conductor layer and plating inside the through hole shall be microsectioned. Each microsection shall be encapsulated and polished in parallel to the microsection to expose the wire and the conductor layer. The integrity of the interfaces of wire and internal conductor (interconnections in the horizontal direction) shall be inspected at a magnification of 50 to 100X.

c) Plating thickness

(1) The plating thickness shall be measured using microsections prepared in accordance with paragraph C.4.4.2.2 a) at a magnification of minimum 200X. Measurements shall be averaged from three determinations for a plated-through hole. Isolated thick or thin sections shall not be used for averaging.

(2) EP and IG + EG plating thickness can not be measured by the cross-section observation using an optical instrument. Therefore, those plating thickness shall be measured by using the X-ray fluorescence film thickness measurement system on the board surface.

d) Layer-to-layer registration

The layer-to-layer registration shall be measured at a magnification of 25 to 100X using microsections prepared in accordance with paragraph C.4.4.2.2 a). The misregistration shall be inspected around the hole in the direction parallel to the board length and the vertical direction (see figure C-9).

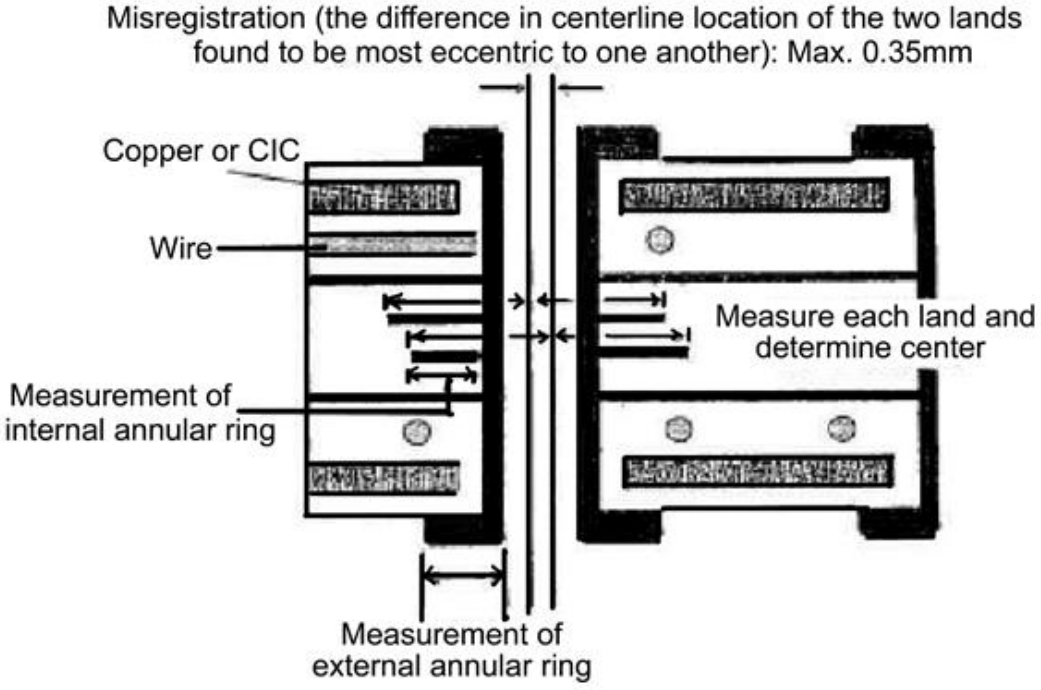


Figure C-9. Measurement of Layer-to-Layer Registration and Annular Ring

e) Dielectric layer thickness
The dielectric layer thickness shall be measured using microsections prepared in accordance with paragraph C.4.4.2.2 a).

f) Annular ring
Measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure C-9).

g) Undercut
The undercut shall be measured using the microsection prepared in accordance with paragraph C.4.4.2.2 a).

h) Spacing between hole wall plating and internal conductor
The spacing between the hole wall plating and an internal conductor layer shall be measured using the microsection prepared in accordance with paragraph C.4.4.2.2 a).

C.4.4.2.3 Marking

The marking test shall be performed under the following conditions. The marking deterioration shall be inspected visually.

a) The specimen shall be immersed in solder of 260 to 270°C for a period of 10 to 11 seconds.
b) The specimen shall be immersed in isopropyl alcohol at room temperature for a period of 30 to 35 minutes.

C.4.4.2.4 Solder Resist Thickness

The solder resist thickness shall be measured using microsections prepared in accordance with paragraph C.4.4.2.2 a) at a magnification of minimum 200X.

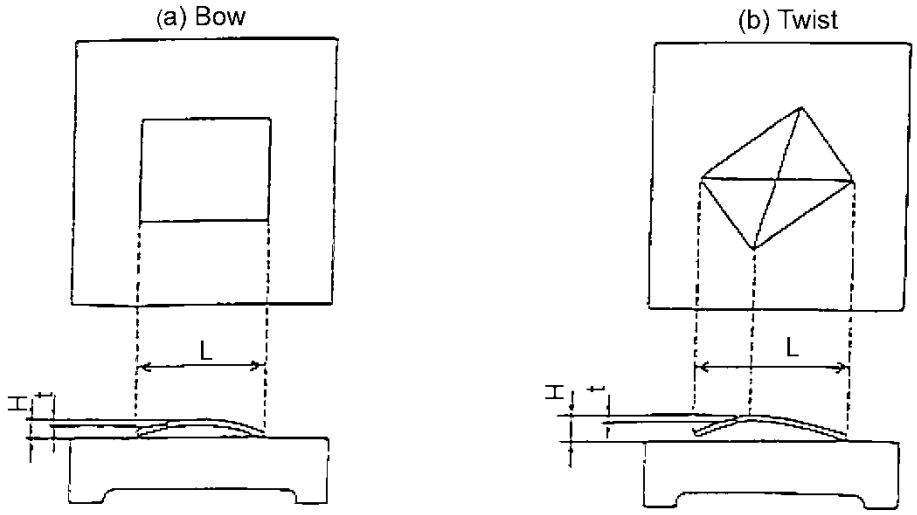
C.4.4.3 Workmanship

The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

C.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure C-10). The percent bow and twist shall be calculated by the following formula.

Percent bow and twist = $\frac{H-t}{L} \times 100$ (%)



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure C-10. Measurement of Bow and Twist

C.4.4.4 Plating Adhesion and Overhang

The test shall be performed in accordance with paragraph 8.5 of JIS C 5012. A strip of pressure sensitive tape (12.7mm wide and a minimum of 50mm in length), conforming to type I, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is evidence of slivers, but not a plating adhesion failure.

C.4.4.5 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 percent by volume of isopropyl alcohol and 25 percent by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6 \times 10^6 \Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top

until 100ml of the wash solution is collected from each board surface of 6.5cm^2 (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table C-12 may be used to perform the cleanliness test.

Table C-12. Equivalent Factors

Method	Resistivity ($\times 10^6 \Omega \cdot$cm)	Equivalent factor	Equivalents of sodium chloride (μg/cm^2)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.20
Ionograph(2)	2	2.01	3.10
Ion Chaser(3)	2	3.25	3.81

Notes:
(1) Alpha Metals Incorporated, “Omega Meter”
(2) Alpha Metals Incorporated, “Ionograph”
(3) E. I. Dupont Company, Incorporated, “Ion Chaser”

C.4.4.6 Electrical Performance

The electrical performance tests shall be performed as follows.

C.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: 1000V±25V_{DC}
b) Duration: 30±3 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

C.4.4.6.2 Connection Resistance

The resistance between the through hole terminals shall be measured using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5mΩ.

C.4.4.6.3 Insulation Resistance

The insulation resistance test shall be performed in accordance with the Test Method 302 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: 500V_{DC}
b) Duration: 1 minute

C.4.4.6.4 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity.

b) Circuit shorts
A voltage of 250V_{DC} shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

C.4.4.7 Mechanical Performance

The mechanical performance tests shall be performed as follows.

C.4.4.7.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.
Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

C.4.4.7.2 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph C.4.4.8.4.

b) Surface solderability
After dipping the specimen into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

C.4.4.8 Environmental Performance

The environmental performance tests shall be performed as follows.

C.4.4.8.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. At the completion of the test, the specimen shall be inspected in accordance with paragraphs C.4.4.2, C.4.4.6.4 and C.4.4.6.2. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
The temperatures specified below shall be reached within five minutes.
1) Type I board
Test conditions: -30°C (for 30 minutes) ⟷ +125°C (for 30 minutes); 1000 cycles.
2) Type II and III board
Test conditions: -30°C (for 30 minutes) ⟷ +100°C (for 30 minutes); 1000 cycles.

b) Thermal shock (II) (applicable to quality conformance inspection)
The temperatures specified below shall be reached within five minutes.
Test conditions: -65°C (for 30 minutes) ⟷ +125°C (for 30 minutes); 100 cycles.

C.4.4.8.2 Humidity Resistance

The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and inspected in accordance with paragraphs C.4.4.2, C.4.4.3.1, C.4.4.6.1 and C.4.4.6.3.

C.4.4.8.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 10 seconds and cooled in water at room temperature for 10 seconds. Immersion and cooling shall be performed for 10 cycles. At the completion of the test, the specimen shall be inspected in accordance with paragraphs C.4.4.2, C.4.4.6.4 and C.4.4.6.2.

C.4.4.8.4 Thermal Stress

The specimen shall be conditioned by drying for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed (TYPE RMA MIL-F-14256) and floated in a solder bath (Sn: 63±5 percent, temperature: 288±5°C) for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defect on the external surface, the sample shall be inspected for any crack on the internal copper foil, wire or metal core layer for heat radiation and laminate voids using the microsection prepared in accordance with paragraph C.4.4.2.2 a). Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

C.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. Tests for dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraphs C.4.4.6.1 and C.4.4.6.3, respectively. The insulation resistance shall be measured in the same circuit as the one used for the dielectric withstanding voltage test.

APPENDIX D

PRINTED WIRING BOARDS,
FLEXIBLE,
POLYIMIDE FILM BASE MATERIAL

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX D

PRINTED WIRING BOARDS, FLEXIBLE, POLYIMIDE FILM BASE MATERIAL

D.1. General

D.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for flexible printed circuits (hereinafter referred to as "FPC"), which are constructed of a flexible insulating film substrate, etched copper conductor strands on one or both sides of the film, and an insulating film laminated to the etched element.

D.1.2 Classification

Products covered by this specification shall be classified as specified in Table D-1.

Table D-1. Classification

Base material	Construction	Remarks
Polyimide film	Single-sided FPC without stiffeners	Applicable for not mounting parts.
	Double-sided FPC without stiffeners	
	Single-sided FPC with stiffeners	Applicable for mounting parts.
	Double-sided FPC with stiffeners	

D.1.3 Part Number

The part number of the FPCs is in the following form.

Example: JAXA(1) 2140/D <u>101</u> <u>I</u> <u>I</u>

101	I	I
Individual identification	Base material code (see D.1.3.1)	Processing code (see D.1.3.2)

Note: (1) "JAXA" indicates the part is for space use and may be abbreviated “J”.

D.1.3.1 Base Material Code

The base material code of the FPC is as follows.

I: FPC base material is polyimide film without stiffener.

I-GI: FPC base material is polyimide film with type GI(1) stiffener specified in IPC-4101 or JPCA/NASDA-SCL01.

Note: (1) Applicable standard for GI type is as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), are as specified in the Application Data Sheet (ADS).

D.1.3.2 Processing Code

The processing code for the FPC is as follows.

I: Single-sided FPC without stiffeners
II: Double-sided FPC without stiffeners
III: Single-sided FPC with stiffeners
IV: Double-sided FPC with stiffeners

D.2. Applicable Documents

The applicable documents shall be as specified in paragraph 2.

D.3. Requirements

D.3.1 Qualification Coverage

Qualification shall be valid for FPC that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs D.3.2 to D.3.8. Products shall have structures, types of flexible base material and base materials of stiffener listed in Table D-2. Products of each processing code are qualified if any representative sample of the processing code is qualified. As shown in Table D-3 processing code IV covers processing code I, II and III, processing code III covers processing code I and processing code II covers processing code I. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

Table D-2. Qualification Coverage

Design conditions / Processing code	Construction	Flexible base material	Stiffener base material
I	Single-sided FPC without stiffeners	Polyimide	-
II	Double-sided FPC without stiffeners	Polyimide	-
III	Single-sided FPC with stiffeners	Polyimide	GI
IV	Double-sided FPC with stiffeners	Polyimide	GI

Table D-3. Classification of Qualification Coverage by Processing Type

Processing code of sample FPC	Processing code of FPC qualified			
	I	II	III	IV
I	O			
II	O	O		
III	O		O	
IV	O	O	O	O

D.3.2 Materials

The materials shall be specified as follows and as specified in paragraph 3.3.

D.3.2.1 Copper-Clad Base Material

The base material shall be polyimide film with a minimum thickness of 25μm and bonded on one or both sides with copper foil. The material shall be in compliance with IPC-4204 or JPCA/NASDA-SCL01. The applicable standards for the copper-clad material shall be specified in the detail specification. The details of GI base material including type and glass transition temperature (Tg), shall be defined in the ADS.

D.3.2.2 Cover Lay

The material used in a cover lay shall be a polyimide film which is coated with adhesive on one side. The material shall be as specified in IPC-4203 or the equivalent.

D.3.2.3 Adhesives

The adhesives shall be type GI prepreg which conforms to IPC-4101 or JPCA/NASDA-SCL01, or bonding film compliant with IPC-4203. The applicable standards for the adhesives used shall be specified in the detail specification. The details of GI base material including type and glass transition temperature (Tg), shall be defined in the ADS.

D.3.2.4 Stiffeners

The stiffeners shall be manufactured using GI type stiffener material specified in accordance with IPC-4101 or JPCA/NASDA-SCL01. The applicable standards for the material used for the stiffener shall be specified in the detail specification. The details of GI base material including type and glass transition temperature (Tg), shall be defined in the ADS.

D.3.2.5 Marking Ink

The marking shall be produced by using epoxy resin base inks that do not easily vanish by any solvent. The marking shall not affect any function, performance or reliability of the FPC.

D.3.3 Design and Construction

D.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

FPCs shall be designed and their manufacturing drawings shall be prepared in accordance with this specification. Unless otherwise specified all locations on drawings shall be indicated at grid points. The basic grid spacing shall be 2.54mm. The secondary grid may be used with 1.27mm spacing. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing

drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

D.3.3.2 Surface Treatment of Exposed Terminals

Unless specified on drawings, the exposed terminals shall be covered with solder coating or plated with fused solder.

D.3.3.3 Plating

D.3.3.3.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

D.3.3.3.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

D.3.3.3.3 Electrolytic Solder Plating

The electrolytic solder plating shall contain 50 to 70 percent tin. The thickness shall be more than that specified in Table D-4 before fusing. After fusing, the electrolytic solder plating shall be uniform, free from pinholes and pits, and completely cover conductive patterns. However, this provision shall not apply to vertical conductor edges.

D.3.3.3.4 Plating Thickness and Others

The thickness of the plating and solder coating shall be as specified in Table D-4.

Table D-4. Plating Thickness and Others

Unit: μm

Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 25
Electrolytic solder	Min. 8 on surface Min. 3 inside a through hole
Solder coating	There are no requirements on thickness, however, it shall meet the solderability requirements. The solder coating shall not exhibit any dewetting, and completely cover conductive patterns. This provision shall not apply to vertical conductor edges.

D.3.3.4 Interlayer Connection

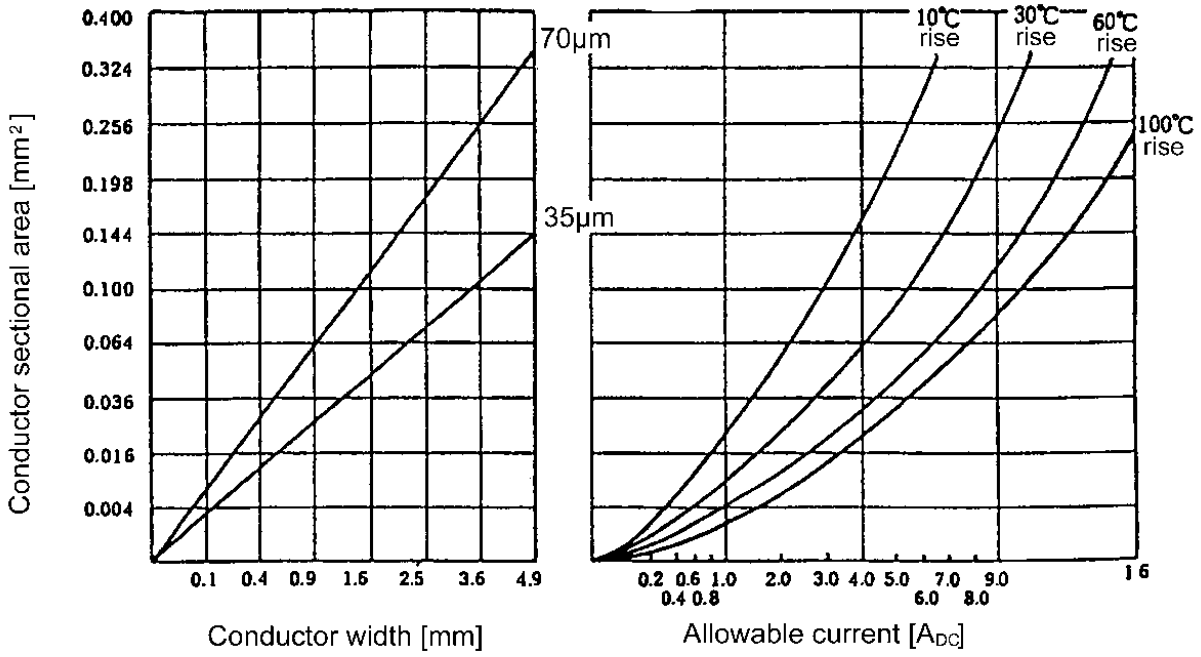
Connection between conductive patterns on both sides of the FPC shall be provided by through holes.

D.3.3.5 Through Hole Diameter After Plating

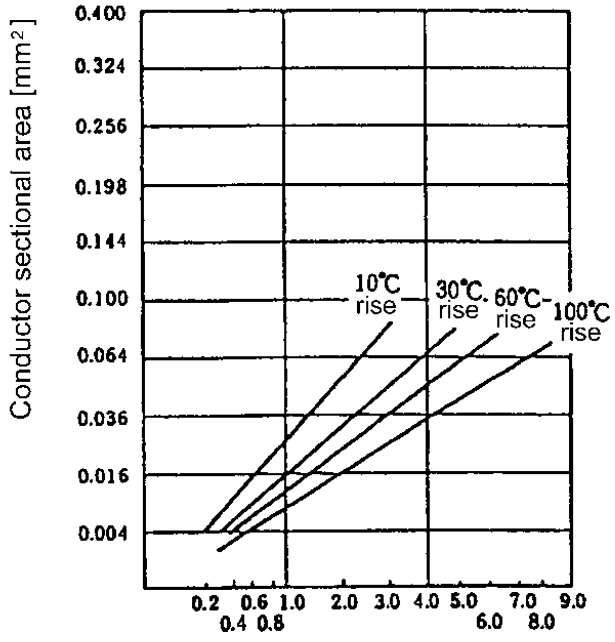
The through hole diameter after plating shall be a minimum of 0.5mm.

D.3.3.6 Conductor Width

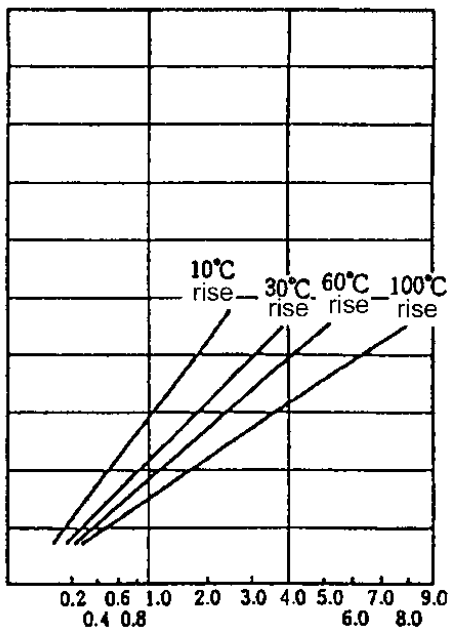
The design value of the conductor width shall be a minimum of 0.3mm. The actual conductor width shall be determined by the current value, allowable temperature rise and conductor sectional area as shown in Figure D-1.



a) When current flows in a single conductor



b) When current flows in multiple conductors (single sided)



c) When current flows in multiple conductors (double sided with an etch-free back surface)

Figure D-1. Conductor Width

D.3.3.7 Conductor Spacing

The design value for the conductor spacing shall be a minimum of 0.3mm. The specific conductor spacing shall depend on the applied voltage as specified in Table D-5.

Table D-5. Conductor Spacing

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing
0-100	0.30
101-300	0.48
301-500	0.86
501 or higher	(0.003xV)+0.1

D.3.3.8 Annular Ring

The design value for the annular ring of a plated-through hole shall be a minimum of 0.3mm. The design value for the annular ring of a plated-through hole shall be a minimum of 0.6mm.

D.3.3.9 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

a) Conductive patterns of FPC
As a rule, the conductive patterns of the FPC shall be smoothly rounded at a pattern corner and at a terminal, as shown in Figure D-2.

b) Lands in large conductive areas of FPC
The lands which are located in large conductive areas shall be provided with relief areas, as shown in Figure D-3.

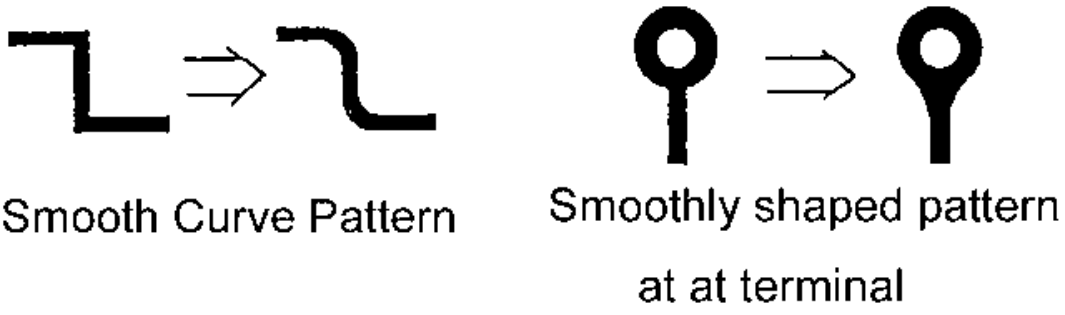


Figure D-2. Smooth Curve Pattern and Smoothly Shaped Pattern at a Terminal

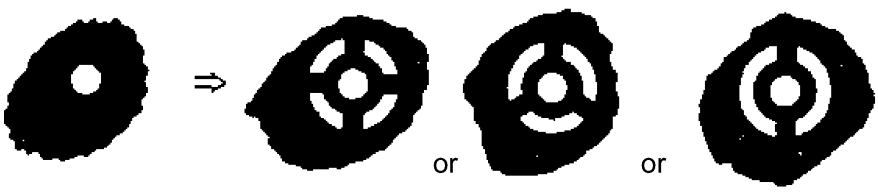


Figure D-3. Lands in Large Conductive Areas

D.3.3.10 Cover Lay

Unless otherwise specified, a cover lay shall be applied over all layers except stiffeners and terminals where a circuit element is soldered. The shape of the cover lay clearance shall be as specified on drawings. The cover lay registration shall be such that the diameter of the access hole, when measured from the portion covered with the polyimide film, shall not be reduced by greater than 0.2mm, due to the extruded adhesive onto lands. The registration shall not reduce the effective annular ring width also. The clearance diameter shall be determined in consideration of the extrusion.

D.3.3.11 Flexible Sections

a) Conductor routing
As a rule, the conductor routing at flexible sections shall be designed to be perpendicular to the bend lines.

b) Pattern density
Unless otherwise specified, the flexible sections shall have a pattern density with uniform conductor width and conductor spacing. The pattern density adjustment shall be made by dividing the pattern or adding dummy patterns.

c) Number of conductor layers
As a rule, the flexible sections shall have a single conductor layer.

d) Location of holes
Plated-through holes and non-plated-through holes shall not be located on flexible sections.

D.3.3.12 Stiffener

As a rule, a stiffener shall be bonded to the portion where a circuit element is soldered in order to protect conductors. The shape of the stiffener shall be as specified on drawings. The stiffener hole diameter shall be at least 0.2mm larger than the diameter of the corresponding plated-through hole and shall be equal to or at least 0.2mm larger than the diameter of the corresponding non-plated-through hole diameter except the FPC plated-through hole without soldering.

D.3.3.12.1 Purpose of Stiffener

A stiffener shall be added to the FPC in order to relieve loads on plated-through holes or non-plated-through holes and protect conductors to prevent damages due to heats generated when components are being soldered.

D.3.3.12.2 Use of FPC Types

A single-sided FPC with stiffeners (processing code III) or double-sided FPC with stiffeners (processing code IV) shall be used for the FPC to which components are soldered.

D.3.3.13 Dimensions

The dimensions of each part of the FPC shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with Table D-6.

Table D-6. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	±0.5 for the dimension of 100 or smaller, and additional 0.15 for every 100 in excess of 100
Board thickness	±10% of standard thickness or ±0.18, whichever is greater
Finished hole diameter	$^{+0.10}_{-0.15}$ for any hole diameter
Conductor width	±0.10 for any conductor width
Conductor spacing	-0.10 for any conductor spacing. The positive tolerance is not specified.
Cover lay	The diameter tolerance of a clearance hole on land shall be ±0.3. The diameter tolerance of a clearance hole on any other part shall be ±0.5.

D.3.3.14 Operating Temperature Range

The FPC shall operate within the temperature range of -65°C to +125°C.

D.3.3.15 Terminal Pull Strength

Implementation design on the FPC shall be designed to control a load for each terminal to be less than 8.83N/hole.

D.3.4 Externals, Dimensions, Marking and Others

D.3.4.1 Externals and Construction

D.3.4.1.1 Externals

a) The FPC shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign material, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance and reliability of the FPC. A slight change of the external surface of the insulating material, such as an excessive conductor removal, shall be acceptable.
b) Unless otherwise specified on drawings, exposed terminals shall be free of dewetting, and the solder shall completely cover conductive patterns. This provision shall not apply to vertical conductor edges.
c) The plating inside through holes shall exhibit no cracks, and shall be continuously smooth from the land. There shall be no voids at through holes.
d) Hole walls shall exhibit no burrs, blistering of plating or other deficiencies, and be well trimmed.

D.3.4.1.2 Plating Thickness

a) Thickness of copper plating
When FPCs are tested in accordance with paragraph D.4.4.2.2, the plating thickness over a surface conductor and inside a through hole shall be not less than 25μm.

b) Thickness of electrolytic solder plating
When FPCs are tested in accordance with paragraph D.4.4.2.2, the plating thickness over a surface conductor and inside a through hole shall be not less than 8μm and 3μm, respectively. The solder shall completely cover conductive patterns (see paragraph D.3.3.3).

D.3.4.2 Dimensions

D.3.4.2.1 Externals

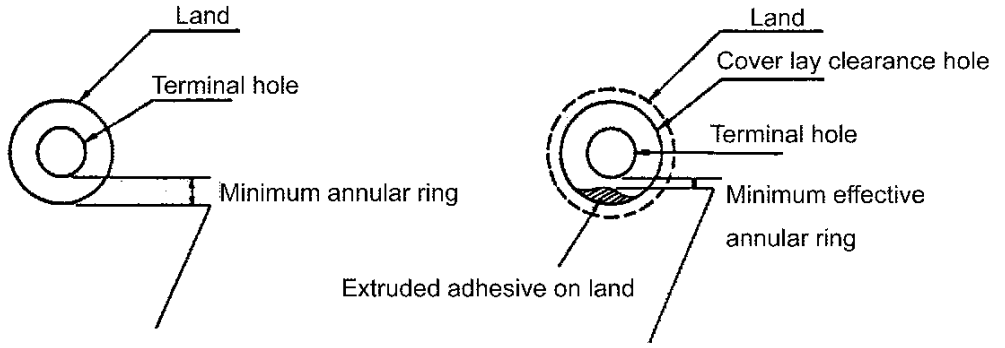
The external dimensions, thickness and finished hole diameter shall be in accordance with the requirements of Table D-6.

D.3.4.2.2 Conductor

a) The conductors and conductor edges shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall meet the following requirements.
   1) The length of any defect shall not exceed the conductor width.
   2) The width of any defect shall not exceed 20 percent of the minimum conductor width.
   3) The width of any defect shall not exceed 20 percent of the defect length.
   4) The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100mm on the FPC.
   5) The roughness at vertical conductor edges shall be less than 0.13mm for the difference between the convex and concave portions, in any range of 13mm in length.

b) The minimum conductor spacing shall be as defined on drawings. When not specified therein, the minimum conductor spacing shall be the minimum dimension specified on drawings minus 0.1mm.

c) The annular ring of a plated-through hole shall be a minimum of 0.1mm when measured from the inside wall of the hole. The annular ring of a non-plated-through hole shall be a minimum of 0.38mm and cannot contain defects (see Figure D-4a). The minimum effective annular ring of a plated-through hole shall be 0.05mm, when measured from the inside wall of the hole. The minimum effective annular ring of a non-plated-through hole shall be 0.25mm, and contain no defects (see Figure D-4b).



Minimum 0.1mm for plated-through hole
Minimum 0.38mm for non-plated through hole

Figure D-4a. Minimum annular ring

Minimum 0.05mm for plated-through hole
Minimum 0.25mm for non-plated through hole

Figure D-4b. Minimum effective annular ring

Figure D-4. Minimum Annular Ring

d) The cladding area of the copper foil and polyimide film substrate shall not exhibit delamination, blistering or wrinkles.

e) The delamination of a cover lay shall be acceptable, provided the following conditions are met:
   1) There is no delamination containing adjacent conductors.
   2) Each delamination is no larger than Φ0.79mm and is not within 1.0 mm from the FPC edge or a clearance hole edge. The delamination is not concentrated at a point.
   3) Along conductor edges, the total delamination does not exceed either 0.5mm in width or 20 percent of the spacing between adjacent conductors, whichever is smaller.

f) Delamination, blistering or wrinkles at the bonding area of FPC and a stiffener shall be acceptable, provided each is no larger than 0.79mm in diameter and is not within 1.0 mm from the FPC edge, and is not concentrated at a point.

g) Each edge of the FPC shall be well trimmed and exhibit no burrs, cracks or other defects.

h) Corner
   1) An internal corner shall be rounded with a radius of 1.5mm as a minimum, unless otherwise specified. When the radius is less than 1.5mm on drawings, the corner shall be rounded with a radius of 2.0mm±0.5mm.
   2) An exterior corner need not be trimmed sharply, unless otherwise specified. When the radius is less than 1.5mm on drawings, the corner may be rounded with the maximum radius of 2.5mm. The exterior corner may be chamfered, as shown in Figure D-5.

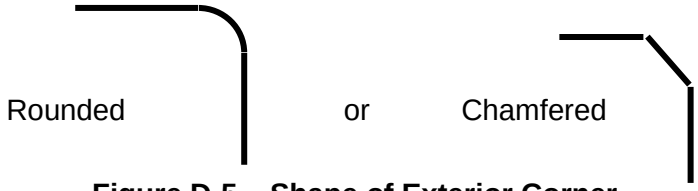


Figure D-5. Shape of Exterior Corner

D.3.4.3 Marking

The marking shall be in accordance with the drawings, and produced by the same process used in producing conductive patterns, by the marking ink specified in paragraph D.3.2.5, or by laser marking. The marking shall not adversely affect any function, performance or reliability of the FPC.

The marking shall remain legible and shall not adversely affect any function of the FPC. Unless otherwise specified, the FPC and test coupons shall be marked with the part number, year and month manufactured, manufacturer's name or its identification code, and production serial number or lot number. The production serial number shall be provided so that the complete manufacturing process can be traced. If marking on each product is impossible, the marking may be placed on a tag.

D.3.5 Workmanship

The FPC shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign material, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the FPC. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

D.3.5.1 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor may be permitted.

D.3.6 Electrical Performance

The FPC shall meet the following electrical performances.

D.3.6.1 Dielectric Withstanding Voltage

When tested as specified in paragraph C.4.4.4.1, there shall be no insulation breakdown, flashover or sparkover.

D.3.6.2 Electrical Conductivity

D.3.6.2.1 Conductor Resistance

When tested as specified in paragraph D.4.4.4.2 a), the conductor resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (R) which is calculated by the following formula.

$$R = R_p + R_T = \sum_i \zeta \frac{2l_i}{W_i(\tau + t)} + \sum_j \zeta \frac{2T}{\pi(t^2 + D_j t)} \ (m\Omega)$$

R_p = Total conductor resistance of conductive pattern
R_T = Total conductor resistance of through hole
W_i = Conductor width (mm)
Ii = Conductor length (mm)
τ = Copper foil thickness (mm)
t = Plating copper thickness (mm)
ζ= Volume resistivity of copper at 20°C: 1.7×10^{-2}mΩ·mm
D_i = Through hole diameter (mm)
T = FPC thickness excluding cover lay thickness (mm)

The resistance measurements shall be recorded not only at room temperature, but also for use in the test specified in paragraph D.3.6.2.2.

D.3.6.2.2 Change of Conductor Resistance

When FPCs are tested as specified in paragraph D.4.4.4.2 b), the change in converted conductor resistance at 20°C before and after the test shall not exceed 10 percent.

D.3.6.3 Insulation Resistance

When FPCs are tested as specified in paragraph D.4.4.4.3, the insulation resistance shall be not less than 100MΩ.

D.3.6.4 Circuitry

When FPCs are tested as specified in paragraph D.4.4.4.4, there shall be no open circuit or short-circuiting between circuit patterns.

D.3.7 Mechanical Performance

FPCs shall meet the following mechanical requirements.

D.3.7.1 Flexibility

D.3.7.1.1 Folding Flexibility

When FPCs are tested as specified in paragraph D.4.4.5.1 a), there shall be no evidence of significant degradation including delamination and conductor damage.

D.3.7.1.2 Flexibility Endurance

When FPCs are tested for the number of cycles specified in drawings in accordance with paragraph D.4.4.5.1 b), there shall be no evidence of significant degradation including delamination and conductor damage. However, the test coupon II shall endure 40 cycles.

D.3.7.2 Terminal Pull Strength

When FPCs are tested as specified in paragraph D.4.4.5.2, the land of a plated-through hole shall withstand a minimum of 8.83N {0.9kgf} pull, and the land of a non-plated-through hole shall withstand a minimum of 8.83N or 343.2N/cm^2 {35.0kgf/cm^2} pull, whichever is smaller. When FPCs are inspected visually, there shall be no loosening around either through holes or conductors.

D.3.7.3 Solderability

When FPCs are tested as specified in paragraph D.4.4.5.3, a minimum of 95 percent of the area which is not covered with any insulator such as cover lays shall be covered uniformly with solder. The scattered existence of pinholes, dewetting or small roughened points on the surface shall be acceptable provided that they are not concentrated in one area. There shall be no delamination of any insulators such as cover lays.

D.3.8 Environmental Performance

FPCs shall meet the following environmental requirements.

D.3.8.1 Thermal Shock

When FPCs are tested as specified in paragraph D.4.4.6.1, there shall be no degradation, damage, corrosion or delamination identifiable by visual inspection.

D.3.8.2 Humidity Resistance

When FPCs are tested as specified in paragraph D.4.4.6.2, conductors and insulators shall exhibit no degradation such as corrosion or delamination, as identified by visual inspection. The insulation resistance after the test shall be not less than 50MΩ.

D.3.8.3 Radiation Hardness

When FPCs are tested as specified in paragraph D.4.4.6.3, the base material shall not exhibit any degradation specified in d), e) or f) of paragraph D.3.4.2. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph D.3.6.1 shall be satisfied.

D.4. Quality Assurance Provisions

D.4.1 In-Process Inspection

The in-process inspection shall be as specified in Table D-7.

Table D-7. In-Process Inspection

No.	Inspection item	Requirement paragraph	Test method paragraph	Quantity of samples	
				Production FPC	Test coupon
1	Externals and dimensions (before cover lay registration)	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	100%	100%

D.4.2 Qualification Test

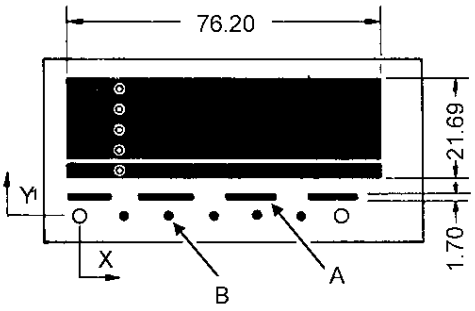
D.4.2.1 Sample

FPC with the minimum conductor width and conductor spacing, at the time the qualification test plan is developed, shall be selected and manufactured as the test specimens together with test coupons specified in Figures D-6 and D-7. If no production plan is available at the time the qualification test plan is developed, the manufacturer can use any pattern sufficient to verify compliance with the requirements of this appendix. Any test coupon may be subject to the approval of JAXA.

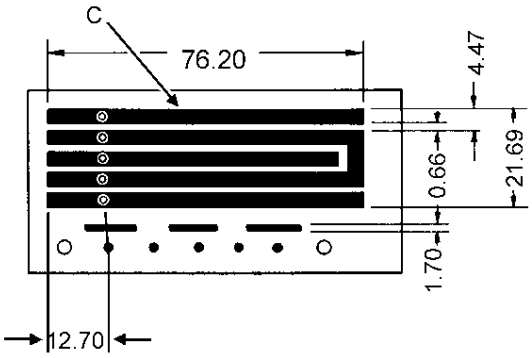
D.4.2.2 Test Items and Number of Samples

The tests within each group shall be performed in the order listed in Table D-8. Upon completion of Group I and II tests, Group III through VII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VII tests may be performed in any order regardless of group number. However, the tests in each group of III through VII shall be performed in the order listed. Six production FPCs and six each of test coupons I and II shall be submitted.

Unit: mm

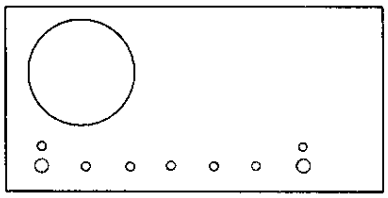


Top surface pattern of double-sided FPC

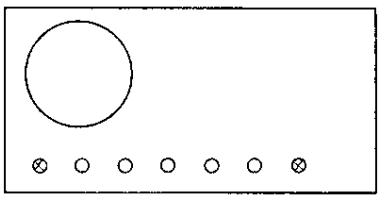


Bottom surface pattern of double-sided FPC
Top surface pattern of single-sided FPC

Figure D-6a. Pattern

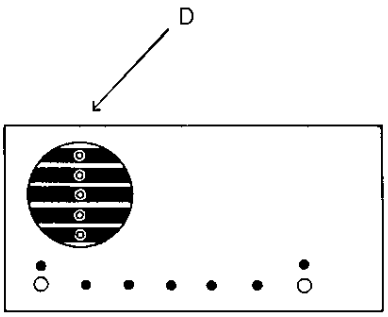


Top cover lay of double-sided FPC



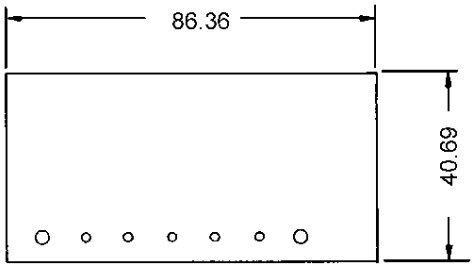
Bottom cover lay of double-sided FPC
Top cover lay of single-sided FPC

Figure D-6b. Cover Lay

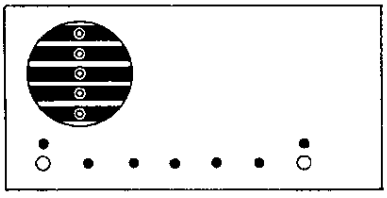


Top appearance of double-sided FPC

Unit: mm



Back side appearance
(Back side of stiffener)



Top appearance of single-sided FPC

Figure D-6c. Appearances and Dimensions

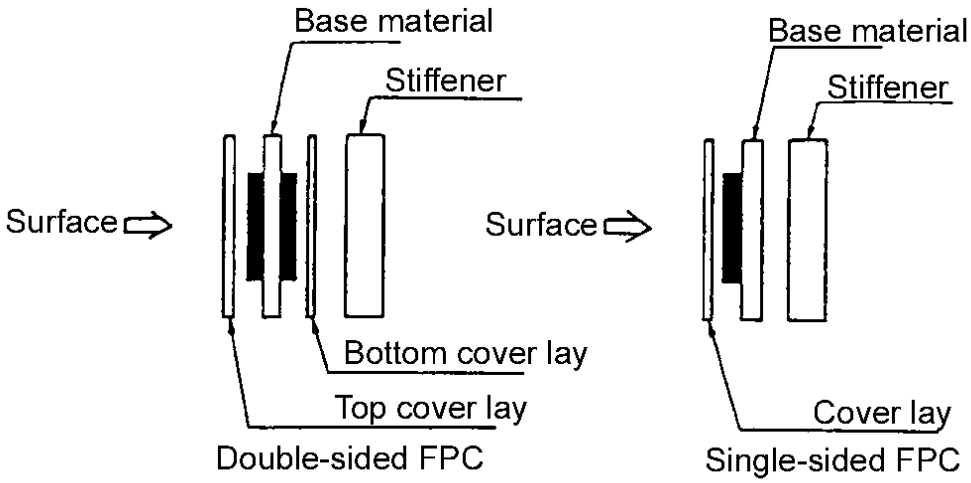


Figure D-6d. Configuration of FPC with Stiffener

Unit: mm

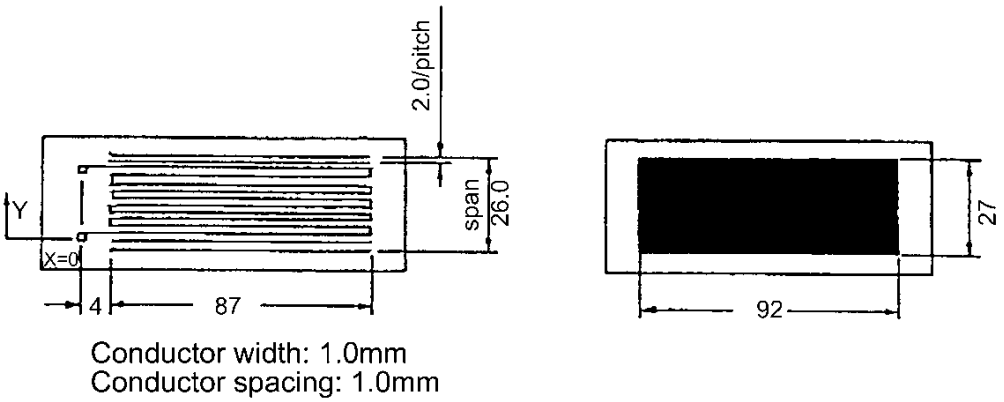
Hole location		Hole diameter			
Φ	0.254	Cover lay(1)		Base material(2)	Stiffener(3)
X	Y	Top	Bottom		
0.00	0.00	3.26	3.26	3.26	3.26
10.16	0.00	2.21	1.60	1.09	1.30
20.32	0.00	2.21	1.60	1.09	1.30
30.48	0.00	2.21	1.60	1.09	1.30
40.64	0.00	2.21	1.60	1.09	1.30
50.80	0.00	2.21	1.60	1.09	1.30
60.96	0.00	3.26	3.26	3.26	3.26
0.00	5.08	2.21	-	-	-
5.08	5.08	-	-	1.09	-
15.24	5.08	-	-	1.09	-
25.40	5.08	-	-	1.09	-
35.56	5.08	-	-	1.09	-
45.72	5.08	-	-	1.09	-
55.85	5.08	-	-	1.09	-
60.96	5.08	2.21	-	-	-
10.16	10.87	-	-	1.09	-
10.16	15.37	-	-	1.09	1.30
10.16	19.81	22.10	22.10	1.09	1.30
10.16	24.28	-	-	1.09	1.30
10.16	28.75	-	-	1.09	-

Notes: (1) (2) and (3) Tolerance of hole diameter

(1) Cover lay	(2) Base material	(3) Stiffener
22.10 ± 0.5	$3.26^{+0.1}_{-0.15}$	$3.26^{+0.1}_{-0.15}$
$3.26^{+0.1}_{-0.15}$	$1.09^{+0.1}_{-0.15}$	$1.30^{+0.30}_{-0.10}$
2.21 ± 0.3		

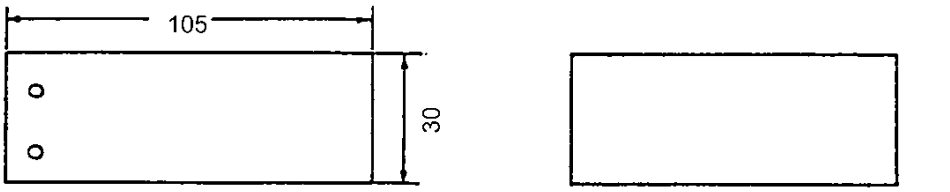
Figure D-6e. Hole Location and Hole Diameter

Figure D-6. Test Coupon I (Figures D-6a to D-6e)



Conductor width: 1.0mm
Conductor spacing: 1.0mm

Figure D-7a. Pattern



Top cover lay

Bottom cover lay of double-sided FPC

Figure D-7b. Appearance and Dimensions of Cover Lay

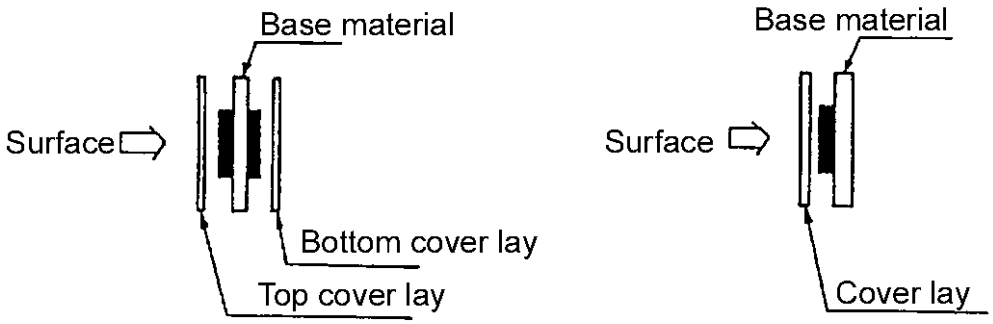


Figure D-7c. Configuration of FPC

Unit: mm

Hole location 0.254		Hole diameter		
		Cover lay		Base material
X	Y	Top	Bottom	
0.00	18.00	1.6	-	-
0.00	18:00	1.6	-	-

Note: Tolerance of hole diameter is 1.6±0.3.

Figure D-7d. Hole Location and Hole Diameter

Figure D-7. Test Coupon II (Figure D-7a to D-7d)

Table D-8. Qualification Test

Test			Requirement paragraph	Test method paragraph	Samples and sample number			Remarks
					Production FPC	Test coupon I	Test coupon II	
Group	Order	Test item			1 2 3 4 5 6	1 2 3 4 5 6	1 2 3 4 5 6	
I	1	Externals and dimensions	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	○ ○ ○ ○ ○ ○	All	○ ○ ○ ○ ○ ○	
	2	Workmanship	D.3.5	D.4.4.3				
II	1	Circuitry	D.3.6.4	D.4.4.4.4	○ ○ ○ ○ ○ ○	A A A A A A	-	
III	1	Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1	-	C C	-	
	2	Solderability	D.3.7.3	D.4.4.5.3	-	D D	-	
	3	Thickness of copper plating	D.3.4.1.2 a)	D.4.4.2.2	○ ○ ○ ○ or	B B B B	-	
	4	Thickness of electrolytic solder plating	D.3.4.1.2 b)	D.4.4.2.2	○ ○ ○ ○ or	B B B B	-	
IV	1	Conductor resistance	D.3.6.2.1	D4.4.4.2 a)	-	A A	-	
	2	Thermal shock (I)	D.3.8.1	D.4.4.6.1 a)	-	A A	-	
	3	Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)	-	A A	-	
V	1	Humidity resistance	D.3.8.2	D.4.4.6.2	○ ○ or	C C	-	Test coupon I shall be used when the production FPC does not have conductor spacing of 0.4 to 0.9mm.
VI	1	Terminal pull strength	D.3.7.2	D.4.4.5.2	○ ○ or	B B	-	Test coupon II shall be used when tests on the production FPC are difficult.
	2	Radiation hardness	D.3.8.3	D.4.4.6.3	○ ○	-	-	
VII	1	Folding flexibility	D.3.7.1.1	D.4.4.5.1 a)	○ ○	-	○ ○ ○	
	2	Flexibility endurance	D.3.7.1.2	D.4.4.5.1 b)	○ ○	-	○ ○ ○	The production FPC shall be used, if possible.

D.4.2.3 Criteria for Pass/Fail

If the number of the samples which fail to meet the requirements of this appendix exceeds the quantity of allowable defects specified in Table D-9, it shall constitute failure of the qualification tests.

Table D-9. Pass/Fail Criteria for Qualification Test and Quality Conformance Inspection (Group B)

Test and inspection item	Requirement paragraph	Test method paragraph	Quantity of allowable defects	
			Qualification test	Quality conformance inspection (Group B)
Externals and dimensions	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	0	-
Workmanship	D.3.5	D.4.4.3		
Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1		0
Conductor resistance	D.3.6.2.1	D.4.4.4.2 a)		
Thermal shock	D.3.8.1	D.4.4.6.1 a) D.4.4.6.1 b)		
Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)		
Insulation resistance	D.3.6.3	D.4.4.4.3		
Humidity resistance	D.3.8.2	D.4.4.6.2		
Circuitry	D.3.6.4	D.4.4.4.4		-
Terminal pull strength	D.3.7.2	D.4.4.5.2		0
Solderability	D.3.7.3	D.4.4.5.3		-
Plating thickness	D.3.4.1.2	D.4.4.2.2		-
Flexibility	D.3.7.1	D.4.4.5.1		0
Radiation hardness	D.3.8.3	D.4.4.6.3		-

D.4.3 Quality Conformance Inspection

D.4.3.1 Quality Conformance Inspection (Group A)

D.4.3.1.1 Sample

The quality conformance inspection shall be performed on all products. Group III tests may be performed using test coupon I manufactured at the same time as the production FPCs. If Group III tests are performed on the production FPCs in lieu of the test coupon I, the coupon I may not be manufactured. However, the production FPCs shall be treated as test coupons I and shall not be shipped as products.

D.4.3.1.2 Inspection Items and Sample Size

The items and test order of Group A inspection shall be as specified in Table D-10. The inspections within each group shall be performed in the order listed.
When Group III tests are performed with production FPCs, the sampling test shall be performed. When multiple coupon types are submitted for inspection at one time, the randomly selected samples shall include at least one test coupon for each type, and the quantity of coupons of each type shall be as equal as possible.
Criteria for pass/fail shall be specified in Table D-10.

Table D-10. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Samples		Quantity of allowable defects	Pass/fail
Group	Order	Inspection item			Production FPC	Test coupon I		
I	1	Externals and dimensions	D.3.3.13 D.3.4.1.1 D.3.4.2	D.4.4.2.1	All	-	0	-
	2	Workmanship	D.3.5	D.4.4.3				
II	1	Circuitry	D.3.6.4	D.4.4.4.4	All	-	0	-
III	1	Solderability	D.3.7.3	D.4.4.5.3	Production FPC or test coupon I(1)		-	AQL 1.0%
	2	Plating thickness	D.3.4.1.2	D.4.4.2.2	Production FPC or test coupon I(1)		-	AQL 1.0%

Note: (1) If the tests for solderability and plating thickness are performed on the production FPC in lieu of the test coupon I, the production FPC shall be regarded as test coupon I.

D.4.3.2 Quality Conformance Inspection (Group B)

D.4.3.2.1 Sample

The production FPCs and test coupons for Group B inspection shall be manufactured with the same materials and processes and basically in the same manufacturing conditions.

D.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table D-11. The inspections within each group shall be performed in the order listed.

Table D-11. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Samples and sample number			Remarks
					Production FPC	Test coupon I	Test coupon II	
Group	Order	Inspection item			1 2 3 4 5 6	1 2 3 4 5 6	1 2 3 4 5 6	
I	1	Dielectric withstanding voltage	D.3.6.1	D.4.4.4.1	-	C C	-	-
	2	Solderability	D.3.7.3	D.4.4.5.3	-	D D	-	-
II	1	Conductor resistance	D.3.6.2.1	D.4.4.4.2 a)	-	A A	-	-
	2	Thermal shock (II)	D.3.8.1	D.4.4.6.1 b)	-	A A	-	-
	3	Change of conductor resistance	D.3.6.2.2	D.4.4.4.2 b)	-	A A	-	-
III	1	Insulation resistance	D.3.6.3	D.4.4.4.3	○ ○ or C C		-	Test coupon I shall be used when the production FPC does not have conductor spacing of 0.4 to 0.9mm.
	2	Humidity resistance	D.3.8.2	D.4.4.6.2	○ ○ or C C		-	-
IV	1	Terminal pull strength	D.3.7.2	D.4.4.5.2	○ ○ or B B		-	Test coupon II shall be used when tests on the production FPC are difficult.
V	1	Folding flexibility	D.3.7.1.1	D.4.4.5.1 a)	○ ○	-	○ ○ ○	-
	2	Flexibility endurance	D.3.7.1.2	D.4.4.5.1 b)	○ ○	-	○ ○ ○	The production FPC shall be used, if possible.

D.4.4 Methods for Test and Inspection

D.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperatures of 15°C to 35°C, a relative humidity of 20% to 80%, and a luminance of minimum 750 lx.

D.4.4.2 Externals, Dimensions, Marking and Others

D.4.4.2.1 Externals and Construction

Materials, design, construction, dimensions and marking of FPCs shall be tested. Dimensions of rated values shall be measured using an optical measuring instrument which has sufficient accuracy. Externals shall be inspected visually.

D.4.4.2.2 Plating Thickness (Copper Plating and Electrolytic Solder Plating)

FPCs having a minimum of three through holes shall be encapsulated in a plastic mold which can be cured without heating or pressurization. Then, the mold shall be polished to create a microsection. The minimum plating thickness shall be measured at a magnification of 50X as a minimum.

D.4.4.3 Workmanship

The workmanship shall be inspected visually.

D.4.4.4 Electrical Performance

The electrical performance tests shall be performed as follows.

D.4.4.4.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $500V_{DC}$
b) Duration: 30 seconds
c) Conductor spacing: 0.4mm to 0.9mm

D.4.4.4.2 Electrical Conductivity

a) Conductor resistance
A test current shall be flown through conductive patterns which are specified on drawings. The conductor resistance shall be measured and recorded, as well as the room temperature.
The conductor resistance measured before and after the test specified in paragraph D.4.4.6.1 shall be defined as R_O and R_X, respectively.

b) Change of conductor resistance
After the test specified in paragraph D.4.4.6.1, the conductor resistance (Rx) shall be measured at the temperature (Tx) shown in Table D-12 in accordance with paragraph D.4.4.4.2 a).

Table D-12. Temperature (Tx)

Unit: °C

Temperature test	Temperature	
	Thermal shock [I]	Thermal shock [II]
Low temperature	-65^{0}_{-5}	-30^{0}_{-5}
Room temperature	15 to 35	15 to 35
High temperature	125^{+5}_{0}	125^{+5}_{0}

The conductor resistance measured at each temperature (Rx) shall be converted to the resistance at 20°C. The converted conductor resistance at 20°C after the test shall be defined as Rx^{20}.

$$Rx^{20} = \frac{Rx}{1 + 0.004(20 - Tx)}$$

The conductor resistance measured in accordance with paragraph D.4.4.4.2 a) (Ro) shall be converted to the resistance at 20°C. The converted conductor resistance at 20°C before the test shall be defined as Ro^{20}. The change rate from Ro to Rx converted to the resistance at 20°C shall be calculated by the following formula.

Conductor resistance change converted to the resistance at 20°C =

$$\frac{Rx^{20} - Ro^{20}}{Ro^{20}} \times 100 \text{ (percent)}$$

D.4.4.4.3 Insulation Resistance

The insulation resistance test shall be performed in accordance with Test Method 302 of MIL-STD-202. The following conditions shall apply.

a) Test condition: B
b) Duration: 60 seconds
c) Points of application: Where the conductor spacing is between 0.4mm to 0.9mm.

D.4.4.4.4 Circuitry

A test current shall be applied to each conductive pattern to verify that there is no open circuit in the pattern or short circuit between patterns.

D.4.4.5 Mechanical Performance

The mechanical performance tests of the FPC shall be performed as follows.

D.4.4.5.1 Flexibility

a) Folding flexibility

A fold cycle shall be defined as taking one end of the sample, folding it around

a mandrel and then unfolding it to the original starting position, traveling 180 degrees in one direction and 180 degrees in the opposite direction. The mandrel radius shall be ten to twelve times as large as the overall material thickness of the FPC. The test shall be performed for five cycles.

b) Flexibility endurance

Insulated lead wires shall be attached to the extreme ends of a conductive pattern of the sample. Using the flexibility endurance fixture shown in Figure D-8, the sample shall be mounted so that the inside diameter of the loop is 9.6mm±0.4mm. The two wires shall then be connected to the relay and the voltage applied to it. The reciprocating travel shall not exceed 10 cycles per minute, and the loop shall travel at least 25.4mm. The test shall be performed for the number of cycles specified on drawings and continued until the conductor is fractured. The number of cycles shall be checked by the associated counter. A failure shall occur when the conductor is fractured within the specified number of cycles, and the fixture does not work.

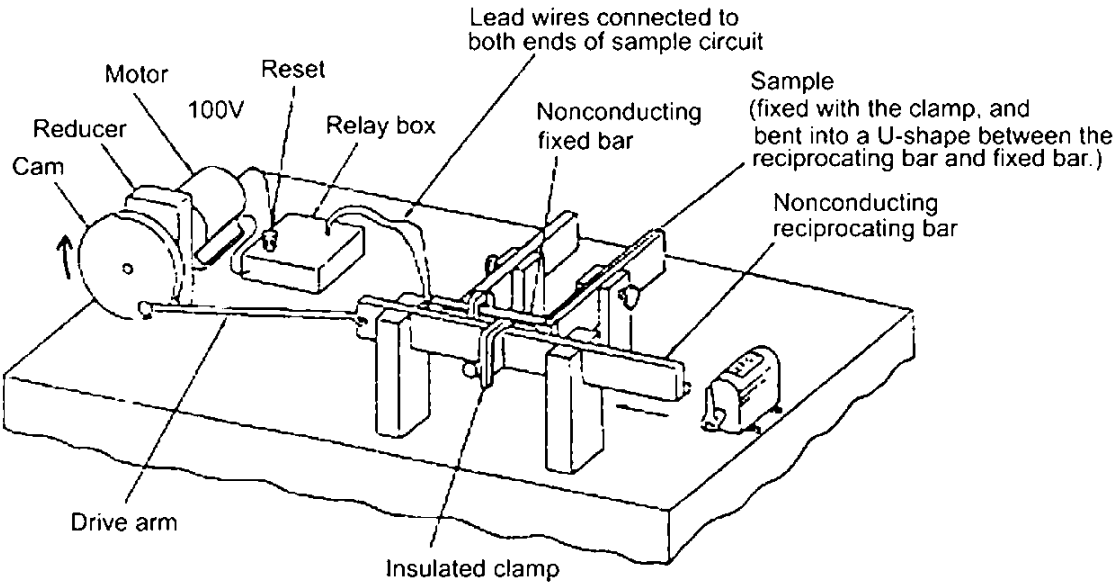


Figure D-8. Flexible Endurance Fixture

D.4.4.5.2 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.

Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the FPC sample shall have been baked for one hour at 90°C. The following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm) -
d_2 = Land diameter (cm)

The condition shall be considered as a failure, when either of the followings occur.

a) When the land around the through hole is loosened.
b) When the through hole is loosened due to soldering a lead wire. In this case, the land condition does not matter.

D.4.4.5.3 Solderability

Solderability shall be tested as follows.

a) The sample shall be baked at 90°C for one hour.
b) Dip the specimen into the flux, composed of 20 percent by gravity of rosin and 80 percent of isopropyl alcohol.
c) Samples shall be taken out from the flux and the flux shall be drained for 60 seconds. (The flux may flow along an edge of the sample until the alcohol evaporates.)
d) Solder shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is 232±5°C. The sample, with the conductor surface remaining downward, shall be floated in a solder bath for 5 seconds.
e) The specimen shall be taken out of the bath. The specimen may be dabbed to remove flux residues, and cooled until the solder is solidified. Fast cooling is not permitted.
f) The condition of solder on the through hole and conductive surface shall be inspected.

D.4.4.6 Environmental Performance

The environmental performance tests of FPCs shall be performed as follows.

D.4.4.6.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
   Test condition B shall be applied. The low temperature shall be changed to -30°C. The number of cycles shall be 1000.
b) Thermal shock (II) (applicable to quality conformance inspection)
   Test condition B-3 shall apply.

D.4.4.6.2 Humidity Resistance

The humidity resistance test shall be performed in accordance with Test Method 106 of MIL-STD-202. The following conditions shall apply.

a) The initial resistance measurement is not necessary.
b) Steps 7A and 7B shall be omitted.
c) Upon completion of step 6 of the final cycle, the sample shall be taken out of the bath and water droplets on the surface shall be removed. The final resistance measurement shall then be taken within one minute.

D.4.4.6.3 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests for dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraphs D.4.4.4.1 and D.4.4.4.3, respectively. The insulation resistance shall be measured in the same circuit as the one used for the dielectric withstanding voltage test.

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RIGID-FLEX PRINTED WIRING BOARDS

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX E

RIGID-FLEX PRINTED WIRING BOARDS

E.1. General

E.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the rigid-flex printed wiring boards (hereinafter referred to as “F/R-PWB”).

E.1.2 Classification

Products covered by this specification shall be classified as specified in Table E-1.

Table E-1. Classification

	Construction of F/R-PWB
Classification	Outer type
	Inner type

E.1.3 Part Number

The part number of the F/R-PWB is in the following form.

Example: JAXA(1) 2140/E 101 GI I 4(2)

101	GI	I	4(2)
Individual identification	Base material code (see E.1.3.1)	Construction code (see E.1.3.2)	Number of layers (see E.1.3.3)

Notes:
(1) "JAXA" indicates the part is for space use and may be abbreviated “J”.
(2) Number of conductor layers

E.1.3.1 Base Material Code

The base material code of F/R-PWB is as specified in Table E-2.

Table E-2. Base Material Code

Base material code(1)	Base material
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

Note: (1) Applicable standards for GI type are as specified in each detail specification. Details of GI base material, including type and glass transition temperature (Tg), shall be as specified in the Application Data Sheet (ADS).

E.1.3.2 Construction Code

The construction code of F/R-PWB is as specified in Table E-3. Each construction shall be as shown in Figures E-1 and E-2.

Table E-3. Construction Code

Construction code	Construction of R/F-PWB
I	Outer type
II	Inner type

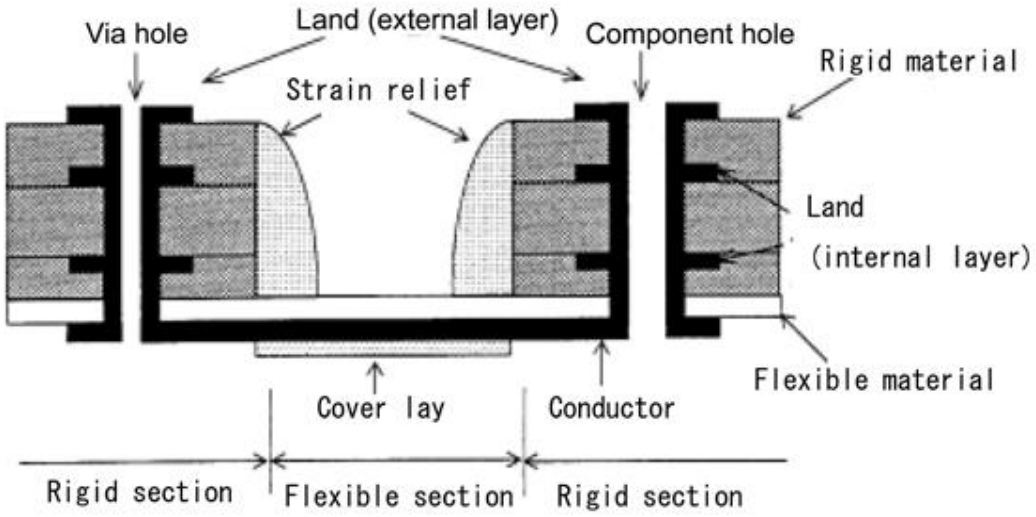


Figure E-1. Cross-Section of Outer Type (Four-Layer Construction)

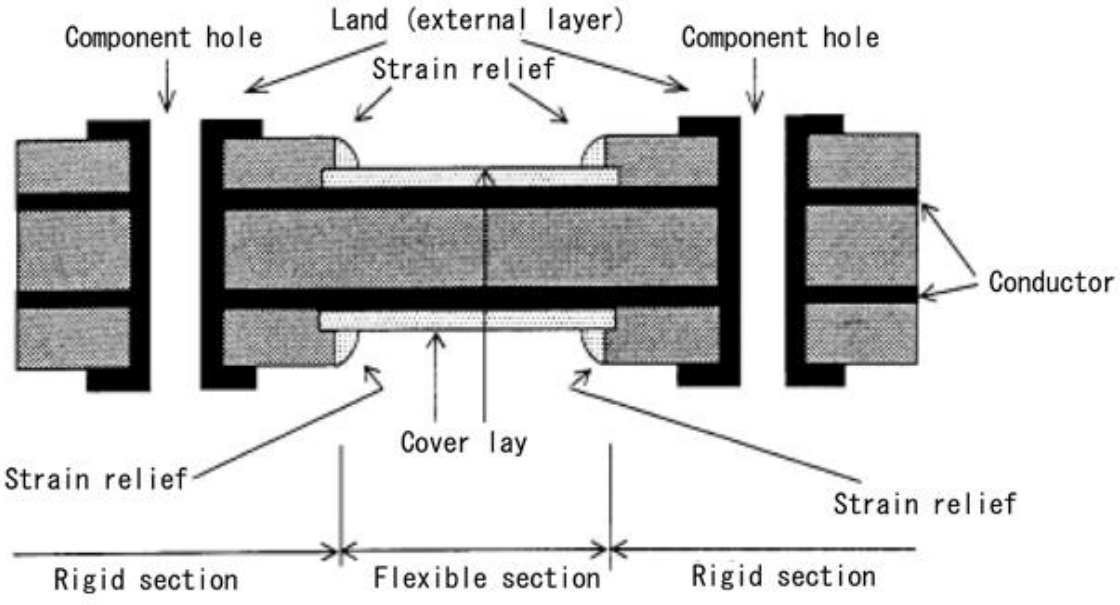


Figure E-2. Cross-Section of Inner Type (Four-Layer Construction)

E.1.3.3 Number of Layers

The number of layers of F/R-PWB is as specified in Table E-4, based on the construction type.

Table E-4. Number of Layers

Construction	Number of layers at rigid section (Number of layers at flexible section)	Maximum number of layers
I	2 to 10 layers (1 layer)	10
II	3 to 8 layers (1 to 4 layers)	8

E.2. Applicable Documents

E.2.1 Reference Documents

The reference documents shall be as specified in paragraph 2.2.

E.3. Requirements

E.3.1 Qualification Coverage

Qualification shall be valid for F/R-PWB that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs E.3.2 to E.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. The maximum thickness and surface plating type shall be specified in the detail specification. All surface plating types specified in this specification are considered qualified if any one of those plating types is qualified. Only solder resist inks used for qualification tests are considered qualified. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

E.3.2 Materials

The materials of F/R-PWB shall be as follows and as specified in paragraph 3.3

E.3.2.1 Rigid Copper-Clad Laminate and Prepreg

The rigid copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The nominal thickness of the base material shall be not less than 0.05mm. The metal foil shall be copper regardless of base material type. The metal foil for the outermost layer shall have a nominal thickness of 18μm as a minimum, and the metal foil for an internal layer shall have a minimum of 35μm. The applicable standards for the material used in the R/F PWB shall be specified in each detail specification. Details of the GI base material, including type and the glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

E.3.2.2 Flexible Copper-Clad Laminate

The flexible copper-clad laminate shall be comprised of polyimide film substrate compliant with IPC-4204 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The nominal thickness of the base material shall be not less than 0.05mm. The copper foil for the outermost layer shall have a nominal thickness of 18μm as a minimum in consideration of additional conductor thickness for plating. The copper foil for an internal layer shall have a nominal thickness of minimum 35μm. The applicable standards for the material used in the printed wiring boards shall be specified in the detail specification. Details of the GI base material, including type and the glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

E.3.2.3 Cover Lay

The cover lay specified in IPC-4203 shall be used. The nominal thickness shall be not less than 12.7μm.

E.3.2.4 Strain Relief

The strain relief shall be comprised of flexible epoxy resin, and be added at the rigid-flex interface. This will serve as strain relief during bending, and will prevent the flex from being damaged against the rigid corner.

E.3.2.5 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

E.3.2.6 Solder Resist

The solder resist of F/R-PWB shall conform to IPC-SM-840 Class H or the equivalent, and be applied exclusively to the rigid section. The application shall be in accordance with manufacturing drawings.

E.3.2.7 Marking Ink

The marking shall be produced using epoxy resin base inks that do not easily vanish by any solvent. The marking shall not affect any function, performance or reliability of the F/R-PWB.

E.3.2.8 Plating

Unless otherwise specified, the solder coating specified in paragraph E.3.2.5 shall be applied to all through holes, lands, and surface conductive patterns, except for where solder resist is applied. All through holes shall be coated with copper plating and subsequently with the same type surface plating as the plating applied on lands. When plating other than the plating applied on lands is partially required except for the fine pitch patterns, electrolytic gold plating may be applied.

E.3.2.8.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

E.3.2.8.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

E.3.2.8.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table E-5. The electrolytic nickel plating specified in paragraph E.3.2.8.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.

Table E-5. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 percent
KNOOP hardness	91 to 129 (inclusive)

E.3.2.8.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and be low stress type.

E.3.3 Design and Construction

E.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

The F/R-PWBs shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

E.3.3.2 Interlayer Connection

Connection between conductive patterns in different layers of F/R-PWBs shall be provided by through holes including small via hole (drill diameter of minimum 0.35).

E.3.3.3 Conductor Width

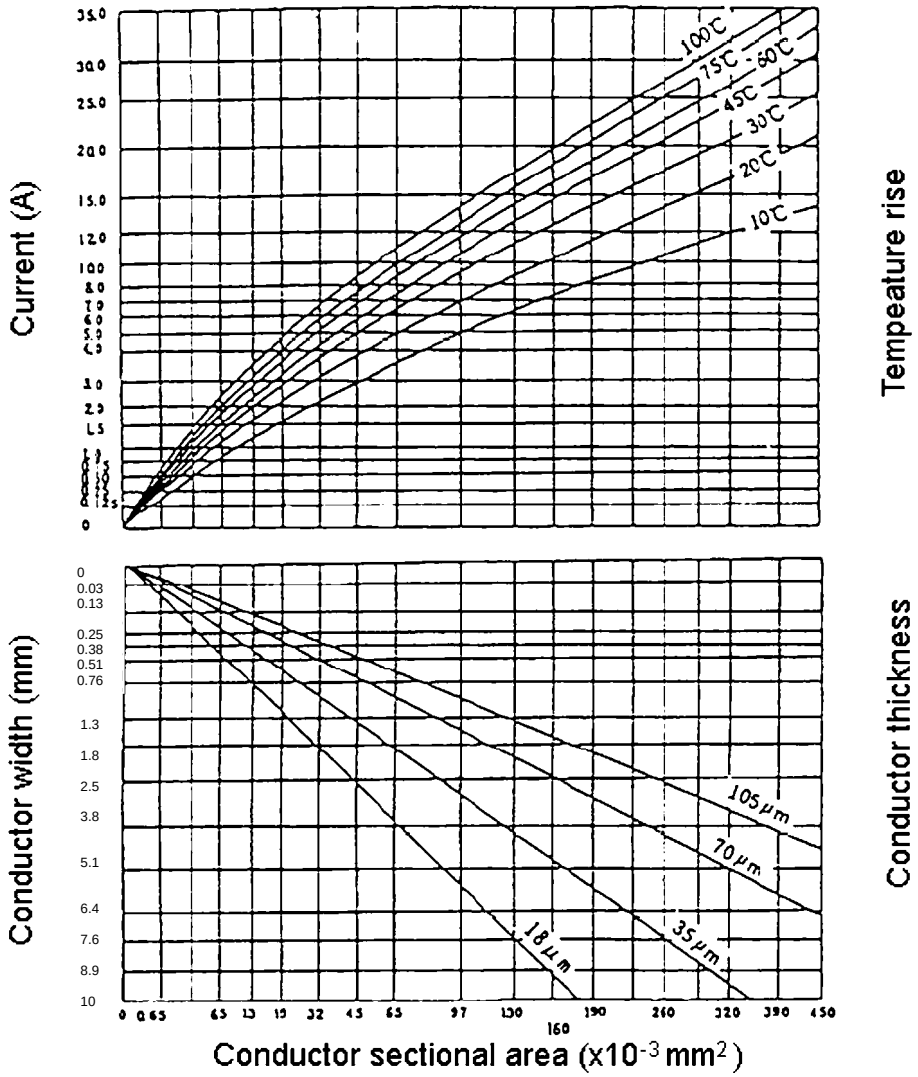
The minimum conductor width at the design value of F/R-PWB shall be as specified in Table E-6 on the basis of the construction type. The actual conductor width of

external and internal layers shall be determined in accordance with Figures E-3 and E-4.

Table E-6. Minimum Design Width of Conductor

Unit: mm

Construction	Rigid section	Flexible section
I	0.13	0.30
II	0.25	0.30



Remarks:

(1) This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from the ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations in etching techniques, conductor thickness and width and cross-sectional area.

(2) Additional derating of 15 percent for the allowable current is suggested under the following conditions:
   a) Where dielectric layer thickness is less than 0.8mm.
   b) Where conductor thickness is greater than 105μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the R/F-PWB and the maximum ambient temperature in the location where the R/F-PWB will be used.

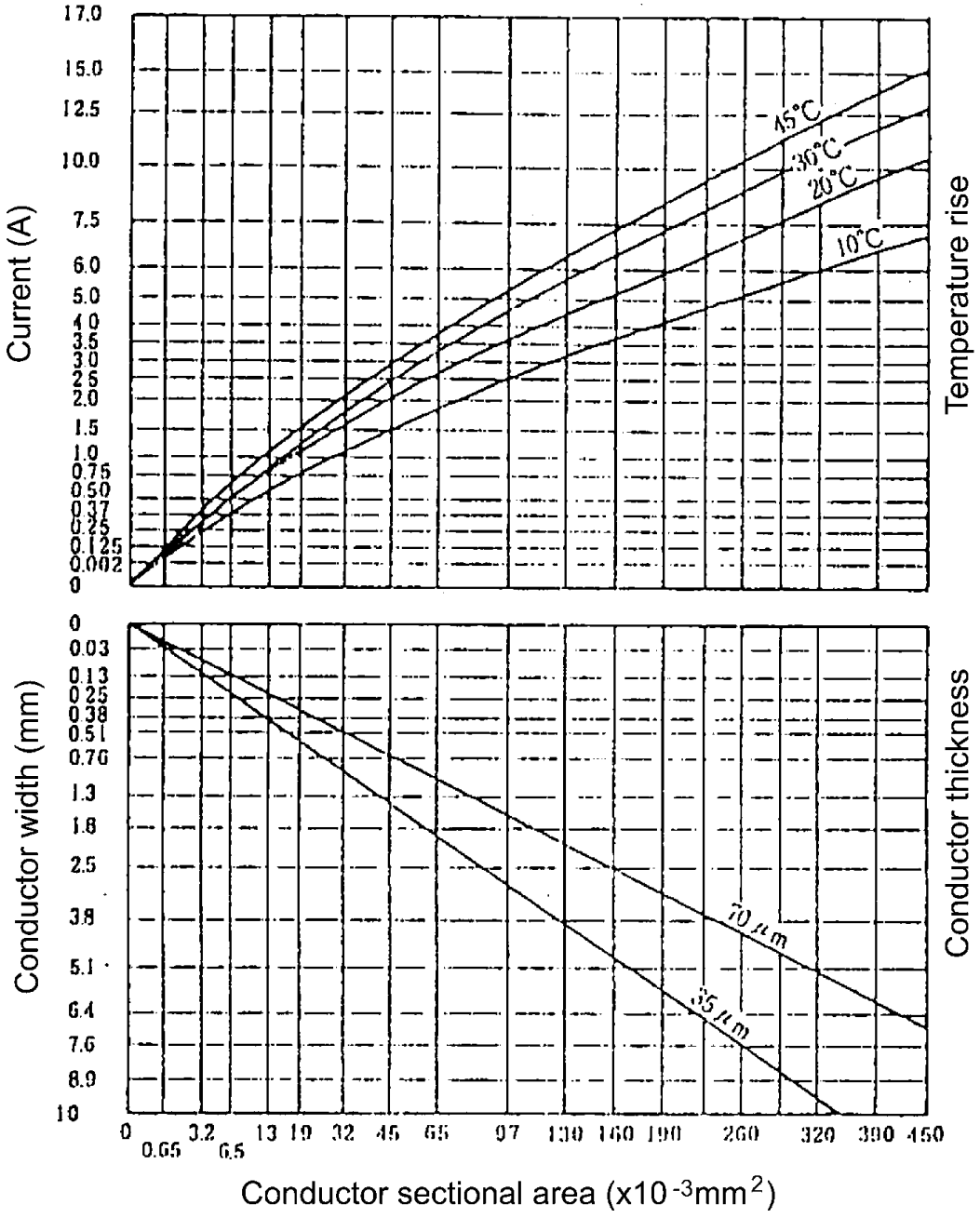
(4) For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperature rises.

(5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.

(6) The effect of heating due to heat generating parts is not considered.

(7) The final conductor thickness in the chart does not include plating thickness of metals other than copper.

Figure E-3. Conductor Width (External Layer)



Remark: (1) Remarks (1) through (7) of Figure E-3 shall apply to this figure.

Figure E-4. Conductor Width (Internal Layer)

E.3.3.4 Conductor Spacing

The minimum design value of conductor spacing shall be as specified in Table E-7 based on the construction type. The actual conductor spacing shall be as specified in Table E-8, which varies on voltage applied between conductors.

Table E-7. Conductor Spacing

Unit: mm

Construction	Rigid section	Flexible section
I	0.18	0.20
II	0.25	0.25

Table E-8. Conductor Spacing of R/F-PWB Covered with Conformal Coating, Solder Resist, Cover Lay or Prepreg

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing (mm)	
	External layer	Internal layer
0 - 100	0.18	0.18
101 - 300	0.48	0.30
301 - 500	0.86	0.35
501 or higher	(0.003×V)+0.1	(0.003×V)+0.1

E.3.3.5 Land Diameter

The design value of the minimum land diameter shall be as specified in Table E-9.

Table E-9. Land Diameter

Unit: mm

Hole	Construction	
	I	II
Small via holes(1)	Drill diameter + 0.4	
Plated-through holes(2)	Finished hole diameter + 0.5	Finished hole diameter + 0.6
Non-plated-through holes	Dill diameter + 1.1	

Notes:

(1) The minimum diameter of the land provided with a small via hole shall be 0.76mm.

(2) The minimum diameter of lands other than round shaped lands shall be measured as the length “A”, as shown in Table E-5.

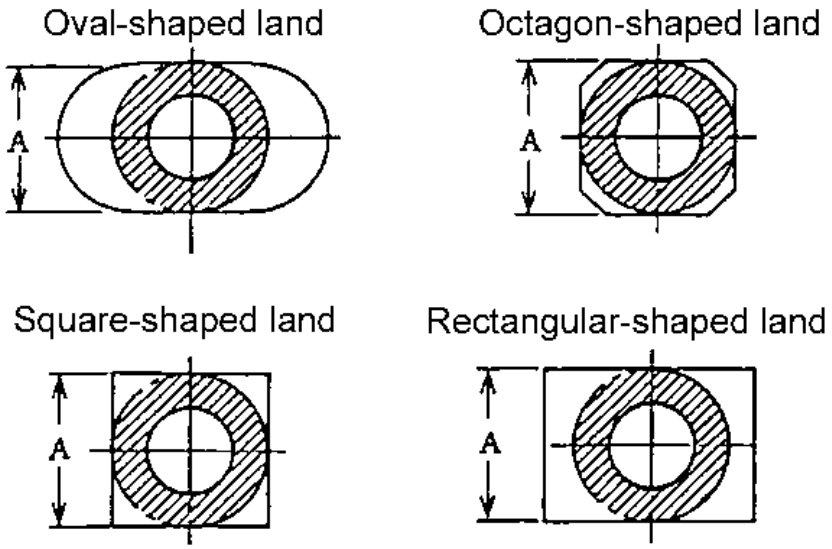


Figure E-5. Measurement of Minimum Diameter of Lands Other than Round Shaped Lands

E.3.3.6 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table E-10.

Table E-10. Plating or Coating Thickness

Unit: μm

Plating material	Surface and through hole plating thickness
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating
Electrolytic copper	Min. 30
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	Min. 5
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.

E.3.3.7 Operating Temperature Range

R/F-PWBs shall operate within the temperature range of the thermal shock (II) test, -65˚C to +125˚C (paragraph E.3.10.1.2).

E.3.4 Externals, Dimensions, Marking and Others

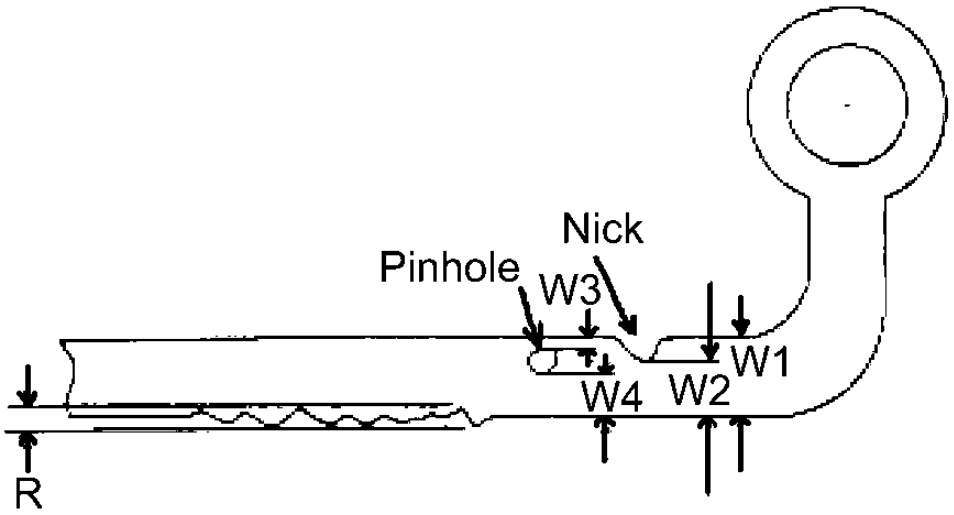
E.3.4.1 Externals and Construction

E.3.4.1.1 Conductive Pattern

The conductive patterns shall conform to the approved or provided artwork master (or original production master).

E.3.4.1.2 Conductor

At rigid sections, the conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100mm×100mm on F/R-PWBs. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is greater than 0.2mm, the roughness shall be not more than 0.13mm (see Figure E-6). Conductors at the rigid-flex interface, including supporting conductive patterns, shall contain no defects including tears, cracks, edge roughness, nicks, pinholes and scratches, exposing the base material. A cover lay coating over the conductors shall not exhibit any scratches.



Unit: mm

W1 ≥ (Minimum finished conductor width) ≥ 0.08
W2 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
W3+W4 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
R in any range of 13 in length
R ≤ 0.08, when the design width of the conductor is less than 0.2
R ≤ 0.13, when the design width of the conductor is 0.2 or more

Figure E-6. Conductor Defects

E.3.4.1.3 Minimum Annular Ring

When the annular rings on the internal and external layers are measured in accordance with paragraph E.4.4.2.3 f), the annular rings of a plated-through hole shall be not less than 0.05mm in diameter. The annular rings of a non-plated-through hole shall be not less than 0.3mm in diameter and shall not contain defects. When the annular ring for plated-through hole on an external layer shall be a minimum of 0.13mm in diameter, a sub-land or other equivalent disposition shall be provided.

E.3.4.1.4 Dielectric Layer Between Conductor Layers

The surface of the dielectric layer between conductor layers shall be free from any residual conductor or foreign material.

E.3.4.1.5 Through Holes

When R/F-PWBs are tested as specified in paragraph E.4.4.2.3, the plating inside through holes shall exhibit no cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall be acceptable, provided that the hole diameter is not reduced below its lower limit specified on drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 80μm and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated (see Figure E-7).

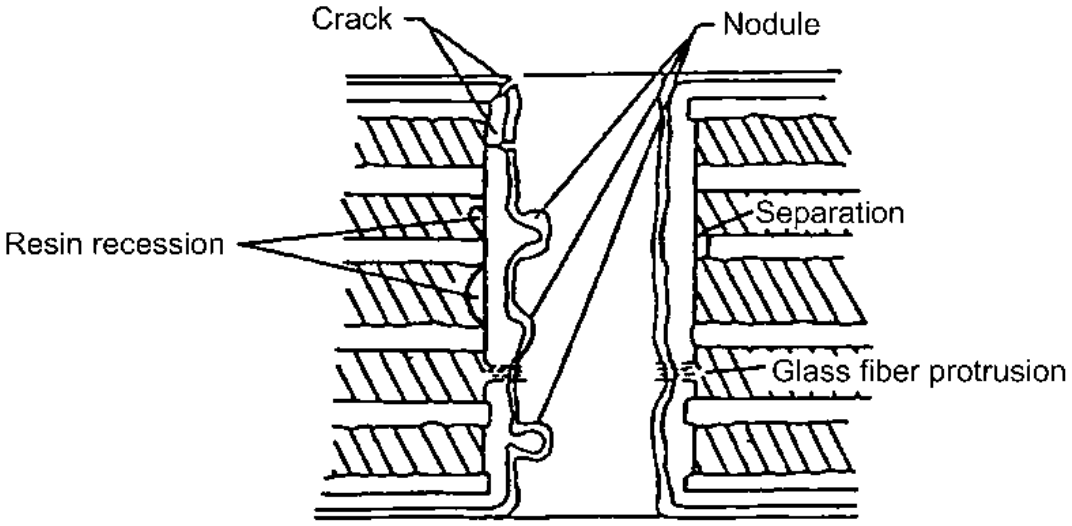


Figure E-7. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure E-8).

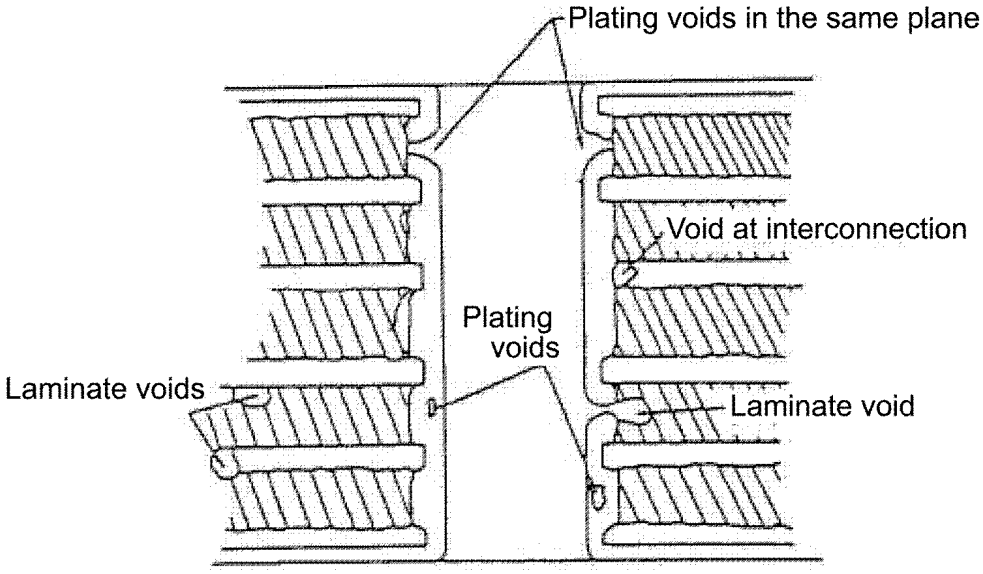


Figure E-8. Voids

b) Conductive interface
The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure E-9).

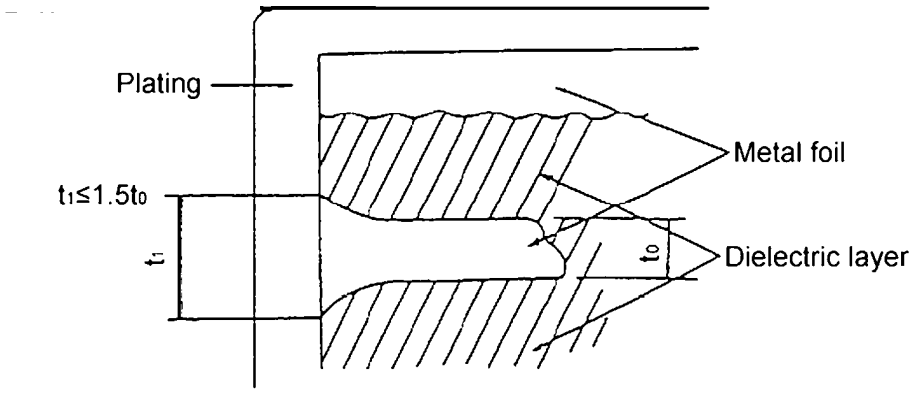


Figure E-9. Nail Heading

c) Layer-to-layer registration
The layer-to-layer registration error shall not exceed 0.20mm.

d) Dielectric layer thickness
The dielectric layer between conductor layers of a rigid dielectric material shall be not less than 0.08mm in thickness. The dielectric layer between conductor layers of a flexible dielectric material shall be greater than 0.038mm in thickness.

e) Plating thickness
The plating thickness shall meet the requirements specified in paragraph E.3.3.6.

f) Annular ring
The annular ring shall meet the requirements specified in paragraph E.3.4.1.3.

E.3.4.1.6 Solder Coating

The solder coating shall be free from pinholes and pits, and completely cover conductive patterns.

E.3.4.1.7 Edges of F/R-PWB

There shall be no nicks, cracks or separation at edges of F/R-PWBs. This provision shall not apply to separate parts of a split board.

E.3.4.1.8 Surface of F/R-PWB

Surface of F/R-PWBs shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the each area does not exceed 1 percent of the surface area of the F/R-PWB, and that the spacing between conductors is not reduced exceeding 25 percent. Crazing along edges of the F/R-PWB shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

E.3.4.1.9 Solder Resist

The cured solder resist shall be free from tackiness, blistering and delamination. Significant visual damage such as thin spots, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application area and registration onto conductive patterns shall meet the provisions of manufacturing drawings.

E.3.4.2 Dimensions

The dimensions of each part of the F/R-PWB shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table E-11.

Table E-11. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. The tolerance of through hole diameters is not specified, when the drill diameter is 0.5 or smaller.
Conductor width	0.13 or more and less than 0.20: ±0.05 0.20 or more and less than 0.50: ±0.10 0.50 or more: ±20 percent of circuit width
Conductor spacing	0.18 ≤ design conductor spacing < 0.2 The tolerance of finished conductor spacing shall be 0.1 or more with respect to the design value. Design conductor spacing ≥ 0.2 The tolerance of finished conductor spacing shall be -0.1 with respect to the design value. The positive side tolerance is not specified. The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

E.3.4.2.1 Solder Resist Thickness

When F/R-PWBs are tested as specified in paragraph E.4.4.2.4, the solder resist thickness shall be not less than 17.5μm, measured at the center of conductors.

E.3.4.3 Marking

The marking shall be produced with the marking ink specified in paragraph E.3.2.7 by the same process as producing conductive patterns, or by laser marking as specified in the drawings. The marking shall not adversely affect any function, performance or reliability of the F/R-PWB.

All marking shall remain legible and in no manner affect the performance of the F/R-PWB. Unless otherwise specified, the following shall be marked on each F/R-PWB. If marking on the F/R-PWB is not practical, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer’s name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

E.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single F/R-PWB) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

E.3.5 Workmanship

F/R-PWBs shall not exhibit defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent or flux residues, which could adversely affect the function, performance or reliability of the F/R-PWB. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

E.3.5.1 Bow and Twist

When R/F-PWBs are tested as specified in paragraph E.4.4.3.1, the maximum limit for bow and twist shall be 1.5 percent for rigid sections, unless otherwise specified on manufacturing drawings. For a split board, bow or twist shall not exceed the above value before separation.

E.3.5.2 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.

E.3.6 Plating Adhesion and Overhang

When F/R-PWBs are tested as specified in paragraph E.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

E.3.7 Cleanliness

F/R-PWBs shall exhibit no fouling including dirt, oil, corrosion, corrosion product, salt, soot, grease, finger print, mold release agent, foreign inclusion and flux residues, or ionic contamination. When F/R-PWBs are tested as specified in paragraph E.4.4.5, the resistivity of the solvent extract shall be not less than $2x10^6 \Omega \cdot cm$.

E.3.8 Electrical Performance

F/R-PWB shall meet the following electrical requirements.

E.3.8.1 Dielectric Withstanding Voltage

When F/R-PWBs are tested as specified in paragraph E.4.4.6.1, there shall be no insulation breakdown, flashover or sparkover.

E.3.8.2 Circuitry

When R/F-PWBs are tested as specified in paragraph E.4.4.6.2, there shall be no open circuits or circuit shorts between circuit patterns.

E.3.8.3 Connection Resistance

When F/R-PWBs are tested as specified in paragraph E.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \cdot t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)

l: Distance between lands (mm)

W: Conductor width (mm)

t: Conductor thickness (mm)

E.3.9 Mechanical Performance

F/R-PWB shall meet the following mechanical requirements.

E.3.9.1 Terminal Pull Strength

When tested as specified in paragraph E.4.4.7.3, F/R-PWBs shall meet the following requirements.

a) Bond strength
The land shall withstand a minimum of 1380N/cm^2.

b) Conductor and land
When F/R-PWBs are inspected visually as specified in paragraph E.4.4.2, there shall be no loosening around the through holes.

c) Microsection of through hole
When F/R-PWBs are microsectioned and inspected in accordance with paragraph E.4.4.2.3 a), there shall be no cracks, blistering, measling or delamination.

E.3.9.2 Folding Flexibility

When tested as specified in paragraph E.4.4.7.1, R/F-PWBs shall not exhibit degradation or rejectable delamination. After completion of the test, the requirements specified in paragraph E.3.8.2 shall be satisfied.

E.3.9.3 Flexibility Endurance

When subjected to the number of cycles specified in drawings as specified in paragraph E.4.4.7.2, F/R-PWBs shall not exhibit degradation or rejectable delamination. After completion of the test, the requirements specified in paragraph E.3.8.2 shall be satisfied. If the number of cycles is not specified in the drawings, it shall be 40 cycles.

E.3.9.4 Solderability

When tested as specified in paragraph E.4.4.7.4, F/R-PWBs shall meet the following requirements.

E.3.9.4.1 Hole Solderability

The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to small via holes.

E.3.9.4.2 Surface Solderability

A minimum of 95 percent of the surface conductor area shall be covered uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated at a point.

E.3.10 Environmental Performance

F/R-PWBs shall meet the following environmental requirements.

E.3.10.1 Thermal Shock

E.3.10.1.1 Thermal Shock (I) (applicable to qualification test)

When F/R-PWBs are tested as specified in E.4.4.8.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph E.4.4.6.2, and connection resistance shall be measured in accordance with paragraph E.4.4.6.3. The F/R-PWB shall meet the requirements specified in paragraph E.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

E.3.10.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When F/R-PWBs are tested as specified in paragraph E.4.4.8.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph E.4.4.6.2, and connection resistance shall be measured in accordance with paragraph E.4.4.6.3. The F/R-PWB shall meet the requirements specified in paragraph E.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

E.3.10.2 Humidity and Insulation Resistance

When R/F-PWBs are tested as specified in paragraph E.4.4.8.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be not less than 500MΩ.

E.3.10.3 Hot Oil Resistance

When F/R-PWBs are tested as specified in paragraph E.4.4.8.3, the change in connection resistance between circuits before and after the test shall be less than 10 percent.

E.3.10.4 Thermal Stress

When tested as specified in paragraph E.4.4.8.4, F/R-PWBs shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Copper foil
There shall be no cracks in internal copper foils in the vertical microsection of through holes.

c) Laminate voids
Laminate voids less than 76μm is permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings.

E.3.10.5 Radiation Hardness

When R/F-PWBs are tested as specified in paragraph E.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph E.3.8.1 shall be satisfied.

E.4. Quality Assurance Provisions

E.4.1 In-Process Inspection

The in-process inspection specified below shall be performed, and F/R-PWBs shall meet the requirements of paragraphs E.3.4.1 and E.3.7.

a) Visual inspection of internal layers, construction and dimensions (100 percent)
b) Cleanliness (sampling)

E.4.2 Qualification Test

E.4.2.1 Sample

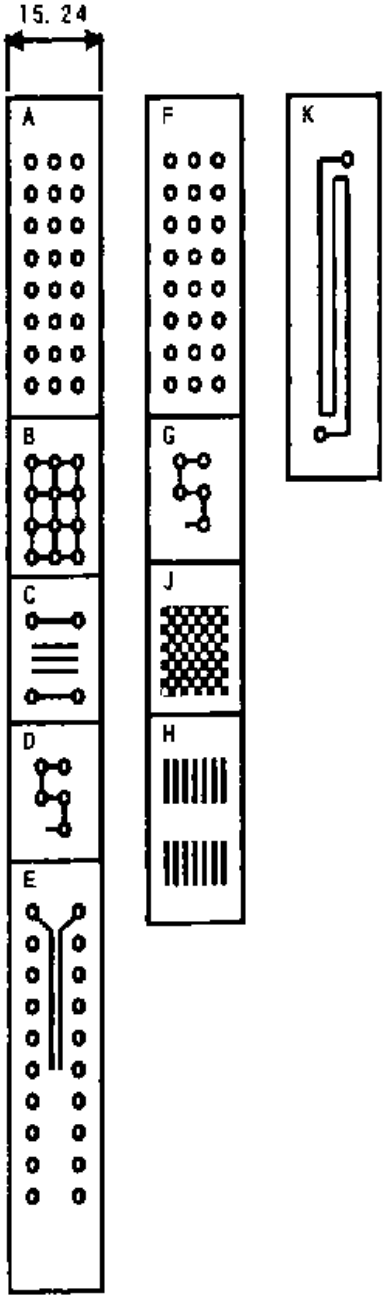
Samples shall be approved by JAXA, and have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure E-10. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation. Samples shall consist of the production F/R-PWB and test coupons fabricated on the same work board as the production F/R-PWB.

E.4.2.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table E-12. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each Group III through VIII shall be performed in the order listed. Six production R/F-

PWBs shall be prepared for each construction. The number of test coupons submitted for each test shall be as specified in Table E-12.

Arrangement of Test Coupons



Unit: mm

Notes:

(1) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(2) For test coupon A, the land diameter shall be the minimum land diameter applicable to the minimum drill diameter of the corresponding F/R-PWB. The hole diameter shall be the maximum hole diameter among the minimum lands. All holes shall be through holes. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E, F and K, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes. The hole diameter shall be 0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding F/R-PWB.

(4) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. Therefore, the conductors shall be formed on all layers in accordance with this figure. At both ends of the circuits of D and G, through holes shall be formed to measure the resistance. The land diameter shall be 1.8mm and hole diameter shall be 0.8mm.
All holes shall be through holes. The hole diameter tolerance is not specified.

(5) Solder resist shall apply to the test coupons E, H and J, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon E shall be the land diameter +0.2mm.

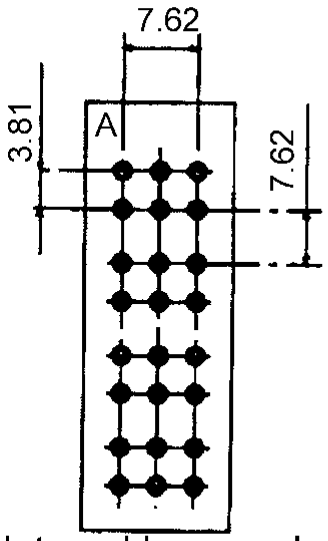
(6) The arrangement of test coupons shown in this appendix is an example; a different arrangement is also acceptable.

(7) The symbols of test coupons (A to H, J and K) shall be used for identification and not for the object of inspection. The marking method is not specified.

Figure E-10. Test Coupons (for Multilayer Printed Wiring Board) (1/4)

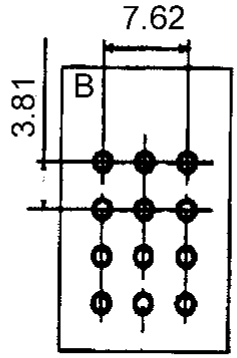
Unit: mm

Test Coupon A

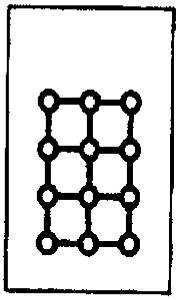


Internal layer and outermost layer

Test Coupon B

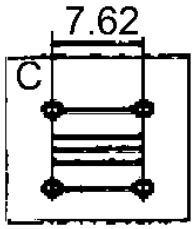


Outermost layer

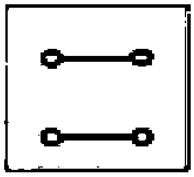


Internal layer

Test Coupon C



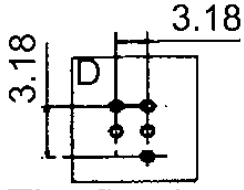
Outermost layer



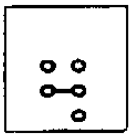
Internal layer

Construction	Conductor width	Conductor spacing
Outer type	0.13	0.18
Inner type	0.25	0.25

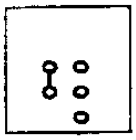
Test Coupon D and G



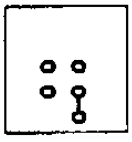
The first layer



The third layer



The second layer



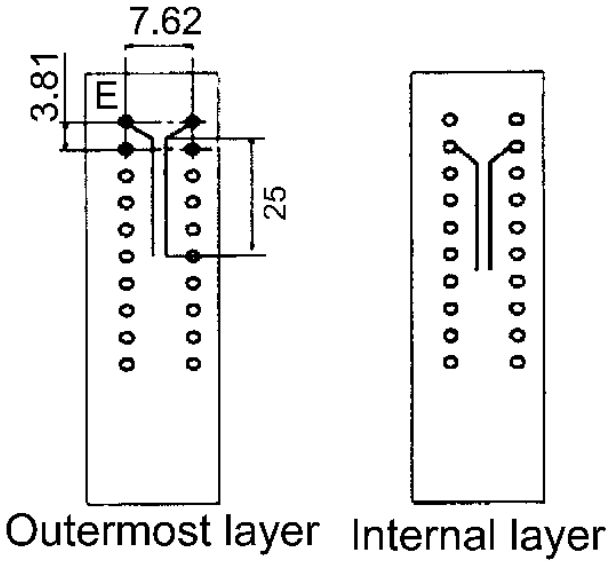
The fourth layer

Construction	Conductor width	Conductor spacing
Outer type	0.13	0.18
Inner type	0.25	0.25

Figure E-10. Test Coupons (for Multilayer Printed Wiring Board) (2/4)

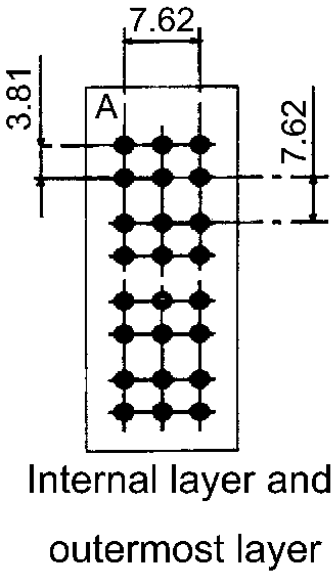
Unit: mm

Test Coupon E



Construction	Conductor width	Conductor spacing
Outer type	0.13	0.18
Inner type	0.25	0.25

Test Coupon F



Test Coupon H

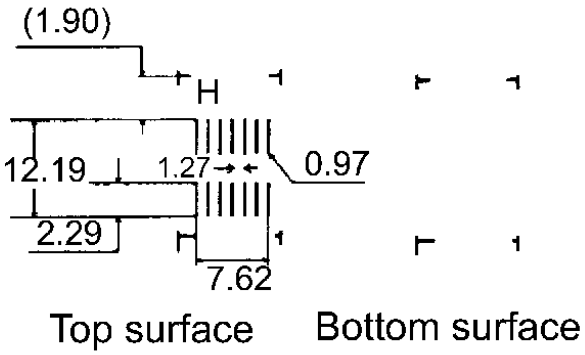
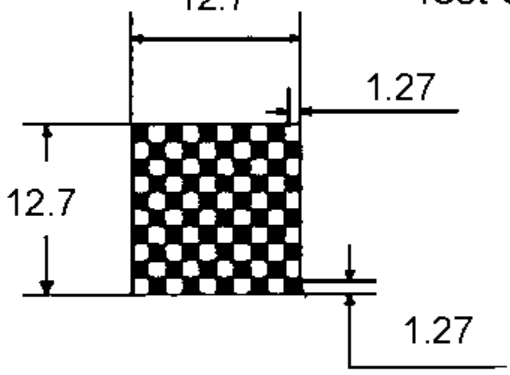


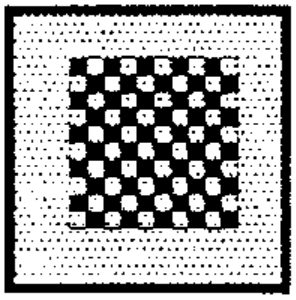
Figure E-10. Test Coupons (for Multilayer Printed Wiring Board) (3/4)

Unit: mm

Test Coupon J

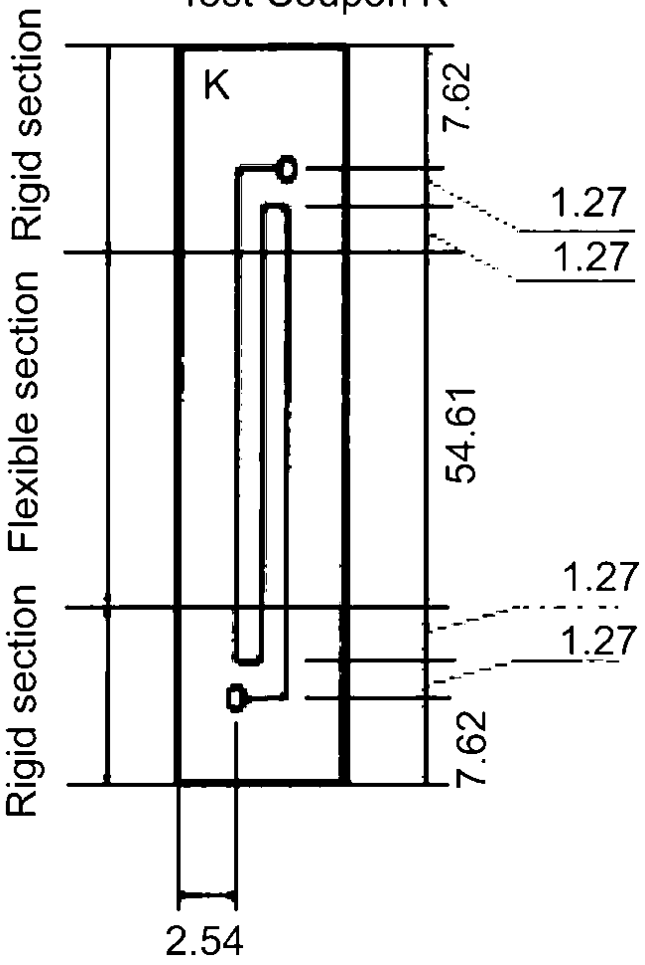


Top surface and bottom surface



Solder resist application area

Test Coupon K



Construction	Conductor width	Conductor spacing
Outer type	0.30	0.20
Inner type	0.30	0.25

Figure E-10. Test Coupons (for Multilayer Printed Wiring Board) (4/4)

Table E-12. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail		
					Samples(1)		Quantity of allowable defects
Group	Order	Test item			Production R/F-PWB	Test coupon(2)	
I	1	Design and construction	E.3.3	E.4.4.2	No. 1 to No. 6	A, B, C, D, E, F, G, H, K and L(4)	0
	2	Externals, dimensions, marking and others	E.3.4	E.4.4.2			
	3	Workmanship(3)	E.3.5	E.4.4.3			
II	1	Plating adhesion and overhang	E.3.6	E.4.4.4	No. 1 to No. 6	C	
	2	Bow and twist	E.3.5.1	E.4.4.3.1		N/A	
III	1	Through holes	E.3.4.1.5	E.4.4.2.3	No. 1	A and F	
	2	Terminal pull strength	E.3.9.1	E.4.4.7.3		F	
	3	Solder resist thickness	E.3.4.2.1	E.4.4.2.4		J	
	4	Folding flexibility	E.3.9.2	E.4.4.7.1		K	
	5	Flexibility endurance	E.3.9.3	E.4.4.7.2		K	
IV	1	Connection resistance	E.3.8.3	E.4.4.6.3	No. 2	D	
	2	Hot oil resistance	E.3.10.3	E.4.4.8.3			
	3	Connection resistance	E.3.8.3	E.4.4.6.3			
V	1	Circuitry	E.3.8.2	E.4.4.6.2	No. 3	E and G(5)	
	2	Connection resistance	E.3.8.3	E.4.4.6.3			
	3	Thermal shock (I)	E.3.10.1.1	E.4.4.8.1 a)			
	4	Circuitry	E.3.8.2	E.4.4.6.2			
	5	Connection resistance	E.3.8.3	E.4.4.6.3			
VI	1	Humidity and insulation resistance	E.3.10.2	E.4.4.8.2	No. 4	E	
	2	Dielectric withstanding voltage	E.3.8.1	E.4.4.6.1			
VII	1	Thermal stress	E.3.10.4	E.4.4.8.4	No. 5	A and B	
	2	Solderability	E.3.9.4	E.4.4.7.4		B and H(6)	
VIII	1	Radiation hardness	E.3.10.5	E.4.4.8.5	No.6	N/A	
IX	1	Materials	E.3.2	-	(7)		-

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type. In order to qualify split boards, split board specimens shall be submitted.

(2) Test coupons and production F/R-PWBs shall be manufactured simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production F/R-PWBs which shall be subjected to the same group test.

(3) Bow and twist (paragraph E.3.5.1) of the samples shall be tested during the second test of Group II tests.

(4) Group I test shall be performed on the test coupons which shall be provided for Group II through VIII tests.

(5) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(6) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

(7) Data shall be submitted to certify compliance with design specifications.

E.4.3 Quality Conformance Inspection

E.4.3.1 Quality Conformance Inspection (Group A)

E.4.3.1.1 Sample

Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to affect the inspection result, the part marked with rejection shall not be used as a specimen. A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

E.4.3.1.2 Inspection Items and Sample Size

The items and test order of the Group A inspection shall be in accordance with Table E-13. The inspections within each group shall be performed in numerical order. The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be fabricated simultaneously and one each of test coupons is subjected to each tests.

E.4.3.2 Quality Conformance Inspection (Group B)

E.4.3.2.1 Sample

The test coupons for the Group B inspection may be manufactured at the same time as the manufacture of the test coupons for the Group A inspection.

E.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be in accordance with Table E-14. The inspections within each group shall be performed in the order listed. One test coupon shall be provided for each group.

Table E-13. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail		
					Samples		Quantity of allowable defects
Group	Order	Inspection item			Production R/F-PWB	Test coupon(1)	
I	1	Externals, dimensions, marking and others	E.3.4	E.4.4.2	All	N/A	0
	2	Workmanship(2)	E.3.5	E.4.4.3			
II	1	Bow and twist	E.3.5.1	E.4.4.3.1	All	N/A	
III	1	Circuitry	E.3.8.2	E.4.4.6.2	All	N/A	
IV	1	Thermal stress	E.3.10.4	E.4.4.8.4	N/A	A and B(1)	
	2	Through holes Conductive interface Plating thickness	E.3.4.1.5 b) e)	E.4.4.2.3 a) E.4.4.2.3 b) E.4.4.2.3 c)			
V	1	Solderability	B.3.9.4	B.4.4.7.4	N/A	B and H(3)	

Notes:

(1) The test coupon A shall be inspected only when the corresponding product is provided with small via holes of which drill diameter is a maximum of 0.5mm.

(2) Bow and twist (paragraph E.3.5.1) of the samples shall be tested during the first test of Group II tests.

(3) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

Table E-14. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	E.3.6	E.4.4.4	C	0
II	1	Terminal pull strength	E.3.9.1	E.4.4.7.3	F	
	2	Connection resistance	E.3.8.3	E.4.4.6.3	D	
	3	Hot oil resistance	E.3.10.3	E.4.4.8.3		
	4	Connection resistance	E.3.8.3	E.4.4.6.3		
III	1	Circuitry	E.3.8.2	E.4.4.6.2	E and G(1)	
	2	Connection resistance	E.3.8.3	E.4.4.6.3		
	3	Thermal shock (II)	E.3.10.1.2	E.4.4.8.1 b)		
	4	Circuitry	E.3.8.2	E.4.4.6.2		
	5	Connection resistance	E.3.8.3	E.4.4.6.3		
IV	1	Humidity and insulation resistance	E.3.10.2	E.4.4.8.2	E	
	2	Dielectric withstanding voltage	E.3.8.1	E.4.4.6.1		
V	1	Folding flexibility	E.3.9.2	E.4.4.7.1	K	
VI	1	Flexibility endurance	E.3.9.3	E.4.4.7.2	K	

Note: (1) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

E.4.4 Methods for Test and Inspection

E.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

E.4.4.2 Externals, Dimensions, Marking and Others

Design, construction, externals, dimensions (conductive patterns and edges) and marking of F/R-PWBs shall be tested. Externals shall be inspected visually.

E.4.4.2.1 Conductive Patterns and Edges

Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument which has sufficient accuracy.

E.4.4.2.2 Annular Ring

The measurement of the annular ring on an external layer shall be from the internal surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the F/R-PWB. Dimensions of annular ring shall be measured using an optical measuring instrument which has sufficient accuracy.

E.4.4.2.3 Through Holes

a) Vertical microsection
The F/R-PWB specimen shall be cut in the vertical plane near the center of a hole. The samples shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, dielectric layer thickness and plating thickness) and the solder resist thickness at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board's length direction.

b) Horizontal microsection
Only multilayer boards shall be subjected to the horizontal microsection inspection. Multilayer boards with through holes shall be encapsulated and polished. Any conductive layer shall be polished in the parallel direction. The microsection is prepared so that the conductive layer is exposed. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X.

c) Plating thickness
The plating thickness shall be measured using microsections prepared in accordance with paragraph E 4.4.2.3 a) at a magnification of 200X as a minimum. Measurements shall be averaged from three determinations for a

plated-through hole. Isolated thick or thin sections shall not be used for averaging.

d) Layer-to-layer registration

The layer-to-layer registration shall be measured at a magnification of 25 to 100X using microsections prepared in accordance with paragraph E.4.4.2.3 a). The misregistration shall be inspected around the hole in the direction parallel to the board length and the vertical direction (see Figure E-11). This provision shall not apply to IVH or SVH.

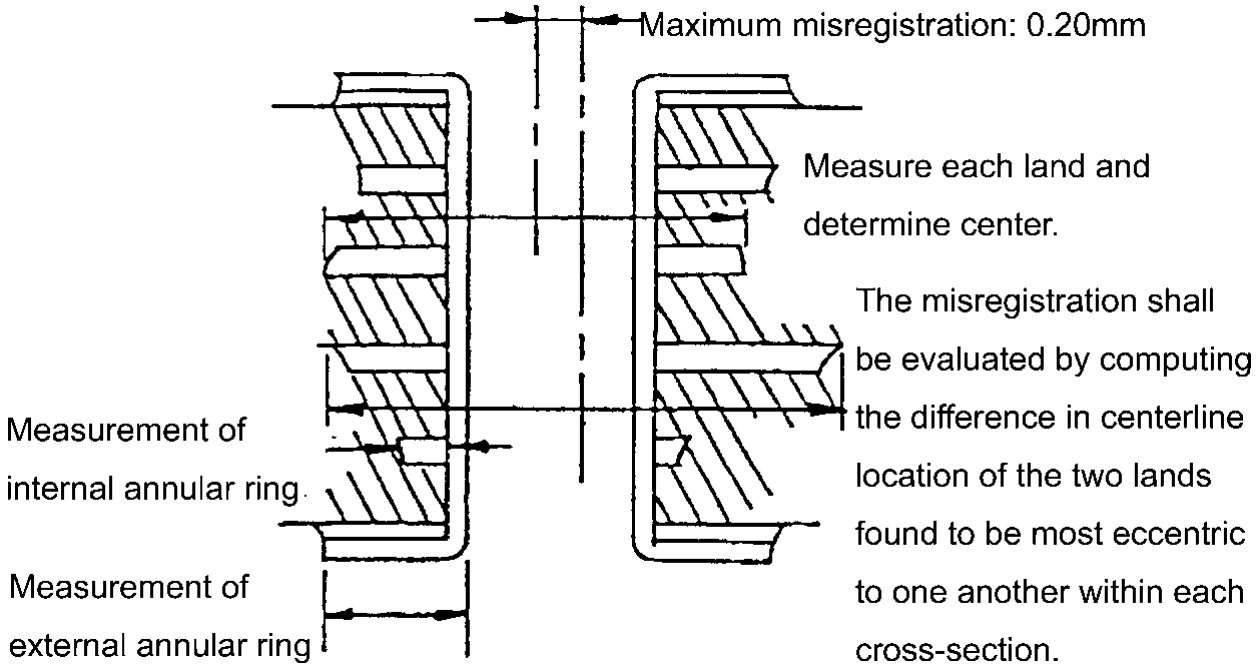


Figure E-11. Measurement of Layer-to-Layer Registration and Annular Ring

e) Dielectric layer thickness

The dielectric layer thickness shall be measured using microsections prepared in accordance with paragraph E.4.4.2.3 a).

f) Annular ring

The annular ring shall be measured using microsections prepared in accordance with paragraph E.4.4.2.3 a). The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the f/R-PWB. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure E-11).

E.4.4.2.4 Solder Resist Thickness

The solder resist thickness shall be measured using a microsection prepared in accordance with paragraph E.4.4.2.3a) at a magnification of 200X as a minimum.

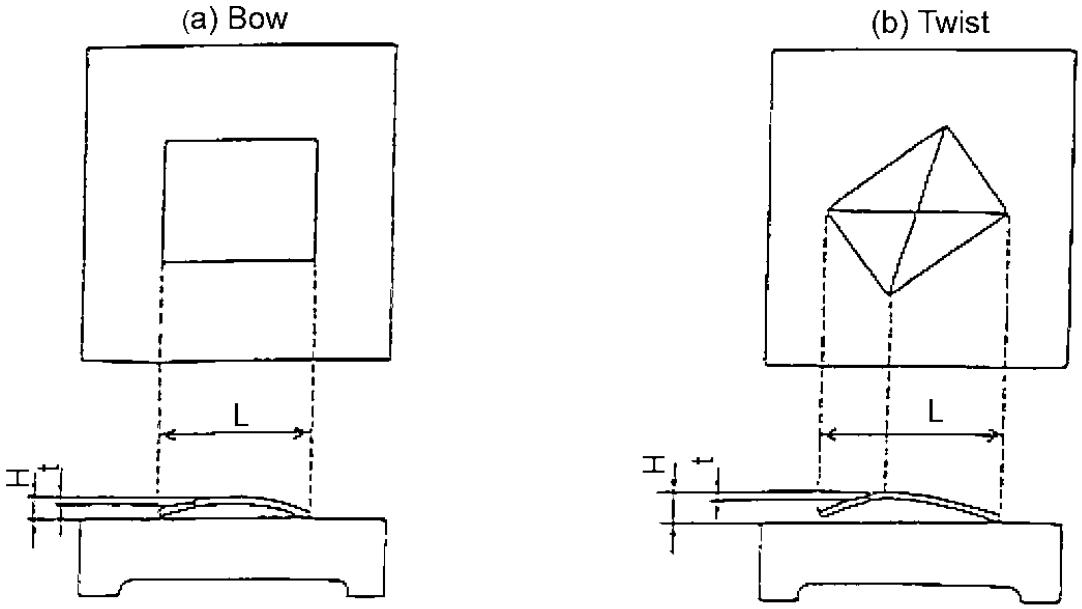
E.4.4.3 Workmanship

The workmanship of F/R-PWB shall be inspected visually. The bow and twist shall be inspected as follows.

E.4.4.3.1 Bow and Twist

The F/R-PWB specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the F/R-PWB shall be measured (see Figure E-12). The percent bow and twist shall be calculated by the following formula.

Percent bow and twist = $\frac{H-t}{L} \times 100$ (%)



H = Height from the reference plate (mm)
t = Thickness of the R/F-PWB (mm)
L = Length of the side or diagonal line (mm)

Figure E-12. Measurement of Bow and Twist

E.4.4.4 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and minimum 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern of the rigid section, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the F/R-PWB. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is evidence of slivers, but not a plating adhesion failure.

E.4.4.5 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. F/R-PWBs shall be suspended within the funnel. A wash solution of 75 percent by volume of isopropyl alcohol and 25 percent by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6 \Omega \cdot cm$. The wash solution shall be poured onto both sides of the F/R-PWB from the top until 100ml of the wash

solution is collected from each board surface of 6.5cm^2 (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. It is imperative that the initial washings be included in the sample to be measured for resistivity. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods given in Table E-15 may be used to perform the cleanliness test.

Table E-15. Equivalent Factors

Method	Resistivity ($\times 10^6 \Omega \cdot$cm)	Equivalent factor	Equivalents of sodium chloride (μg/cm^2)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.20

Note: (1) Alpha Metals Incorporated, “Omega Meter”

E.4.4.6 Electrical Performance

The electrical performance tests of the F/R-PWB shall be performed as follows.

E.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: 1000V_{AC} peak or 1000V_{DC}
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

E.4.4.6.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity.
b) Circuit shorts
A voltage of 250V_{DC} shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

E.4.4.6.3 Connection Resistance

An electrical wire shall be soldered at two lands of through holes to obtain proper electrical conductivity. The resistance between the lands shall be measured using a measuring instrument capable of measuring a resistance below 0.5mΩ.

E.4.4.7 Mechanical Performance

The mechanical performance tests of the F/R-PWB shall be performed as follows.

E.4.4.7.1 Folding Flexibility

A fold cycle shall be defined as taking one end of the sample, folding it around a mandrel and then unfolding it to the original starting position, traveling 180 degrees in one direction and 180 degrees in the opposite direction. The mandrel radius shall be ten to twelve times as large as the flexible material thickness of the F/R-PWB. The test shall be performed for five cycles. After the test, the F/R-PWB shall be tested as specified in paragraph E.4.4.6.2 and shall not exhibit degradation or rejectable delamination at the folded portion.

E.4.4.7.2 Flexibility Endurance

Insulated lead wires shall be attached to the extreme ends of a conductive pattern of the sample. Using the flexibility endurance fixture shown in Figure E-13, the sample shall be mounted so that the inside diameter of the loop is 9.6mm±0.4mm. The two wires shall then be connected to the relay and the voltage applied to it. The reciprocating travel shall not exceed 10 cycles per minute, and the loop shall travel at least 25.4mm. The test shall be performed for the number of cycles specified on drawings and continued until the conductor is fractured. The number of cycles shall be checked by the associated counter. A failure shall occur when the conductor is fractured within the specified number of cycles, and the fixture does not work. After the test, F/R-PWBs shall be tested as specified in paragraph E.4.4.6.2 and shall not exhibit degradation or rejectable delamination at the folded portion.

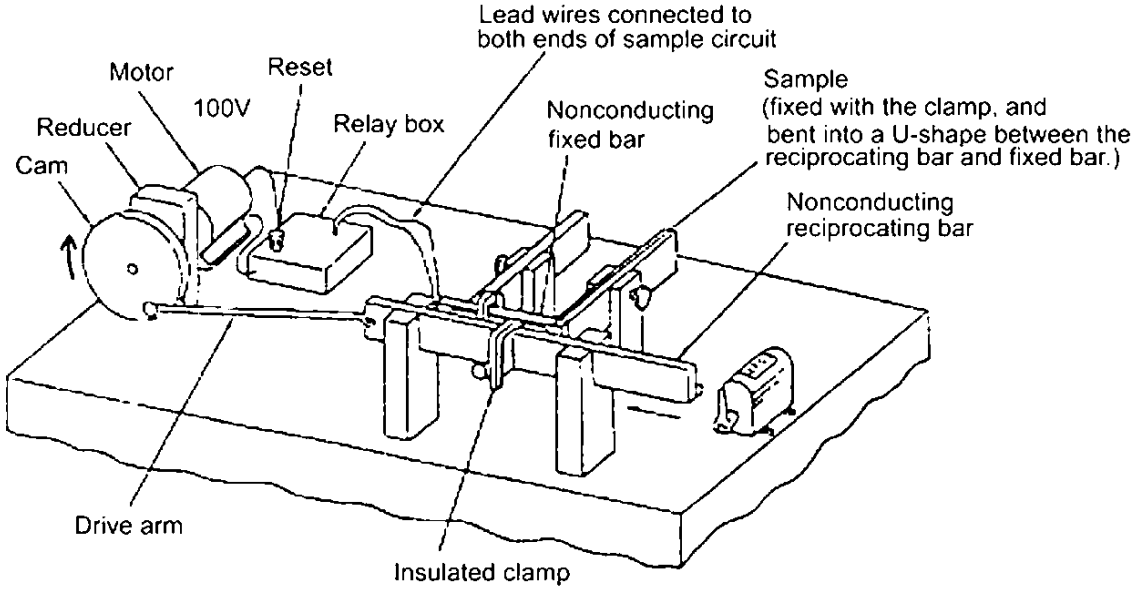


Figure E-13. Flexible Endurance Fixture

E.4.4.7.3 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.

Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

E.4.4.7.4 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection prepared in accordance with paragraph E.4.4.8.4.

b) Surface solderability
After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

E.4.4.8 Environmental Performance

The environmental performance tests shall be performed as follows.

E.4.4.8.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
A cycle shall consist of 30 minutes at -30°C and 30 minutes at +100°C. The specimen shall be subjected to 1000 cycles in total. Transfer time from the low temperature to the high temperature, or the reverse, shall not exceed 2 minutes.

b) Thermal shock (II) (applicable to quality conformance inspection)
The test shall be performed under the test condition B-3. The time for step 2 and 4 shall be within 2 minutes each.

E.4.4.8.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of $100V \pm 10V_{DC}$ shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

E.4.4.8.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. Immersion and cooling shall be performed for 10 cycles. At the completion of the test, the specimen shall be inspected in accordance with paragraph E.4.4.6.3.

E.4.4.8.4 Thermal Stress

The specimen shall be conditioned by drying for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 percent maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for any crack on the internal copper foil and laminate voids using the microsection prepared in accordance with paragraph E.4.4.2.3 a). Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

E.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose

amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests for dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph E.4.4.6.1 and E.4.4.8.2 b), respectively. The insulation resistance shall be measured in the same circuit as the one used for the dielectric withstanding voltage test.

APPENDIX F

**PRINTED WIRING BOARDS,
CIC CONTROLLED THERMAL EXPANSION,
GLASS BASE WOVEN POLYIMIDE RESIN
BASE MATERIAL**

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX F

PRINTED WIRING BOARDS, CIC CONTROLLED THERMAL EXPANSION, GLASS BASE WOVEN POLYIMIDE RESIN BASE MATERIAL

F.1. General

F.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the fine pitch printed wiring boards with a low thermal expansion characteristics using CIC (Copper-Invar-Copper-clad) that has a low coefficient of thermal expansion for the purpose of improving the connection reliability on surface mounted parts, and the boards use glass base woven polyimide resin as a base material (hereinafter referred to as "printed wiring boards")

F.1.2 Classification

Products covered by this specification shall be classified as specified in Table F-1.

Table F-1. Classification

Base material	Construction	Remarks
Glass base woven polyimide resin	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
	Double-sided printed wiring board	
	Multilayer printed wiring board	

F.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA(1) 2140/F	105	GI	III	4(2)
	Individual identification	Base material code (F.1.3.1)	Processing code (F.1.3.2)	Number of layers (F.1.3.3)

Notes:
(1) "JAXA" indicates the part is for space use and may be abbreviated “J”.
(2) Number of conductor layers

F.1.3.1 Base Material Code

The base material code of the printed wiring boards is as specified in Table F-2.

Table F-2. Base Material Code

Base material code(1)	Base material
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

Note: (1) Applicable standards for GI types are as specified in the detail specification. Details of GI base material, including type and glass transition temperature (Tg), are as specified in the Application Data Sheet (ADS).

F.1.3.2 Processing Code

The processing code of the printed wiring boards is as specified in Table F-3.

Table F-3. Processing Code

Processing code	Construction	Remarks
I	Single-sided printed wiring board	Including double-sided printed wiring boards without through holes
II	Double-sided printed wiring board	
III	Multilayer printed wiring board	

F.1.3.3 Number of Layers

The maximum number of layers of the printed wiring boards shall be specified in each detail specification.

F.2. Applicable Documents

F.2.1 Reference Documents

The reference documents shall be as specified in paragraph 2.2.

F.3. Requirements

F.3.1 Qualification Coverage

Qualification shall be valid for printed circuit boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs F.3.2 to F.3.10. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers, less thickness and fewer CIC than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. Test data taken using samples with the same base and the same metal foil may be used as test data for samples with a different number of layers except for the thermal shock test. In this case the sample shall have more layers than the samples for qualification test. Within this coverage, the manufacture is allowed to supply qualified products

in compliance with the detail specification. If necessary, additional qualification coverage shall be specified in the detail specification.

F.3.2 Materials

The materials of the printed wiring boards shall be specified as follows and as specified in paragraph 3.3.

F.3.2.1 Metal-Clad Laminate, Prepreg and Metal Foil

The metal-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings. The base material shall be polyimide resin (paragraph F.1.2). The nominal thickness of the base material shall be not less than 0.05mm.
The metal foil shall be copper if metal-clad laminate or metal foils are stacked on top of each other with prepreg. The copper foil for the outermost layer shall have a thickness of 18μm (nominal) as a minimum in consideration of additional conductor thickness for plating. Only when printed wiring boards have surface via holes (SVH), the copper foil for the outermost layer shall have an additional thickness of 9μm (nominal) as a minimum. The copper foil for an internal layer shall have a nominal thickness of 35μm as a minimum. However, it shall be a minimum of 18μm (nominal) in consideration of additional conductor thickness for plating, only when SVH is provided. The applicable standards for the material used in the printed wiring boards shall be specified in each detail specification. Details of GI base material, including type and the glass transition temperature (Tg), shall be defined in the Application Data Sheet (ADS).

F.3.2.2 CIC

The low thermal expansion material, CIC utilized for the printed wiring boards is three-layer structured board (see figure F-1) with invar (Fe-Ni36% alloy) in the middle sandwiched by copper, 0.15mm in nominal thickness and 12.5/75/12.5 in nominal ratio.

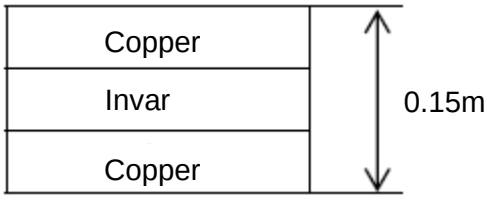


Figure F-1. CIC Cross-section View

F.3.2.3 Solder Coating

The solder used for solder coating shall contain 50 to 70 percent tin.

F.3.2.4 Solder Resist

The solder resist applied on the printed wiring boards shall conform to IPC-SM-840 Class H or the equivalent. The application shall be in accordance with manufacturing drawings.

F.3.2.5 Marking Ink

The marking shall be produced using epoxy resin base ink that does not easily vanish by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

F.3.2.6 Plating

Unless otherwise specified, the solder coating specified in paragraph F.3.2.3 shall be applied to all through holes (excluding SVH and small via holes), lands and surface conductive patterns, except for where solder resist is applied. All through holes except SVH shall be coated with copper plating and subsequently with the same type surface plating as the plating applied on lands. When plating other than the plating applied on lands is partially required in through holes except for the fine pith patterns, electrolytic gold plating may be applied.

F.3.2.6.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating inside through holes to form a conductor layer over the insulating material.

F.3.2.6.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 percent.

F.3.2.6.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table F-4. The electrolytic nickel plating specified in paragraph F.3.2.6.4 may be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 percent except for the metal added to increase the hardness.

Table F-4. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 percent
KNOOP hardness	91 to 129 (inclusive)

F.3.2.6.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.

F.3.3 Design and Construction

F.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. As a rule, all locations on drawings shall be indicated at grid points and the grid spacing shall be 2.54mm. Any location deviating from grid points shall be indicated, showing the corresponding dimensions. If manufacturing drawings and artwork masters (or original production masters) are

created based on the same CAD drawing data, the indication of grid points and dimensions of the locations deviating from grid points may be omitted. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

F.3.3.2 CIC

CIC shall not be used for conductor layer unless CIC is used as a ground layer.

F.3.3.3 Connector for Printed Wiring Boards

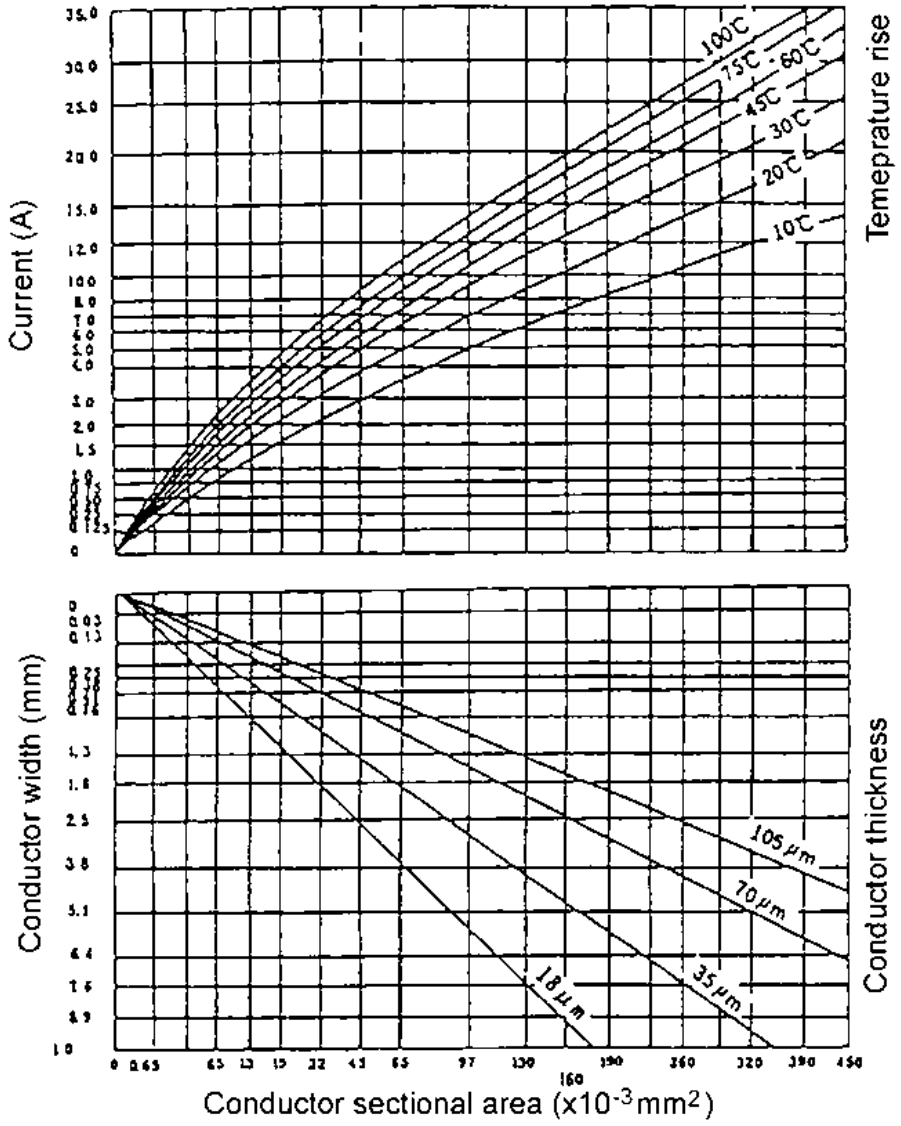
A direct connector (one-part connector or edge-board connector) shall not be used.

F.3.3.4 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by through holes including small via holes and SVH. The small via holes shall be a minimum of 0.3mm in its drill diameter. The SVH shall have a minimum of 0.15mm in its diameter.

F.3.3.5 Conductor Width

The design width of the conductor shall be not less than 0.13mm. The actual conductor width of external and internal layers shall be designed in accordance with Figures F-2 and F-3.



Remarks:

(1) This chart has been prepared as an aid in estimating relationships between the conductor sectional area and the current flowing in the conductor or the temperature rise from ambient temperature. The conductor surface area is assumed to be relatively small, compared to the adjacent insulating plate area. The allowable current value of this curve includes a nominal of 10 percent derating to allow for normal variations due to etching techniques, conductor thickness and width and cross-sectional areas.

(2) Additional derating of 15 percent for the allowable current is suggested under the following conditions:
   a) Where dielectric layer thickness is less than 0.8mm.
   b) Where conductor thickness is greater than 105μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.

(4) For single conductor applications, the chart may be used for determining conductor widths, cross-sectional area and allowable current (current-carrying capacity) for various temperature rises.

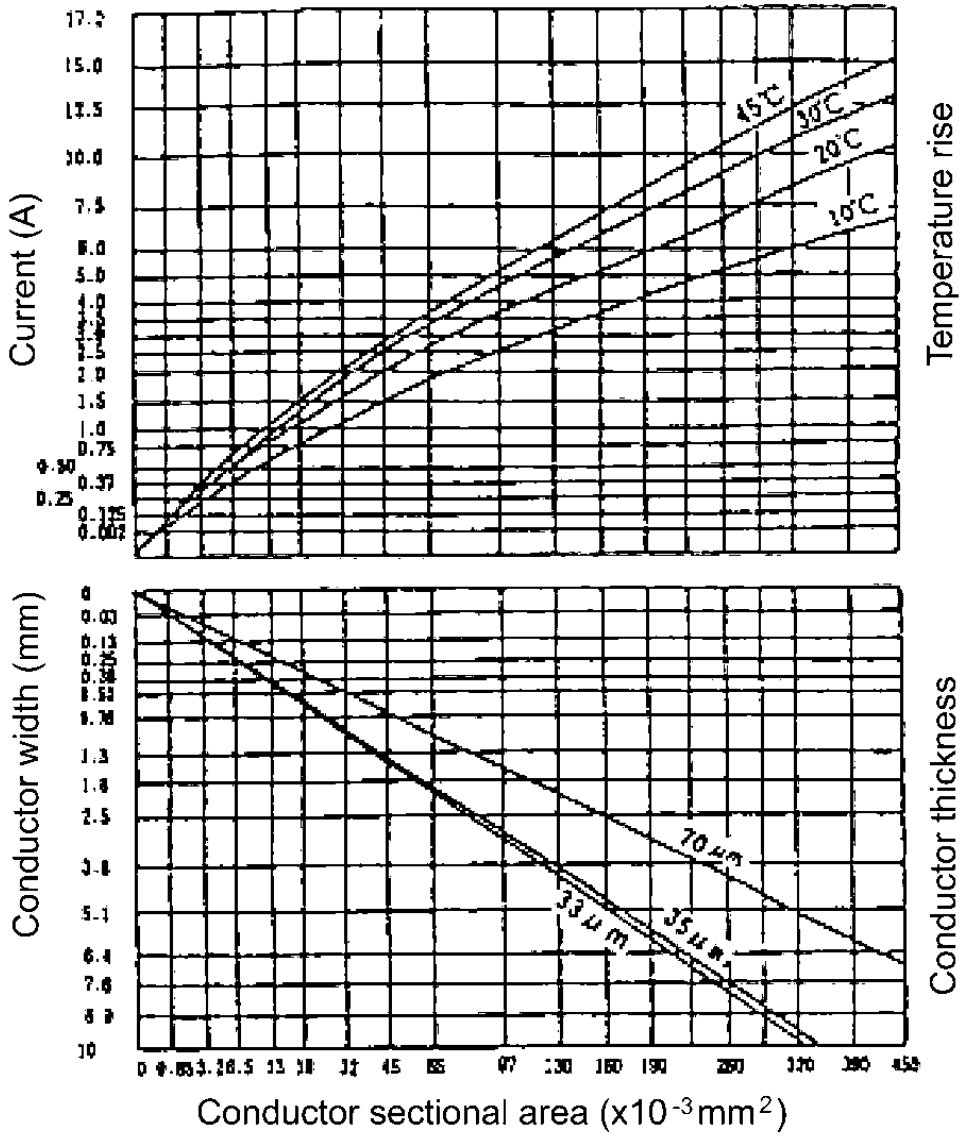
(5) For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross section and an equivalent current.

(6) The effect of heating due to heat generating parts is not considered.

(7) The final conductor thickness in the chart does not include plating thickness of metals other than copper.

(8) The 54μm line shall apply to an external layer with SVH.

Figure F-2. Conductor Width (External Layer)



Remarks:

(1) Remarks (1) through (7) of Figure F-2 shall apply to this figure.

(2) The 33μm line shall apply to internal layers with SVH.

Figure F-3. Conductor Width (Internal Layer)

F.3.3.6 Conductor Spacing

The conductor spacing in design shall be not less than 0.18mm. The specific conductor spacing shall depend on the voltage applied between conductors as specified in Table F-5.

Table F-5. Conductor Spacing for Coated Printed Wiring Board

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing (**mm)**	
	External layer	Internal layer
0 - 100	0.18	0.18
101 - 300	0.48	0.30
301 - 500	0.86	0.35
501 or higher	(0.003xV)+0.1	(0.003xV)+0.1

F.3.3.7 Land Diameter

The minimum design value of land diameter shall be as specified in Table F-6 (see Figure F-4).

Table F-6. Land Diameter

Unit: mm

Hole	Minimum land diameter(1)
SVH and small via holes	Drill diameter + 0.4(2)
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

Notes:

(1) The minimum diameter of lands other than round shaped lands shall be measured as the length “A”, as shown in Table F-4.

(2) The minimum diameter of the land provided with a small via hole shall be 0.76mm.

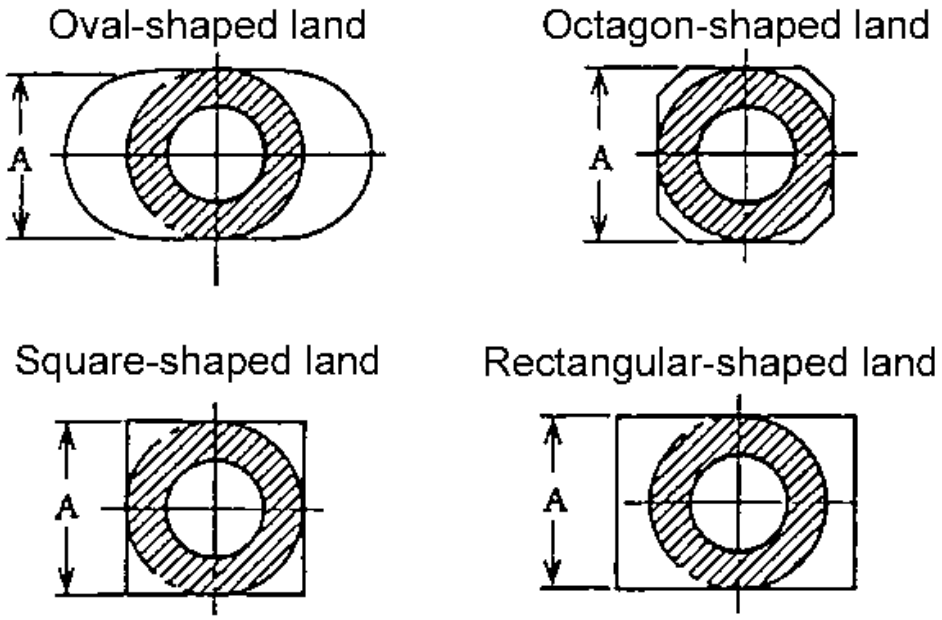


Figure F-4. Measurement of Minimum Diameter of Lands Other than Round Shaped Lands

F.3.3.8 Plating Thickness and Others

The thickness of plating and solder coating shall be as specified in Table F-7.

Table F-7. Plating or Coating Thickness

Unit: μm

Plating material	Surface and through hole plating thickness	
Electroless copper	Necessary and sufficient thickness for the subsequent process, electrolytic copper plating	
Electrolytic copper	Component hole	Min. 25
	Small via hole	Min. 30
	SVH	Min. 15
Electrolytic gold	1.3 to 4.0	
Electrolytic nickel	Min. 5	
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements.	

F.3.3.9 Operating Temperature Range

Printed wiring boards shall operate within the temperature range (–65°C to +170°C) of the thermal shock (II) test (paragraph F.3.10.1.2).

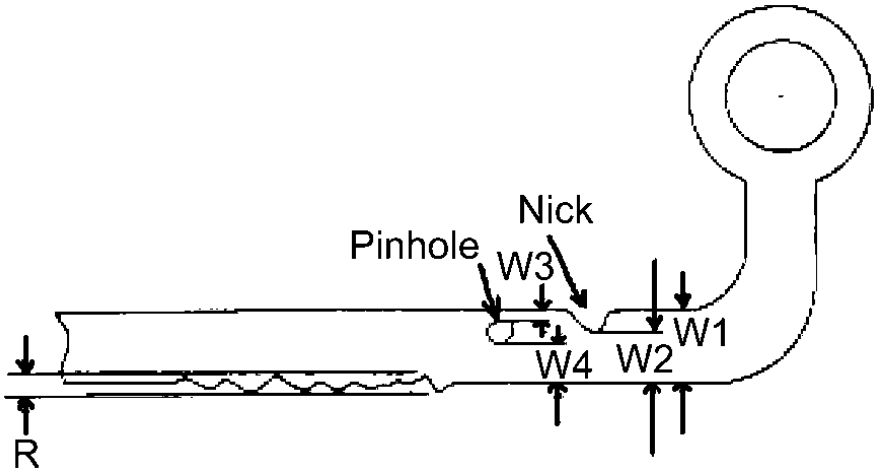
F.3.4 Externals, Dimensions, Marking and Others

F.3.4.1 Externals and Construction

F.3.4.1.1 Externals of Conductive Pattern, Base Material and Solder Resist

a) Conductive pattern
The conductive patterns and CIC shall conform to the approved or provided artwork master (or original production master).

b) Conductor
The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the base material shall not reduce the conductor width to less than 80 percent of the minimum finished conductor width. The minimum finished conductor width shall be 0.08mm. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall be no more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall be not more than 0.08mm in the difference between the convex and concave portions in any range of 13mm in length. When the design width of the conductor is not less than 0.2mm, the roughness shall be maximum 0.13mm (see Figure F-5).



Unit: mm

W1 ≥ (Minimum finished conductor width) ≥ 0.08
W2 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
W3+W4 ≥ 0.80×(Minimum finished conductor width) ≥ 0.08
R in any range of 13 in length
R ≤ 0.08, when the design width of the conductor is less than 0.2
R ≤ 0.13, when the design width of the conductor is 0.2 or more

Figure F-5. Conductor Defects

c) Annular ring
When the annular ring on the internal and external layers are measured in accordance with paragraph F.4.4.2.2 f), the annular ring of a plated-through hole shall be not less than 0.05mm. The annular ring of a non-plated-through hole shall be not less than 0.38mm and shall not contain any defect. When the annular ring for plated-through hole on an external layer shall be a minimum of 0.13mm in diameter, a sub-land or other equivalent alternative shall be provided.

d) Dielectric layer between conductor layers
The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.

e) Electrolytic solder plating and solder coating
The electrolytic solder plating and solder coating shall be free from pinholes or pits, and completely cover conductive patterns.

f) Edges of printed wiring board
Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board and exposure of CIC.

g) Surface of printed wiring board
Surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall be acceptable, provided that the area of each does not exceed 1 percent of the surface area of the printed wiring board, and the spacing between conductors is not reduced

exceeding 25 percent. Crazing along edges of the printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

h) Solder resist

The cured solder resist shall be free from tackiness, blistering and delamination. Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted. The solder resist shall not encroach onto lands. Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist. The application range and registration onto conductive patterns shall meet the provisions of manufacturing drawings.

F.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table F-8.

Table F-8. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.
Conductor width	0.13 or more and less than 0.20: ±0.05 0.20 or more and less than 0.50: ±0.10 0.50 or more: ±20 percent of circuit width
Conductor spacing	For the design of three patterns between basic grids, the tolerance of conductor spacing shall be -0.08. (The positive side tolerance is not specified.) For the design of maximum two patterns between basic grids, the tolerance of conductor spacing shall be -0.10. (The positive side tolerance is not specified.) The minimum tolerance of conductor spacing on an external layer shall be 0.13.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

F.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph F.3.2.5 by the same process as producing conductive patterns, or by laser marking. The marking shall not adversely affect any function, performance or reliability of printed wiring boards.

All marking shall remain legible and in no manner affect the performance of the printed wiring boards. Unless otherwise specified, the following shall be marked on

each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

F.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

F.3.4.4 Through Holes

When printed circuit boards are tested as specified in paragraph F.4.4.2.2, the plating of through holes, small via holes and SVH shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land. Nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings. Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80μm, and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated. The cross-section diagram for the area of through holes shall be show in Figure F-6. (The parts indicated in black are CIC)

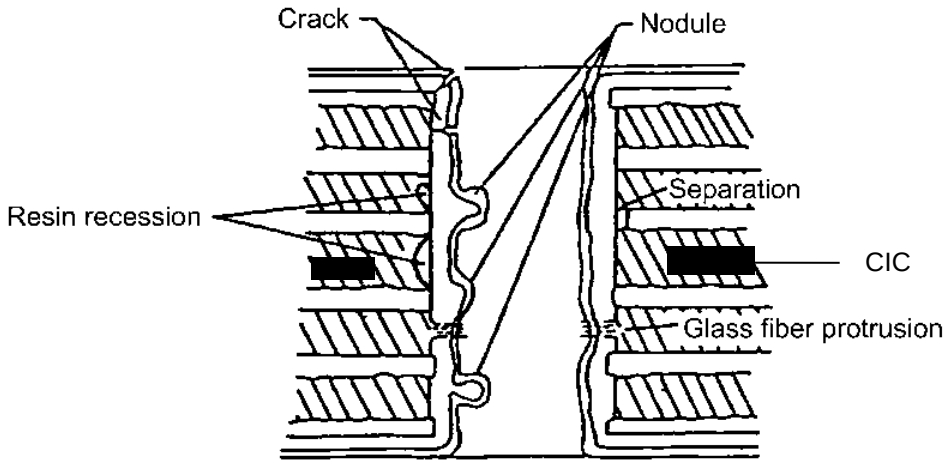


Figure F-6. Through Hole Deficiencies

a) Voids

A plated-through hole shall not exhibit more than three plating voids. The total of the circumferential length of voids shall not exceed 10 percent of the through hole circumference, and the total length of voids in the vertical direction shall not exceed 5 percent of the hole wall length. No voids shall be allowed at the interface with a conductor or on both sides of a hole in the same plane (see Figure F-7).

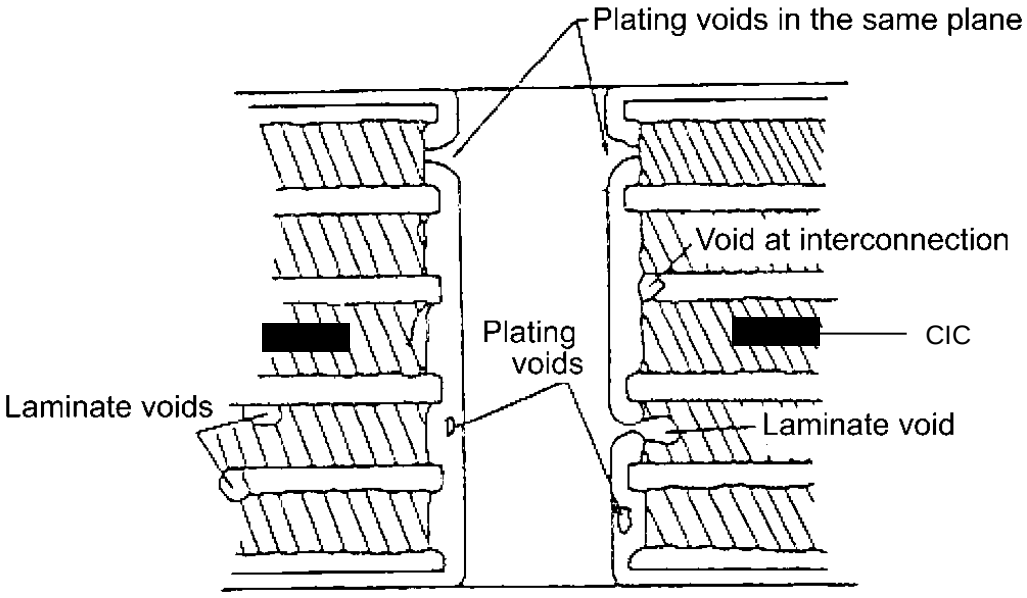


Figure F-7. Voids

b) Conductive interface

The resin smear at the interface of the hole wall plating and an internal conductor layer shall not exceed 25 percent of the through hole circumference in horizontal microsection, and 50 percent of the interface in the same plane in vertical microsection. Nail heading of a conductor layer shall not exceed 50 percent of the metal foil thickness (see Figure F-8).

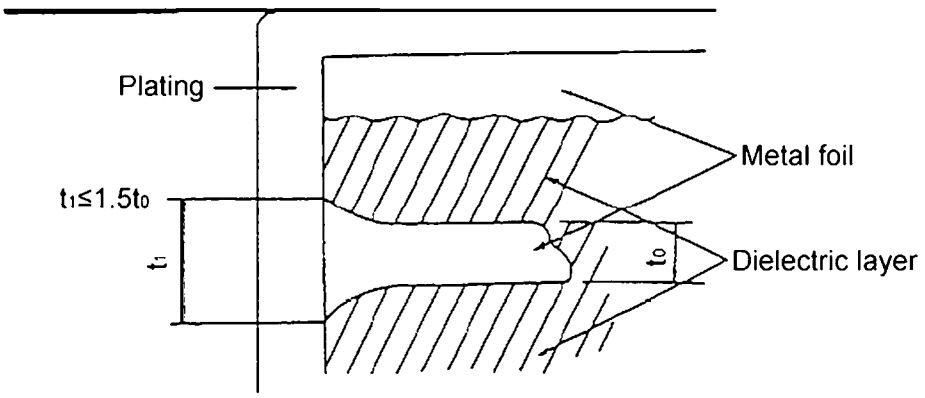


Figure F-8. Nail Heading

c) Layer-to-layer registration
The layer-to-layer registration error shall not exceed 0.20mm.

d) Dielectric layer thickness
The dielectric layer between conductor layers of a multilayer printed wiring board shall be not less than 0.08mm in thickness.

e) Plating thickness
The plating thickness shall meet the requirements specified in paragraph F.3.3.6.

f) Annular ring
The annular ring shall meet the requirements specified in paragraph F.3.4.1.1 c).

F.3.4.5 Solder Resist Thickness

When printed circuit boards are tested as specified in paragraph F.4.4.2.3, the solder resist thickness shall be not less than 17.5μm, measured at the center of conductors.

F.3.5 Workmanship

The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

F.3.5.1 Bow and Twist

When printed circuit boards are tested as specified in paragraph F.4.4.3.1, the maximum limit for bow and twist shall be 0.8 percent, unless otherwise specified on manufacturing drawings. For a split board, the percent bow and twist shall not exceed the value specified above, before separation.

F.3.5.2 Repair

The insulating plates or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted.

F.3.6 Plating Adhesion and Overhang

When printed circuit boards are tested as specified in paragraph F.4.4.4, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

F.3.7 Cleanliness

The printed wiring boards shall exhibit no fouling including dirt, oil, corrosion, corrosion product, salt, soot, grease, finger print, mold release agent, foreign inclusion and flux residues, or ionic contamination. When printed circuit boards are tested as specified in paragraph F.4.4.5, the resistivity of the solvent extract shall be not less than $2 \times 10^6 \Omega \cdot cm$.

F.3.8 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

F.3.8.1 Dielectric Withstanding Voltage

When tested as specified in paragraph F.4.4.6.1, printed circuit boards shall not exhibit insulation breakdown, flashover or sparkover.

F.3.8.2 Circuitry

When tested as specified in paragraph F.4.4.6.2, printed circuit boards shall not exhibit open circuit or short-circuiting between circuit patterns.

F.3.8.3 Connection Resistance

When printed circuit boards are tested as specified in paragraph F.4.4.6.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \cdot t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

F.3.9 Mechanical Performance

Printed wiring boards shall meet the following mechanical requirements.

F.3.9.1 Terminal Pull Strength

When tested as specified in paragraph F.4.4.7.1, printed wiring boards shall meet the following requirements. This provision shall not apply to SVH or small via holes.

a) Bond strength
The land shall withstand 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph F.4.4.2.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with paragraph F.4.4.2.2, there shall be no cracks, blistering, measling or delamination.

F.3.9.2 Solderability

When tested as specified in paragraph F.4.4.7.2, printed wiring boards shall meet the following requirements.

a) Hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to SVH or small via holes.

b) Surface solderability
A minimum of 95 percent of the surface conductor area shall be covered

uniformly with new solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area.

F.3.10 Environmental Performance

Printed wiring boards shall meet the following environmental requirements.

F.3.10.1 Thermal Shock

F.3.10.1.1 Thermal Shock (I) (applicable to qualification test)

When printed circuit boards are tested as specified in paragraph F.4.4.8.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph F.4.4.6.2, and connection resistance shall be measured in accordance with paragraph F.4.4.6.3. Printed wiring boards shall meet the requirements specified in paragraph F.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

F.3.10.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed circuit boards are tested as specified in paragraph F.4.4.8.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. At the completion of the test, circuit continuity and circuit shorts shall be tested in accordance with paragraph F.4.4.6.2, and connection resistance shall be measured in accordance with paragraph F.4.4.6.3. Printed wiring boards shall meet the requirements specified in paragraph F.3.8.2 after the test, and the change in connection resistance between circuits before and after the test shall be less than 10 percent.

F.3.10.2 Humidity and Insulation Resistance

When printed circuit boards are tested as specified in paragraph F.4.4.8.2, there shall be no blistering, measling or delamination. The insulation resistances between conductors and between conductor and CIC shall be not less than 500MΩ.

F.3.10.3 Hot Oil Resistance

When printed circuit boards are tested as specified in paragraph F.4.4.8.3, the change in connection resistance between circuits before and after the test shall be less than 10 percent.

F.3.10.4 Thermal Stress

When tested as specified in paragraph F.4.4.8.4, printed wiring boards shall meet the following requirements.

a) Externals
   There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.
b) Cross-section of through holes
   There shall be no cracks in internal copper foils in the vertical microsection of

through holes, or no separation of through hole plating in internal copper and CIC.

c) Laminate voids
Laminate voids with the longest dimension of 76μm as a maximum shall be permitted, provided the conductor spacing within a layer or between layers shall comply with the requirements of the minimum conductor spacing specified on manufacturing drawings.

F.3.10.5 Radiation Hardness

When printed circuit boards are tested as specified in paragraph F.4.4.8.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in paragraph F.3.8.1 shall be satisfied.

F.3.10.6 Thermal Expansion Coefficient

When printed circuit boards are tested as specified in paragraph F.4.4.8.6, the maximum value of the measured thermal expansion coefficient for the length direction of the printed wiring boards and the vertical direction to the length direction shall be 13ppm/°C.

F.4. Quality Assurance Provisions

F.4.1 In-Process Inspection

The in-process inspection specified below shall be performed, and printed wiring board shall meet the requirements of paragraphs F.3.4.1, F.3.4.2, F.3.4.3 and F.3.7.

a) Visual inspection of internal layers, construction and dimensions (100 percent)
b) Cleanliness (sampling)

F.4.2 Qualification Test

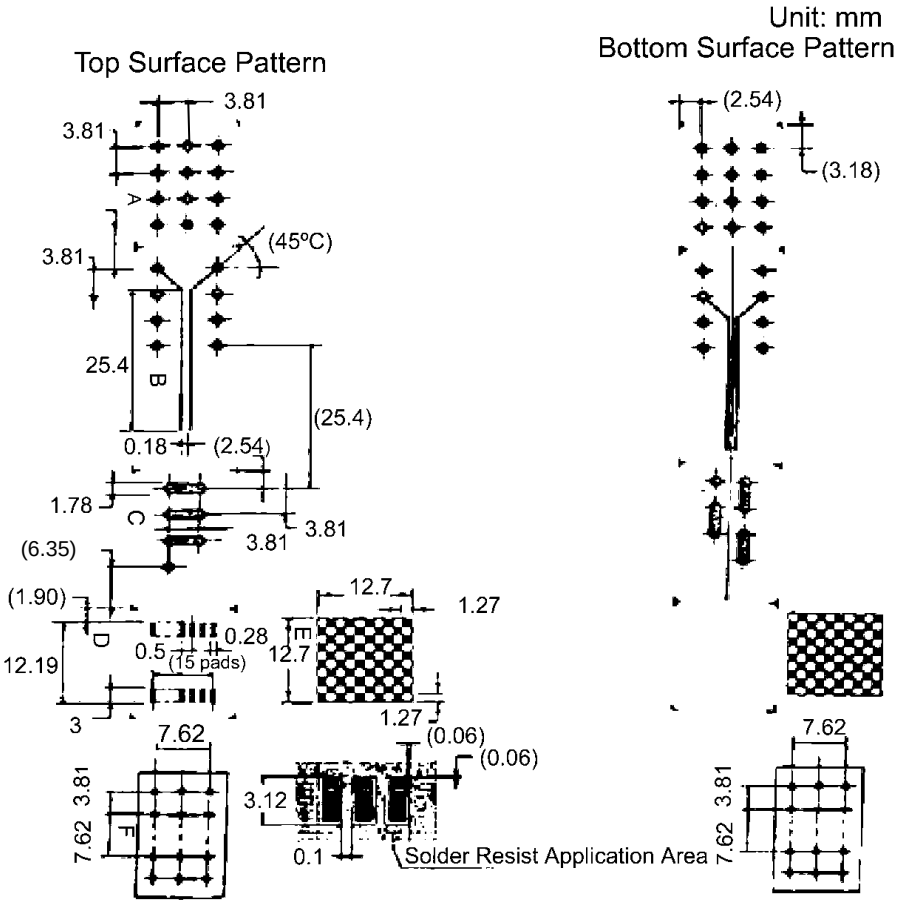
F.4.2.1 Sample

Samples shall have the minimum conductor width, conductor spacing and number of layers sufficient to verify compliance with the requirements of this appendix. The test coupons shall be as specified in Figure F-9 for single-sided or double-sided printed wiring boards and Figure F-10 for multilayer printed wiring boards. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board.

F.4.2.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table F-9. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. There shall be six

samples for each printed wiring board. The number of samples for test coupons shall be as specified in Table F-9.



Notes:

(1) For the test coupons A and B, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. The hole diameter shall be 0.8mm. For the test coupons C and F, the land diameter shall be the minimum land diameter of the corresponding printed wiring board, and the land shape shall be the same as that of the products. The hole diameter shall be the maximum hole diameter of the corresponding land. The test coupon F shall be prepared, only when the corresponding product has small via holes. All holes shall be through holes. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board. The CIC shall be produced so as to form the same structure as those of the corresponding product, and the proper clearance shall be set between CIC and through hole wall surface for the test coupon containing through holes. However, for any product with CIC/through hole interface, the interface shall be set at A area in the figure.

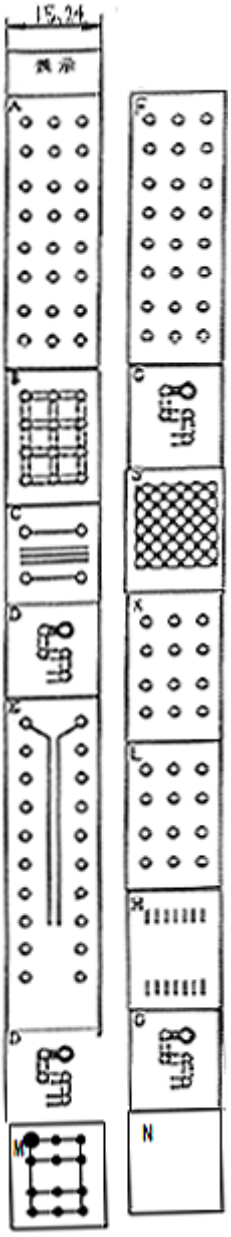
(2) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(3) The dimensions in the parentheses are reference dimensions.

(4) Solder resist shall apply to the test coupons B, D, and E, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon B shall be the land diameter increased by 0.2mm. For coupon E, the solder resist shall apply to the entire layer.

Figure F-9. Test Coupons (for Single-Sided or Double-Sided Printed Wiring Board)

Arrangement of Test Coupons



Unit: mm

Notes:

(1) The conductor width shall be 0.5±0.1mm unless otherwise specified.

(2) For test coupon A, the land diameter shall be the minimum land diameter of small via holes for the corresponding printed wiring board. The hole diameter shall be the maximum hole diameter among the minimum lands. All holes shall be through holes. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes. The hole diameter shall be 0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(4) Test coupons D and G are different in the number of layers and via hole structure. Each coupon shall be produced so as to form the same number of layers and via hole structure as those of the corresponding product, and to have a circuit continuity through all layers by via holes.
The land diameter shall be that of each SVH and small via hole of the corresponding products. The land shape shall be the typical land shape of the products.
The hole diameter shall be the maximum hole diameter applied for the minimum lands. On both ends of the printed wiring board, through holes shall be formed to measure the resistance. The land diameter shall be 1.8mm and hole diameter shall be 0.8mm. All holes shall be through holes. The hole diameter tolerance is not specified.

(5) The land diameter for the test coupon M shall be that of small via hole of the corresponding products. The land shape shall be the typical land shape of the products. The hole diameter shall be the maximum hole diameter applied for the minimum lands. Through holes shall be formed to measure the resistance. The land diameter shall be 1.8mm and hole diameter shall be 0.8mm. All holes shall be through holes. The hole diameter tolerance is not specified.

(6) The CIC shall be produced so as to form the same structure as those of the corresponding product, and the proper clearance shall be set between CIC and through hole wall surface for the test coupon containing through holes. However, for any product with CIC/through hole interface, the interface shall be formed at B area.

(7) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist applied on the test coupon E shall be equal to the land diameter +0.2mm.

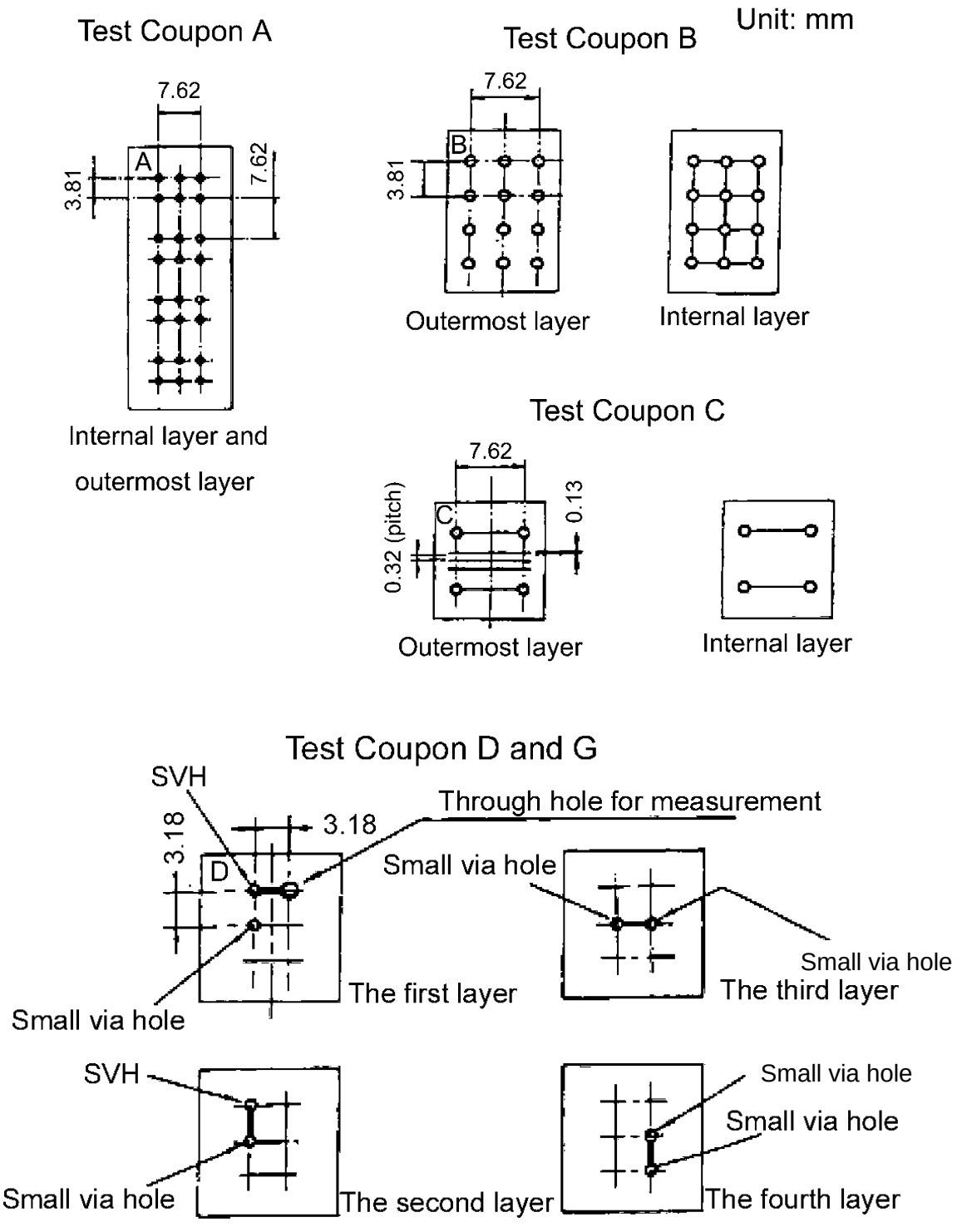
(8) Test coupons K and L shall be prepared, when the corresponding products have SVH. Those coupons are different in the number of layers and via hole structure.
The land shall be formed only on the layers which are connected by SVH.

(9) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. Therefore, the conductors shall be formed on all layers in accordance with this figure.

(10) The arrangement of test coupons shown in this appendix is an example; a different arrangement is also acceptable.

(11) The symbols of test coupons (A to H and J to N) shall be used for identification and not for the object of inspection. The marking method is not specified.

Figure F-10. Test Coupons (for Multilayer Printed Wiring Board) (1/4)



In this figure, the first and the second layers are connected by a SVH.

Figure F-10. Test Coupons (for Multilayer Printed Wiring Board) (2/4)

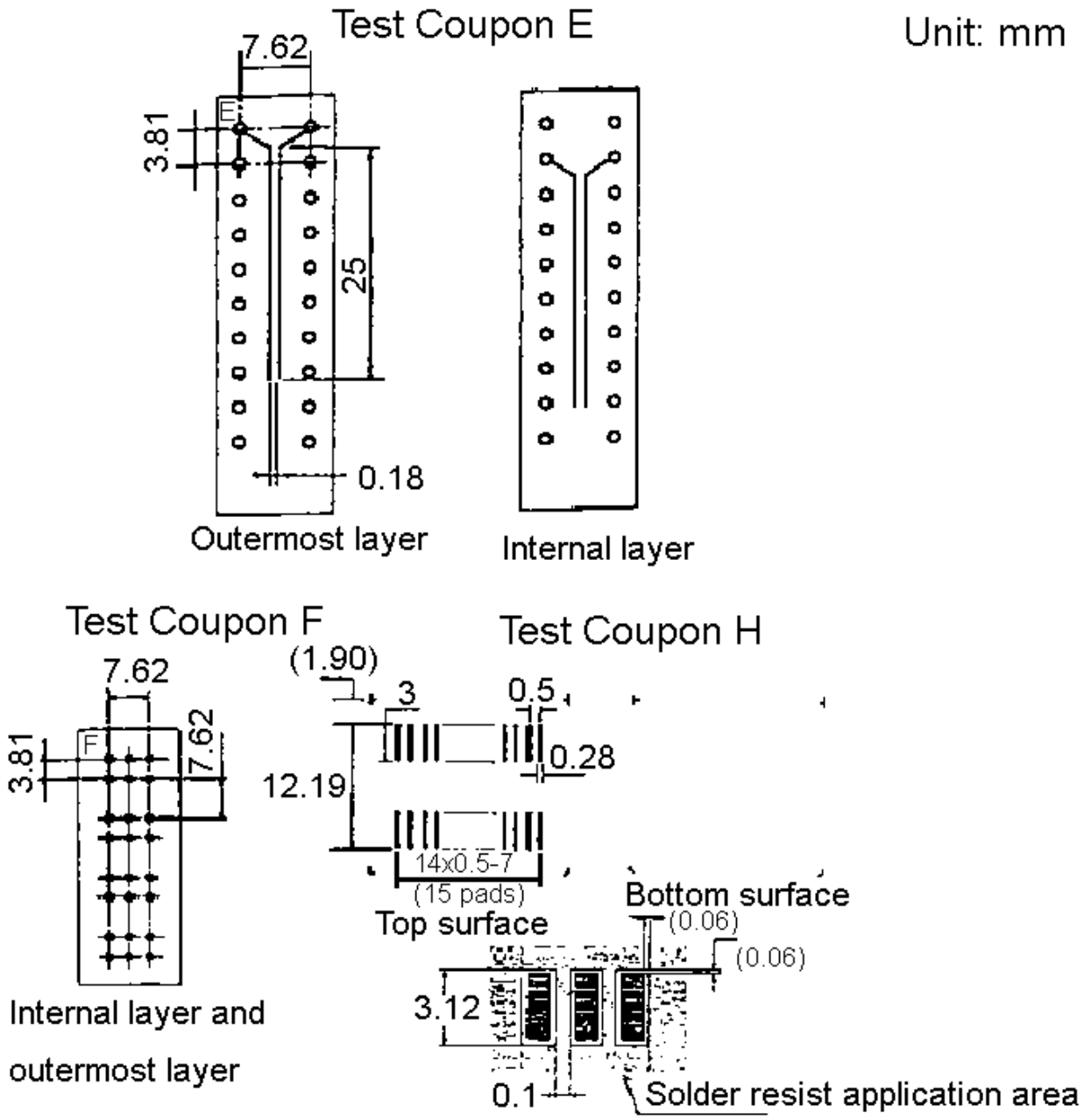
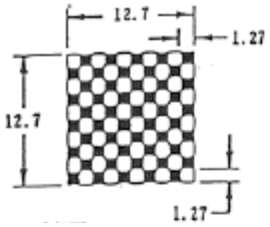
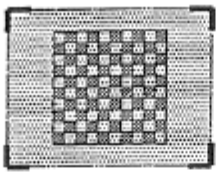


Figure F-10. Test Coupons (for Multilayer Printed Wiring Board) (3/4)

Test coupon J

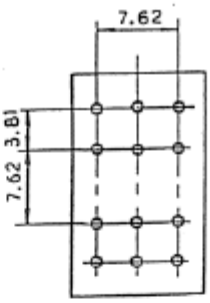


Top and bottom surface

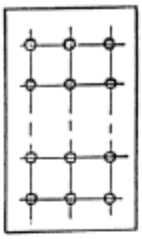


Solder resist application

Test coupon K and L



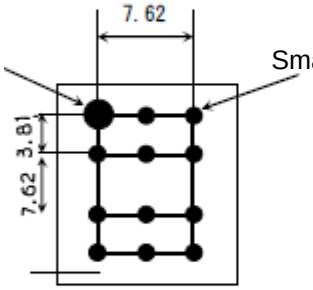
Outermost layer



Internal layer with SVH

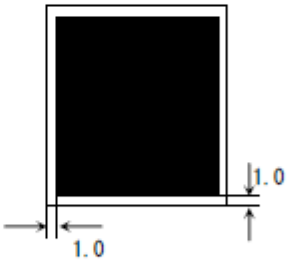
Test coupon M

Through holes for measurement

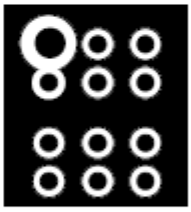


Small via holes

Outermost area

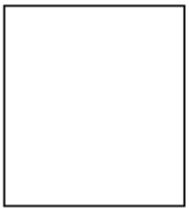


Internal layer (conductor layer)

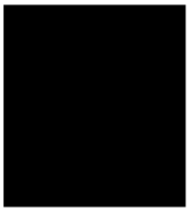


Internal layer with CIC

Test coupon N



Outermost and internal layer



Internal layer with CIC

The conductor does not exist. (Only the CIC does)

Figure F-10. Test Coupons (for Multilayer Printed Wiring Board) (4/4)

Table F-9. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail		
					Samples(1)		Quantity of allowable defects
Group	Order	Test item			Production printed wiring boards	Test coupon (2)	
I	1	Design and construction	F.3.3	F.4.4.2.1	No. 1 to No. 6	A, B, C, D or E, F, G or H, K, L, M and N(4)	0
	2	Externals, dimensions, marking and others Externals and construction Dimensions Marking	F.3.4.1 F.3.4.2 F.3.4.3	F.4.4.2.1			
	3	Workmanship(3)	F.3.5	F.4.4.3			
II	1	Plating adhesion and overhang	F.3.6	F.4.4.4	No. 1 to No. 6	C	
	2	Bow and twist	F.3.5.1	F.4.4.3.1		N/A	
III	1	Through holes	F.3.4.4	F.4.4.2.2	No. 1	A, F and K	
	2	Terminal pull strength	F.3.9.1	F.4.4.7.1		F	
	3	Solder resist thickness	F.3.4.5	F.4.4.2.3		J	
IV	1	Connection resistance	F.3.8.3	F.4.4.6.3	No. 2	D	
	2	Hot oil resistance	F.3.10.3	F.4.4.8.3			
	3	Connection resistance	F.3.8.3	F.4.4.6.3			
V	1	Circuitry	F.3.8.2	F.4.4.6.2	No. 3	E and G(5)	
	2	Connection resistance	F.3.8.3	F.4.4.6.3			
	3	Thermal shock (I)	F.3.10.1.1	F.4.4.8.1 a)			
	4	Circuitry	F.3.8.2	F.4.4.6.2			
	5	Connection resistance	F.3.8.3	F.4.4.6.3			
VI	1	Humidity and insulation resistance	F.3.10.2	F.4.4.8.2	No. 4	E and M	
	2	Dielectric withstanding voltage	F.3.8.1	F.4.4.6.1			
VII	1	Thermal stress	F.3.10.4	F.4.4.8.4	No. 5	A, B and L	
	2	Solderability	F.3.9.2	F.4.4.7.2		B and H(6)	
VIII	1	Thermal expansion coefficient	F.3.10.6	F.4.4.8.6	No. 5	N	
IX	1	Radiation hardness	F.3.10.5	F.4.4.8.5	No.6	N/A	
-	1	Materials	F.3.2	N/A	(7)		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. In order to qualify split boards, split board specimens shall be submitted as the production samples.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) Bow and twist (paragraph F.3.5.1) of the samples shall be tested during the second test of Group II tests.

(4) Group I test shall be performed on the test coupons which are to be provided for Group II through VIII tests. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(5) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(6) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively. The coupon B for the hole solderability test shall be the coupon which has been subjected to the thermal stress test.

(7) Data to certify compliance with design specifications shall be submitted.

F.4.3 Quality Conformance Inspection

F.4.3.1 Quality Conformance Inspection (Group A)

F.4.3.1.1 Sample

The quality conformance inspection shall be performed on all products. Test coupons and sample product shall be manufactured simultaneously.
Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen. A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

F.4.3.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table F-10. The inspections within each group shall be performed in the order listed.
For Group IV and V tests, one test coupon shall be provided for each coupon type specified in Table F-10.

Table F-10. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail		
					Quantity of samples		Quantity of allowable defects
Group	Order	Inspection item			printed wiring boards	Test coupon(1)	
I	1	Externals, dimensions, marking and others Externals and construction Dimensions Marking	F.3.4.1 F.3.4.2 F.3.4.3	F.4.4.2.1	All	N/A	0
	2	Workmanship(2)	F.3.5	F.4.4.3			
II	1	Bow and twist	F.3.5.1	F.4.4.3.1	All	N/A	
III	1	Circuitry	F.3.8.2	F.4.4.6.2	All	N/A	
IV	1	Thermal stress	F.3.10.4	F.4.4.8.4	N/A	A, B and K(3), (4)	
	2	Through holes Conductive interface Plating thickness	F.3.4.4 b) e)	F.4.4.2.2 a) and d) c)		A,F and L (A and F)(3) (4)	
V	1	Solderability	F.3.9.2	F.4.4.7.2	N/A	B and H (A and D)(5)	

Notes:

(1) A letter inside the parentheses shows the test coupon for a single-sided or double-sided printed wiring board, and a letter outside the parentheses shows the test coupon for a multilayer printed wiring board.

(2) Bow and twist (paragraph F.3.5.1) of the samples shall be tested during the first test of Group II tests.

(3) For a multilayer printed wiring board, test coupon A shall be inspected, when the corresponding product is provided with small via holes. Test coupons K and L shall be inspected when the corresponding products have SVH.

(4) For a single-sided or double-sided printed wiring board, test coupon F shall be inspected, only when the corresponding product is provided with small via holes.

(5) Test coupons A and B shall have been subjected to the test for Thermal stress. Also, test coupons A and B shall be subjected to the test for hole solderability, and coupons D and H shall be subjected to the test for surface solderability.

F.4.3.2 Quality Conformance Inspection (Group B)

F.4.3.2.1 Sample

Test coupons for Group B inspection may be manufactured at the same time as those for Group A inspection are manufactured.

F.4.3.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table F-11. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

Table F-11. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	F.3.6	F.4.4.4	C	0
II	1	Terminal pull strength	F.3.9.1	F.4.4.7.1	F	
III	1	Connection resistance	F.3.8.3	F.4.4.6.3		
	2	Hot oil resistance	F.3.10.3	F.4.4.8.3	D	
	3	Connection resistance	F.3.8.3	F.4.4.6.3		
IV	1	Circuitry	F.3.8.2	F.4.4.6.2	E and G(1)	
	2	Connection resistance	F.3.8.3	F.4.4.6.3		
	3	Thermal shock (II)	F.3.10.1.2	F.4.4.8.1 b)		
	4	Circuitry	F.3.8.2	F.4.4.6.2		
	5	Connection resistance	F.3.8.3	F.4.4.6.3		
V	1	Humidity and insulation resistance	F.3.10.2	F.4.4.8.2	E	
	2	Dielectric withstanding voltage	F.3.8.1	F.4.4.6.1		
VI	1	Thermal expansion coefficient	F.3.10.6	F.4.4.8.6	N	

Note: (1) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

F.4.4 Methods for Test and Inspection

F.4.4.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The reference condition shall be performed at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

F.4.4.2 Externals, Dimensions, Marking and Others

F.4.4.2.1 Externals and Construction

Design, construction, externals, dimensions (conductive patterns and edges) and marking of the printed wiring board shall be tested.

a) Conductive patterns and edges
Dimensions of conductive patterns and edges shall be measured using an optical measuring instrument which has sufficient accuracy.

b) Annular ring
The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. Dimensions of annular ring shall be measured using an optical measuring instrument which has sufficient accuracy.

F.4.4.2.2 Through Holes

a) Vertical microsection
The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected for the solder resist thickness and plating integrity (plating voids, internal connection of the vertical side, layer-to-layer registration, base material thickness and plating thickness) at a magnification of 50 to 100X. To inspect the layer-to-layer registration, one of the through holes shall be microsectioned parallel to the length direction of the multilayer board and the other shall be microsectioned perpendicular to the board's length direction.

b) Horizontal microsection
Only multilayer boards shall be subjected to the horizontal microsection inspection. Multilayer boards with through holes shall be encapsulated and polished. A conductor layer shall be polished in the parallel direction. The microsection is prepared to expose the conductor layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X.

c) Plating thickness
The plating thickness shall be measured using microsections prepared in accordance with paragraph F 4.4.2.2 a) at a magnification of minimum 200X. Measurements shall be averaged from three determinations for a plated-through hole. Isolated thick or thin sections shall not be used for averaging.

d) Layer-to-layer registration
The layer-to-layer registration shall be measured at a magnification of 25 to 100X using microsections prepared in accordance with paragraph F.4.4.2.2 a). The misregistration shall be inspected around the hole in the direction parallel

to the board length and the vertical direction. This provision shall not apply to CIC. (See Figure F-11.)

e) Dielectric layer thickness
The dielectric layer thickness shall be measured using microsections prepared in accordance with paragraph F.4.4.2.2 a).

f) Annular ring
The annular ring shall be measured using microsections prepared in accordance with paragraph F.4.4.2.2 a). The measurement of the annular ring on an external layer shall be from the inside surface (within the hole) of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure F-11). The SVH shall not be subjected to the cross-sectional observation. However, they shall be inspected for the annular ring in accordance with paragraph F.4.4.2.1 b).

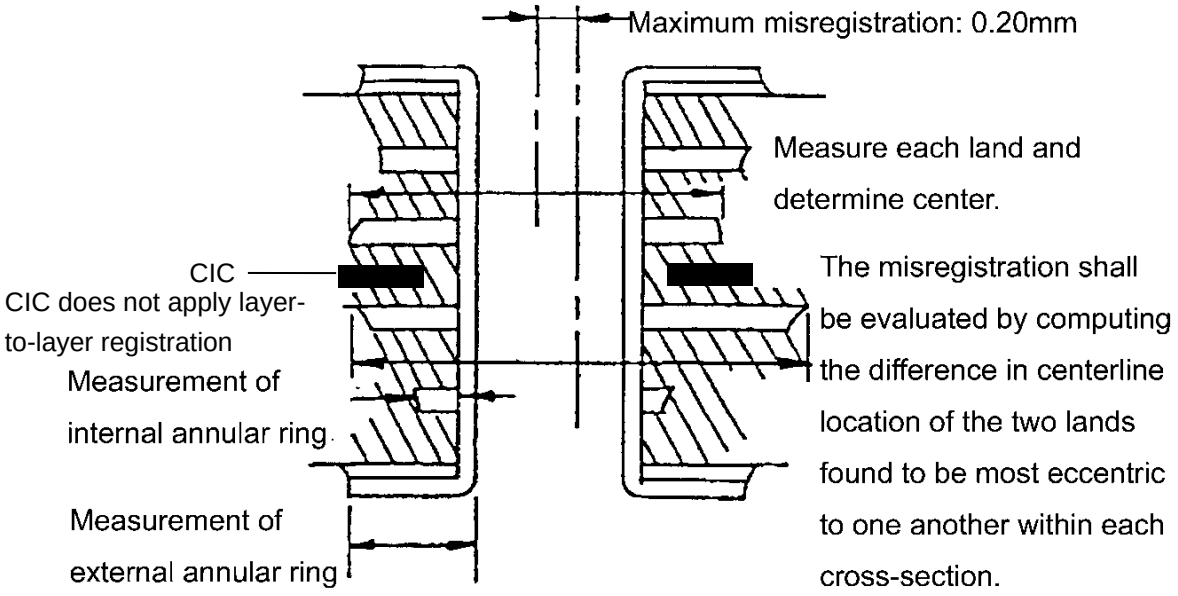


Figure F-11. Measurement of Layer-to-Layer Registration and Annular Ring

F.4.4.2.3 Solder Resist Thickness

The solder resist thickness shall be measured using a microsection prepared in accordance with paragraph F.4.4.2.2 a) at a magnification of minimum 200X.

F.4.4.3 Workmanship

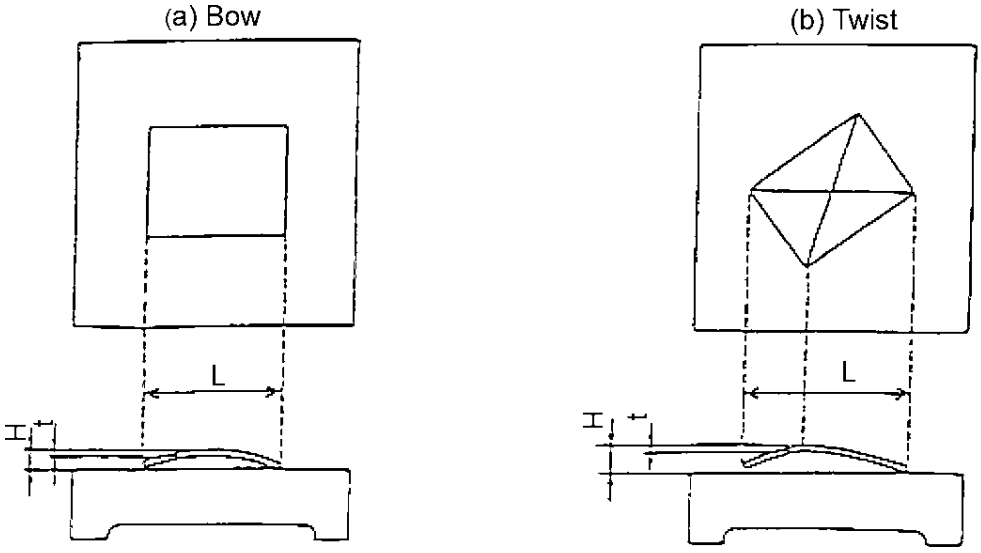
The workmanship shall be inspected visually. The bow and twist shall be inspected as follows.

F.4.4.3.1 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see

Figure F-12). The percent bow and twist shall be calculated by the following formula.

Percent bow and twist = $\frac{H\text{-}t}{L} \times 100$ (%)



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure F-12. Measurement of Bow and Twist

F.4.4.4 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and minimum 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

F.4.4.5 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 percent by volume of isopropyl alcohol and 25 percent by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6 \Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range

and accuracy. The alternate test methods specified in Table F-12 may be used to perform the cleanliness test.

Table F-12. Equivalent Factors

Method	Resistivity ($\times 10^6 \Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.20

Note: (1) Alpha Metals Incorporated, “Omega Meter”

F.4.4.6 Electrical Performance

The electrical performance tests shall be performed as follows.

F.4.4.6.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $1000V_{AC}$ peak or $1000V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer (including CIC).

F.4.4.6.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

F.4.4.6.3 Connection Resistance

The resistance between the through hole terminals shall be measured using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5 mΩ.

F.4.4.7 Mechanical Performance

The mechanical performance tests shall be performed as follows.

F.4.4.7.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at minimum 6mm away from the land, peeled and pulled toward the land, and cut off by applying the sharp knife at the joining point of the conductor and land so as not to degrade the land adherence strength.

Then, a lead wire sufficient in length for installing a tensile tester shall be selected and the following procedure shall be used for soldering and solder removal by using a soldering iron.

a) Solder a lead wire in to the through hole.
b) Remove the lead wire from the through hole (solder removal)
c) Re-solder the lead wire in to the through hole.
d) Remove the lead wire from the through hole (solder removal)
e) Re-solder the lead wire in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the bare minimum.
After the completion of re-soldering in e) above, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Disconnection or the lead wire being pulled out shall not be regarded as a failure, and a new lead wire shall be soldered and pull test shall be performed again. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

F.4.4.7.2 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph F.4.4.8.4.

b) Surface solderability
After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be

permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

F.4.4.8 Environmental Performance

The environmental performance tests shall be performed as follows.

F.4.4.8.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
The test shall be performed under the test condition B. The low temperature shall be –30°C and the time for step 2 and 4 shall be within 2 minutes each. The number of cycle shall be 1000 cycles.

b) Thermal shock (II) (applicable to quality conformance inspection)
The test shall be performed under the test condition F-3. The high temperature shall be +170°C, and the time for step 2 and 4 shall be within 2 minutes each.

F.4.4.8.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers (including CIC) during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

F.4.4.8.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. Immersion and cooling shall be performed for 10 cycles.

F.4.4.8.4 Thermal Stress

The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 percent maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for any crack on the internal copper foil and for laminate voids, and for any connection between internal copper/CIC and through holes using the microsection prepared in accordance with paragraph F.4.4.2.2 a). Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.

F.4.4.8.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraph F.4.4.6.1 and F.4.4.8.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

F.4.4.8.6 Thermal Expansion Coefficient

The test shall be performed in accordance with JIS K 7197 and as follows.

a) Specimen conditioning
   The temperature for the specimen shall be kept between 121 and 149°C for 2 hours. Eliminate any moisture from the specimen and cool it to the room temperature.
b) Specimen dimensions
   The specimen shall be tabular form with 10mm x 10mm x board thickness (mm).
c) Measured temperature range: T_1 = 30°C, T_2 = 180°C
d) Direction of measurement
   The directions of measurement for the specimen shall be 2 directions: the multi-layer board length direction and the vertical direction to the length direction.

APPENDIX G

PRINTED WIRING BOARDS,
AREA ARRAY PACKAGING

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX G

PRINTED WIRING BOARDS, AREA ARRAY PACKAGING

G.1. General

G.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards capable of area packaging design such as BGA (Ball Grid Array) and CGA (Column Grid Array) (hereinafter referred to as "printed wiring boards").

G.1.2 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA([1]) 2140 / G106 GI 14([2])

G106	GI	14([2])
Individual identification	Base material code (G.1.2.1)	Number of layers (G.1.2.2)

Notes:
([1]) "JAXA" indicates the common part for space use and may be abbreviated to “J”.
([2]) Number of conductor layers

G.1.2.1 Base Material Code

The base material code is as specified in Table G-1.

Table G-1. Base Material Code

Base material code	Base material
GF	Glass base woven epoxy resin, compliant to IPC-4101 or JPCA/NASDA-SCL01
GI	Glass base woven polyimide resin, compliant to IPC-4101 or JPCA/NASDA-SCL01

G.1.2.2 Number of Layers

The maximum number of layers shall be specified in each detail specification.

G.2. Applicable Documents etc.

G.2.1 Applicable Documents

The applicable documents shall be as follows and as specified in paragraph 2.1.

a) JERG-0-043 Standards for Surface Mount Soldering Process in Space Application
b) JIS C 6481 Test methods of copper-clad laminates for printed wiring boards
c) IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design

G.2.2 Reference Documents

The reference documents shall be as follows and as specified in paragraph 2.2.

a) JERG-0-054 Standards for BGA/CGA Soldering Process in Space Application
b) JIS C 6012 Qualification and Performance Specification for Rigid Printed Boards

G.3. Requirements

G.3.1 Qualification Coverage

Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs G.3.2 through G.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. If necessary, additional qualification coverage shall be specified in the detail specification.

G.3.2 Materials

The materials shall be specified as follows.

G.3.2.1 Metal-Clad Laminate and Prepreg

The copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings.
The nominal thickness of the base material shall be no less than 0.05mm.
The thickness of the copper foil shall be as specified in Table G-2.

Table G-2. Thickness of Copper Foil (Nominal)

Unit: µm

Layer	Classification	Copper foil thickness
External layer	With SVH	9 minimum
	Without SVH	18 minimum
Internal layer	SVH layer	9 minimum
	Any layer other than SVH layer or a layer without SVH	35 minimum

The thermal expansion coefficient of the board thickness direction (direction Z) of GF shall be less than 50ppm/°C when the test is performed in accordance with JIS C 6481.
The standard applied to the materials used in the printed wiring boards shall be clearly specified in the detail specification. The detailed information about base materials such as type of resin and glass-transition temperature shall be specified in the Application Data Sheet (hereinafter referred to as “ADS”).

G.3.2.2 Via Hole Filling Materials (Filling Resin)

The filling materials for SVH and small through hole shall be resin. The detailed information about the filling materials such as type of resin and glass-transition temperature shall be specified in ADS.

G.3.2.3 Solder Resist Ink

The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent.

G.3.2.4 Marking Ink

The marking shall be conducted using epoxy resin base ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

G.3.2.5 Plating

Electroless and electrolysis plating shall be applied to all through holes and for cap plating. Solder coating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.

G.3.2.5.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating to form a conductive layer over the insulating material.

G.3.2.5.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 %.

G.3.2.5.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table G-3. The electrolytic nickel plating specified in paragraph G.3.2.5.4 shall be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 % except for the metal added to increase the hardness.

Table G-3. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 %
KNOOP hardness	91 to 129 (inclusive)

G.3.2.5.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.

G.3.2.5.5 Solder Coating

The solder used for solder coating shall contain 50 to 70 % tin.

G.3.3 Design and Construction

G.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

G.3.3.2 Connector for Printed Wiring Boards

A direct connector (one-part connector or edge-board connector) shall not be used.

G.3.3.3 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by small via holes, SVH or through holes.

G.3.3.4 Connection Method for BGA Pads

The connection method for contact pads such as BGA pads shall be made by Dog-Bone structure or Via-in-Pad (hereinafter referred to as “VIP”) structure.
Dog-Bone structure is to connect small via hole by drawing the circuit out of the contact pads such as BGA pads as shown in Figure G-1. The small via hole shall be filled with resin and closed by plating (cap plating).
VIP structure is the structure where cap plating as BGA pad is directly on top of the small via hole filled with resin as shown in Figure G-2.

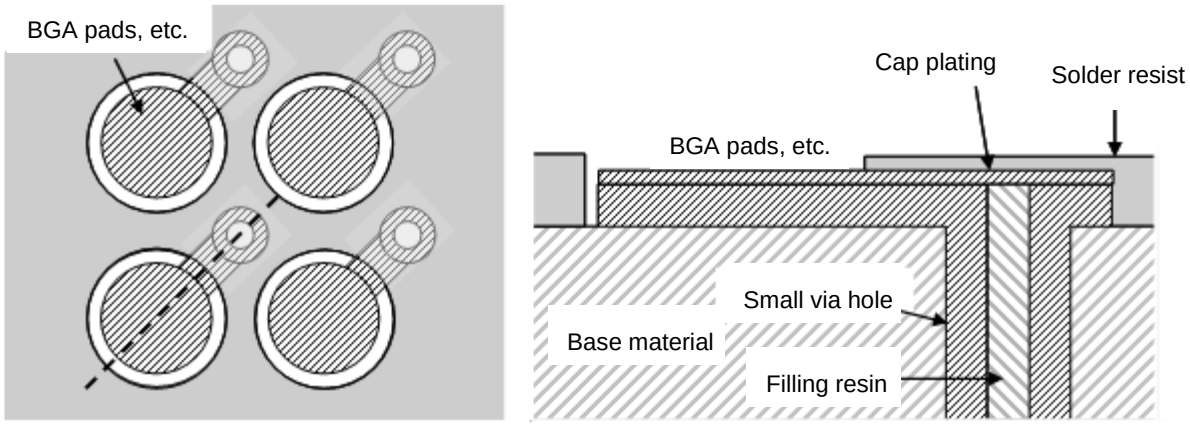


Figure G-1. External and Cross-Section View of Dog-Bone Structure

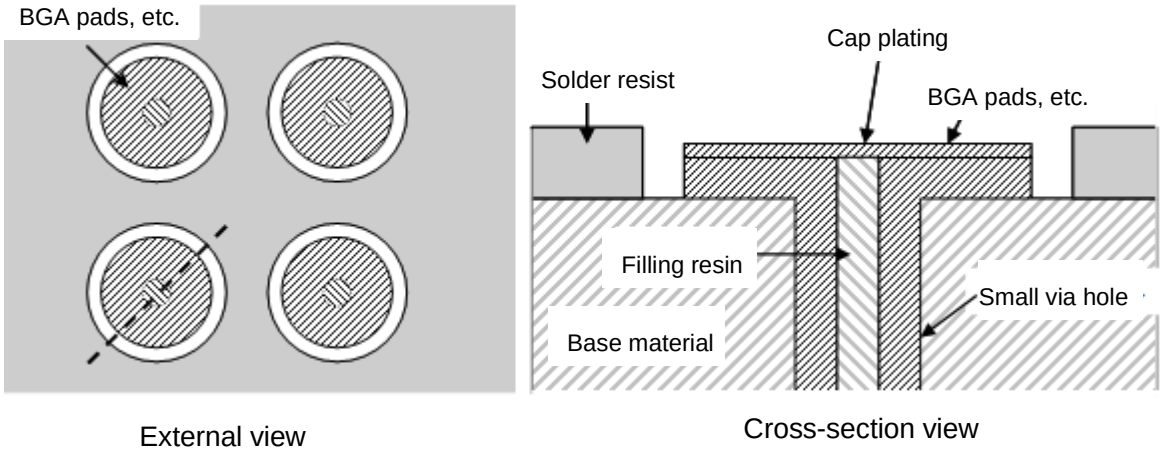


Figure G-2. External and Cross-Section View of Via-in-Pad Structure

G.3.3.5 Through Hole Diameter

The minimum hole diameter for small via hole and SVH shall be φ0.20mm as a drill hole. When the land of via hole is used as BGA pads, etc., the drill hole for via hole shall be φ0.20mm as a maximum.

G.3.3.6 Filling Resin for Through Hole

The small via hole to be filled with via filling materials shall be specified in the production drawing. The small via holes and SVH in VIP structure shall be filled with via filling materials.

G.3.3.7 Conductor Width and Thickness

The minimum design value for conductor width shall be as specified in Table G-4. The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor. Figures G-3, G-4, G-5, and G-6 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this will apply to both internal and external layers of the conductor under vacuum and space environmental conditions. The details shall be specified in IPC-2152.
When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.

Table G-4. Conductor Width (Design Value)

Unit: mm

Layer	Conductor thickness	Minimum conductor width
External	All	0.10
Internal	More than 35μm	0.10
	35μm or less	0.08

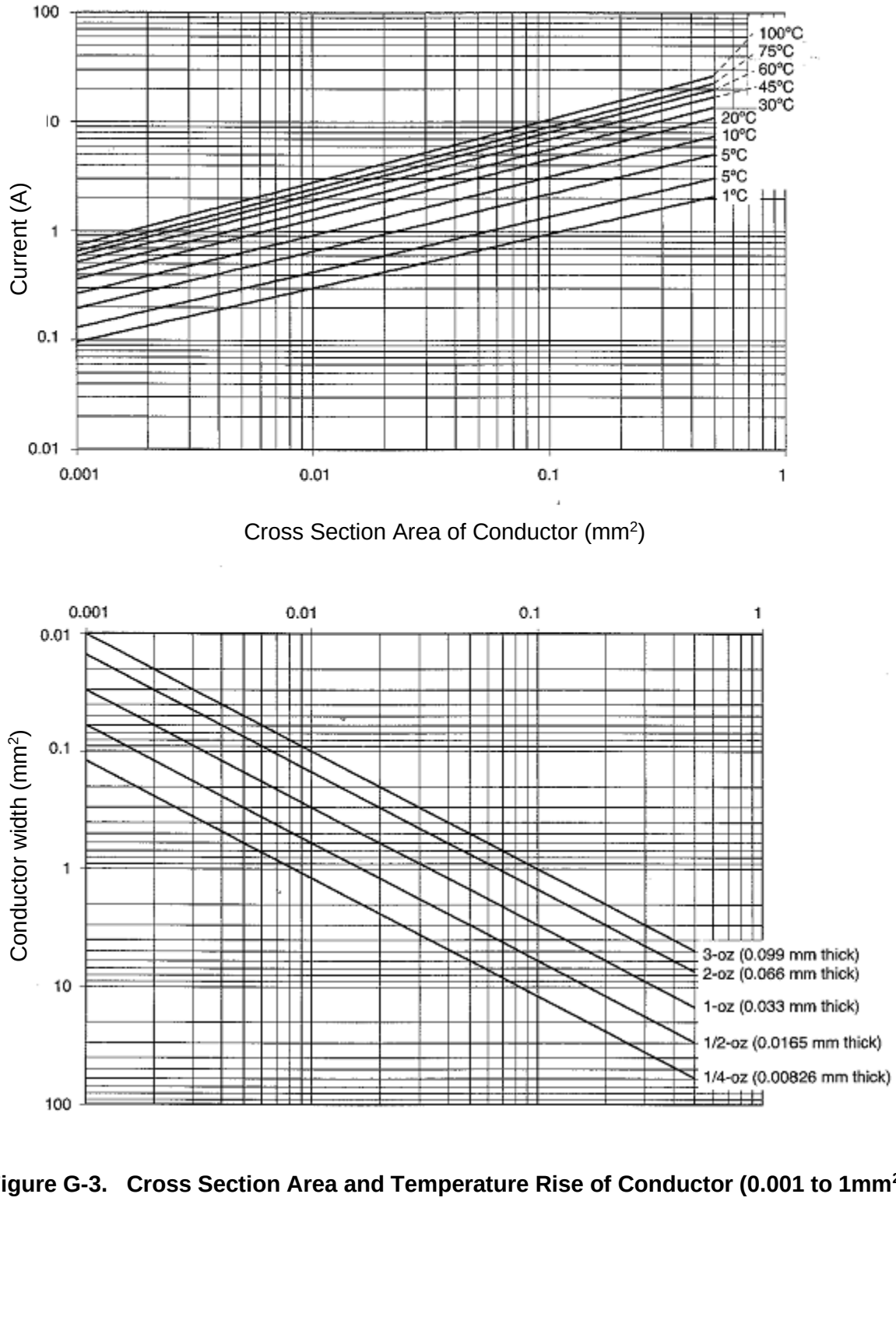


Figure G-3. Cross Section Area and Temperature Rise of Conductor (0.001 to 1mm²)

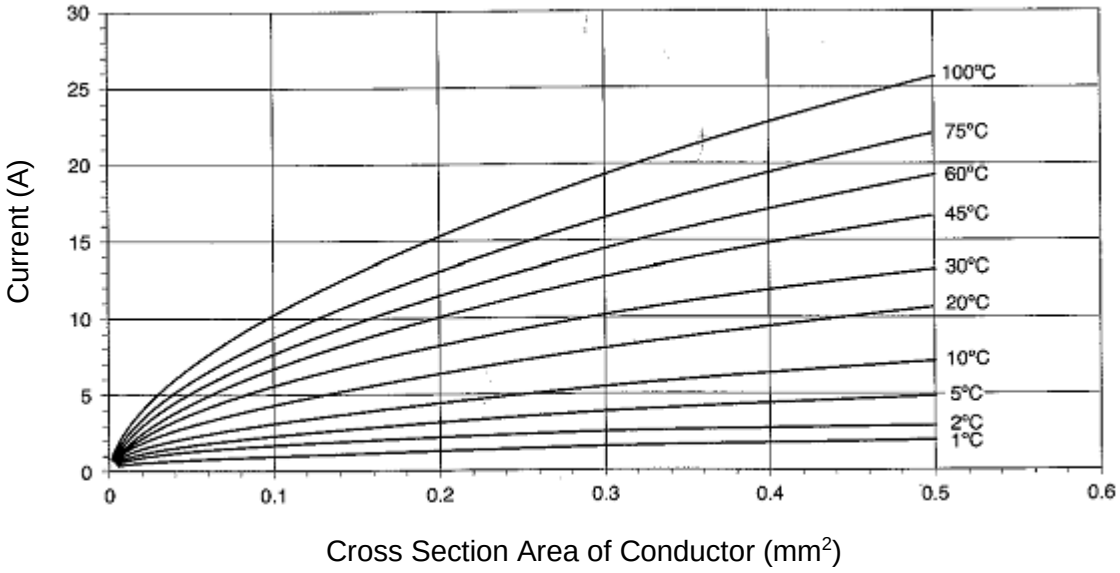


Figure G-4. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.5mm²)

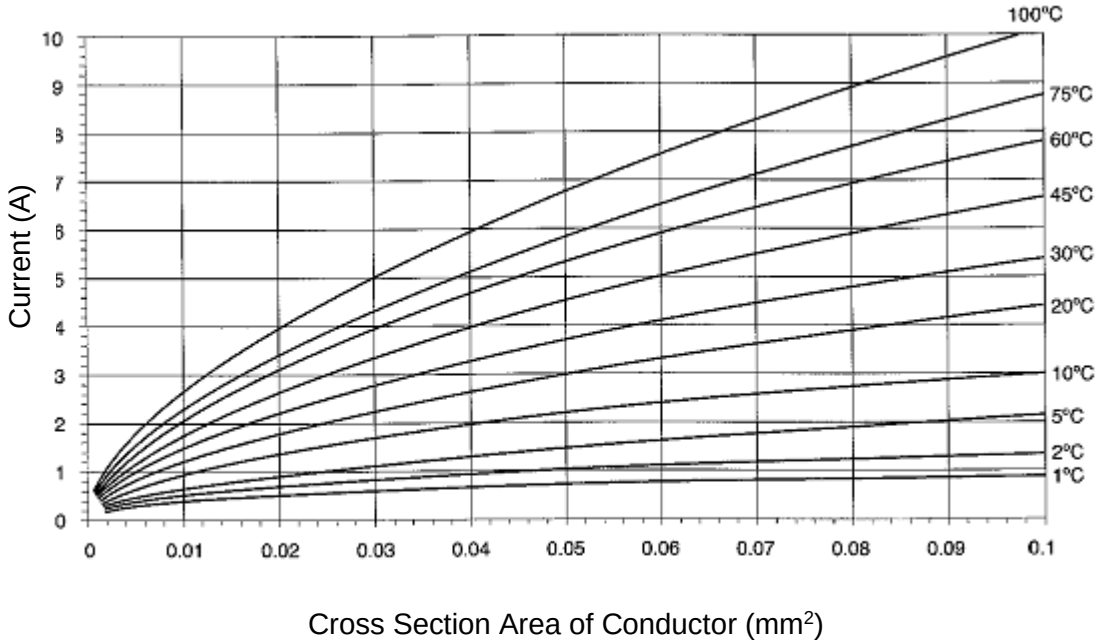


Figure G-5. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.1mm²)

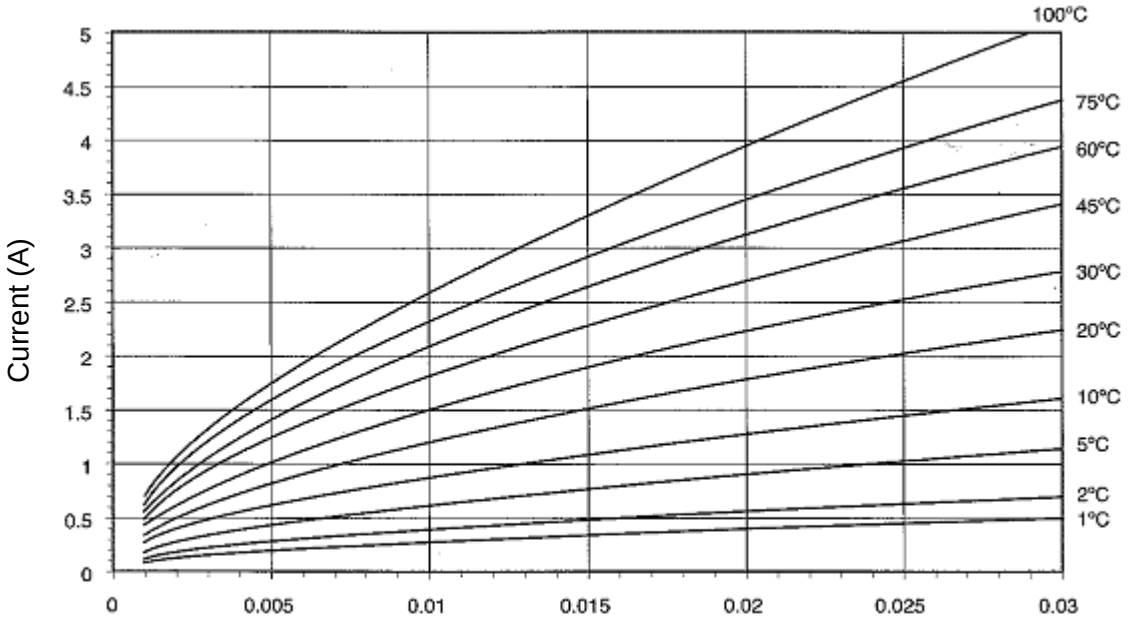


Figure G-6. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.03mm^2)

G.3.3.8 Conductor Spacing

The minimum design value of conductor spacing shall be as specified in Table G-5. The specific conductor spacing shall depend on the voltage applied between conductors as specified in Table G-5.

Table G-5. Conductor Spacing (Design Value)

Unit: mm

Layer	Conductor thickness	Minimum conductor spacing
External	All	0.15
Internal	More than 35μm	0.15
	35μm or less	0.08

Table G-6. Conductor Spacing for Printed Wiring Boards

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	
	External layer	Internal layer
0 to 50	0.15	0.08
51 to 100	0.15	0.10
101 - 300	0.40	0.20
301 - 500	0.80	0.25
501 or higher	(0.003xV)	(0.0025xV)

G.3.3.9 Land Diameter

The minimum design value of land diameter shall be as specified in Table G-7 (see Figure G-7). Non-functional land is not necessary when maintenance of conductor spacing and electrical characteristics requirements are specified.

Table G-7. Land Diameter

Unit: mm

Hole	Minimum land diameter([1])
SVH and small via holes	Drill diameter + 0.25
Plated-through holes except the above	Finished hole diameter + 0.5
Non-plated-through holes	Drill diameter + 1.1

Notes:

([1]) The minimum diameter of lands other than round shaped lands shall be the measure of the length “A” shown in Table G-7.

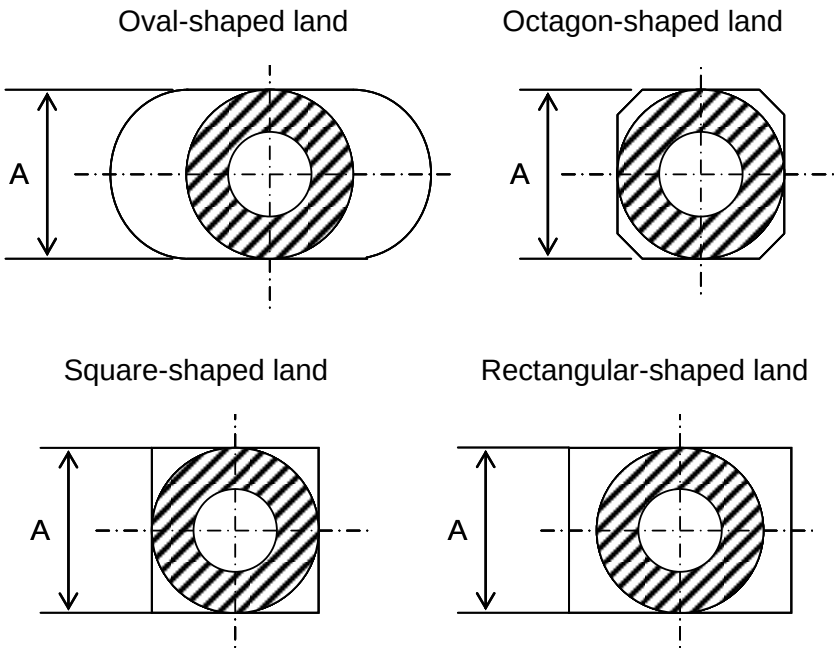


Figure G-7. Measurements of Minimum Diameter of Lands Other than Round Shaped Lands (A)

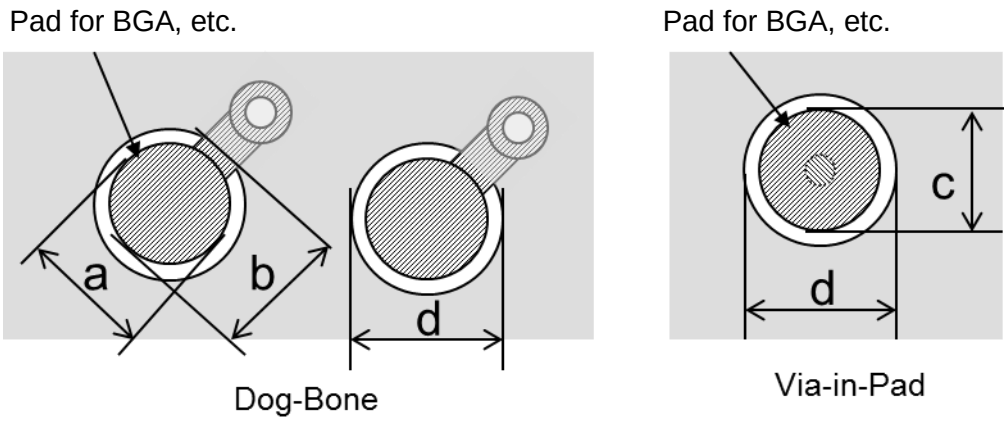
G.3.3.10 Pads for BGA etc.

The sizes of the pads for BGA, etc. for each section shown in Table G-8 shall be specified.

Table G-8. Dimensions of BGA Pads, etc.

Unit: mm

Section		
Pad size (Bottom of conductor)	Dog-Bone	Pad (see Figure G-8 a)
		Fan-out direction (see Figure G-8 b) Fan-out direction
	Via-in-Pad (see Figure G-8 c)	
Size of solder resist opening (Resist surface)	Dog-Bone (see Figure G-8 d)	
	Via-in-Pad (see Figure G-8 d)	
Total board thickness	Total board thickness including conductor and solder resist thickness	

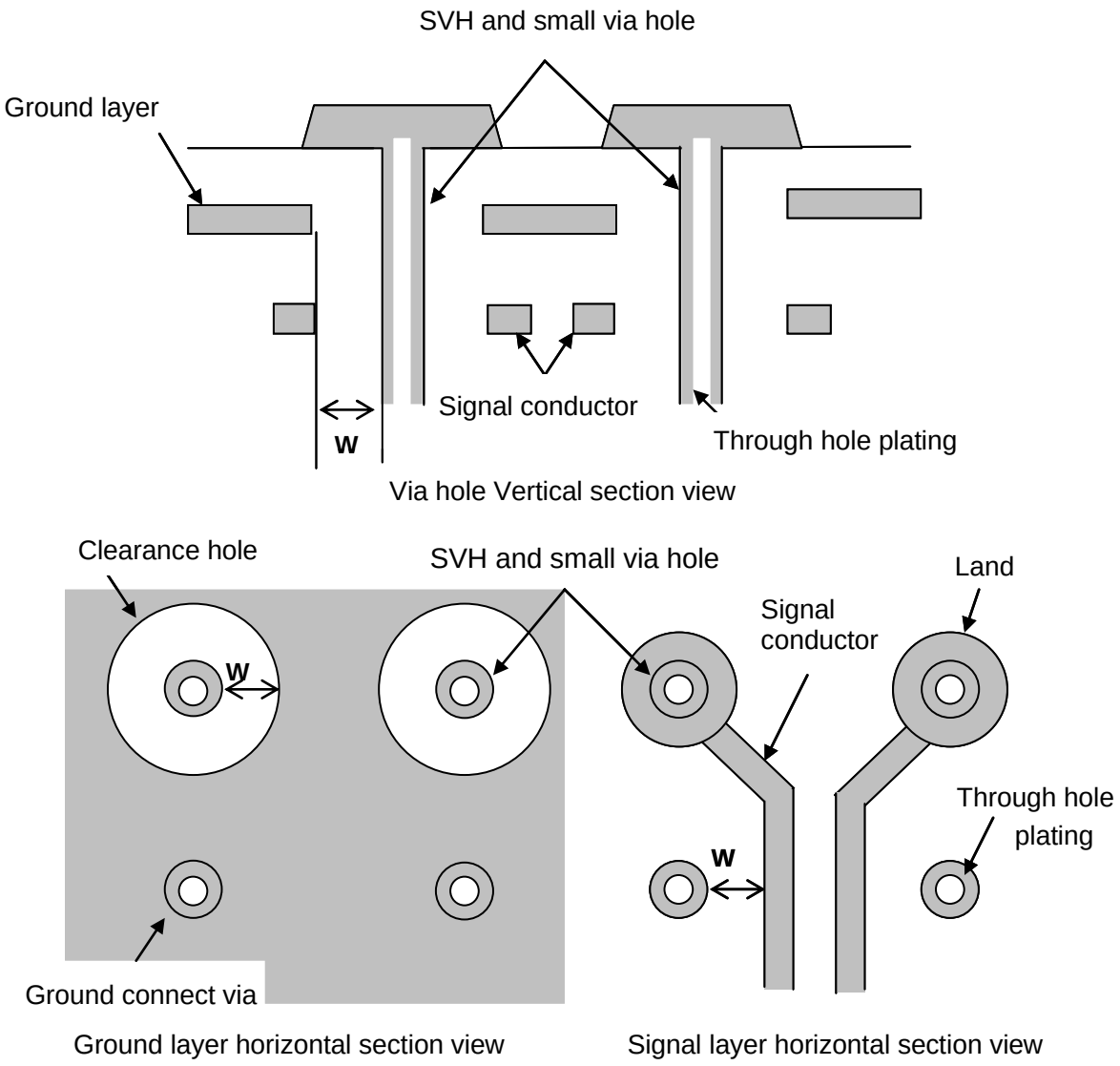


a: Pad size in Dog-bone structure b: Fan-out pad size c: Pad size in Via-in-Pad
d: Size of solder resist opening

Figure G-8. Measurements of Pads for BGA, etc.

G.3.3.11 Internal Layer Clearance

The distance (internal layer clearance) from the SVH and small via hole to the hole wall of the conductor nearby shall be as specified in Figure G-9.



W= Internal layer clearance ≥ 0.28mm

Figure G-9. Cross Section View of Via Holes

G.3.3.12 Surface Finish Plating

The thickness of the surface finish plating and solder coating specified in the manufacturing drawing shall be in accordance with Table G-9. The electrolytic Nickel plating shall be applied as an undercoat of electrolytic gold plating, and shall not be used for the surface finish. If more strict requirements than the ones specified in Table G-9 are necessary, consult with manufacturer and specify on the manufacturing drawing.

Table G-9. Thickness of Surface Finish Plating

Unit: μm

Plating material	Surface plating thickness
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	5 as a minimum
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (paragraph G.3.10.2).

G.3.3.13 Solder Resist

The solder resist application shall be specified except for the land, pads (incl. Via-in-Pad), and the small via holes without resin filling.
The lands of small via hole and SVH in the dog-bone structure shall be coated with solder resist.
Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.
The minimum distance from the edge of the board to the solder resist shall be 0.3mm.

G.3.3.14 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph G.3.11.1.2) and within -65 to +125°C.

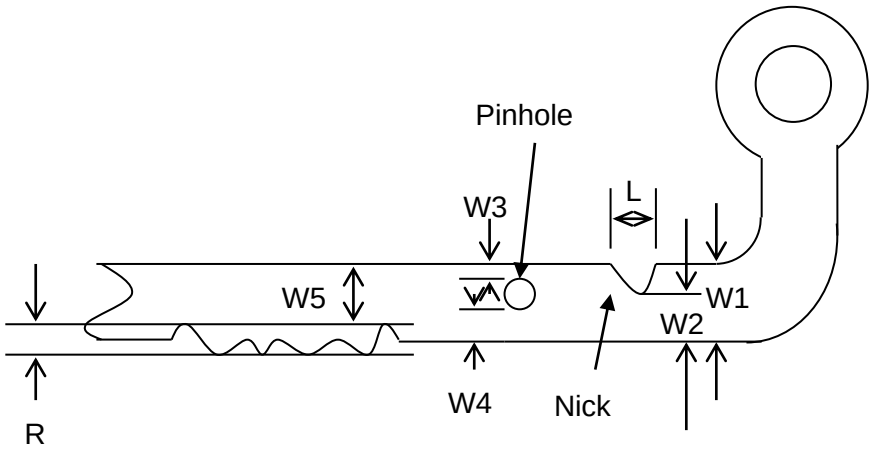
G.3.4 Externals, Dimensions, Marking and Others

G.3.4.1 Externals of Conductor, Base Material and Solder Resist

G.3.4.1.1 Conductor

a) Conductive pattern
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor
The conductors shall contain no tears or cracks. Any combination of edge roughness, nicks, pinholes or scratches exposing the insulation board shall not reduce the conductor width to less than 80 % of the minimum finished conductor width. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall not be more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall meet the conductor width tolerance (see Figure G-10).
The tolerances of conductor width and conductor spacing shall be as specified in Table G-10.
The nicks and pinholes on the ground surface and power supply surface shall not exceed 1.0mm in the maximum length and 4 pieces per 625cm^2 in number.



W1 ≥ (Minimum finished conductor width)
W2 ≥ 0.80 × (Minimum finished conductor width)
W3 + W4 ≥ 0.80 ×Minimum finished conductor width)
W5 + R ≥ Conductor width tolerance ≥ W5-R
L = Length of defect

Figure G-10. Passing Criteria for Conductor Defects

Table G-10. Tolerance of Conductor Width and Conductor Spacing

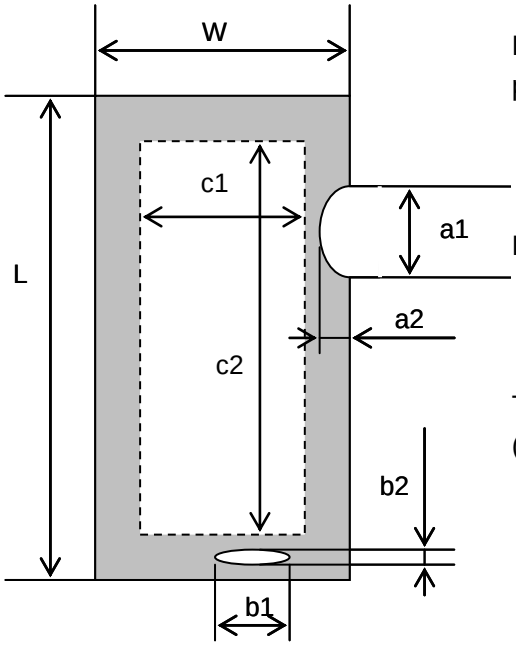
Unit: mm

Dimension		Tolerance
Conductor width	0.08 to less than 0.13	+0.05 -0.03
	0.13 to less than 0.20	±0.05
	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
Conductor spacing	Less than 0.10	0.05 as a minimum
	0.10 to less than 0.14	0.06 as a minimum
	0.14 and more	0.10 as a minimum
	The positive side tolerance is not specified for all design value.	

c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure G-11).

The pad length and width shall be based on the design value.



Defects along the external edge of the pad
a1 ≤ L X 0.2
a2 ≤ W X 0.2

Defects inside the pad
b1 ≤ L X 0.1
b2 ≤ W X 0.1

The area where no defect is allowed (from the center of the pad)
c1 = W X 0.8
c2 = L X 0.8

Figure G-11. Passing Criteria for Defects on the Rectangular Surface Mount Pad

d) Mounting Pad for BGA, etc.
The defects such as nicks, dent and pinholes along the edge of the pad shall not exceed 10% of the diameter of the pad expanding in a radial direction of the land center. The defects inside the pad shall not exceed 20% of the circumference of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center of the pad diameter to the 80% of the pad (see Figure G-12).
The pad diameter shall be based on the design value.

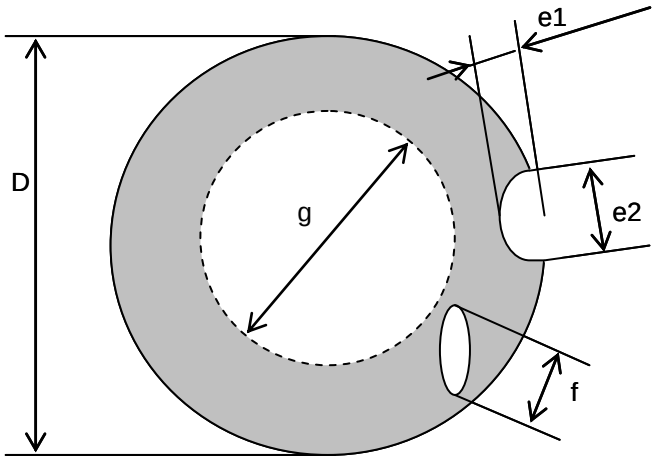


Figure G-12. Passing Criteria for Defects on the Mount Pad

e) Probe mark from Electrical test
The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

f) Dielectric layer between conductor layers
The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.

g) Solder coating
The solder coating shall be free from pinholes or pits, and completely cover conductive patterns.

h) Electrolytic nickel and electrolytic gold plating
The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on the conductor side is permitted.

G.3.4.1.2 Base Materials

a) Edges of printed wiring board
Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board. Crazing along the edges of printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

b) Surface of printed wiring boards
The surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall not be permitted.

G.3.4.1.3 Solder Resist

a) The cured solder resist shall be free from tackiness, blistering and delamination.
b) Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted.
c) Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist.
d) The solder resist shall not encroach onto lands for mounting parts.
e) The application range and misalignment of solder resist and conductive patterns shall meet the provisions of manufacturing drawings.
f) Unless otherwise specified on the manufacturing drawings, adjacent conductor shall not be exposed in the solder resist opening area.
g) In the Dog-Bone structure, solder resist shall completely cover the land of small via hole and SVH.

G.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table G-11.

Table G-11. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
Outline dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

G.3.4.2.1 Dimensions of BGA Pads, etc.

Unless otherwise specified, the dimension tolerance for BGA pads, etc. shall be in accordance with the requirements specified in Table G-12.

Table G-12. Dimensions for BGA Pads, etc.

Unit. (mm)

Item			Tolerance
Pad size (conductor bottom size)	Dog-Bone	Pad (Figure G-8 a)	±0.05
		Fan-out direction (Figure G-8 b)	±0.075
	Via-in-Pad (Figure G-8 c)		±0.05
Solder resist opening diameter (resist surface)	Dog-Bone (Figure G-8 d)		±0.05
	Via-in-Pad (Figure G-8 d)		±0.05
Accurate alignment	Length of row of BGA pads		±0.05
Pad thickness (conductor thickness)			±0.01
Total board thickness (incl. solder resist)			±8%
Co-planarity (flatness): Normal state			0.05mm or less for diagonal diameter of BGA pads

G.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph G.3.2.4, by copper etching or laser marking. The marking shall remain legible and shall not adversely affect any function, performance or reliability of printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

G.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

G.3.4.4 Structural Integrity

G.3.4.4.1 Through Holes

When printed wiring boards are tested as specified in paragraph G.4.5.5.1, the following requirements shall be satisfied (see Figure G-13).

a) Plating of through holes, small via holes and SVH shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land.
b) Protrusion of plating caused by burr and nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings.
c) Partial pits of plating shall not exceed 10% of the plating thickness specified in paragraph G.3.4.4.6.
d) Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80μm, and the resin recession on any side of the plated-through hole does not exceed 40 % of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.
e) The pits of plating caused by negative etchback shall be permitted, provided that the negative etchback satisfies the requirements specified in paragraph G.3.4.4.5.

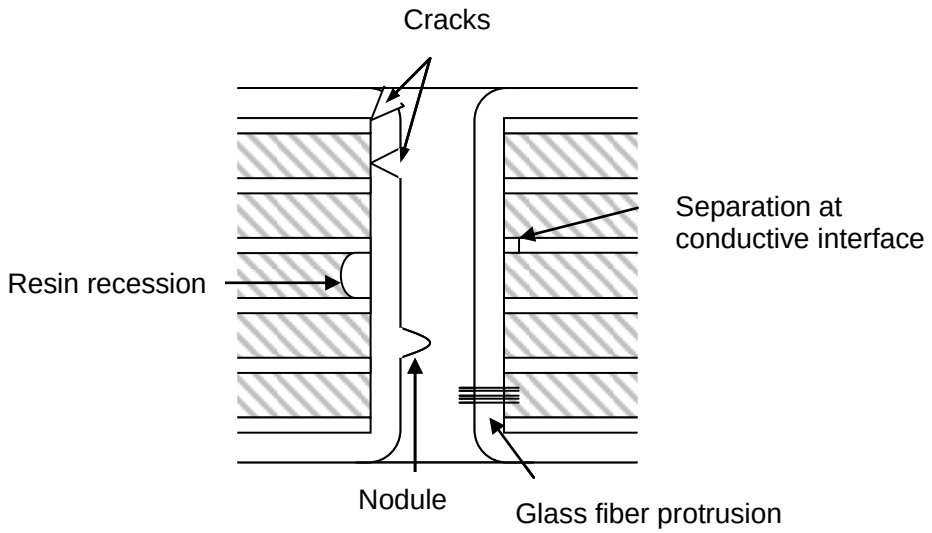


Figure G-13. Through Hole Defects

G.3.4.4.2 Voids

There shall not be any plating voids or laminate voids (see Figure G-14).

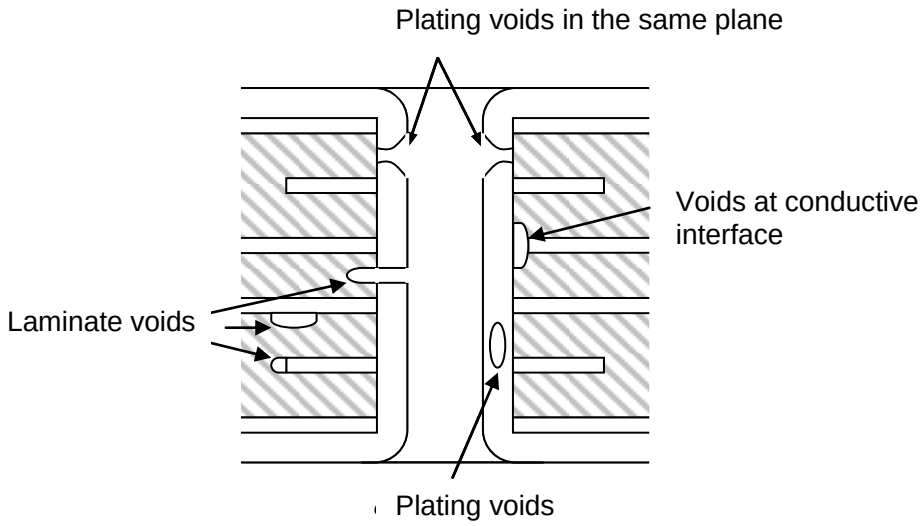


Figure G-14. Voids

G.3.4.4.3 Separation of Lands

Separation of lands shall not be permitted.

G.3.4.4.4 Cracks on Copper Foil

There shall not be any cracks on the copper foil in the external and internal layers.

G.3.4.4.5 Conductive interface

The resin smear at the interface of the through hole wall plating and an internal conductor layer shall not be permitted. Nail heading of a conductor layer shall not exceed 50 % of the metal foil thickness (see Figure G-15). Internal layer negative etchback shall not exceed 13µm.

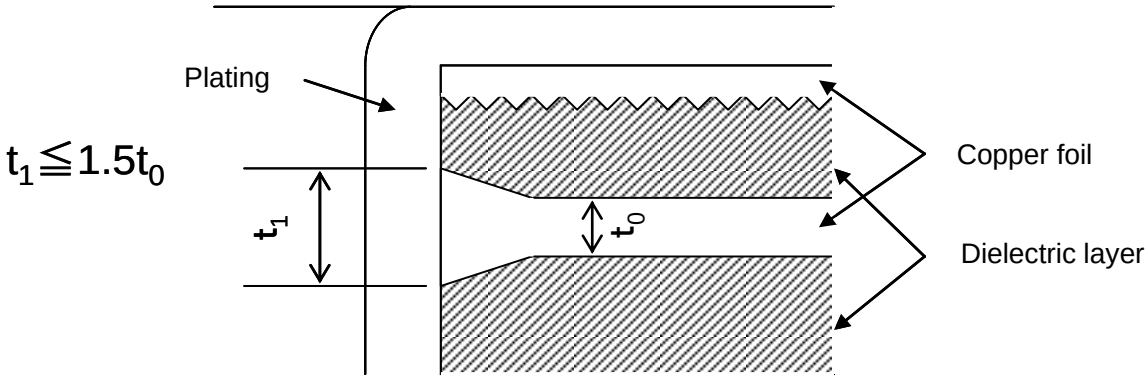


Figure G-15. Nail Heading

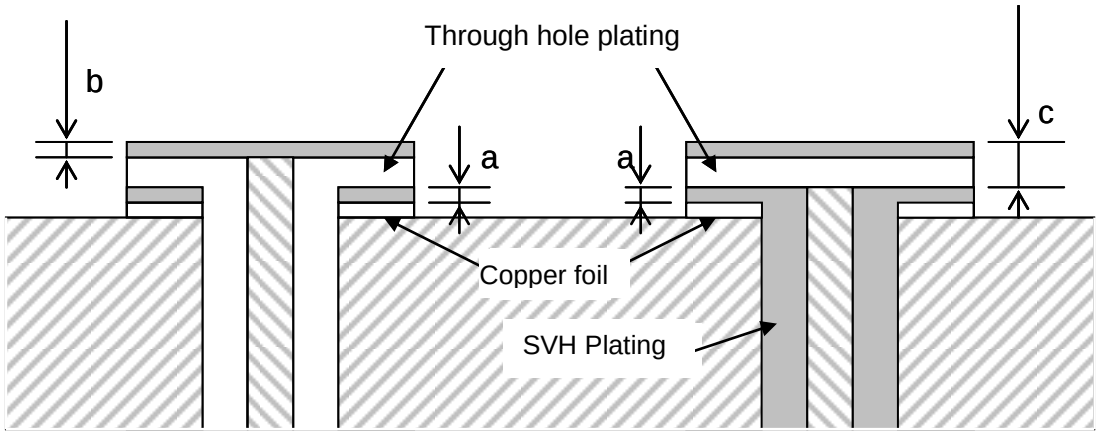
G.3.4.4.6 Plating thickness

Unless otherwise specified, the plating thickness and solder coating thickness shall meet the requirements specified in Table G-13.

Table G-13. Thickness of Plating and Solder Coating

Unit: μm

Type	Surface and through hole wall thickness		
Electroless copper plating	Thickness necessary and sufficient for electrolytic copper plating in the subsequent process		
Electrolytic copper plating	Via hole for part mount		25 as a minimum
	Small via hole		25 as a minimum
	SVH		30 as a minimum
	SVH plating on land (Figure G-16 a)		5 as a minimum
	Cap plating	Small via hole (Figure G-16 b)	As specified in detail specification
		SVH (Figure G-16 c)	As specified in detail specification
Electrolytic gold plating	1.3 to 4.0		
Electrolytic nickel plating	5 as a minimum		
Solder coating	Thickness is not specified. However, the requirements of Solderability (paragraph G.3.10.2) shall be satisfied.		



a: SVH plating thickness on lands
b: Cap plating thickness on small via hole
c: Cap plating on SVH

Figure G-16. Cap Plating Thickness

G.3.4.4.7 Laminate Cracks

Cracks on laminate shall not be permitted.

G.3.4.4.8 Delamination and Blister

Delamination and blister shall not be permitted.

G.3.4.4.9 Layer-to-layer Registraion

The layer-to-layer registration error shall not exceed 0.15mm.

G.3.4.4.10 Annular Ring

The minimum annular ring of internal and external layer shall meet the requirements specified in Table G-14.

Table G-14. Annular Ring

Unit: mm

Through hole type	Layer	Annular ring
Through hole	External	0.05
	Internal	0.025
Non-through hole	External	0.38

G.3.4.4.11 Dielectric Layer Thickness

The dielectric layer between conductor layers of a multilayer printed wiring board shall not be less than 0.08mm in thickness.

G.3.4.4.12 Adhesion between Cap Plating and Filled Resin

When the cap plating is used as BGA pad, the gap between cap plating and filled resin shall be less than 5μm. When the cap plating is not used as BGA pad, the requirements specified in paragraph G.3.4.4.13 shall be satisfied (see Figure G-17).

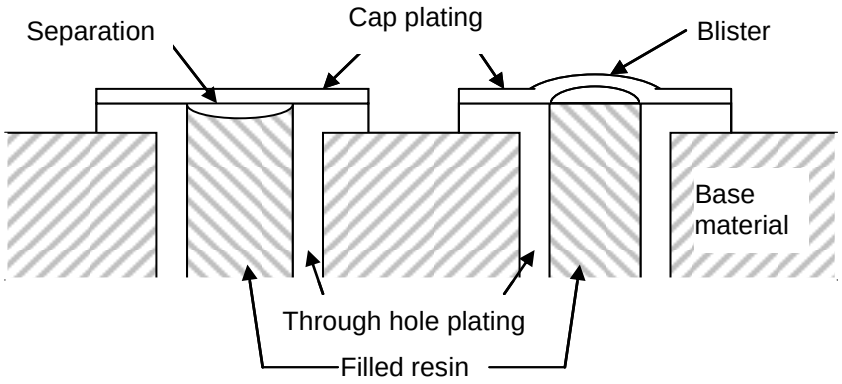


Figure G-17. Adhesion between Cap Plating and Filled Resin

G.3.4.4.13 Protrusion and Pit of Cap Plating

When the surface of the land where the resin wasn't filled underneath is used as a reference, the protrusion and pit of the filled resin shall not be more than 50µm and 76µm, respectively (see Figure G-18).

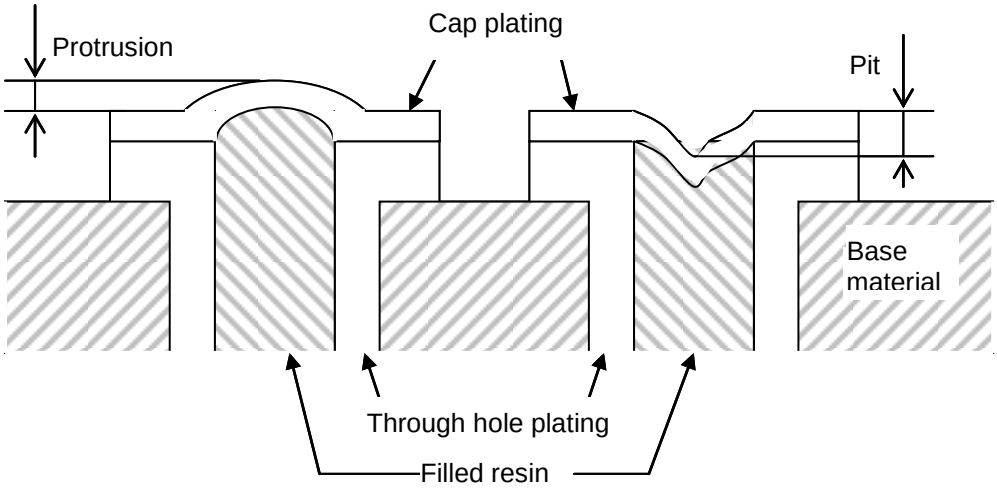


Figure G-18. Protrusion and Pit of Cap Plating

G.3.4.4.14 Filling of Resin

The resin shall be filled a minimum of 90% of the hole volume. The pit of the surface shall satisfy the requirements specified in paragraph G.3.4.4.13 (see Figure G-19).

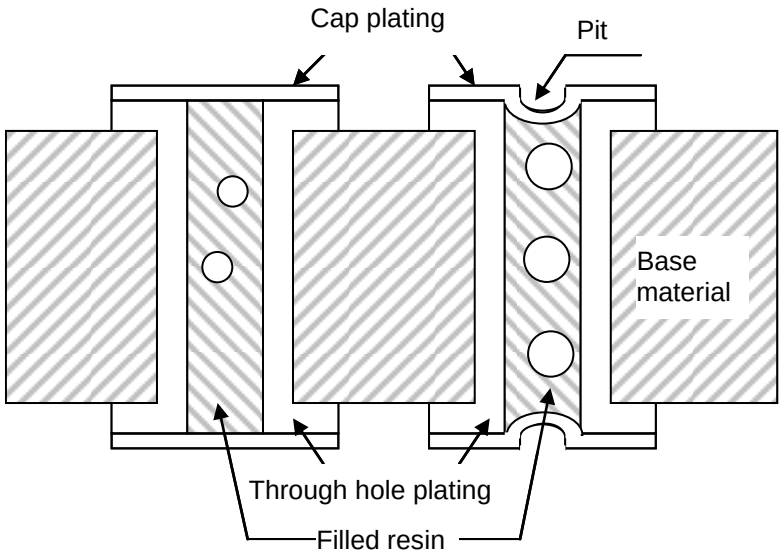


Figure G-19. Filling of Resin

G.3.4.5 Solder Resist Thickness

When printed wiring boards are tested as specified in paragraph G.4.5.6, the solder resist thickness shall not be less than 17.5μm, measured at the center of conductors.

G.3.5 Bow and Twist

When printed wiring boards are tested as specified in paragraph G.4.5.7, the maximum limit for bow and twist shall be 0.5%, unless otherwise specified on manufacturing drawings. For a split board, the percent bow and twist shall not exceed the value specified above, before separation.

G.3.6 Workmanship

The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could adversely affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

G.3.6.1 Repair

The insulating plates, BGA conductor pads or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted, provided that the repaired solder resist thickness shall not be more than the surrounding solder resist thickness.

G.3.7 Plating Adhesion and Overhang

When printed wiring boards are tested as specified in paragraph G.4.5.9, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

G.3.8 Cleanliness

When printed wiring boards are tested as specified in paragraph G.4.5.10, the resistivity of the solvent extract shall not be less than $2x10^6 \Omega \cdot cm$.

G.3.9 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

G.3.9.1 Dielectric Withstanding Voltage

When tested as specified in paragraph G.4.5.11.1, printed wiring boards shall not exhibit insulation breakdown, flashover or sparkover.

G.3.9.2 Circuitry

When tested as specified in paragraph G.4.5.11.2, printed wiring boards shall not exhibit open circuit or short-circuiting between circuit patterns.

G.3.9.3 Connection Resistance

When printed wiring boards are tested as specified in paragraph G.4.5.11.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \cdot t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

G.3.10 Mechanical Performance

Printed wiring boards shall meet the following mechanical requirements.

G.3.10.1 Terminal Pull Strength

When tested as specified in paragraph G.4.5.12.1, printed wiring boards shall meet the following requirements. This provision shall not apply to SVH or small via holes.

a) Bond strength
The land shall withstand a minimum of 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph G.4.5.4.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with paragraph G.4.5.5, there shall be no cracks, blistering, measling or delamination.

G.3.10.2 Solderability

When tested as specified in paragraph G.4.5.12.2, printed wiring boards shall meet the following requirements.

a) Through hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to SVH or small via holes.

b) Surface solderability
A minimum of 95 % of the surface conductor area shall be covered uniformly with fresh solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area.

G.3.11 Environmental Performance

Printed wiring boards shall meet the following environmental requirements.

G.3.11.1 Thermal Shock

G.3.11.1.1 Thermal Shock (I) (applicable to qualification test)

When printed wiring boards are tested as specified in paragraph G.4.5.13.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph G.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

G.3.11.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed wiring boards are tested as specified in paragraph G.4.5.13.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph G.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

G.3.11.2 Humidity and Insulation Resistance

When printed wiring boards are tested as specified in paragraph G.4.5.13.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall not be less than 500MΩ.

G.3.11.3 Hot Oil Resistance

When printed wiring boards are tested as specified in paragraph G.4.5.13.3, the change in connection resistance between circuits before and after the test shall be less than 10%.

G.3.11.4 Thermal Stress

When tested as specified in paragraph G.4.5.13.4, printed wiring boards shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Structural Integrity
In the vertical microsection of through holes, the following requirements shall be satisfied.

1) Through hole
There shall be no corner cracks or barrel cracks.

2) Laminate void
When the conductor spacing on the same plane or between layers satisfies the minimum conductor spacing specified in the manufacturing drawings, the spacing shall not exceed 76µm.

3) Lifting of lands
Lifting of lands after thermal stress test shall be permitted.

4) Cracks on copper foil
There shall be no cracks which penetrate through the copper foil.

5) Internal layer connection
There shall be no separation between copper foil of internal layer and through hole plating.

6) Laminate Cracks
After the thermal stress test, the laminate cracks between the lands of a through holes or on the lands shall not exceed 80µm, and the laminate cracks other than the ones on the land area shall not cause the spacing between adjacent conductors fall below the minimum conductor spacing.

7) Delamination and blister
There shall be no delamination and blisters.

8) Adhesion of cap plating and filled resin
The interface between cap plating and filled resin shall meet the requirements specified in paragraph G.3.4.4.12.

G.3.11.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph G.4.5.13.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall not be less than 500MΩ. After the test, the requirements specified in paragraph G.3.9.1 shall be satisfied.

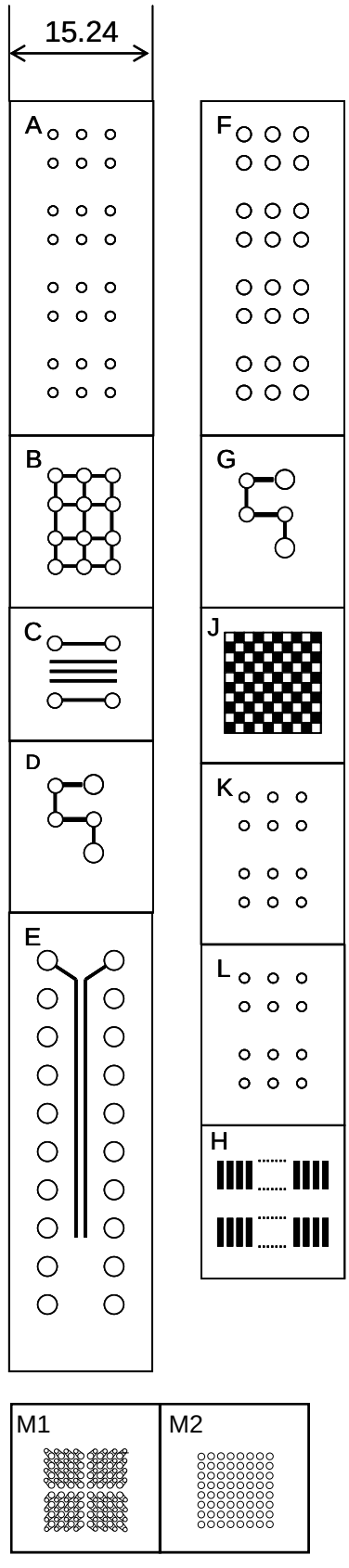
G.4. Quality Assurance Provisions

G.4.1 Test Pattern

The test pattern provided for qualification test and quality conformance inspection shall be in accordance with Figure G-20. The test pattern shall have the same structure as the product produced from the identical work board.
A set of the test pattern shall be assigned for each printed wiring board.

Arrangement of test pattern

Unit: mm



Notes

(1) Unless otherwise specified, the conductor width shall be 0.5±0.1mm.

(2) Test coupon A indicates the minimum hole diameter of the through hole (incl. small via hole) for the corresponding printed wiring board, and the land diameter shall be the minimum land diameter of the through holes. When applied, small via holes shall be filled with resin. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes and diameter shall be 0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(4) The patterns of test coupons D and G vary depending on the number of layers and via hole structure. Each coupon shall be produced so as to form the same number of layers and via hole structure as those of the corresponding product, and to have a circuit continuity through all layers by via holes. The hole and land diameter shall be the minimum diameter for each SVH and small via hole of the corresponding products, and the land shape shall be the typical land shape of the products. On both ends of the printed wiring board, through holes shall be formed to measure the resistance, the diameter of the land and hole shall be ϕ1.8mm and ϕ0.8mm, respectively. The hole diameter tolerance is not specified.

(5) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist shall be the clearance diameter for the corresponding printed wiring board. If the hole diameter for the product is unknown, the land diameter shall be equal to the land diameter + 0.2mm.

(6) Test coupons K and L shall be prepared only when the corresponding products have SVH. Those coupons vary depending on the number of layers and via hole structure. The land shall be formed only on the layers which are connected by SVH.

(7) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. The conductors shall be formed on all layers in accordance with this figure.

(8) The arrangement of test coupons shown in this figure is an example; a different arrangement is also acceptable.

(9) The symbols of test coupons (A to H and J to M2) shall be used for identification and not for the object of inspection. The marking method is not specified.

(10) Only when the BGA pads, etc. are required, the test coupon M1 (Dog-bone structure) or test coupon M2 (VIP structure) in accordance with the pad structure. A example of test coupons M1 and M2 is shown to the left. See detail specification for the more detailed information.

Figure G-20. Test Coupon (1/8)

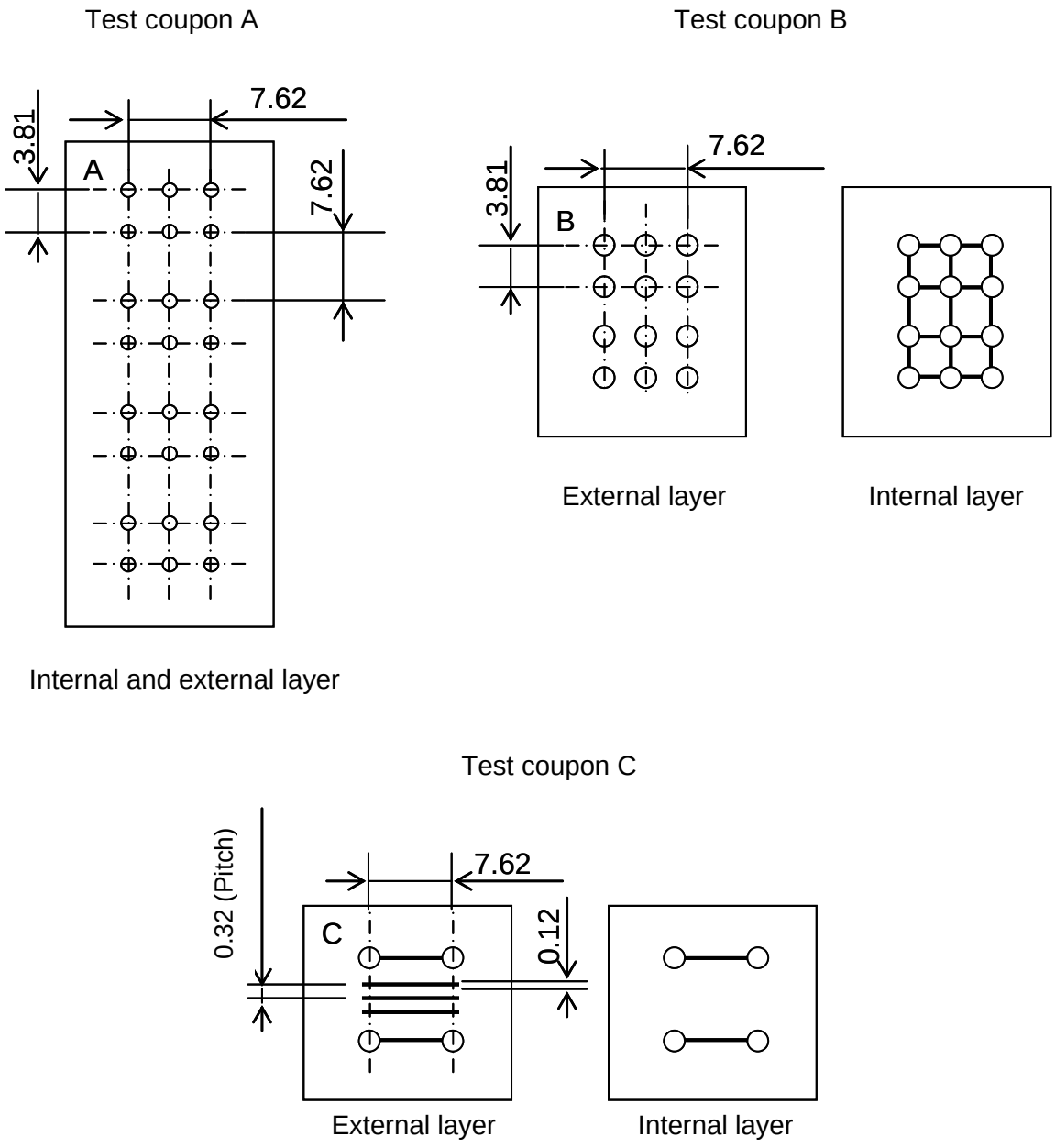
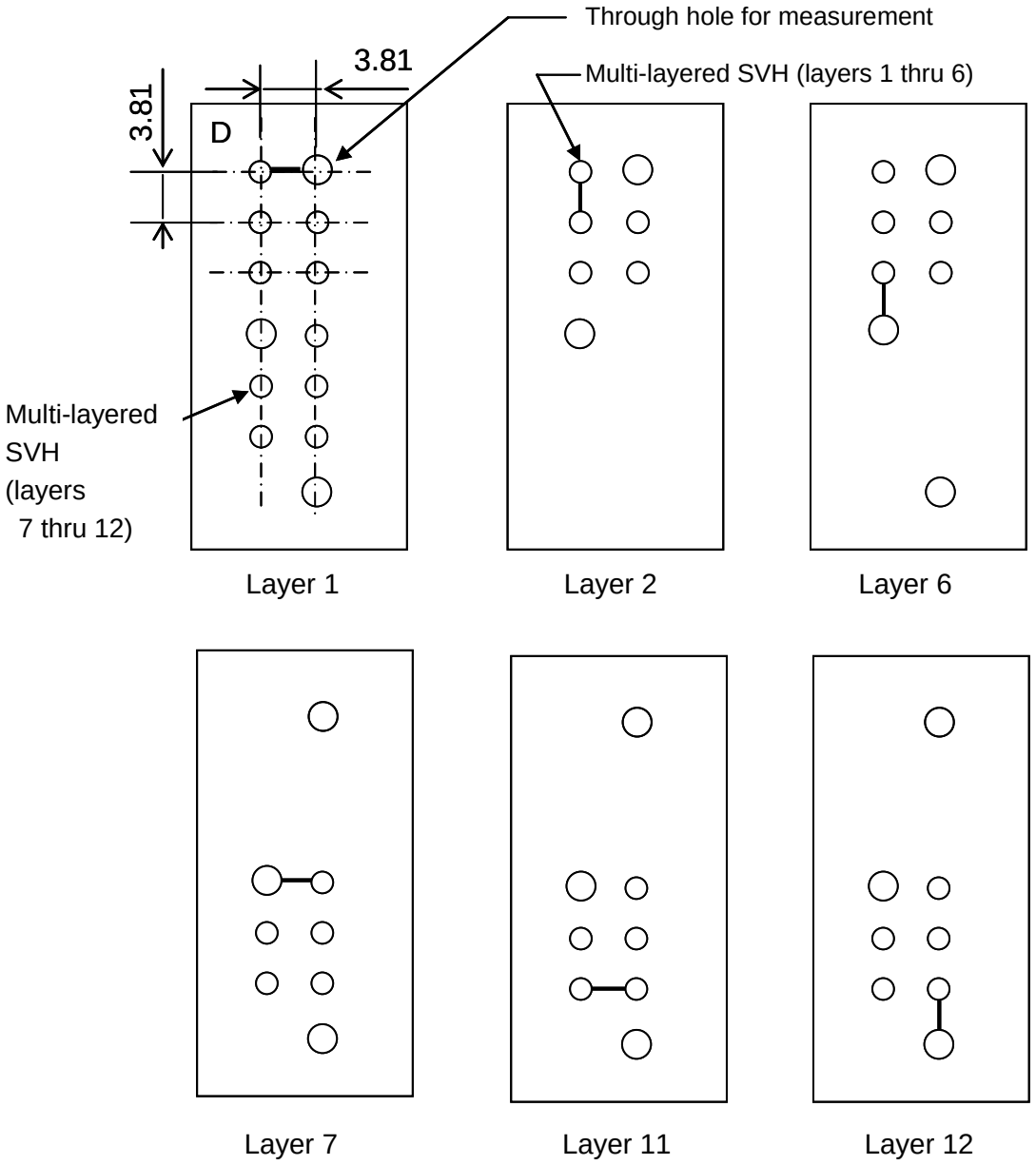


Figure G-20. Test Coupon (Multi-layer Boards) (2/8)

Test coupon D and G

Unit: mm

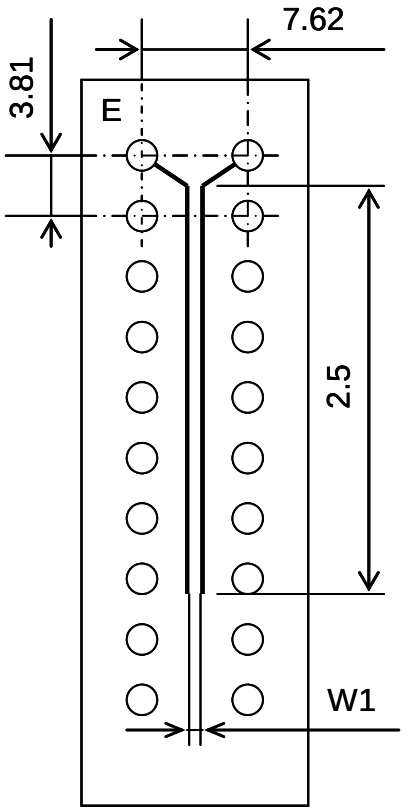


This figure shows an example of layers 1 through 6 and 7 through 12 of SVH.

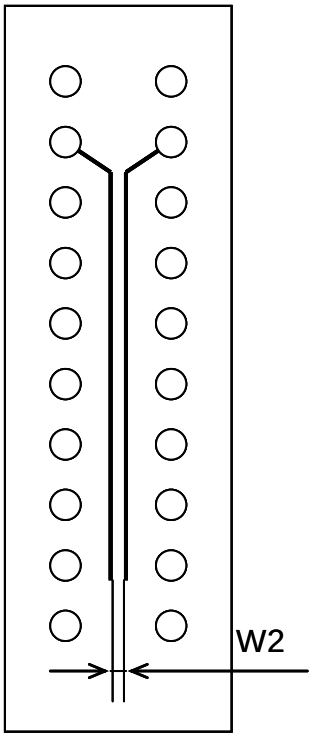
Figure G-20. Test Coupon (Multi-layer Boards) (3/8)

Unit: mm

Test coupon E

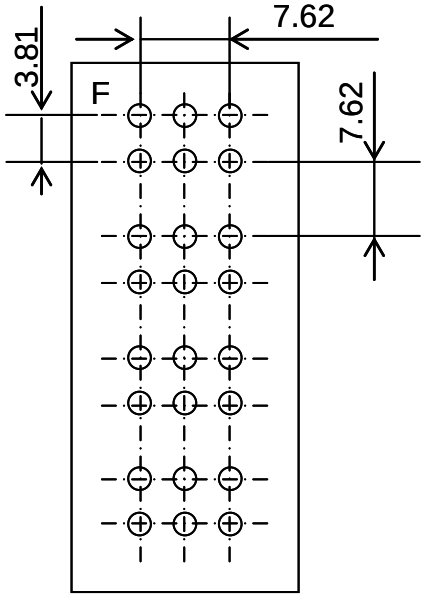


Layer 1



Layer 2

Test coupon F



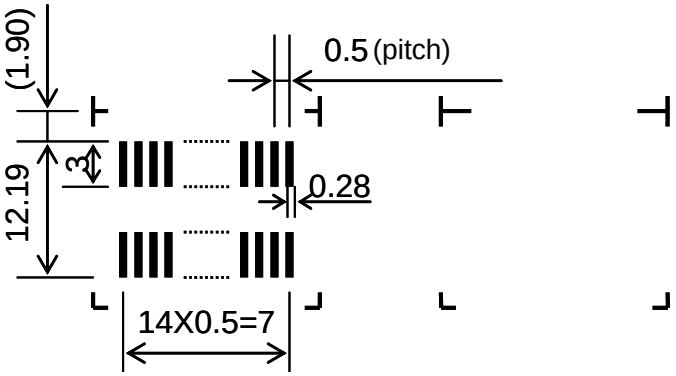
External and Internal layer

W1: Minimum conductor spacing on the external layer of the product or 0.15mm
W2: Minimum conductor spacing on the internal layer of the product or 0.08mm

Figure G-20. Test Coupon (Multi-layer Boards) (4/8)

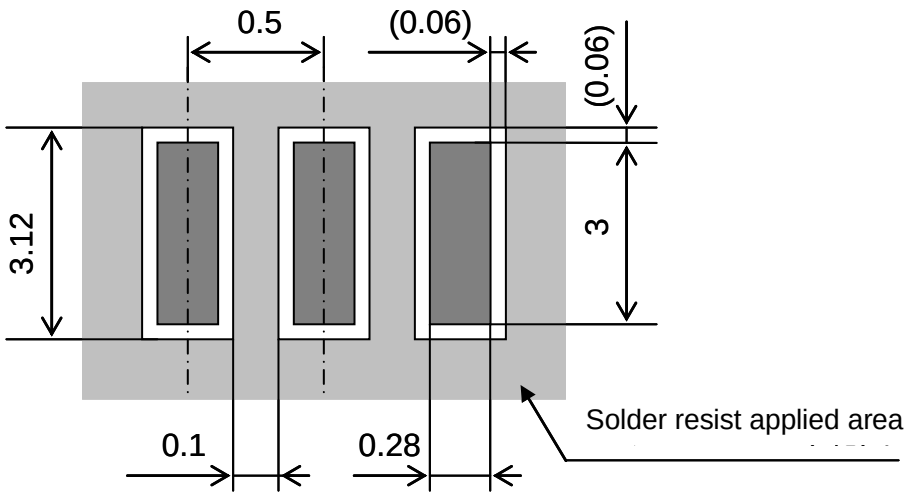
Test coupon H

Unit: mm



Number of pads: 15
(in this range)

Top surface Bottom surface (no pattern)

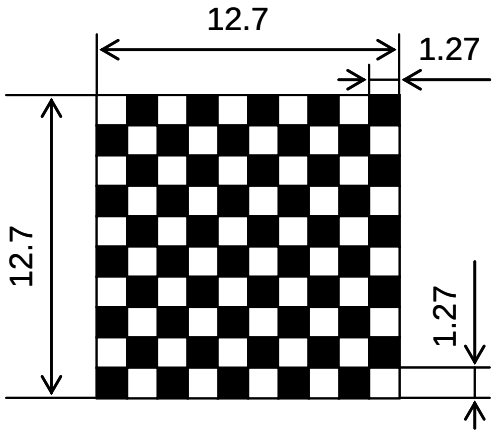


Enlarged view of pad area

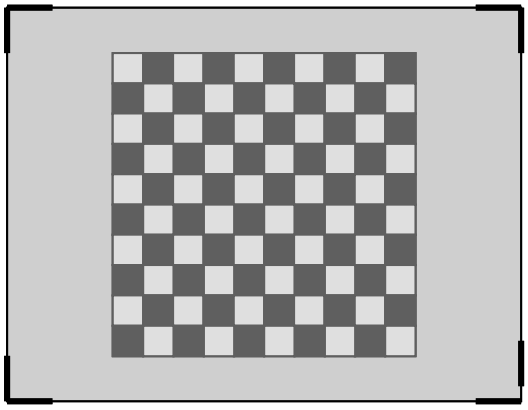
Figure G-20. Test Coupon (Multi-layer Boards) (5/8)

Test coupon J

Unit: mm

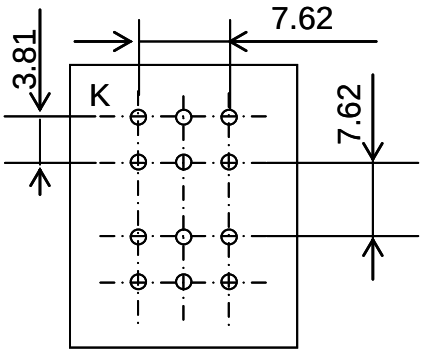


Top and bottom surface

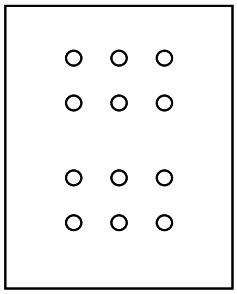


Solder resist applied area

Test coupons K and L



External layer

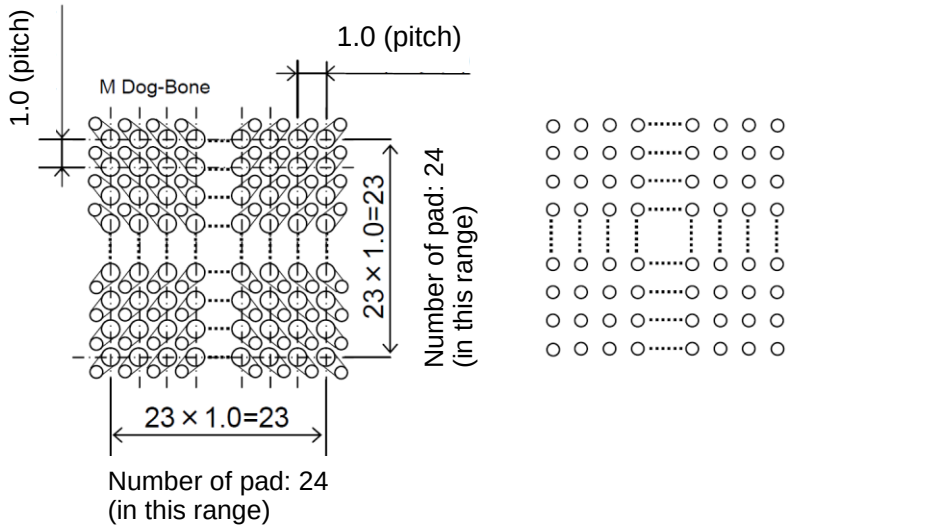


Internal layer (SVH layer)

Figure G-20. Test Coupon (Multi-layer Boards) (6/8)

Test coupon M1 (Dog-Bone structure)

Unit: mm



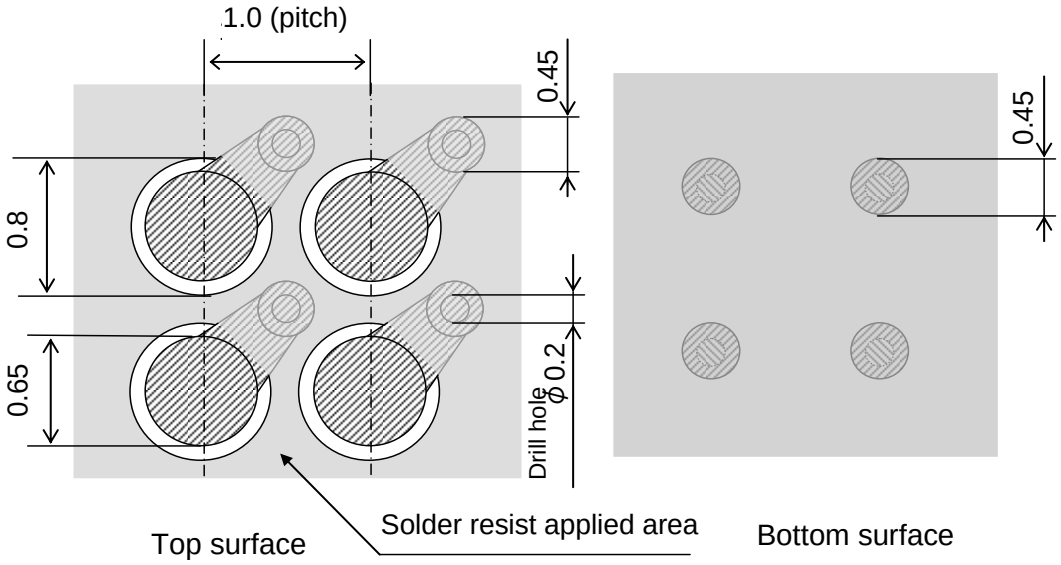


Figure G-20. Test Coupon (Example of BGA pads) (7/8)

Test coupon M2 (VIP structure)

Unit: mm

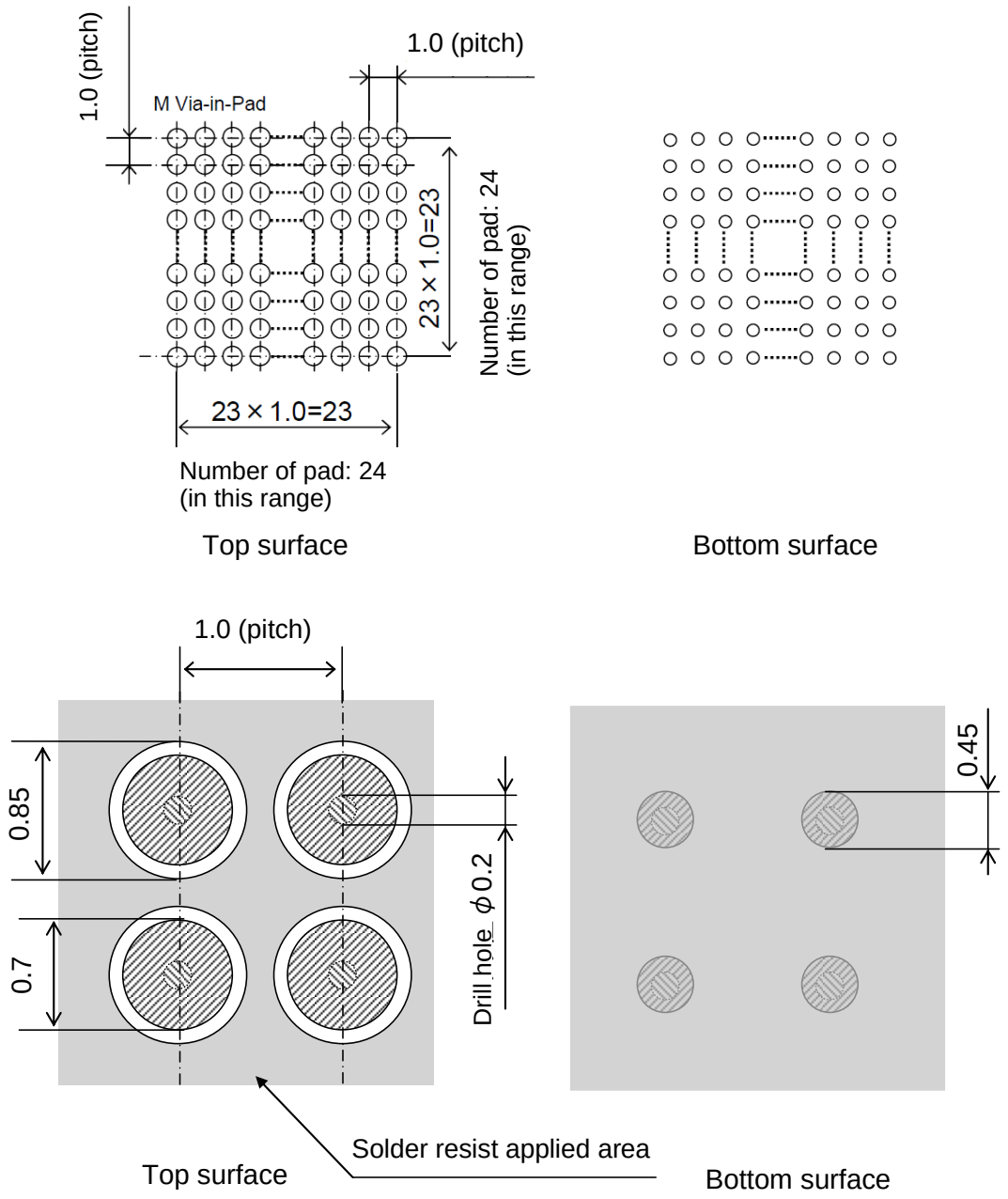


Figure G-20. Test Coupon (Example of BGA pads) (8/8)

G.4.2 In-Process Inspection

The in-process inspection specified in Table G-15 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs G.3.4.1 (Externals of Conductor, Base Material and Solder Resist), G.3.4.2 (Dimensions), G.3.4.3 (Marking), G.3.8 (Cleanliness), and G.3.4.2.1 (Dimensions of BGA Pads, etc)

Table G-15. In-Process Inspection

No.	Item	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	G.3.4.1 G.3.4.2 G.3.4.3	G.4.5.4.1 G.4.5.4.2 G.4.5.4.3	All	After forming internal circuit and before pre-treating the laminate layer
2	Conductor of external layer Base material of external layer	G.3.4.1.1 G.3.4.1.2	G.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	G.3.8	G.4.5.10	Sampling([1])	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	G.3.4.2.1	G.4.5.4.2	All	After forming solder resist and before solder coating

Note ([1]) Sampling inspection shall be performed based on 1.0% of the acceptable quality level (AQL) in "Normal Inspection Level II" specified in JIS Z 9015-1. The lot shall be processed in the same circuit forming process on the same day the sampling inspection was performed and can be subjected to solder resist application.

G.4.3 Qualification Test

G.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole and number of layers sufficient to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation.

G.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table G-16. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table G-16.

Table G-16. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail Criteria		
					Samples		Quantity of allowable defects
Group	Order	Test item			Production printed wiring boards	Test coupon (1) (2)	
I	1	Externals of conductor, base materials, and solder resist Externals, dimensions, Dimensions Marking	G.3.4.1 G.3.4.2 G.3.4.3	G.4.5.4.1 G.4.5.4.2 G.4.5.4.3	No. 1 to No. 6	A, B, C, D, E, F, G, H, K, L and M	0
	2	Workmanship(3)	G.3.6	G.4.5.8			
II	1	Plating adhesion and overhang	G.3.7	G.4.5.9	No. 1 to No. 6	C	
	2	Bow and twist	G.3.5	G.4.5.7		N/A	
III	1	Structural integrity	G.3.4.4	G.4.5.5	No. 1	A, F, K and M	
	2	Terminal pull strength	G.3.10.1	G.4.5.12.1		F	
	3	Solder resist thickness	G.3.4.5	G.4.5.6		J	
IV	1	Connection resistance	G.3.9.3	G.4.5.11.3	No. 2	D	
	2	Hot oil resistance	G.3.11.3	G.4.5.13.3			
	3	Connection resistance	G.3.9.3	G.4.5.11.3			
V	1	Circuitry	G.3.9.2	G.4.5.11.2	No. 3	E and G(3)	
	2	Connection resistance	G.3.9.3	G.4.5.11.3			
	3	Thermal shock (I)	G.3.11.1.1	G.4.5.13.1a)			
	4	Circuitry	G.3.9.2	G.4.5.11.2			
	5	Connection resistance	G.3.9.3	G.4.5.11.3			
VI	1	Humidity and insulation resistance	G.3.11.2	G.4.5.13.2	No. 4	E	
	2	Dielectric withstanding voltage	G.3.9.1	G.4.5.11.1			
VII	1	Thermal stress	G.3.11.4	G.4.5.13.4	No. 5	A, B, L and M	
	2	Solderability	G.3.10.2	G.4.5.12.2		B and H(4)	
VIII	1	Radiation hardness	G.3.11.5	G.4.5.13.5	No.6	N/A	
-	-	Materials	G.3.2	G.4.5.2	N/A		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(4) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

G.4.4 Quality Conformance Inspection

G.4.4.1 Quality Conformance Inspection (Group A)

G.4.4.1.1 Sample

The quality conformance inspection shall be performed with the test coupons. The test coupons and sample product shall be manufactured simultaneously. Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen. A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

G.4.4.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table G-17. The inspections within each group shall be performed in the order listed. One test coupon shall be provided for each of Group IV and V test.

Table G-17. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria		
					Quantity of samples		Quantity of allowable defects
Group	Order	Inspection item			Production printed wiring boards	Test coupon	
I	1	Design and construction	G.3.3	G.4.5.3	All	N/A	0
	2	Externals of conductor, base materials, and solder resist Externals, dimensions, Dimensions Marking	G.3.4.1 G.3.4.2 G.3.4.3	G.4.5.4.1 G.4.5.4.2 G.4.5.4.3	All	N/A	
	3	Workmanship	G.3.6	G.4.5.8			
II	1	Bow and twist	G.3.5	G.4.5.7	All	N/A	
III	1	Circuitry	G.3.9.2	G.4.5.11.2	All	N/A	
IV	1	Thermal stress	G.3.11.4	G.4.5.13.4	N/A	A, F, K(1) and M(2)	
V	1	Solderability	G.3.10.2	G.4.5.12.2	N/A	F and H(3)	

Notes:

(1) Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the products is provided with SVH.

(2) Test coupon M shall be inspected when the products is provided with BGA pads, etc.

(3) Test coupons F and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

G.4.4.2 Quality Conformance Inspection (Group B)

G.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection are manufactured and selected from the lot which passed Group A inspection.

G.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table G-18. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

Table G-18. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	G.3.7	G.4.5.9	C	0
II	1	Terminal pull strength	G.3.10.1	G.4.5.12.1	F	
III	2	Connection resistance	G.3.9.3	G.4.5.11.3	D	
	3	Hot oil resistance	G.3.11.3	G.4.5.13.3		
	4	Connection resistance	G.3.9.3	G.4.5.11.3		
IV	1	Circuitry	G.3.9.2	G.4.5.11.2	E and G(1)	
	2	Connection resistance	G.3.9.3	G.4.5.11.3		
	3	Thermal shock (II)	G.3.11.1.2	G.4.5.13.1b)		
	4	Circuitry	G.3.9.2	G.4.5.11.2		
	5	Connection resistance	G.3.9.3	G.4.5.11.3		
V	1	Humidity and insulation resistance	G.3.11.2	G.4.5.13.2	E	
	2	Dielectric withstanding voltage	G.3.9.1	G.4.5.11.1		

Note: (1) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

G.4.5 Methods for Test and Inspection

G.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

G.4.5.2 Materials

The copper clad laminates and prepreg shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.

G.4.5.3 Design and Construction

The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.

G.4.5.4 Externals, Dimensions, Marking and Others

G.4.5.4.1 Externals of Conductor, Base Material and Solder Resist

External inspection shall be performed with 4X to 10X magnifier.

a) Conductors
For conductive pattern inspection, Automatic Optical Inspection machine (AOI) can be used. Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

b) Base Materials
Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

c) Solder Resist
Pass or fail shall be determined by using 10X magnifier.

G.4.5.4.2 Dimensions

Dimensions shall be measured by using a measuring instrument with sufficient accuracy.

a) Dimensions of BGA pads, etc.
The dimensions of printed wiring boards with BGA pads, etc. shall be measured as follows. For the board with multiple BGA pads, the BGA pad with the largest area shall be selected for measurement. If all the BGA pad areas are the same size, any one of the pad shall be selected for measurement. The detailed measurement sections shall be shown in Figure G-21.

1) Dimension of BGA pads and solder resist opening diameter
Each section of grid corner (outer) of the center area (inner) shall be measured by an optical measuring instrument.

2) Position accuracy for BGA pads, etc.
The directions of X and Y axes of circumference for BGA pads shall be measured with a 2-dimension end-measuring machine or an equivalent measuring instrument sufficient enough for measurement.

3) Height from the base material for BGA pads, etc. (pad thickness)
Each section of grid corner (outer) and the center area (inner) shall be measured by the focal depth method using a metallograph.

4) Total board thickness for BGA pads, etc.
For the total board thickness including solder coating and solder resist, the center section shall be measured by using a micrometer.

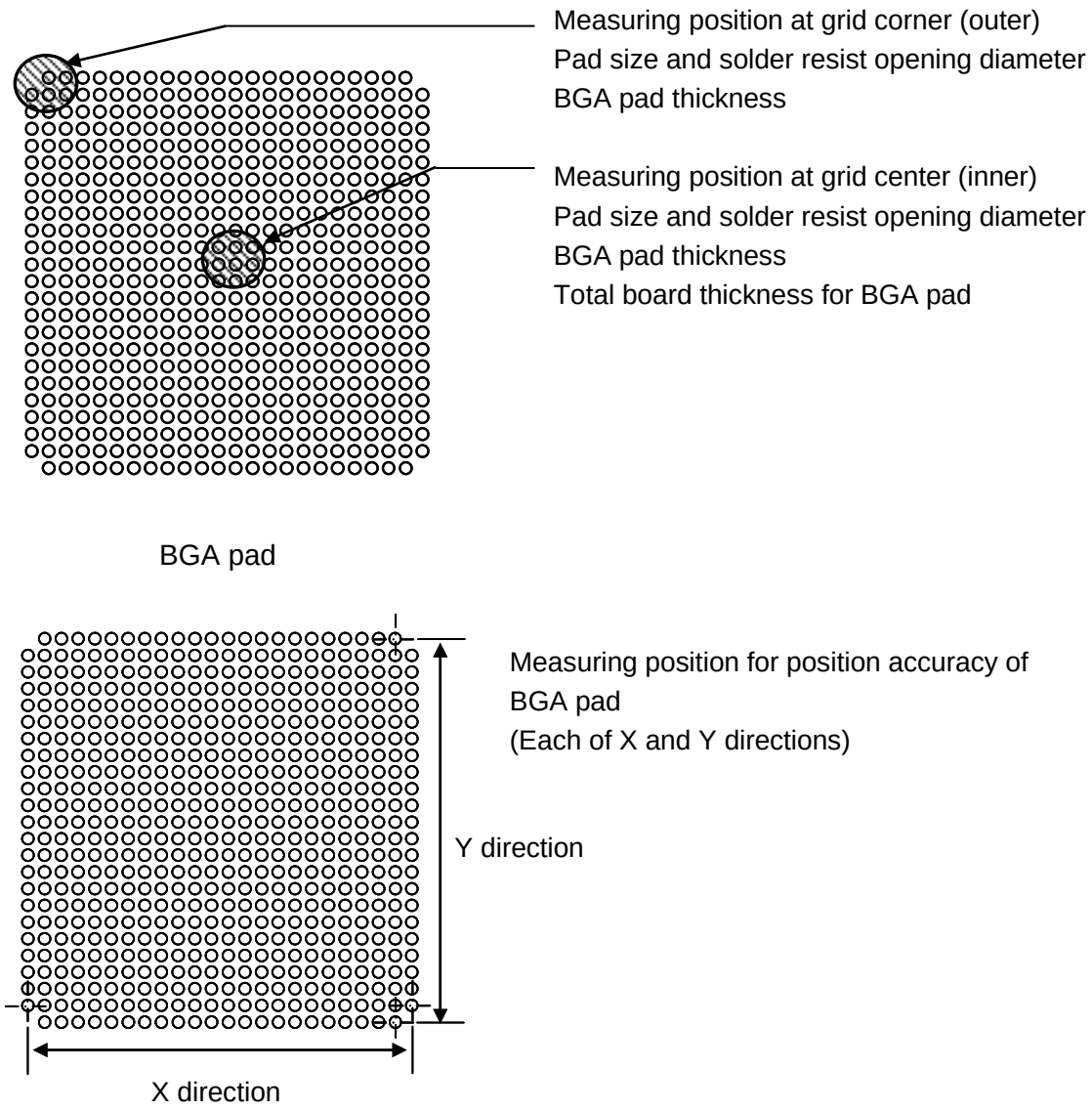


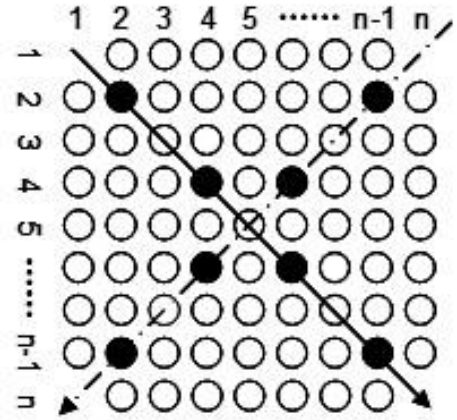
Figure G-21. Measuring Points for BGA Pad

5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure G-22)

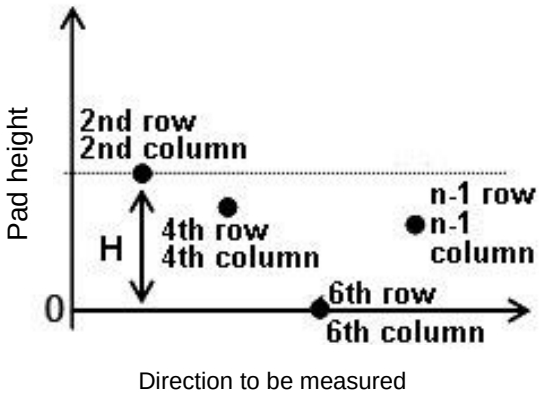
Directions of the pad to be measured



Direction 1 Direction 2

●: Pad to be measured

Co-planarity



H: Co-planarity (at max.)

Figure G-22. Measuring of Co-Planarity

G.4.5.4.3 Marking

Marking shall be inspected visually (naked eyed inspection).

G.4.5.5 Structural Integrity

G.4.5.5.1 Through Holes

a) Vertical microsection

The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated in resin and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. The vertical microsection shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching to clarify the borderline of copper plating and copper foil shall not be conducted at the observation of internal connection and resin smear.

b) Horizontal microsection
Multilayer boards with through holes shall be encapsulated in resin and polished. A conductor layer shall be polished in the parallel direction to expose the conductor layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching shall not be performed on the cross section surface.

G.4.5.5.2 Voids

The microsection prepared in paragraph G.4.5.5.1 a) shall be inspected for any void at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.3 Lifting of Lands

Lands shall be inspected for any lifting by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.4 Cracks on Copper Foil

Copper foil shall be inspected for any crack by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.5 Internal Layer Connection

Internal layer connection shall be inspected by using the microsection prepared in paragraphs G.4.5.5.1 a) and b) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.6 Plating Thickness

Plating thickness shall be inspected by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 200X as a minimum. Plating thickness shall be the average value of three measurements for a plated through hole. If any of the measured value is significantly different from the other values, the value shall not be used for calculating the average.
Cap plating thickness shall be measured at the thinnest area of a hole.

G.4.5.5.7 Laminate Cracks

Laminate shall be inspected for any crack by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.8 Delamination and Blister

The microsection prepared in paragraph G.4.5.5.1 a) shall be inspected for any delamination and blister at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.9 Layer-to-layer registration

The layer-to-layer registration shall be measured by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 25 to 100X. The misregistration shall be measured around the hole in the direction parallel to the board length and the vertical direction. The microsections for inspection of layer-to-layer misregistration shall be prepared by cutting the multi-layer printed wiring board in the direction parallel to the board length for at least one hole and the vertical direction for another one hole as a minimum. (See Figure G-23)

G.4.5.5.10 Annular ring

The annular ring shall be measured by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 25 to 100X. The measurement of the annular ring on an external layer shall be from the surface of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure G-23).

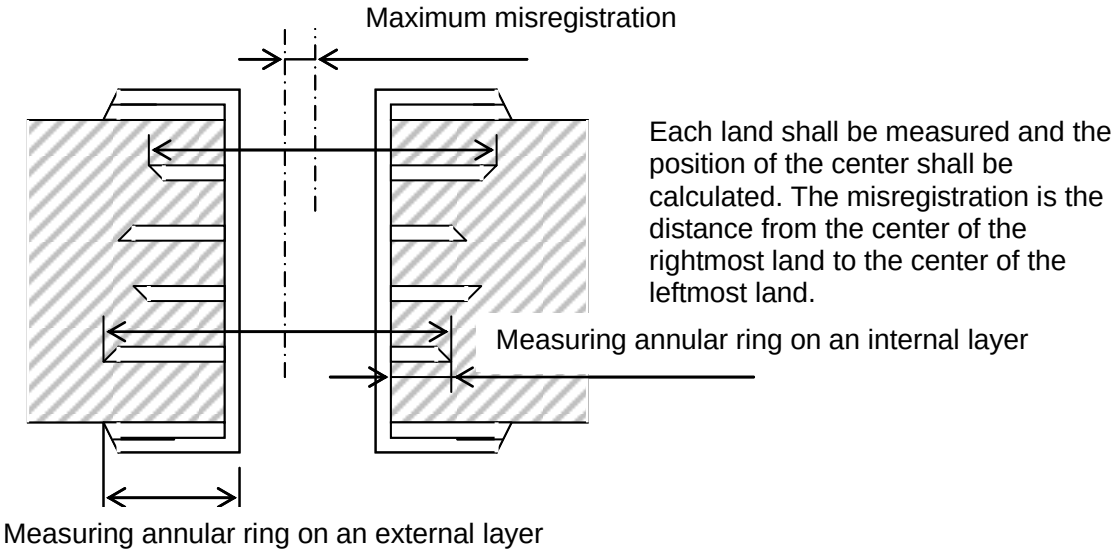


Figure G-23. Measurement of Layer-to-Layer Misregistration and Annular Ring

G.4.5.5.11 Insulation Layer Thickness

Insulation Layer Thickness shall be measured by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 50 to 100X.

G.4.5.5.12 Adhesion of Cap Plating and Filled Resin

Adhesion of cap plating and filled resin shall be observed and measured by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

G.4.5.5.13 Protrusion and Pit of Cap Plating

Protrusion and pit of cap plating shall be observed and measured by using the microsection prepared in G.4.5.5.1 a) at a magnification of 50X as a minimum.

G.4.5.5.14 Filling of Resin

Filled resin shall be observed and measured by using the microsection prepared in paragraph G.4.5.5.1 a) at a magnification of 25 to 50X.

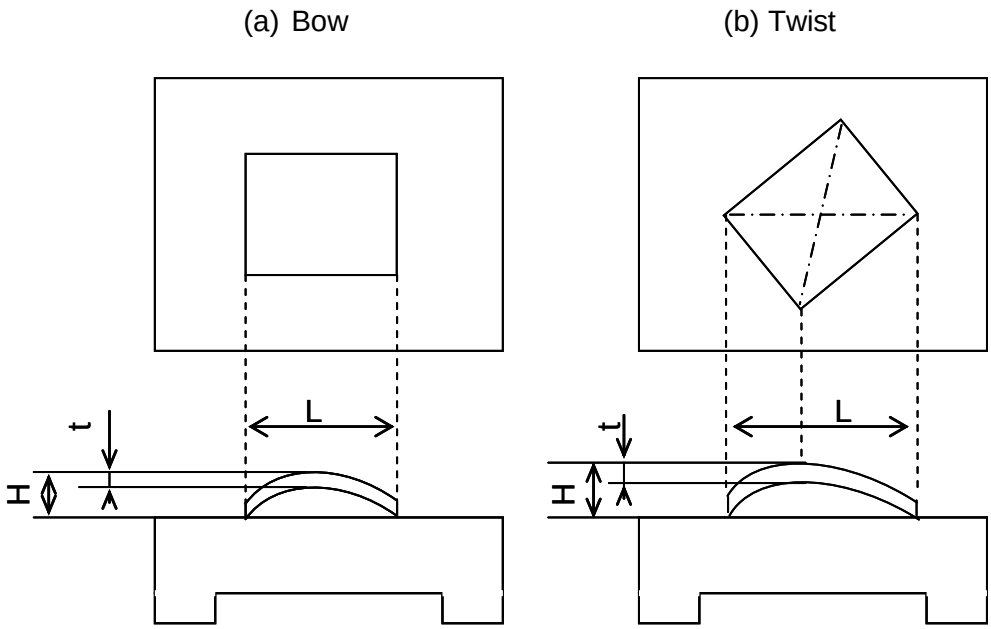
G.4.5.6 Solder Resist Thickness

Solder resist shall be cut vertically near the conductor and encapsulated in resin and polished to expose the center of the conductor. The solder resist thickness shall be measured at a magnification of 200X as a minimum.

G.4.5.7 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure G-24). The bow and twist shall be calculated as follows.
The percent bow and twist shall be calculated by the following formula.

$$\text{Percent bow and twist} = \frac{H\text{-}t}{L} \times 100\ (\%)$$



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure G-24. Measurement of Bow and Twist

G.4.5.8 Workmanship

The workmanship of the printed wiring boards shall be inspected at a magnification of 4 to 10X.

G.4.5.9 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and a minimum of 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

G.4.5.10 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 % by volume of isopropyl alcohol and 25 % by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6\Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table G-19 may be used to perform the cleanliness test.

Table G-19. Equivalent Measuring Method

Method	Resistivity ($\times 10^6\Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.2

Note: (1) Alpha Metals Incorporated, “Omega Meter”

G.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

G.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

G.4.5.11.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

G.4.5.11.3 Connection Resistance

The resistance between the through hole terminals shall be measured by using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5 mΩ.

G.4.5.12 Mechanical Performance

The mechanical performance tests shall be performed as follows.

G.4.5.12.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at a minimum of 6mm from the land, peeled and pulled toward the land, and shall be cut off by applying the sharp knife at the joining point of the conductor and land without degrading the land adherence strength. Then, a lead wire sufficient in length for installing a tensile tester shall be inserted in the hole and soldered. After that, a cycle of solder removal and resoldering by using a soldering iron shall be performed.

a) A lead wire shall be soldered in to the through hole.
b) The lead wire shall be removed from the through hole (solder removal).
c) A lead wire shall be resoldered in to the through hole.
d) The lead wire shall be removed from the through hole (solder removal).
e) A lead wire shall be resoldered in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the required minimum. Upon completion of e) resoldering, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Breaking off or pulling out the lead wire shall not be regarded as a failure, and a new lead wire shall be soldered and pulled. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

G.4.5.12.2 Solderability

a) Hole solderability
The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph G.4.5.5.1.

b) Surface solderability
After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

G.4.5.13 Environmental Performance

The environmental performance tests shall be performed as follows.

G.4.5.13.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
The test shall be performed under the test condition B. However, the lowest temperature shall be -30°C and the number of cycle shall be 1000 cycles. The time for step 2 and 4 shall be within 2 minutes each. Reflow soldering of total heating process in accordance with JERG-0-043 shall be performed three times as a pre-treatment of the printed wiring board. The heating condition shall be as follows.
1) Heating condition: 200°C min. for 45 seconds min.
2) Peak temperature: 230°C min.

b) Thermal shock (II) (applicable to quality conformance inspection)
The test shall be performed under the test condition B-3(-65 to +125℃).
The time for step 2 and 4 shall be within 2 minutes each.

G.4.5.13.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

G.4.5.13.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. This Immersion and cooling shall be performed for 10 cycles.

G.4.5.13.4 Thermal Stress

The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 % maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for the structural integrity using the microsection prepared in accordance with paragraph G.4.5.5.1. Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder. Evaluation specimen of Adhesion of cap plating and filled resin (paragraph G.3.4.4.12) shall be floated in a solder bath for a period of 10 seconds and cooled down. This floating and cooling shall be performed three times.

G.4.5.13.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraphs G.4.5.11.1 and G.4.5.13.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

APPENDIX H

PRINTED WIRING BOARDS
FOR HIGH-SPEED SIGNALS

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX H

PRINTED WIRING BOARDS FOR HIGH-SPEED SIGNALS

H.1. General

H.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards for high-speed signal with reduced transmission loss (hereinafter referred to as "printed wiring boards").

H.1.2 Part Number

The part number of the printed wiring boards is in the following form.

Example: JAXA([1]) 2140 / H107 / 102 / 18([2])

- H107: Individual identification
- 102: Base material code (H.1.2.1)
- 18([2]): Number of layers (H.1.2.2)

Notes:
([1]) "JAXA" indicates the common part for space use and may be abbreviated to “J”.
([2]) Number of conductor layers

H.1.2.1 Base Material Code

The base material code is as specified in Table H-1.

Table H-1. Base Material Code

Base material code	Insulation board material
102	Glass base woven polyphenylene ether resin, compliant to IPC-4101/102

H.1.2.2 Number of Layers

The maximum number of layers shall be specified in each detail specification.

H.2. Applicable Documents etc.

H.2.1 Applicable Documents

The applicable documents shall be as follows and as specified in paragraph 2.1.

a) JERG-0-043 Standards for Surface Mount Soldering Process in Space Application
b) JIS C 6481 Test methods of copper-clad laminates for printed wiring boards
c) IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design
d) IPC-TM-650 Test Methods Manual

H.2.2 Reference Documents

The reference documents shall be as follows and as specified in paragraph 2.2.

a) JERG-0-054 Standards for BGA/CGA Soldering Process in Space Application
b) JIS C 6012 Qualification and Performance Specification for Rigid Printed Boards

H.3. Requirements

H.3.1 Qualification Coverage

Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs H.3.2 through H.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test. Products with fewer layers and less thickness than the qualified sample units are considered qualified. Surface plating and solder coating types other than those used for the qualified sample units are considered qualified. Only solder resist inks used for qualification tests are considered qualified. If necessary, additional qualification coverage shall be specified in the detail specification.

H.3.2 Materials

The materials shall be specified as follows.

H.3.2.1 Metal-Clad Laminate, Prepreg and Copper foil

The copper-clad laminate and prepreg shall conform to the applicable standard, IPC-4101 or JPCA/NASDA-SCL01, and shall be as specified on drawings.
The copper foil laminated to prepreg on the outermost layer shall be as specified in the drawing.
The nominal thickness of the base material shall be no less than 0.05mm.
The thickness of the copper foil shall be as specified in Table H-2 and the type of copper foil shall be specified in the detail specification.

Table H-2. Thickness of Copper Foil (Nominal)

Unit: μm

Layer	Classification	Copper foil thickness
External layer	With SVH	9 minimum
	Without SVH	18 minimum
Internal layer	SVH layer	9 minimum
	Any layer other than SVH layer or a layer without SVH	18 minimum

For electrical property of the copper laminate board, dielectric constant shall be 4.0 as a maximum at 1GHz, and dielectric dissipation factor shall be 0.01 as a maximum at 1GHz when the test is performed in accordance with Paragraph 2.5.5.9 of IPC-TM-650.
The standards (including delamination strength) applied to the materials used in the printed wiring boards shall be clearly specified in the detail specification. The detailed information about base materials such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the Application Data Sheet (hereinafter referred to as “ADS”).

H.3.2.2 Via Hole Filling Materials (Filling Resin)

The filling materials for SVH and small through hole shall be resin. The detailed information about the filling materials such as type of resin and glass-transition temperature shall be specified in ADS.

H.3.2.3 Solder Resist Ink

The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent.

H.3.2.4 Marking Ink

The marking shall be conducted using epoxy resin base ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

H.3.2.5 Plating

Electroless and electrolysis plating shall be applied to all through holes and for cap plating. Solder coating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.

H.3.2.5.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic plating to form a conductive layer over the insulating material.

H.3.2.5.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 %.

H.3.2.5.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table H-3. The electrolytic nickel plating specified in paragraph H.3.2.5.4 shall be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 % except for the metal added to increase the hardness.

Table H-3. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 %
KNOOP hardness	91 to 129 (inclusive)

H.3.2.5.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent, and shall be of a low stress type.

H.3.2.5.5 Solder Coating

The solder used for solder coating shall contain 50 to 70 % tin.

H.3.3 Design and Construction

H.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Printed wiring boards shall be designed and their manufacturing drawings shall be prepared in accordance with this appendix. The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

H.3.3.2 Connector for Printed Wiring Boards

A direct connector (one-part connector or edge-board connector) shall not be used.

H.3.3.3 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by small via holes, SVH or through holes.

H.3.3.4 Connection Method for Area Array Packaging Pads

The connection method for contact pads of area array packages such as BGA pads (hereinafter referred to as “BGA pads, etc.”) shall be made by Dog-Bone structure or Via-in-Pad (hereinafter referred to as “VIP”) structure.
Dog-Bone structure is to connect small via hole by drawing the circuit out of the contact pads such as BGA pads as shown in Figure H-1. The small via hole shall be filled with resin and closed by plating (cap plating).
VIP structure is the structure where cap plating as BGA pad is directly on top of the small via hole filled with resin as shown in Figure H-2.

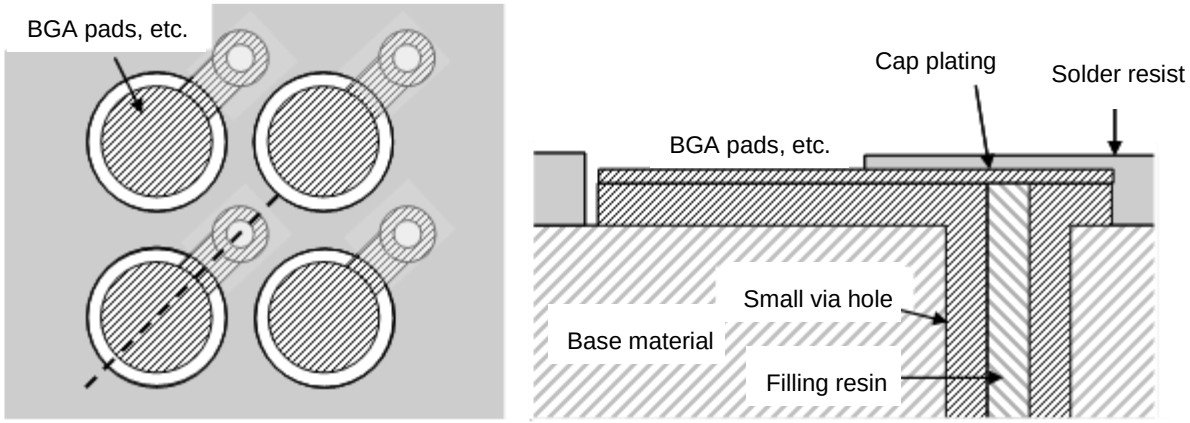


Figure H-1. External and Cross-Section View of Dog-Bone Structure

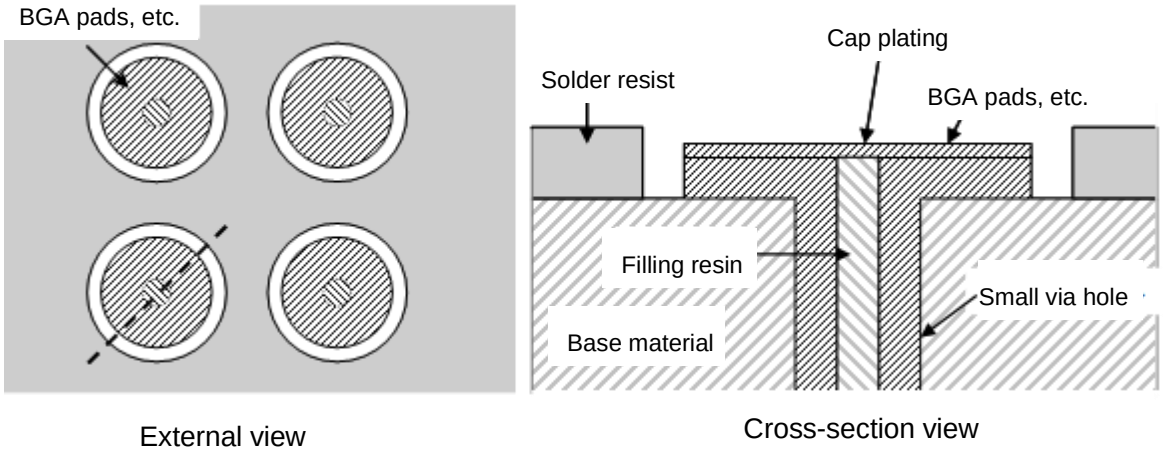


Figure H-2. External and Cross-Section View of Via-in-Pad Structure

H.3.3.5 Through Hole Diameter

The minimum hole diameter for small via hole and SVH shall be φ0.20mm as a drill hole. When the land of via hole is used as BGA pads, etc., the drill hole for via hole shall be φ0.20mm as a maximum.

H.3.3.6 Filling Resin for Through Hole

The small via hole to be filled with via filling materials shall be specified in the production drawing. The small via holes and SVH in VIP structure shall be filled with via filling materials.

H.3.3.7 Conductor Width and Thickness

The minimum design value for conductor width shall be as specified in Table H-4. The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor. Figures H-3, H-4, H-5, and H-6 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this will apply to both internal and external layers of the conductor under vacuum and space environmental conditions. The details shall be specified in IPC-2152.
When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.

Table H-4. Conductor Width (Design Value)

Unit: mm

Layer	Conductor thickness	Minimum conductor width
External	All	0.12
Internal	More than 35μm	0.10
	35μm or less	0.07

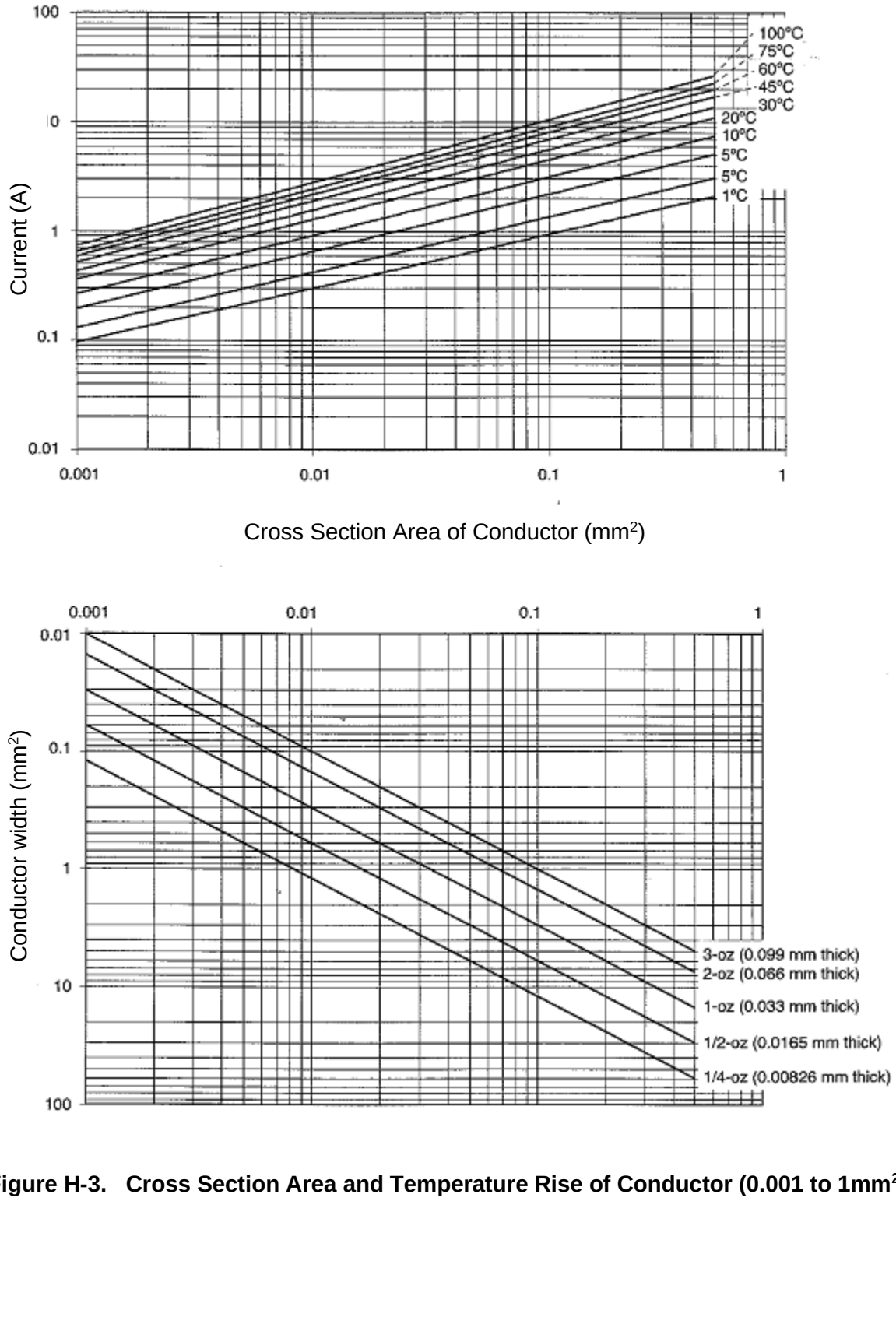


Figure H-3. Cross Section Area and Temperature Rise of Conductor (0.001 to 1mm²)

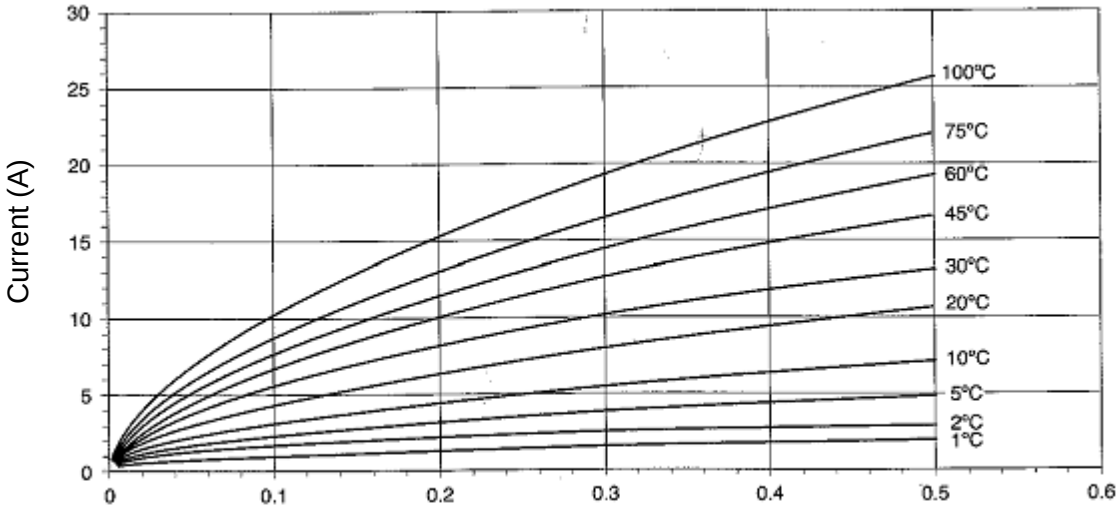


Figure H-4. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.5mm²)

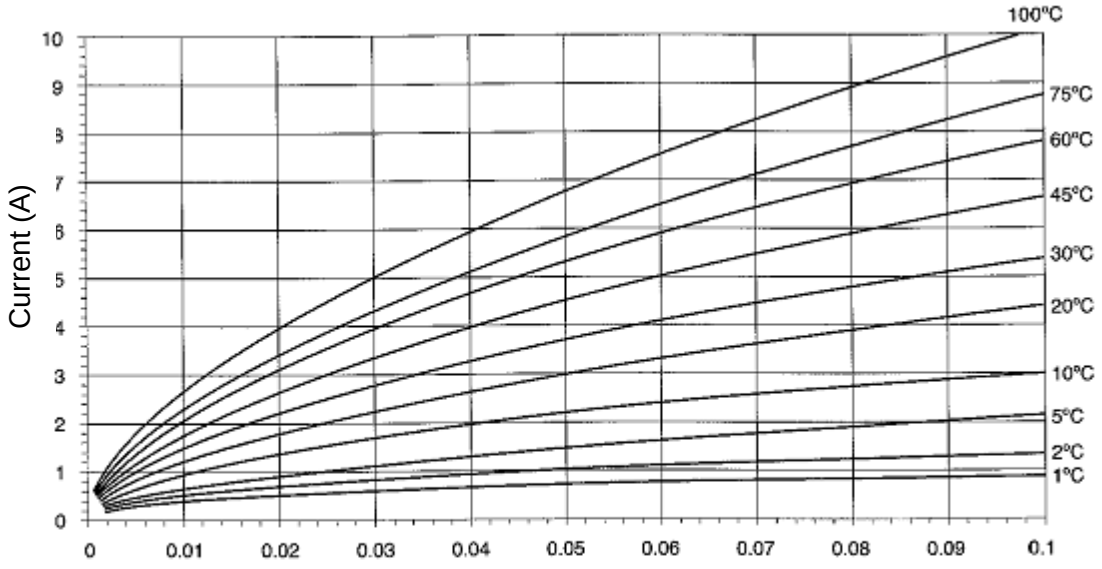


Figure H-5. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.1mm²)

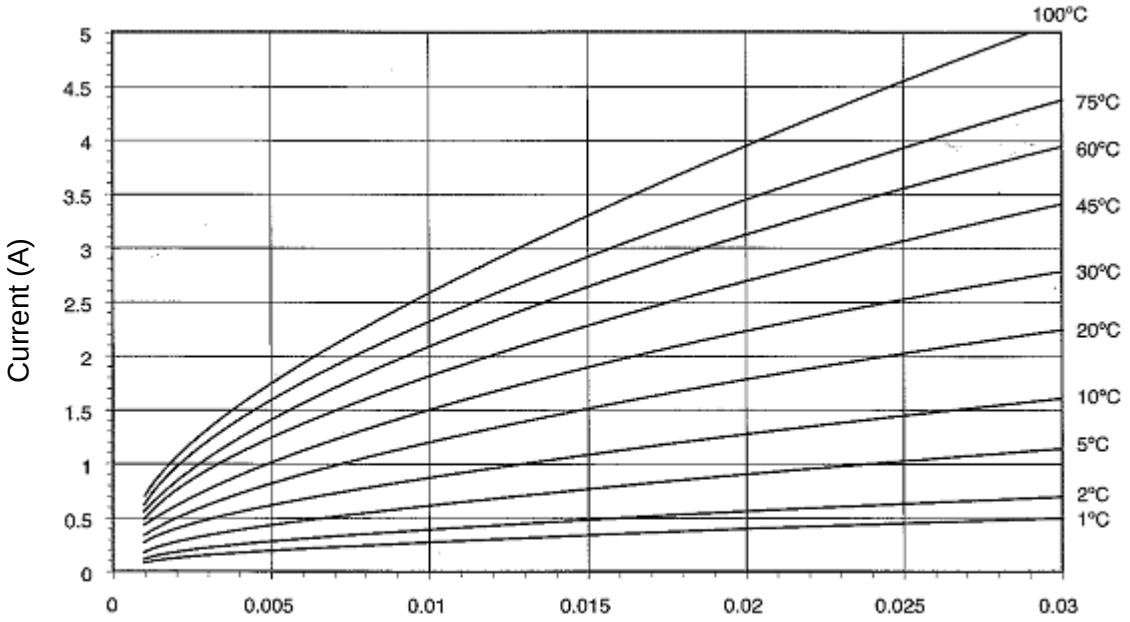


Figure H-6. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.03mm^2)

H.3.3.8 Conductor Spacing

The minimum design value of conductor spacing shall be as specified in Table H-5. The specific conductor spacing shall depend on the voltage applied between conductors as specified in Table H-5.

Table H-5. Conductor Spacing (Design Value)

Unit: mm

Layer	Conductor thickness	Minimum conductor spacing
External	All	0.14
Internal	More than 35μm	0.15
	35μm or less	0.08

Table H-6. Conductor Spacing for Printed Wiring Boards

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	
	External layer	Internal layer
0 to 50	0.15	0.08
51 to 100	0.15	0.10
101 - 300	0.40	0.20
301 - 500	0.80	0.25
501 or higher	(0.003xV)	(0.0025xV)

H.3.3.9 Land Diameter

The minimum design value of land diameter shall be as specified in Table H-7 (see Figure H-7). Non-functional land is not necessary when maintenance of conductor spacing and electrical characteristics requirements are specified.

Table H-7. Land Diameter

Unit: mm

Hole	Minimum land diameter([1])
SVH and small via holes	ϕ (Drill diameter + 0.25)
Plated-through holes except the above	ϕ (Finished hole diameter + 0.5)
Non-plated-through holes	ϕ (Drill diameter + 1.1)

Notes:

([1]) The minimum diameter of lands other than round shaped lands shall be the measure of the length “A” shown in Table H-7.

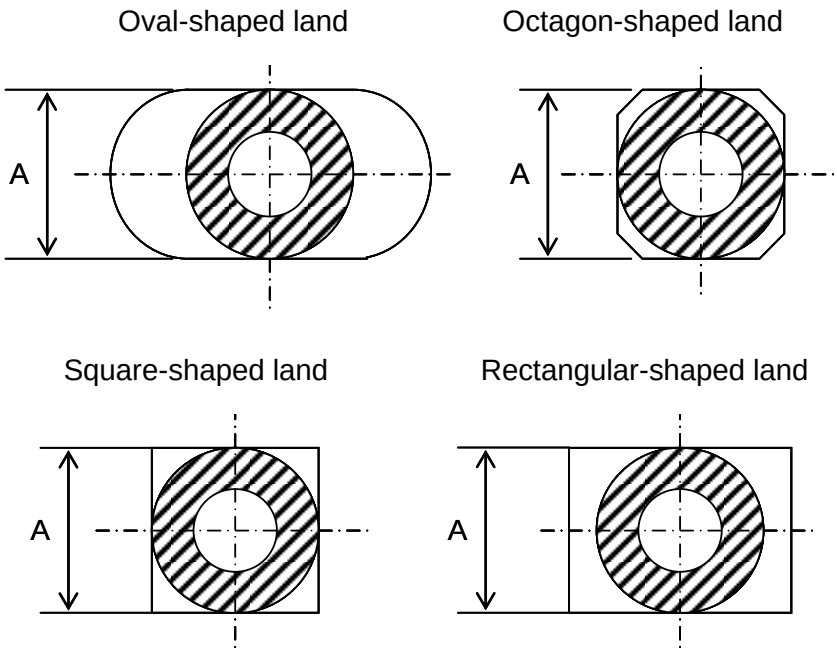


Figure H-7. Measurements of Minimum Diameter of Lands Other than Round Shaped Lands (A)

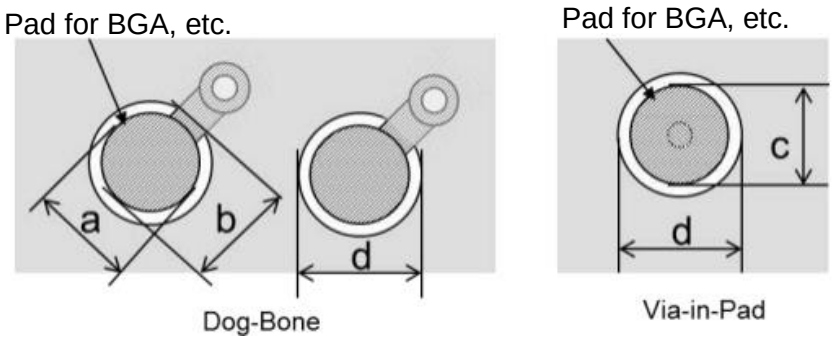
H.3.3.10 Pads for BGA etc.

The sizes of the pads for BGA, etc. for each section shown in Table H-8 shall be specified.

Table H-8. Dimensions of BGA Pads, etc.

Unit: mm

Section		
Pad size (Bottom of conductor)	Dog-Bone	Pad (see Figure H-8 a)
		Fan-out direction (see Figure H-8 b)
	Via-in-Pad (see Figure H-8 c)	
Size of solder resist opening (Resist surface)	Dog-Bone (see Figure H-8 d)	
	Via-in-Pad (see Figure H-8 d)	
Total board thickness	Total board thickness including conductor and solder resist	

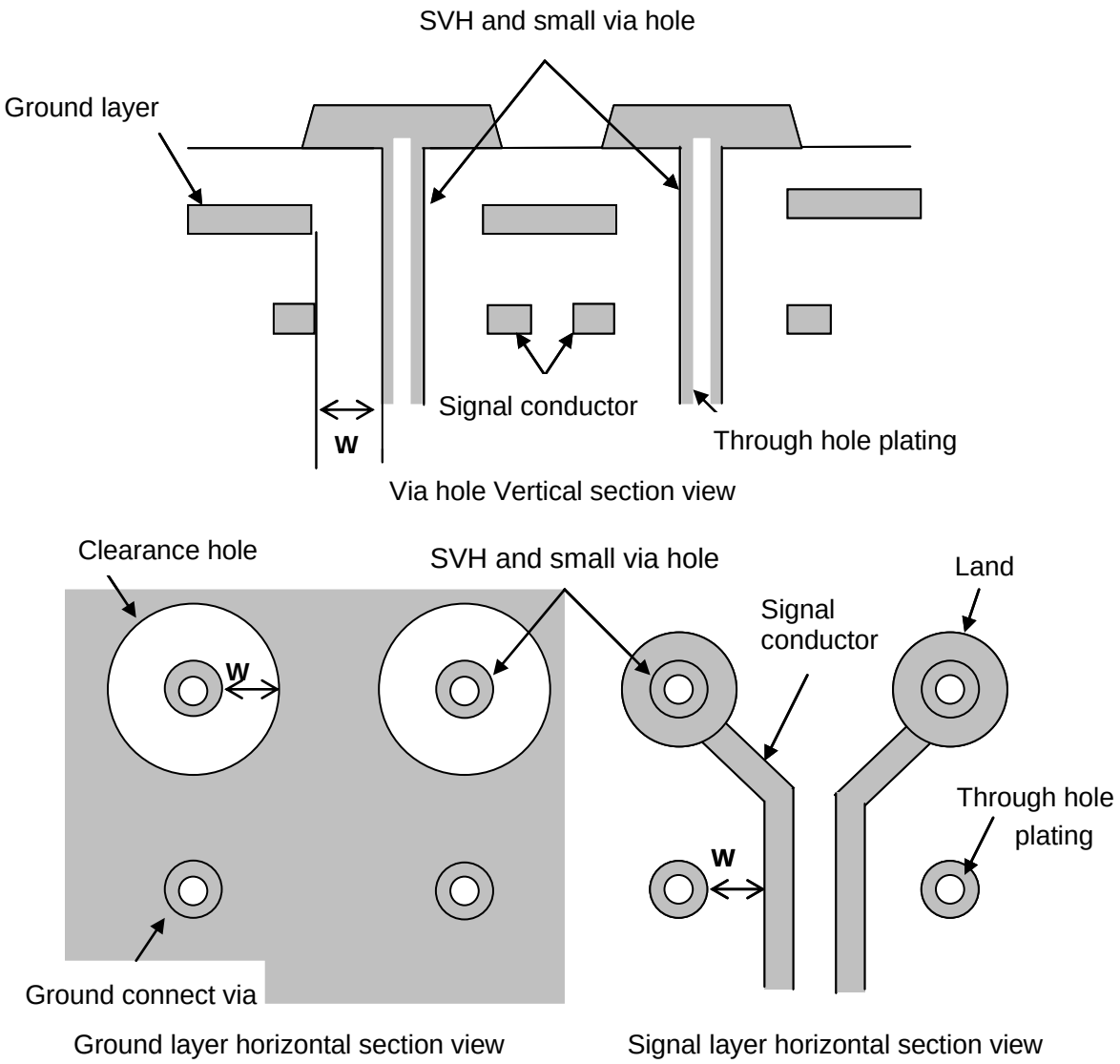


a: Pad size in Dog-bone structure b: Fan-out pad size c: Pad size in Via-in-Pad
d: Size of solder resist opening

Figure H-8. Measurements of Pads for BGA, etc.

H.3.3.11 Internal Layer Clearance

The distance (internal layer clearance) from the SVH and small via hole to the hole wall of the conductor nearby shall be as specified in Figure H-9.



W= Internal layer clearance ≥ 0.28mm

Figure H-9. Cross Section View of Via Holes

H.3.3.12 Surface Finish Plating

The thickness of the surface finish plating and solder coating specified in the manufacturing drawing shall be in accordance with Table H-9. The electrolytic Nickel plating shall be applied as an undercoat of electrolytic gold plating, and shall not be used for the surface finish. If more strict requirements than the ones specified in Table H-9 are necessary, consult with manufacturer and specify on the manufacturing drawing.

Table H-9. Thickness of Surface Finish Plating

Unit: μm

Plating material	Surface plating thickness
Electrolytic gold	1.3 to 4.0
Electrolytic nickel	5 as a minimum
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (paragraph H.3.10.2).

H.3.3.13 Solder Resist

The solder resist application shall be specified except for the land, pads (incl. Via-in-Pad), and the small via holes without resin filling.
The lands of small via hole and SVH in the dog-bone structure shall be coated with solder resist.
Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.
The minimum distance from the edge of the board to the solder resist shall be 0.3mm.

H.3.3.14 Plating on Outer Perimieter Sidewall of the Board

The plating on outer perimeter sidewall of the board (hereinafter referred to as “Sidewall plating”) shall be specified in the manufacturing drawing if applied.
The detailed design of the sidewall plating shall be specified in detail specification.

H.3.3.15 Characteristic Impedance

The characteristic impedance of the printed wiring boards shall be specified in the manufacturing drawing if applied.

H.3.3.16 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph H.3.11.1.2) and within -65 to +125°C.

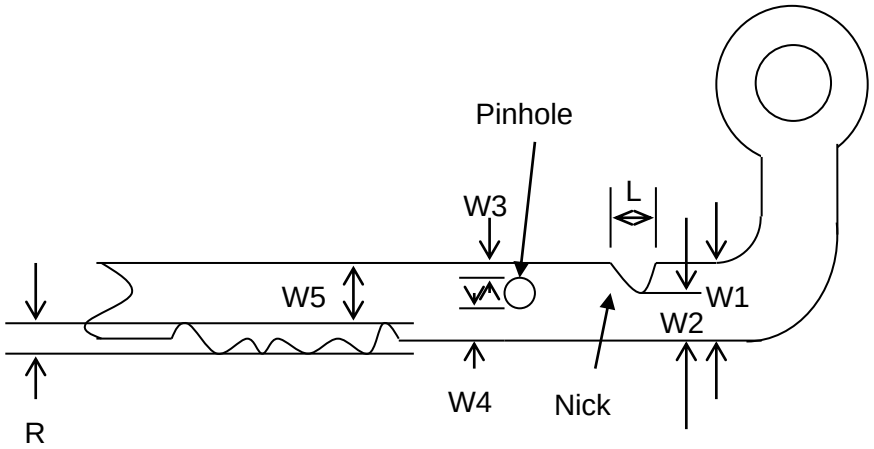
H.3.4 Externals, Dimensions, Marking and Others

H.3.4.1 Externals of Conductor, Base Material and Solder Resist

H.3.4.1.1 Conductor

a) Conductive pattern
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor
The conductors including sidewall plating shall contain no tears, cracks, lifting, or separation. Any combination of edge roughness, nicks, pinholes or scratches exposing the insulation board shall not reduce the conductor width to less than 80 % of the minimum finished conductor width. The length of any defect shall not exceed the design width of the conductor. The number of defects exceeding 0.05mm in width shall not be more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall meet the conductor width tolerance (see Figure H-10).
The tolerances of conductor width and conductor spacing shall be as specified in Table H-10.
The nicks and pinholes on the ground surface and power supply surface shall not exceed 1.0mm in the maximum length and 4 pieces per 625cm^2 in number.



W1 ≥ (Minimum finished conductor width)
W2 ≥ 0.80 × (Minimum finished conductor width)
W3 + W4 ≥ 0.80 ×Minimum finished conductor width)
W5 + R ≥ Conductor width tolerance ≥ W5-R
L = Length of defect

Figure H-10. Passing Criteria for Conductor Defects

Table H-10. Tolerance of Conductor Width and Conductor Spacing

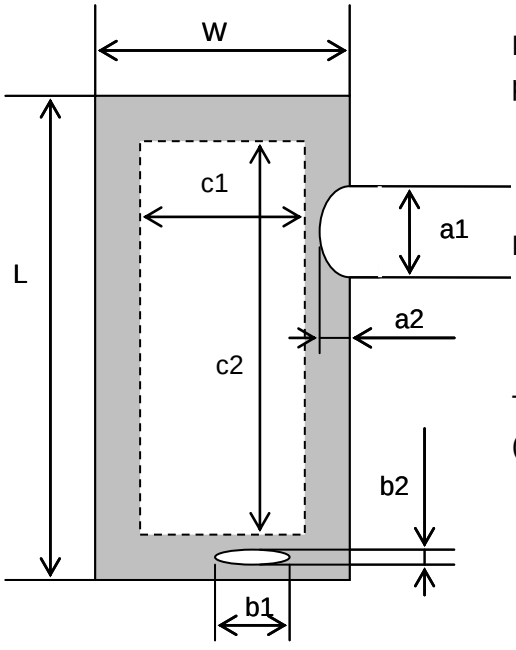
Unit: mm

Dimension		Tolerance
Conductor width	0.07 to less than 0.13	+0.05 -0.03
	0.13 to less than 0.20	±0.05
	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
Conductor spacing	Less than 0.10	0.05 as a minimum
	0.10 to less than 0.14	0.06 as a minimum
	0.14 and more	0.10 as a minimum
	The positive side tolerance is not specified for all design value.	

c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure H-11).

The pad length and width shall be based on the design value.



Defects along the external edge of the pad
a1 ≤ L X 0.2
a2 ≤ W X 0.2

Defects inside the pad
b1 ≤ L X 0.1
b2 ≤ W X 0.1

The area where no defect is allowed (from the center of the pad)
c1 = W X 0.8
c2 = L X 0.8

Figure H-11. Passing Criteria for Defects on the Rectangular Surface Mount Pad

d) Mounting Pad for BGA, etc.
The defects such as nicks, dent and pinholes along the edge of the pad shall not exceed 10% of the diameter of the pad expanding in a radial direction of the land center. The defects inside the pad shall not exceed 20% of the circumference of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center of the pad diameter to the 80% of the pad (see Figure H-12).
The pad diameter shall be based on the design value.

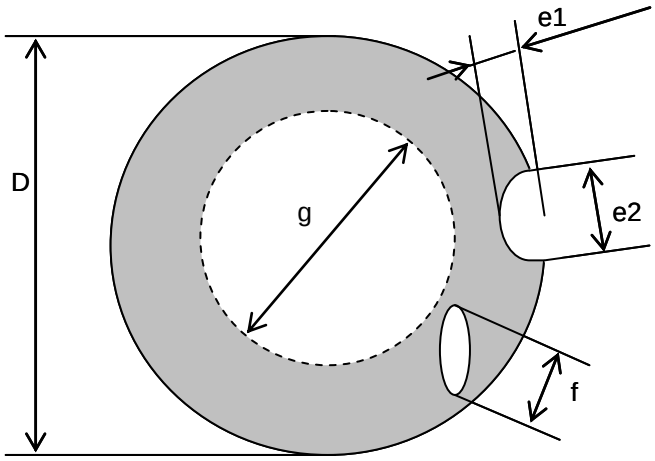


Figure H-12. Passing Criteria for Defects on the Mount Pad

e) Probe mark from Electrical test
The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

f) Dielectric layer between conductor layers
The surface of a dielectric layer between conductor layers shall be free from adhesion of any residual conductor or foreign inclusion.

g) Solder coating
The solder coating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on sidewall plating side is permitted.

h) Electrolytic nickel and electrolytic gold plating
The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductive patterns. However, the copper exposure on the conductor side is permitted.

H.3.4.1.2 Base Materials

a) Edges of printed wiring board
Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board. Crazing along the edges of printed wiring board shall be permitted, when the spacing between the crazing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

b) Surface of printed wiring boards
The surface of printed wiring boards shall not exhibit cracks or separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the base material shall not be permitted.

H.3.4.1.3 Solder Resist

a) The cured solder resist shall be free from tackiness, blistering and delamination.
b) Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted.
c) Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist.
d) The solder resist shall not encroach onto lands for mounting parts.
e) The application range and misalignment of solder resist and conductive patterns shall meet the provisions of manufacturing drawings.
f) Unless otherwise specified on the manufacturing drawings, adjacent conductor shall not be exposed in the solder resist opening area.
g) In the Dog-Bone structure, solder resist shall completely cover the land of small via hole and SVH.

H.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table H-11.

Table H-11. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
Outline dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH and small via holes is not specified.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.

H.3.4.2.1 Dimensions of BGA Pads, etc.

Unless otherwise specified, the dimension tolerance for BGA pads, etc. shall be in accordance with the requirements specified in Table H-12.

Table H-12. Dimensions for BGA Pads, etc.

Unit. (mm)

Item			Tolerance
Pad size (conductor bottom size)	Dog-Bone	Pad (Figure H-8 a)	±0.05
		Fan-out direction (Figure H-8 b)	±0.075
	Via-in-Pad (Figure H-8 c)		±0.05
Solder resist opening diameter (resist surface)	Dog-Bone (Figure H-8 d)		±0.05
	Via-in-Pad (Figure H-8 d)		±0.05
Accurate alignment	Length of row of BGA pads		±0.05
Pad thickness (conductor thickness)			±0.01
Total board thickness (incl. solder resist)			±8%
Co-planarity (flatness): Normal state			0.05mm or less for diagonal diameter of BGA pads

H.3.4.3 Marking

The marking shall be produced with the marking inks specified in paragraph H.3.2.4, by copper etching or laser marking. The marking shall remain legible and shall not adversely affect any function, performance or reliability of printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

H.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

H.3.4.4 Structural Integrity

H.3.4.4.1 Through Holes

When printed wiring boards are tested as specified in paragraph H.4.5.5.1, the following requirements shall be satisfied (see Figure H-13).

a) Plating of through holes, small via holes, sidewall of outer perimeter, and SVH shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land.
b) Protrusion of plating caused by burr and nodules in through holes shall not reduce the hole diameter below its lower limit specified on manufacturing drawings.
c) Partial pits of plating shall not exceed 10% of the plating thickness specified in paragraph H.3.4.4.6.
d) Resin recession at the outer surface of the plated-through hole barrel shall be permitted, provided the maximum depth as measured from the barrel wall does not exceed 80μm, and the resin recession on any side of the plated-through hole does not exceed 40 % of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.
e) The pits of plating caused by negative etchback shall be permitted, provided that the negative etchback satisfies the requirements specified in paragraph H.3.4.4.5.

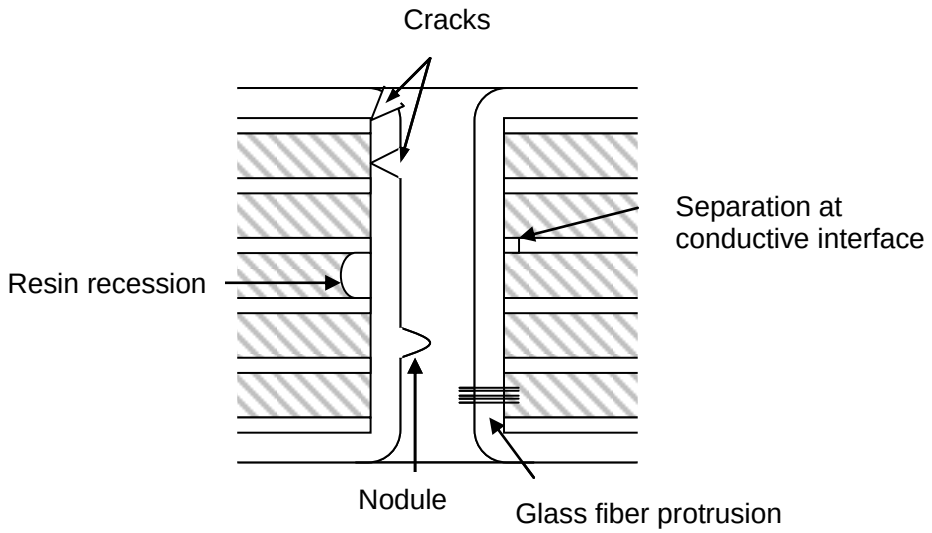


Figure H-13. Through Hole Defects

H.3.4.4.2 Voids

There shall not be any plating voids or laminate voids (see Figure H-14).

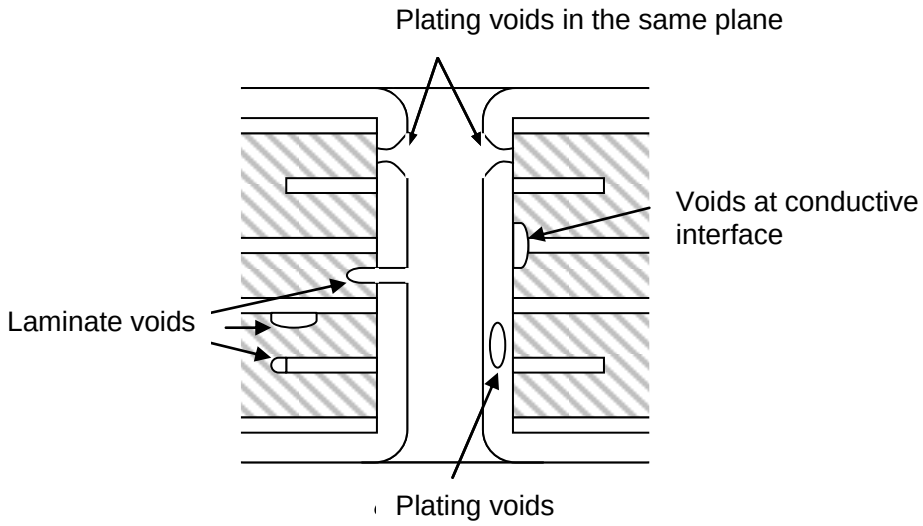


Figure H-14. Voids

H.3.4.4.3 Separation of Lands

Separation of lands shall not be permitted.

H.3.4.4.4 Cracks on Copper Foil

There shall not be any cracks on the copper foil in the external and internal layers.

H.3.4.4.5 Conductive interface

The resin smear at the interface of the through hole wall plating and an internal conductor layer shall not be permitted. Nail heading of a conductor layer shall not exceed 50 % of the metal foil thickness (see Figure H-15). Internal layer negative etchback shall not exceed 13µm.

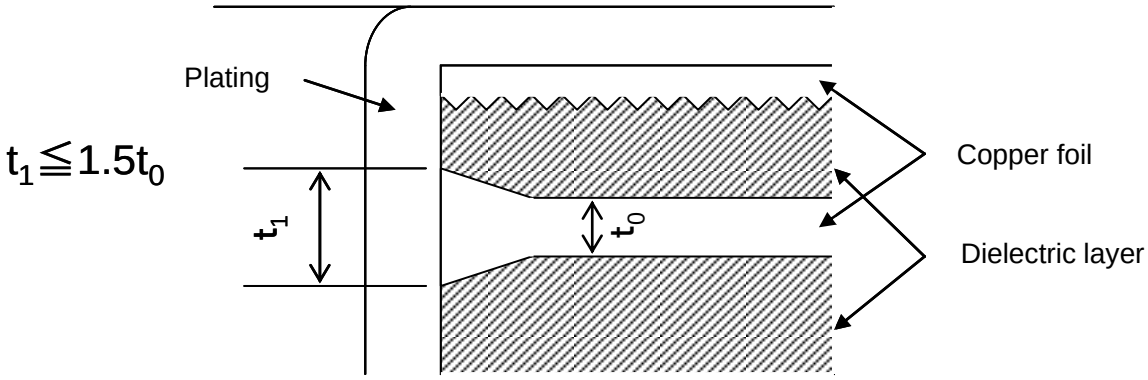


Figure H-15. Nail Heading

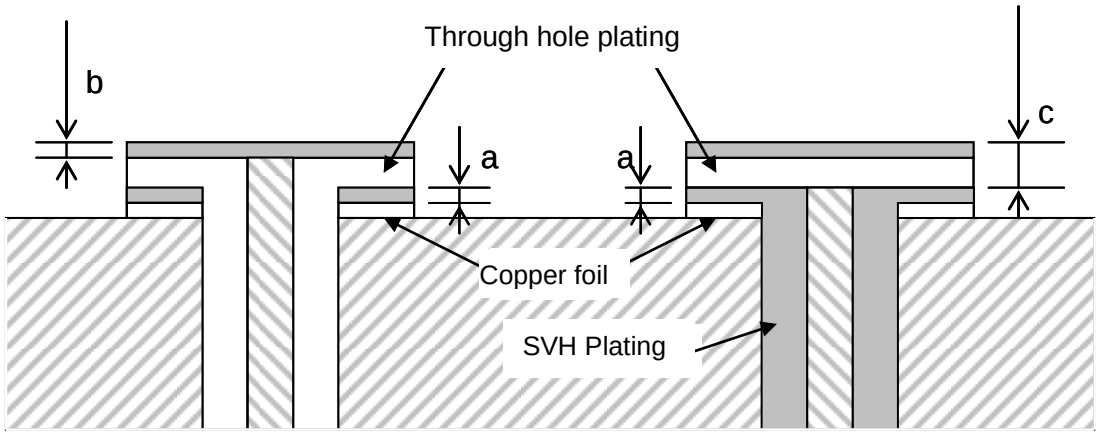
H.3.4.4.6 Plating thickness

Unless otherwise specified, the plating thickness and solder coating thickness shall meet the requirements specified in Table H-13.

Table H-13. Thickness of Plating and Solder Coating

Unit: μm

Type	Surface and through hole wall thickness		
Electroless copper plating	Thickness necessary and sufficient for electrolytic copper plating in the subsequent process		
Electrolytic copper plating	Via hole for part mount		25 as a minimum
	Small via hole		25 as a minimum
	SVH		30 as a minimum
	SVH plating on land (Figure H-16 a)		5 as a minimum
	Cap plating	Small via hole (Figure H-16 b)	As specified in detail specification
		SVH (Figure H-16 c)	As specified in detail specification
	Sidewall plating		25 as a minimum
Electrolytic gold plating	1.3 to 4.0		
Electrolytic nickel plating	5 as a minimum		
Solder coating	Thickness is not specified. However, the requirements of Solderability (paragraph H.3.10.2) shall be satisfied.		



a: SVH plating thickness on lands
b: Cap plating thickness on small via hole
c: Cap plating on SVH

Figure H-16. Cap Plating Thickness

H.3.4.4.7 Laminate Cracks

Cracks on laminate shall not be permitted.

H.3.4.4.8 Delamination and Blister

Delamination and blister shall not be permitted.

H.3.4.4.9 Layer-to-layer Registraion

The layer-to-layer registration error shall not exceed 0.15mm.

H.3.4.4.10 Annular Ring

The minimum annular ring of internal and external layer shall meet the requirements specified in Table H-14.

Table H-14. Annular Ring

Unit: mm

Through hole type	Layer	Annular ring
Through hole	External	0.05
	Internal	0.025
Non-through hole	External	0.38

H.3.4.4.11 Dielectric Layer Thickness

The dielectric layer between conductor layers of a multilayer printed wiring board shall not be less than 0.08mm in thickness.

H.3.4.4.12 Adhesion between Cap Plating and Filled Resin

When the cap plating is used as BGA pad, the gap between cap plating and filled resin shall be less than 5μm. When the cap plating is not used as BGA pad, the requirements specified in paragraph H.3.4.4.13 shall be satisfied (see Figure H-17).

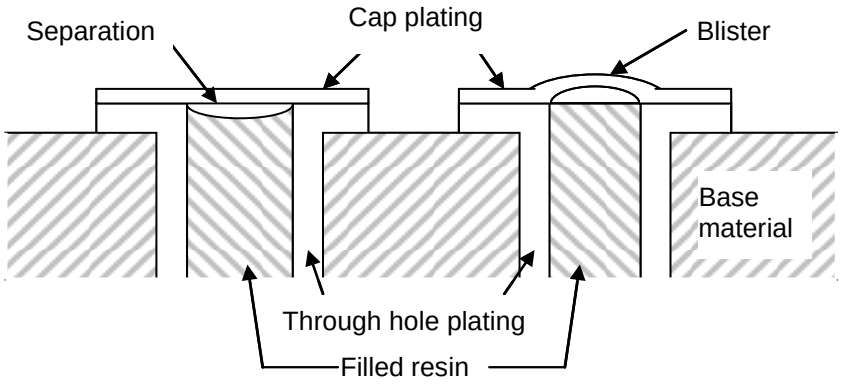


Figure H-17. Adhesion between Cap Plating and Filled Resin

H.3.4.4.13 Protrusion and Pit of Cap Plating

When the surface of the land where the resin wasn't filled underneath is used as a reference, the protrusion and pit of the filled resin shall not be more than 50µm and 76µm, respectively (see Figure H-18).

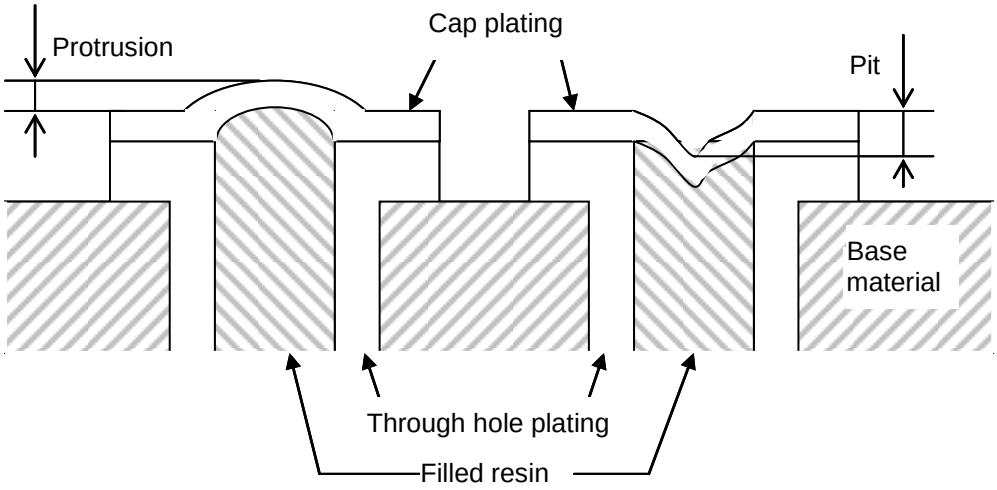


Figure H-18. Protrusion and Pit of Cap Plating

H.3.4.4.14 Filling of Resin

The resin shall be filled a minimum of 90% of the hole volume. The pit of the surface shall satisfy the requirements specified in paragraph H.3.4.4.13 (see Figure H-19).

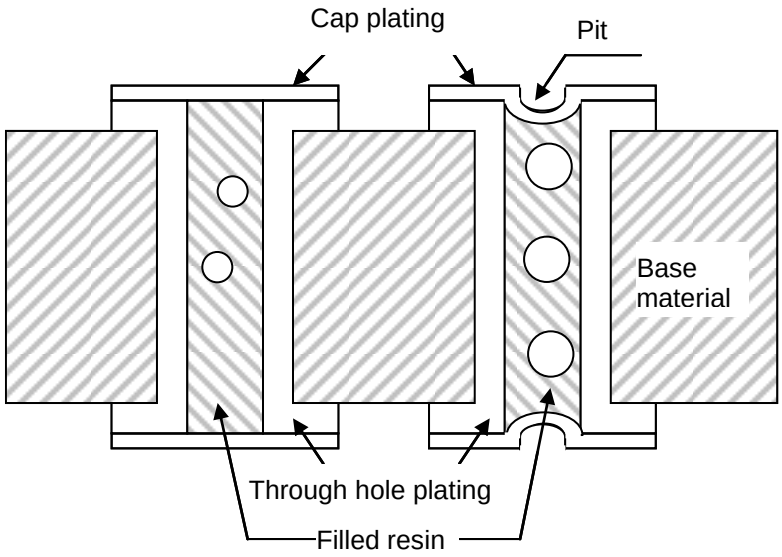


Figure H-19. Filling of Resin

H.3.4.5 Solder Resist Thickness

When printed wiring boards are tested as specified in paragraph H.4.5.6, the solder resist thickness shall not be less than 17.5μm, measured at the center of conductors.

H.3.5 Bow and Twist

When printed wiring boards are tested as specified in paragraph H.4.5.7, the maximum limit for bow and twist shall be 0.5%, unless otherwise specified on manufacturing drawings. For a split board, the percent bow and twist shall not exceed the value specified above, before separation.

H.3.6 Workmanship

The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could adversely affect the function, performance or reliability of the printed wiring boards. The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

H.3.6.1 Repair

The insulating plates, BGA conductor pads or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted, provided that the repaired solder resist thickness shall not be more than the surrounding solder resist thickness.

H.3.7 Plating Adhesion and Overhang

When printed wiring boards are tested as specified in paragraph H.4.5.9, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

H.3.8 Cleanliness

When printed wiring boards are tested as specified in paragraph H.4.5.10, the resistivity of the solvent extract shall not be less than $2x10^6 \Omega \cdot cm$.

H.3.9 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

H.3.9.1 Dielectric Withstanding Voltage

When tested as specified in paragraph H.4.5.11.1, printed wiring boards shall not exhibit insulation breakdown, flashover or sparkover.

H.3.9.2 Circuitry

When tested as specified in paragraph H.4.5.11.2, printed wiring boards shall not exhibit open circuit or short-circuiting between circuit patterns.

H.3.9.3 Connection Resistance

When printed wiring boards are tested as specified in paragraph H.4.5.11.3, the resistance between two lands connecting a circuit on all conductor layers shall not exceed the value (Ri) which is calculated by the formula specified below. When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.

$$Ri = 2\rho \frac{l}{W \cdot t} \ (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

H.3.9.4 Characteristic Impedance

When printed wiring boards are tested as specified in paragraph H.4.5.11.4, the characteristic impedance shall be within the range specified in the manufacturing drawing. If the tolerance is not specified, the impedance shall be within ±10% of the specified value.

H.3.10 Mechanical Performance

Printed wiring boards shall meet the following mechanical requirements.

H.3.10.1 Terminal Pull Strength

When tested as specified in paragraph H.4.5.12.1, printed wiring boards shall meet the following requirements. This provision shall not apply to SVH or small via holes.

a) Bond strength
The land shall withstand a minimum of 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph H.4.5.4.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected in accordance with paragraph H.4.5.5, there shall be no cracks, blistering, measling or delamination.

H.3.10.2 Solderability

When tested as specified in paragraph H.4.5.12.3, printed wiring boards shall meet the following requirements.

a) Through hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall not apply to SVH or small via holes.

b) Surface solderability
A minimum of 95 % of the surface conductor area shall be covered uniformly with fresh solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area.

H.3.10.3 Peel Strength of Surface Conductor

When tested as specified in paragraph H.4.5.12.2, printed wiring boards shall meet the requirements specified in the detail specification.

H.3.11 Environmental Performance

Printed wiring boards shall meet the following environmental requirements.

H.3.11.1 Thermal Shock

H.3.11.1.1 Thermal Shock (I) (applicable to qualification test)

When printed wiring boards are tested as specified in paragraph H.4.5.13.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph H.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

H.3.11.1.2 Thermal Shock (II) (applicable to quality conformance inspection)

When printed wiring boards are tested as specified in paragraph H.4.5.13.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph H.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

H.3.11.2 Humidity and Insulation Resistance

When printed wiring boards are tested as specified in paragraph H.4.5.13.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be a minimum of 500MΩ.

H.3.11.3 Hot Oil Resistance

When printed wiring boards are tested as specified in paragraph H.4.5.13.3, the change in connection resistance between circuits before and after the test shall be less than 10%.

H.3.11.4 Thermal Stress

When tested as specified in paragraph H.4.5.13.4, printed wiring boards shall meet the following requirements.

a) Externals
There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Structural Integrity
In the vertical microsection of through holes, the following requirements shall be satisfied.

1) Through hole
There shall be no corner cracks or barrel cracks.

2) Laminate void
When the conductor spacing on the same plane or between layers satisfies the minimum conductor spacing specified in the manufacturing drawings, the spacing shall not exceed 76μm.

3) Lifting of lands
Lifting of lands after thermal stress test shall be permitted.

4) Cracks on copper foil
There shall be no cracks which penetrate through the copper foil.

5) Internal layer connection
There shall be no separation between copper foil of internal layer and through hole plating.

6) Laminate Cracks
After the thermal stress test, the laminate cracks between the lands of a through holes or on the lands shall not exceed 80μm, and the laminate cracks other than the ones on the land area shall not cause the spacing between adjacent conductors fall below the minimum conductor spacing.

7) Delamination and blister
There shall be no delamination and blisters.

8) Adhesion of cap plating and filled resin

The interface between cap plating and filled resin shall meet the requirements specified in paragraph H.3.4.4.12.

H.3.11.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph H.4.5.13.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall not be less than 500MΩ. After the test, the requirements specified in paragraph H.3.9.1 shall be satisfied.

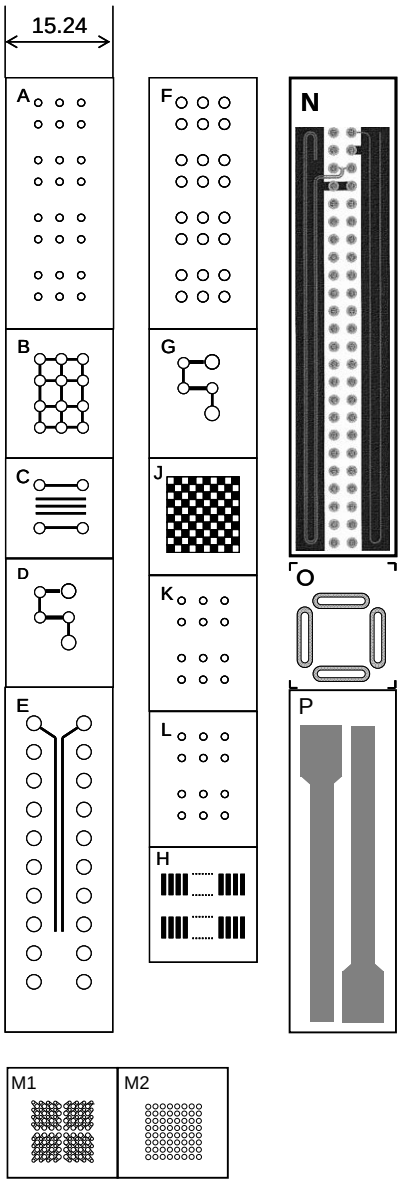
H.4. Quality Assurance Provisions

H.4.1 Test Pattern

The test pattern provided for qualification test and quality conformance inspection shall be in accordance with Figure H-20. The test pattern shall have the same structure as the product produced from the identical work board.
A set of the test pattern shall be assigned for each printed wiring board.

Arrangement of test pattern

Unit: mm



Notes

(1) Unless otherwise specified, the conductor width shall be 0.5±0.1mm.

(2) Test coupon A indicates the minimum hole diameter of the through hole (incl. small via hole) for the corresponding printed wiring board, and the land diameter shall be the minimum land diameter of the through holes. When applied, small via holes shall be filled with resin. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes and diameter shall be ϕ0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(4) The patterns of test coupons D and G vary depending on the number of layers and via hole structure. Each coupon shall be produced so as to form the same number of layers and via hole structure as those of the corresponding product, and to have a circuit continuity through all layers by via holes. The hole and land diameter shall be the minimum diameter for each SVH and small via hole of the corresponding products, and the land shape shall be the typical land shape of the products. On both ends of the printed wiring board, through holes shall be formed to measure the resistance, the diameter of the land and hole shall be ϕ1.8mm and ϕ0.8mm, respectively. The hole diameter tolerance is not specified.

(5) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist shall be the clearance diameter for the corresponding printed wiring board. If the hole diameter for the product is unknown, the land diameter shall be equal to the land diameter + 0.2mm.

(6) Test coupons K and L shall be prepared only when the corresponding products have SVH. Those coupons vary depending on the number of layers and via hole structure.
The land shall be formed only on the layers which are connected by SVH.

(7) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. The conductors shall be formed on all layers in accordance with this figure.

(8) The arrangement of test coupons shown in this figure is an example; a different arrangement is also acceptable.

(9) The symbols of test coupons (A to H and J to M2) shall be used for identification and not for the object of inspection. The marking method is not specified.

(10) Only when the BGA pads, etc. are required, the test coupon M1 (Dog-bone structure) or test coupon M2 (VIP structure) shall be formed in accordance with the pad structure. An example of test coupons M1 and M2 is shown to the left. See detail specification for more detailed information.

(11) Only when the characteristic impedance is required, the test coupon N shall be formed.

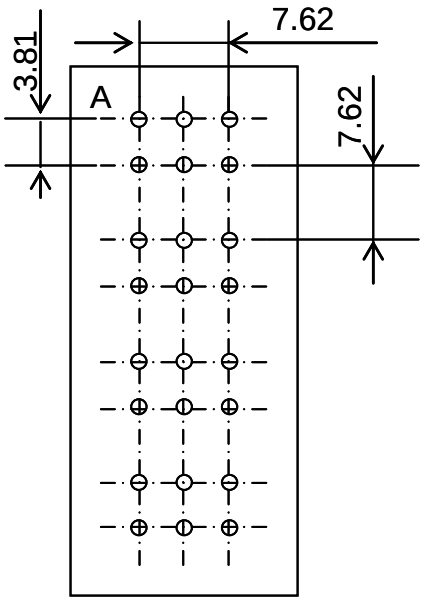
(12) Only when the outer perimeter sidewall plating is required, the test coupon O shall be formed. An example of test coupons O is shown to the left. See detail specification for more detailed information.

(13) Only when the structure where copper foil is laminated on the outer layer is required, the test coupon P shall be formed.

Figure H-20. Test Coupon (1/11)

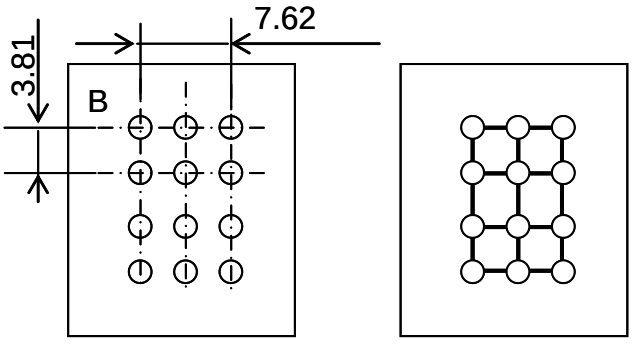
Unit: mm

Test coupon A



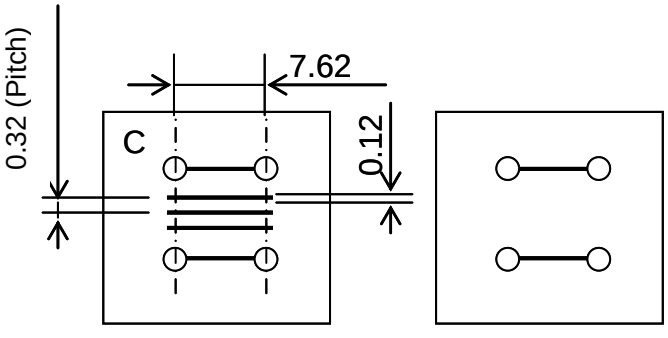
Internal and external layer

Test coupon B



External layer Internal layer

Test coupon C

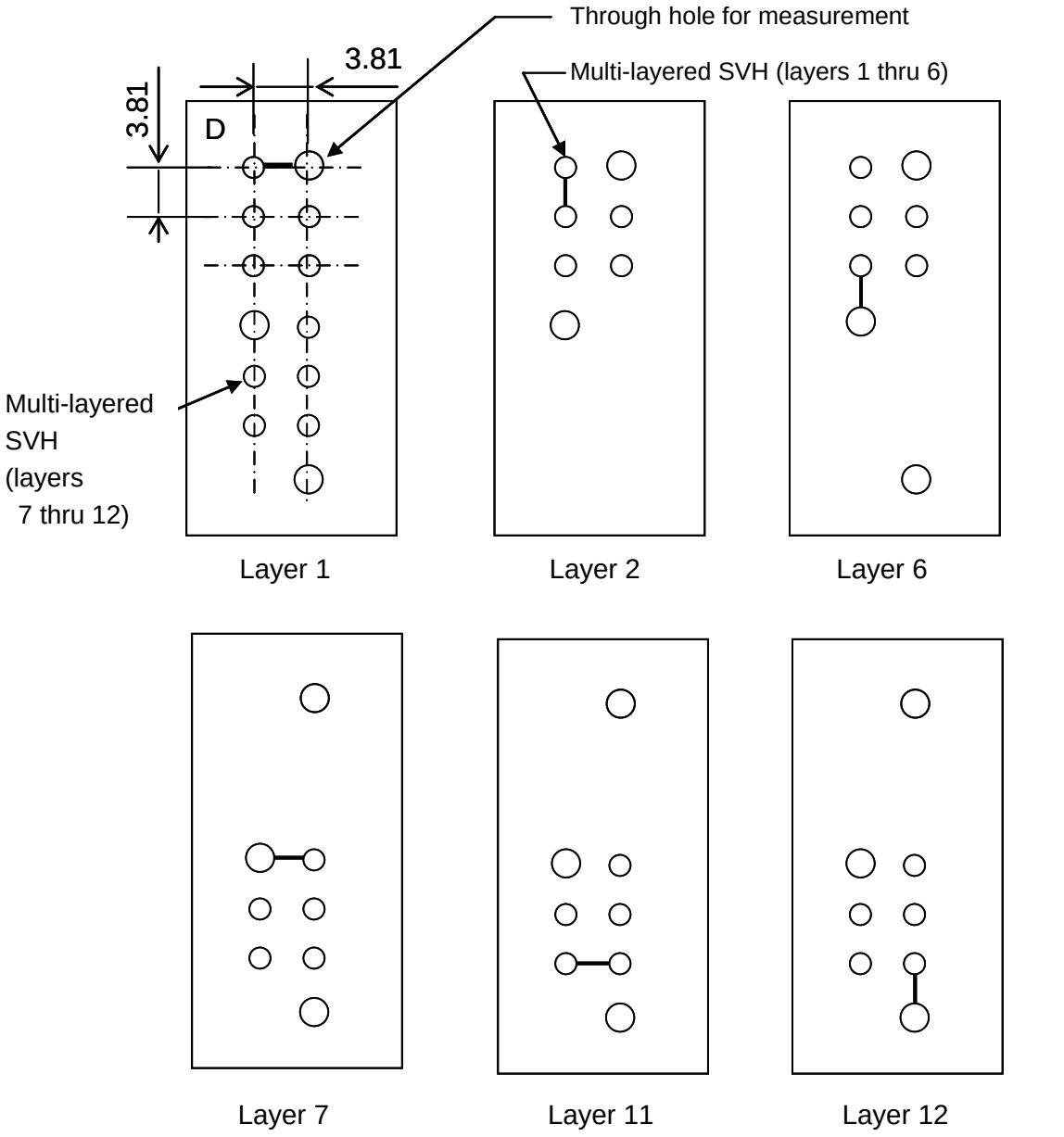


External layer Internal layer

Figure H-20. Test Coupon (Multi-layer Boards) (2/11)

Test coupon D and G

Unit: mm

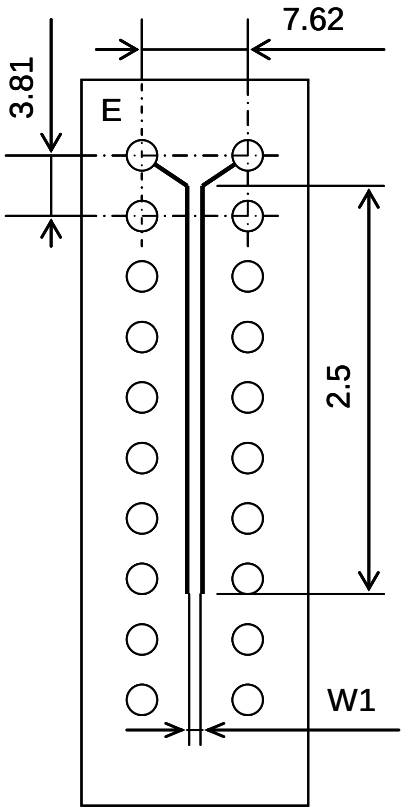


This figure shows an example of layers 1 through 6 and 7 through 12 of SVH.

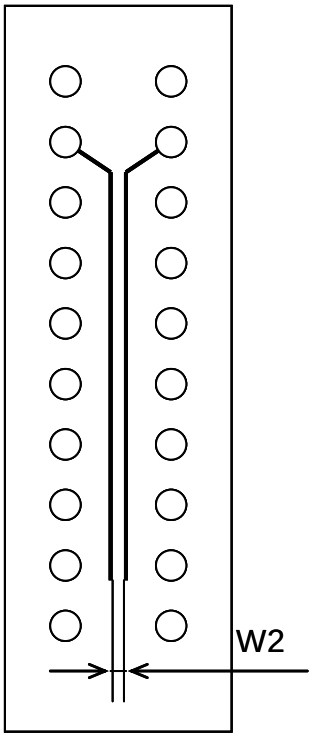
Figure H-20. Test Coupon (Multi-layer Boards) (3/11)

Unit: mm

Test coupon E

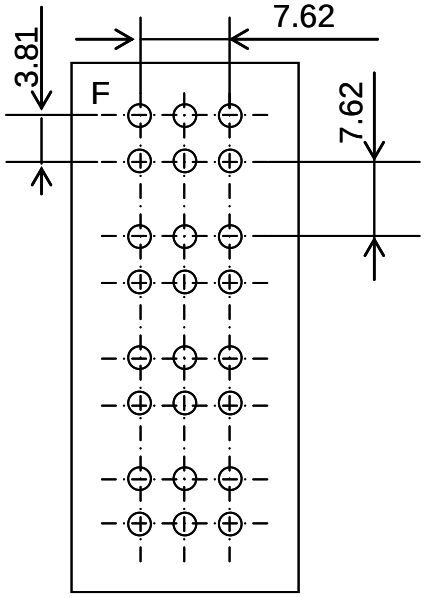


Layer 1



Layer 2

Test coupon F



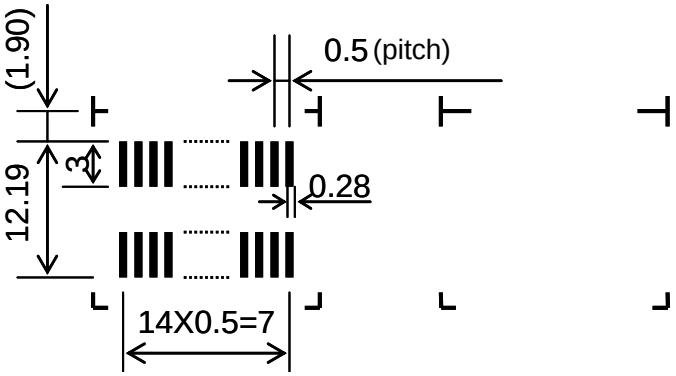
External and Internal layer

W1: Minimum conductor spacing on the external layer of the product or 0.14mm
W2: Minimum conductor spacing on the internal layer of the product or 0.08mm

Figure H-20. Test Coupon (Multi-layer Boards) (4/11)

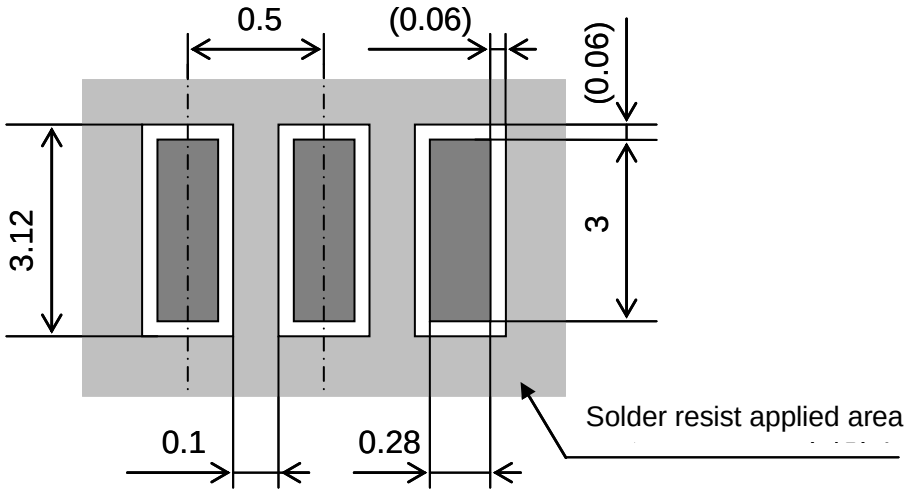
Test coupon H

Unit: mm



Number of pads: 15
(in this range)

Top surface Bottom surface (no pattern)

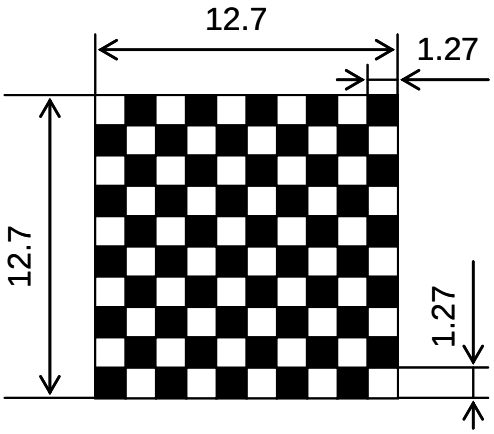


Enlarged view of pad area

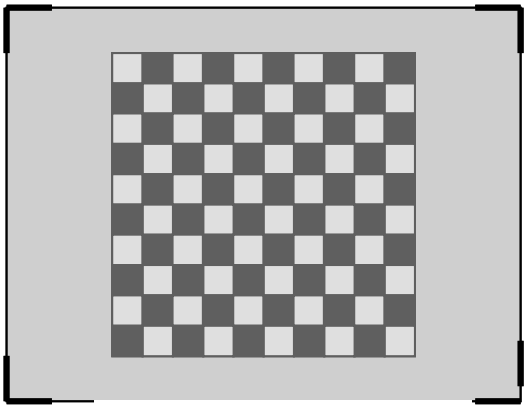
Figure H-20. Test Coupon (Multi-layer Boards) (5/11)

Test coupon J

Unit:mm

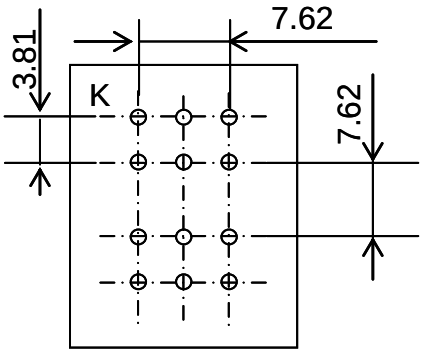


Top and bottom surface
表面及び裏面

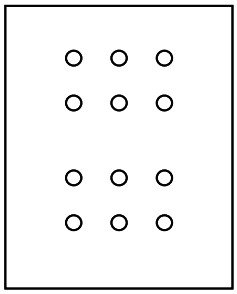


Solder resist applied area
ソルダレジスト塗布範囲

Test coupons K and L



External layer

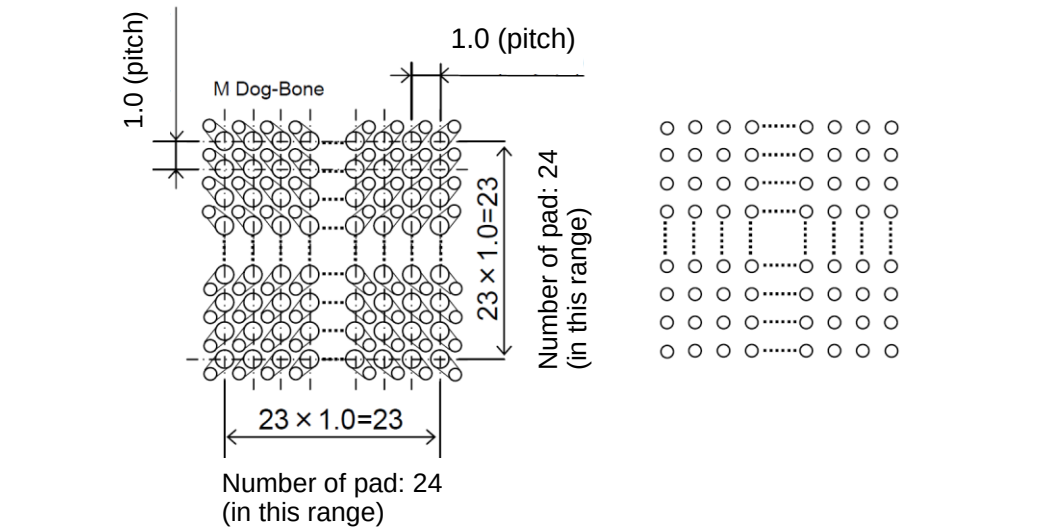


Internal layer (SVH layer)

Figure H-20. Test Coupon (Multi-layer Boards) (6/11)

Test coupon M1 (Dog-Bone structure)

Unit:mm



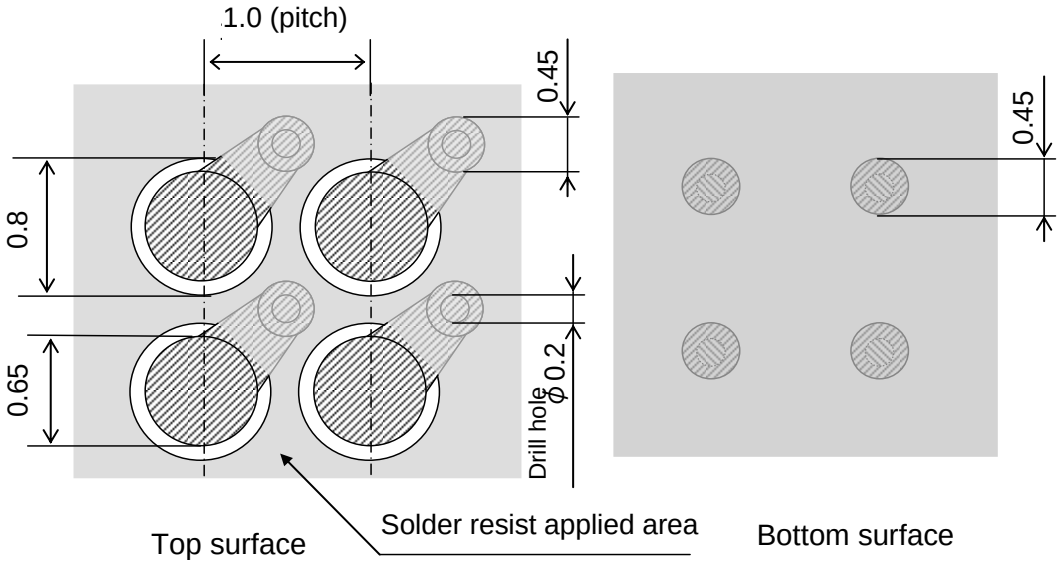


Figure H-20. Test Coupon (Example of BGA pads) (7/11)

Test coupon M2 (VIP structure)

Unit:mm

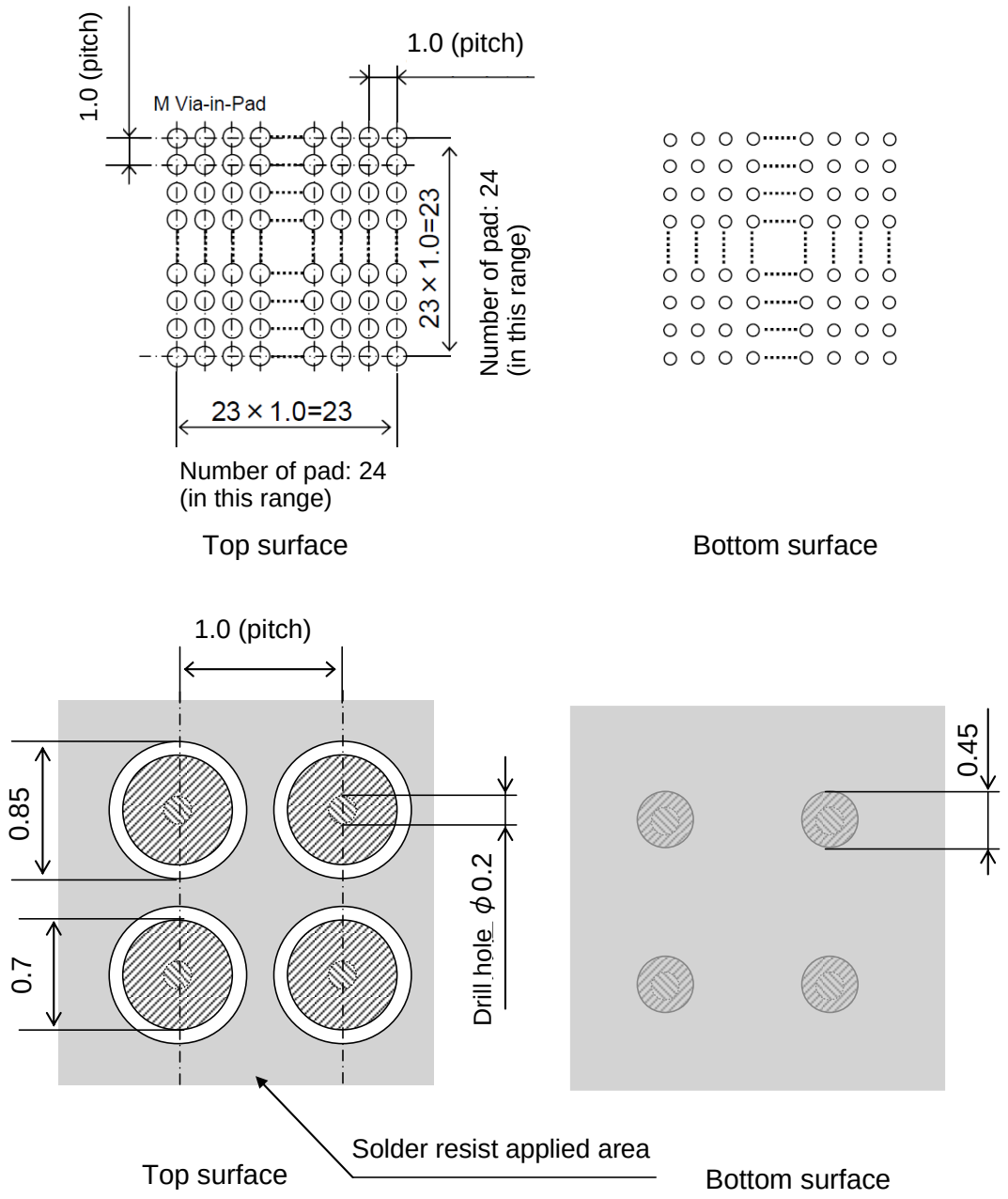
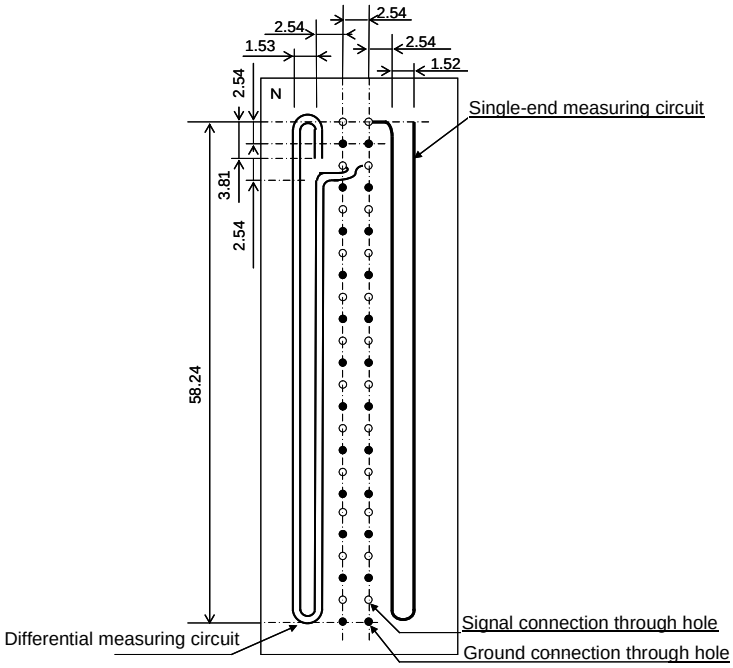
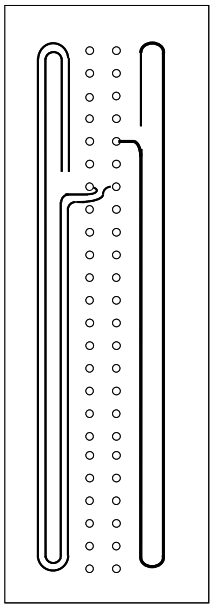


Figure H-20. Test Coupon (Example of BGA pads) (8/11)

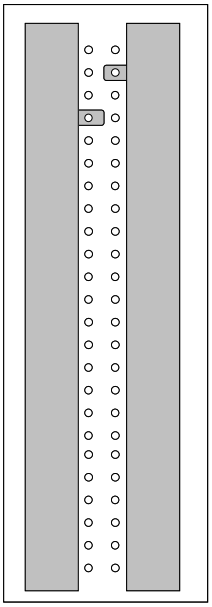
Test coupon N

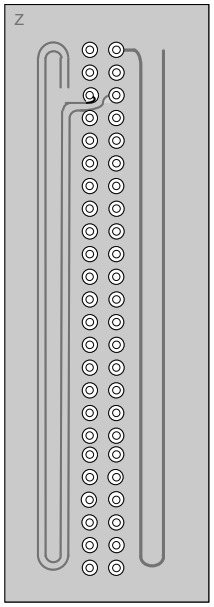




External layer

Internal layer (impedance control layer)





Internal layer (ground layer)

Solder resist applied area

Figure H-20. Characteristic Impedance Test Coupons (9/11)

Test coupon O

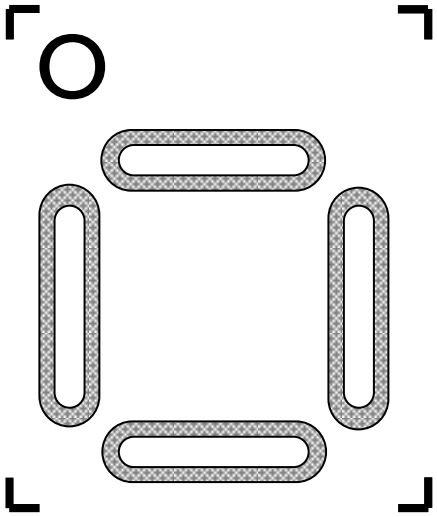
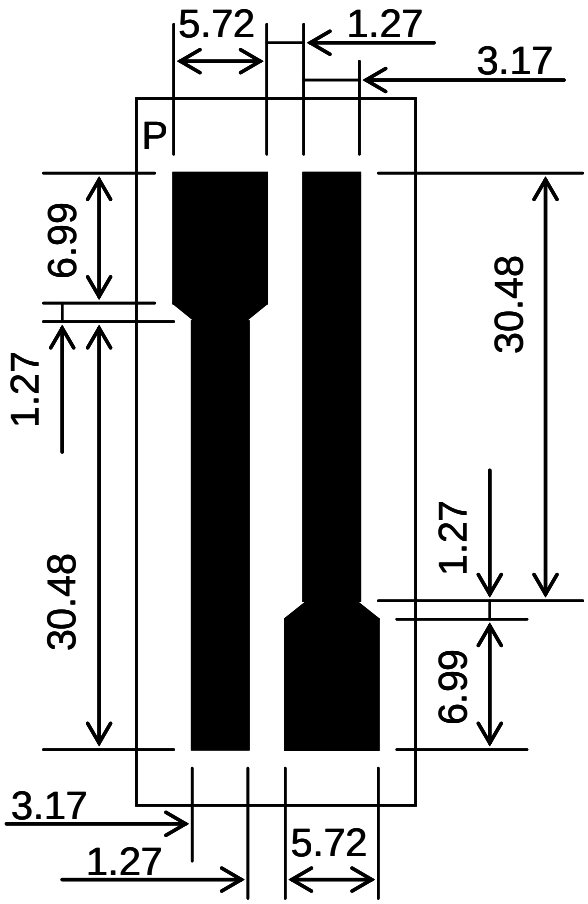


Figure H-20. Test Coupons (10/11)

Test coupon P

Unit:mm



Front surface and back surface

Figure H-20. Peel Strength Test Coupons (11/11)

H.4.2 In-Process Inspection

The in-process inspection specified in Table H-15 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs H.3.4.1 (Externals of Conductor, Base Material and Solder Resist), H.3.4.2 (Dimensions), H.3.4.3 (Marking), H.3.8 (Cleanliness), and H.3.4.2.1 (Dimensions of BGA Pads, etc)

Table H-15. In-Process Inspection

No.	Item	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	H.3.4.1 H.3.4.2 H.3.4.3	H.4.5.4.1 H.4.5.4.2 H.4.5.4.3	All	After forming internal circuit and before pre-treating the laminate layer
2	Conductor of external layer Base material of external layer	H.3.4.1.1 H.3.4.1.2	H.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	H.3.8	H.4.5.10	Sampling([1])	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	H.3.4.2.1	H.4.5.4.2	All	After forming solder resist and before solder coating

Note ([1]) Sampling inspection shall be performed based on 1.0% of the acceptable quality level (AQL) in "Normal Inspection Level II" specified in JIS Z 9015-1. The lot shall be processed in the same circuit forming process on the same day the sampling inspection was performed and can be subjected to solder resist application.

H.4.3 Qualification Test

H.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole and number of layers sufficient to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board. In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include a deep-hole-shape slit, V-groove cut and continuous perforation.

H.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table H-16. Upon completion of Group I and II tests, Group III through VIII tests shall be performed using specimens allocated to the appropriate group tests. Group III through VIII tests may be performed in any order regardless of group number. However, tests in each of Group III through VIII shall be performed in the order listed. Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table H-16.

Table H-16. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail Criteria		
					Samples		Quantity of allowable defects
Group	Order	Test item			Production printed wiring boards	Test coupon (1) (2)	
I	1	Externals of conductor, base materials, and solder resist Externals, dimensions, Dimensions Marking	H.3.4.1 H.3.4.2 H.3.4.3	H.4.5.4.1 H.4.5.4.2 H.4.5.4.3	No. 1 to No. 6	A, B, C, D, E, F, G, H, K, L, M, N, O and P	0
	2	Workmanship	H.3.6	H.4.5.8			
	3	Characteristic impedance	H.3.3.15	H.4.5.11.4		N	
II	1	Plating adhesion and overhang	H.3.7	H.4.5.9	No. 1 to No. 6	C	
	2	Bow and twist	H.3.5	H.4.5.7		N/A	
III	1	Structural integrity	H.3.4.4	H.4.5.5	No. 1	A, F, K, M and O	
	2	Terminal pull strength	H.3.10.1	H.4.5.12.1		F	
	3	Solder resist thickness	H.3.4.5	H.4.5.6		J	
	4	Peel strength of surface conductor(3)	H.3.10.3	H.4.5.12.2		P	
IV	1	Connection resistance	H.3.9.3	H.4.5.11.3	No. 2	D	
	2	Hot oil resistance	H.3.11.3	H.4.5.13.3			
	3	Connection resistance	H.3.9.3	H.4.5.11.3			
V	1	Circuitry	H.3.9.2	H.4.5.11.2	No. 3	E and G(4)	
	2	Connection resistance	H.3.9.3	H.4.5.11.3			
	3	Thermal shock (I)	H.3.11.1.1	H.4.5.13.1a)			
	4	Circuitry	H.3.9.2	H.4.5.11.2			
	5	Connection resistance	H.3.9.3	H.4.5.11.3			
VI	1	Humidity and insulation resistance	H.3.11.2	H.4.5.13.2	No. 4	E	
	2	Dielectric withstanding voltage	H.3.9.1	H.4.5.11.1			
VII	1	Thermal stress	H.3.11.4	H.4.5.13.4	No. 5	A, B, L M and O	
	2	Solderability	H.3.10.2	H.4.5.12.2		B and H(5)	
VIII	1	Radiation hardness	H.3.11.5	H.4.5.13.5	No.6	N/A	
-	-	Materials	H.3.2	H.4.5.2	N/A		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through VIII tests. For Group II through VIII tests, one test coupon shall be provided for each coupon type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through VIII tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) This test shall be performed when copper foil laminate structure is under the qualification coverage.

(4) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(5) The test coupons B and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

H.4.4 Quality Conformance Inspection

H.4.4.1 Quality Conformance Inspection (Group A)

H.4.4.1.1 Sample

The quality conformance inspection shall be performed with the test coupons. The test coupons and sample product shall be manufactured simultaneously. Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen. A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

H.4.4.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table H-17. The inspections within each group shall be performed in the order listed. One test coupon shall be provided for each of Group IV and V test.

Table H-17. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria		
					Quantity of samples		Quantity of allowable defects
Group	Order	Inspection item			Production printed wiring boards	Test coupon	
I	1	Design and construction	H.3.3	H.4.5.3	All	N/A	0
	2	Externals of conductor, base materials, and solder resist Externals, dimensions, Dimensions Marking	H.3.4.1 H.3.4.2 H.3.4.3	H.4.5.4.1 H.4.5.4.2 H.4.5.4.3			
	3	Workmanship	H.3.6	H.4.5.8			
	4	Characteristic impedance	H.3.3.15	H.4.5.11.4		N[(1)]	
II	1	Bow and twist	H.3.5	H.4.5.7	All	N/A	
III	1	Circuitry	H.3.9.2	H.4.5.11.2	All	N/A	
IV	1	Thermal stress	H.3.11.4	H.4.5.13.4	N/A	A, F, K[(2)], M[(3)] and O[(4)]	
V	1	Solderability	H.3.10.2	H.4.5.12.2	N/A	F and H[(5)]	

Notes:

(1) Test coupon N shall be inspected when characteristic impedance is required.

(2) Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the products is provided with SVH.

(3) Test coupon M shall be inspected when the products is provided with BGA pads, etc.

(4) Test coupon O shall be inspected when the sidewall plating is required.

(5) Test coupons F and H shall be subjected to the tests for hole solderability and surface solderability, respectively.

H.4.4.2 Quality Conformance Inspection (Group B)

H.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection are manufactured and selected from the lot which passed Group A inspection.

H.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table H-18. The inspections within each group shall be performed in the order listed. One test coupon shall be subjected to each of test Groups.

Table H-18. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	H.3.7	H.4.5.9	C	0
II	1	Terminal pull strength	H.3.10.1	H.4.5.12.1	F	
III	2	Connection resistance	H.3.9.3	H.4.5.11.3	D	
	3	Hot oil resistance	H.3.11.3	H.4.5.13.3		
	4	Connection resistance	H.3.9.3	H.4.5.11.3		
IV	1	Circuitry	H.3.9.2	H.4.5.11.2	E and G(1)	
	2	Connection resistance	H.3.9.3	H.4.5.11.3		
	3	Thermal shock (II)	H.3.11.1.2	H.4.5.13.1b)		
	4	Circuitry	H.3.9.2	H.4.5.11.2		
	5	Connection resistance	H.3.9.3	H.4.5.11.3		
V	1	Humidity and insulation resistance	H.3.11.2	H.4.5.13.2	E	
	2	Dielectric withstanding voltage	H.3.9.1	H.4.5.11.1		
VI	1	Peel strength of surface conductor	H.3.10.3	H.4.5.12.2	P(2)	

Notes:

(1) Under the circuitry test, the test coupons G and E shall be subjected to the continuity test and circuit shorts test, respectively.

(2) Peel strength of surface conductor is performed when copper foil laminate structure is used. If copper foil laminate structure is in qualification coverage however, group B inspection is performed on a sample without this structure, the inspection shall be performed again on the first lot of the products with this structure.

H.4.5 Methods for Test and Inspection

H.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

H.4.5.2 Materials

The copper clad laminates, prepreg and copper foil shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.

H.4.5.3 Design and Construction

The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.

H.4.5.4 Externals, Dimensions, Marking and Others

H.4.5.4.1 Externals of Conductor, Base Material and Solder Resist

External inspection shall be performed with 4X to 10X magnifier.

a) Conductors
For conductive pattern inspection, Automatic Optical Inspection machine (AOI) can be used. Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

b) Base Materials
Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

c) Solder Resist
Pass or fail shall be determined by using 10X magnifier.

H.4.5.4.2 Dimensions

Dimensions shall be measured by using a measuring instrument with sufficient accuracy.

a) Dimensions of BGA pads, etc.
The dimensions of printed wiring boards with BGA pads, etc. shall be measured as follows. For the board with multiple BGA pads, the BGA pad with the largest area shall be selected for measurement. If all the BGA pad areas are the same size, any one of the pad shall be selected for measurement. The detailed measurement sections shall be shown in Figure H-21.

1) Dimension of BGA pads and solder resist opening diameter
Each section of grid corner (outer) of the center area (inner) shall be measured by an optical measuring instrument.

2) Position accuracy for BGA pads, etc.
The directions of X and Y axes of circumference for BGA pads shall be measured with a 2-dimension end-measuring machine or an equivalent measuring instrument sufficient enough for measurement.

3) Height from the base material for BGA pads, etc. (pad thickness)
Each section of grid corner (outer) and the center area (inner) shall be measured by the focal depth method using a metallograph.

4) Total board thickness for BGA pads, etc.
For the total board thickness including solder coating and solder resist, the center section shall be measured by using a micrometer.

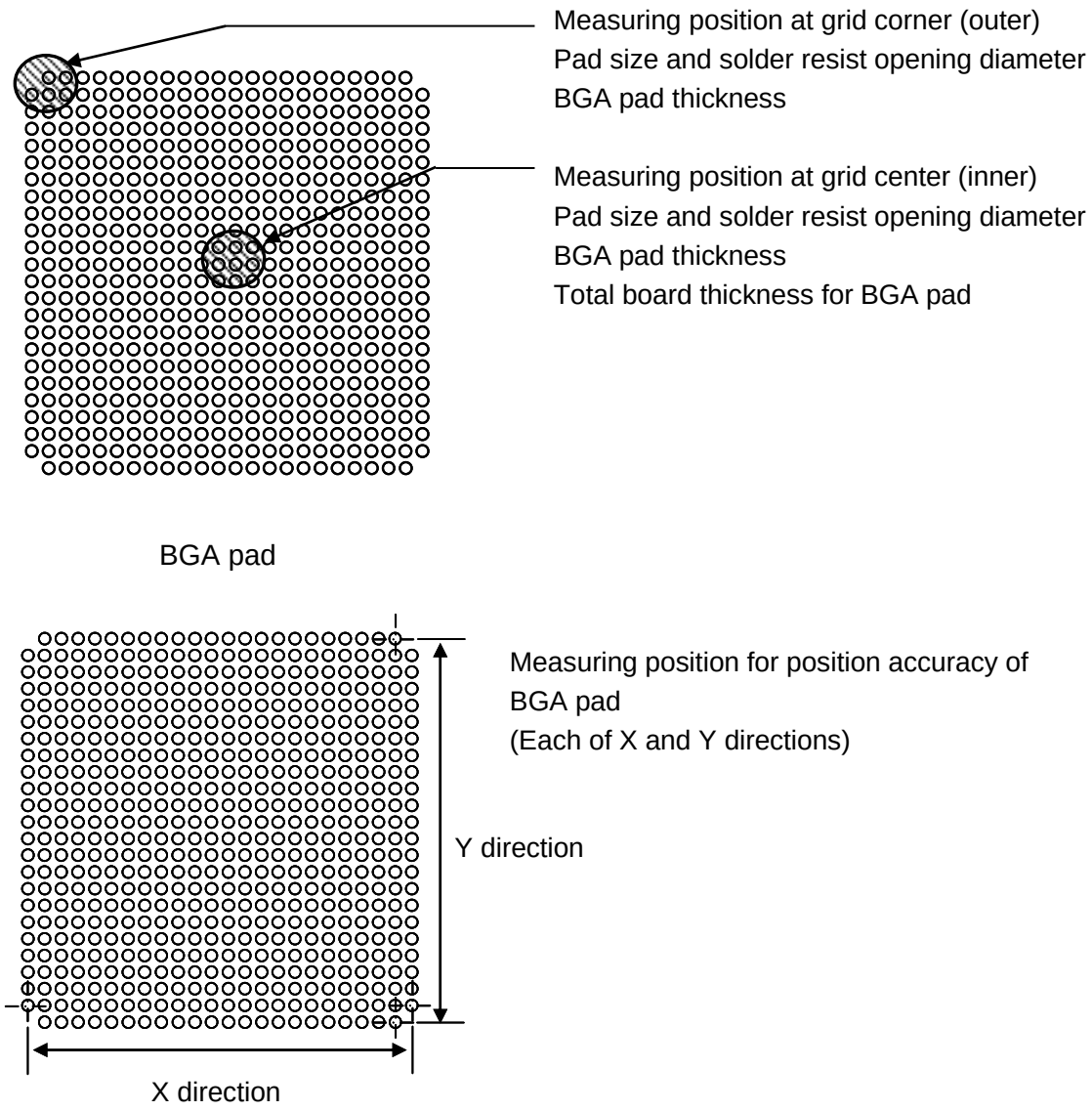


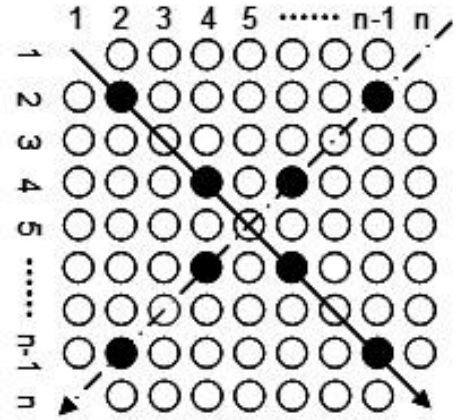
Figure H-21. Measuring Points for BGA Pad

5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure H-22)

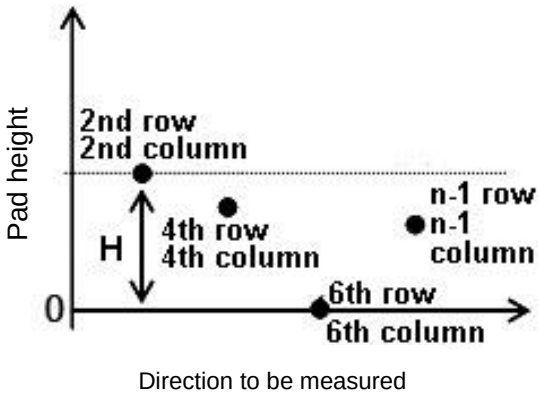
Directions of the pad to be measured



Direction 1 Direction 2

●: Pad to be measured

Co-planarity



H: Co-planarity (at max.)

Figure H-22. Measuring of Co-Planarity

H.4.5.4.3 Marking

Marking shall be inspected visually (naked eyed inspection).

H.4.5.5 Structural Integrity

H.4.5.5.1 Through Holes

a) Vertical microsection

The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated in resin and polished to expose the center of the hole. At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. For measurement of layer to layer registration and annular ring, the hole to be measured shall be far from the starting point of drilling. The vertical microsection shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

Soft etching to clarify the borderline of copper plating and copper foil shall not be conducted at the observation of internal connection and resin smear.

b) Horizontal microsection
Multilayer boards with through holes shall be encapsulated in resin and polished. A conductor layer shall be polished in the parallel direction to expose the conductor layer. The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching shall not be performed on the cross section surface.

H.4.5.5.2 Voids

The microsection prepared in paragraph H.4.5.5.1 a) shall be inspected for any void at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.3 Lifting of Lands

Lands shall be inspected for any lifting by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.4 Cracks on Copper Foil

Copper foil shall be inspected for any crack by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.5 Internal Layer Connection

Internal layer connection shall be inspected by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.6 Plating Thickness

Plating thickness shall be inspected by using the microsection prepared in paragraphs H.4.5.5.1 a) and b) at a magnification of 200X as a minimum. Plating thickness shall be the average value of three measurements for a plated through hole. If any of the measured value is significantly different from the other values, the value shall not be used for calculating the average.
Cap plating thickness shall be measured at the thinnest area of a hole.

H.4.5.5.7 Laminate Cracks

Laminate shall be inspected for any crack by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.8 Delamination and Blister

The microsection prepared in paragraph H.4.5.5.1 a) shall be inspected for any delamination and blister at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.9 Layer-to-layer registration

The layer-to-layer registration shall be measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 25 to 100X. The misregistration shall be measured around the hole in the direction parallel to the board length and the vertical direction. The microsections for inspection of layer-to-layer misregistration shall be prepared by cutting the multi-layer printed wiring board in the direction parallel to the board length for at least one hole and the vertical direction for another one hole as a minimum. (See Figure H-23)

H.4.5.5.10 Annular ring

The annular ring shall be measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 25 to 100X. The measurement of the annular ring on an external layer shall be from the surface of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure H-23).

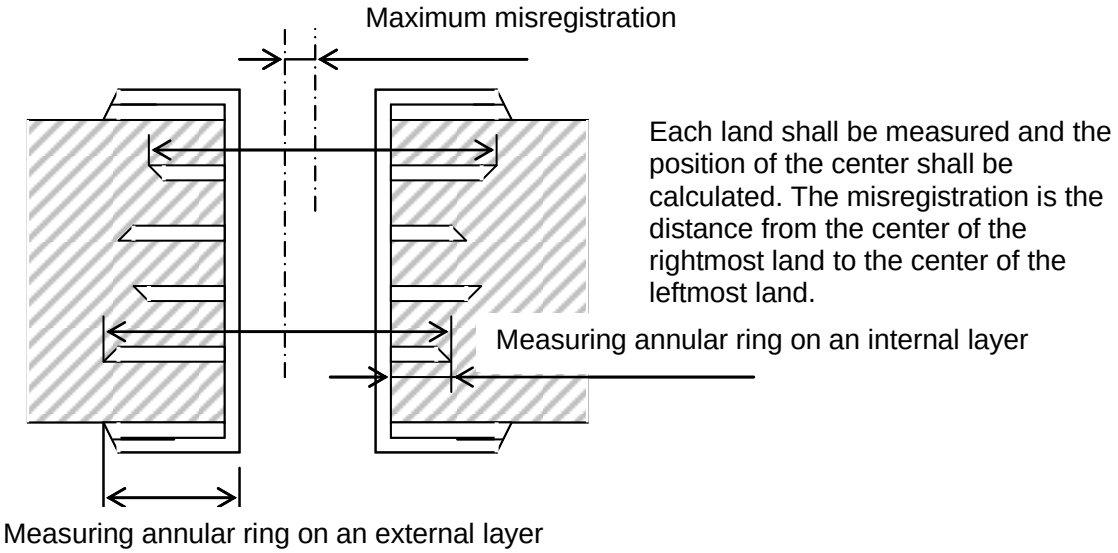


Figure H-23. Measurement of Layer-to-Layer Misregistration and Annular Ring

H.4.5.5.11 Insulation Layer Thickness

Insulation Layer Thickness shall be measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X.

H.4.5.5.12 Adhesion of Cap Plating and Filled Resin

Adhesion of cap plating and filled resin shall be observed and measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50 to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

H.4.5.5.13 Protrusion and Pit of Cap Plating

Protrusion and pit of cap plating shall be observed and measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 50X as a minimum.

H.4.5.5.14 Filling of Resin

Filled resin shall be observed and measured by using the microsection prepared in paragraph H.4.5.5.1 a) at a magnification of 25 to 50X.

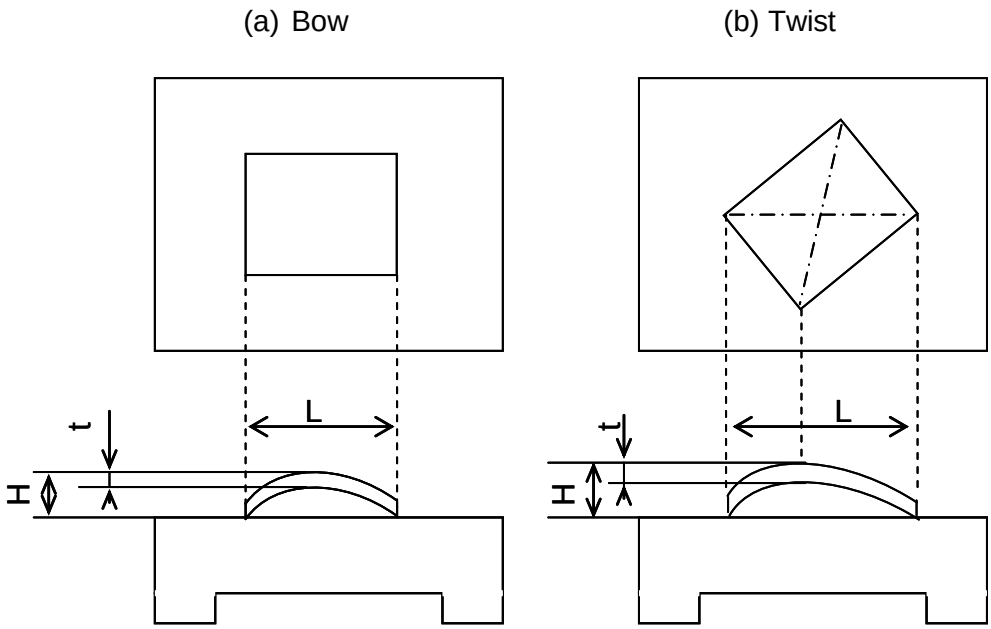
H.4.5.6 Solder Resist Thickness

Solder resist shall be cut vertically near the conductor and encapsulated in resin and polished to expose the center of the conductor. The solder resist thickness shall be measured at a magnification of 200X as a minimum.

H.4.5.7 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure H-24).
The bow and twist shall be calculated as follows.
The percent bow and twist shall be calculated by the following formula.

$$\text{Percent bow and twist} = \frac{H\text{-}t}{L} \times 100\ (\%)$$



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure H-24. Measurement of Bow and Twist

H.4.5.8 Workmanship

The workmanship of the printed wiring boards shall be inspected at a magnification of 4 to 10X.

H.4.5.9 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and a minimum of 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

H.4.5.10 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 % by volume of isopropyl alcohol and 25 % by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6\Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy. The alternate test methods specified in Table H-19 may be used to perform the cleanliness test.

Table H-19. Equivalent Measuring Method

Method	Resistivity ($\times 10^6\Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.2

Note: (1) Alpha Metals Incorporated, “Omega Meter”

H.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

H.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

H.4.5.11.2 Circuitry

a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

H.4.5.11.3 Connection Resistance

The resistance between the through hole terminals shall be measured by using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5 mΩ.

H.4.5.11.4 Characteristic Impedance

The characteristic impedance shall be measured in accordance with Paragraph 2.5.5.7 of IPC-TM-650.

H.4.5.12 Mechanical Performance

The mechanical performance tests shall be performed as follows.

H.4.5.12.1 Terminal Pull Strength

A conductor shall be cut with a sharp knife at a minimum of 6mm from the land, peeled and pulled toward the land, and shall be cut off by applying the sharp knife at the joining point of the conductor and land without degrading the land adherence strength. Then, a lead wire sufficient in length for installing a tensile tester shall be inserted in the hole and soldered. After that, a cycle of solder removal and resoldering by using a soldering iron shall be performed.

a) A lead wire shall be soldered in to the through hole.
b) The lead wire shall be removed from the through hole (solder removal).
c) A lead wire shall be resoldered in to the through hole.
d) The lead wire shall be removed from the through hole (solder removal).
e) A lead wire shall be resoldered in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the required minimum. Upon completion of e) resoldering, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Breaking off or pulling out the lead wire shall not be regarded as a failure, and a new lead wire shall be soldered and pulled. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

H.4.5.12.2 Peel Strength of Surface Conductor

The peel strength of surface conductor is performed in accordance with Paragraph 2.4.8 of IPC-TM-650 and as follows.

a) Normal state
   Test condition A shall be applied.
b) After Thermal stress
   Test condition B shall be applied.

H.4.5.12.3 Solderability

a) Hole solderability
   The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph H.4.5.5.1.
b) Surface solderability and sidewall plating
   After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

H.4.5.13 Environmental Performance

The environmental performance tests shall be performed as follows.

H.4.5.13.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
   The test shall be performed under the test condition B. However, the lowest temperature shall be -30°C and the number of cycle shall be 1000 cycles. The time for step 2 and 4 shall be within 2 minutes each. Reflow soldering of total heating process in accordance with JERG-0-043 shall be performed three times as a pre-treatment of the printed wiring board. The heating condition shall be as follows.
   1) Heating condition: 200°C min. for 45 seconds min.
   2) Peak temperature: 230°C min.

b) Thermal shock (II) (applicable to quality conformance inspection)

The test shall be performed under the test condition B-3 (-65°C to +125°C). The time for step 2 and 4 shall be within 2 minutes each.

H.4.5.13.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

H.4.5.13.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. This Immersion and cooling shall be performed for 10 cycles.

H.4.5.13.4 Thermal Stress

The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 % maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for the structural integrity using the microsection prepared in accordance with H.4.5.5.1. Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder.
Evaluation specimen of Adhesion of cap plating and filled resin (paragraph H.3.4.4.12) shall be floated in a solder bath for a period of 10 seconds and cooled down. This floating and cooling shall be performed three times.

H.4.5.13.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be performed in accordance with paragraphs H.4.5.11.1 and H.4.5.13.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

APPENDIX J

PRINTED WIRING BOARDS,
HIGH HEAT RADIATION

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this specification: January 16, 2024

APPENDIX J

PRINTED WIRING BOARDS, HIGH HEAT RADIATION

J.1. General

J.1.1 Scope

This appendix establishes the general requirements and quality assurance provisions for the printed wiring boards, high heat radiation (hereinafter referred to as "printed wiring boards"), that applies constructions and materials with high heat radiation and can radiate heat by heat conduction from mounted components more efficiently than other substrates defined in other appendixes.

J.1.2 Classification

Classification of printed wiring boards is shown in Table J-1. A summary of each construction is shown in Figure J-1.
Base materials, copper inlay embedding and laminating processes are specified in detail specification.

Table J-1. Classification of Printed Wiring Boards

Classification	Construction
Type I	Copper inlay (exposed) / boards (Appendix B, H, etc.) ([1])
Type II	Copper inlay (exposed) / boards (Thermal conductive multilayer materials) ([2])
Type III	Copper inlay (embedded) / boards (Thermal conductive multilayer materials) and build-up layer (High thermal conductive materials and LVH) ([3])

Notes ([1]): Copper inlay was added to boards which were certified by existing appendixes.
([2]): Thermal conductive multilayer materials have better thermal conductivity than normal multilayer materials.
([3]): High thermal conductive materials have high heat radiation characteristics and is used only in build-up laminate section.
LVH: Laser Via Hole (Microvia)

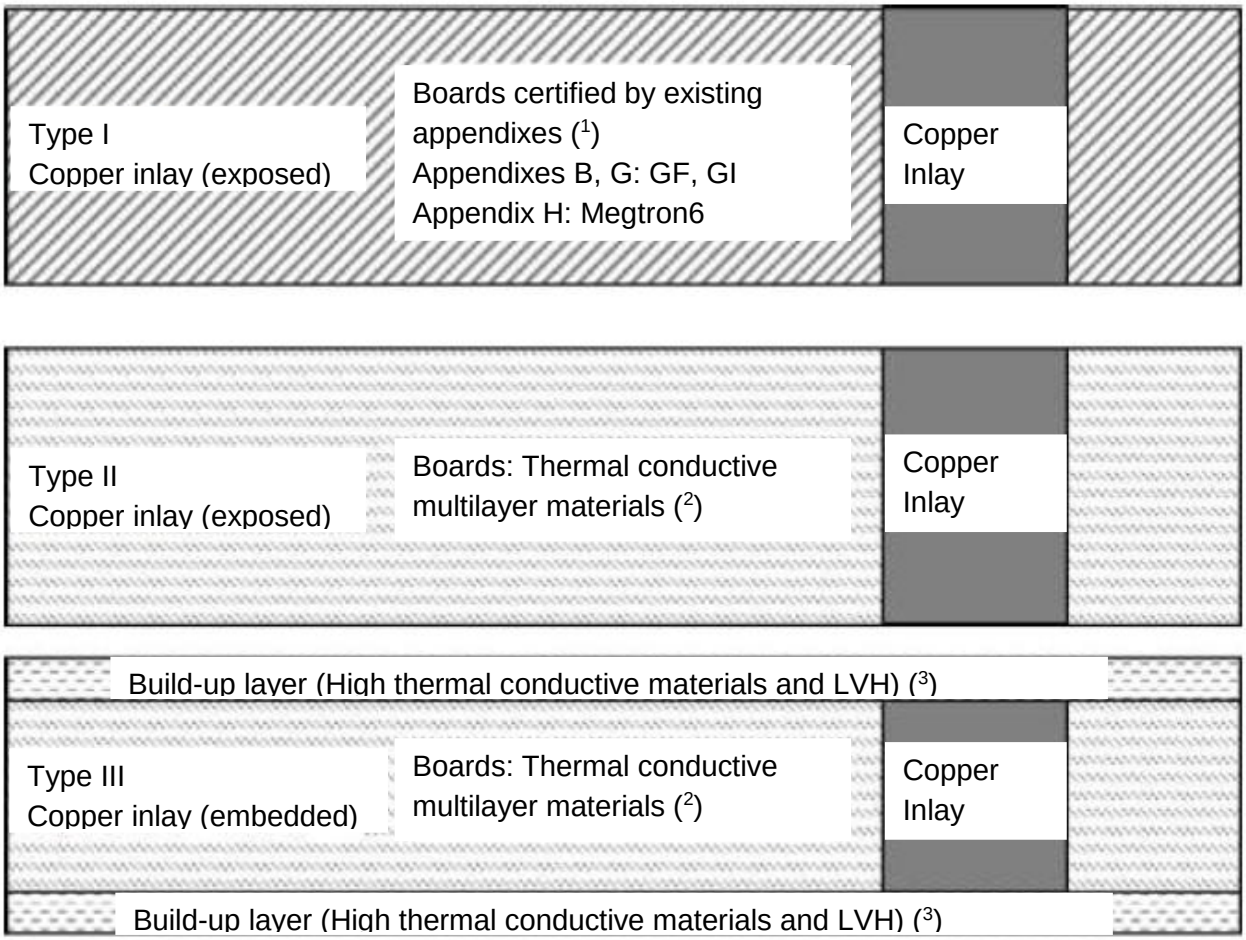


Figure J-1. Drawings of Each Construction Type

J.1.3 Part Number

The part number of the printed wiring boards is in the following form.

Example : JAXA(1) 2140/J	xxx	x	xxx	xx(2)
	Individual identification	Classification	Base material code	Number of layers
		(J.1.2)	(J.1.3.1)	(J.1.3.2)

Notes:

(1) "JAXA" indicates the common part for space use and may be abbreviated to “J”.

(2) Number of conductive layers

Example : JAXA(1) 2140/J	308	II H2 12	<=Type II, thermal conductive material, 12 layers
	Individual identification	Identification for board type	

J.1.3.1 Base Material Code

The base material code is as specified in Table J-2.

Table J-2. Base Material Code

Base material code	Insulation board material
GF	Glass base woven epoxy resin, compliant to IPC-4101, JPCA/NASDA-SCL-01
GI	Glass base woven polyimide resin, compliant to IPC-4101, JPCA/NASDA-SCL-01
102	Glass base woven modified polyphenylene ether resin, compliant to IPC-4101/102
H1	Thermal conductive materials (less than 1W/m · K)
H2	Thermal conductive materials (1W/m · K or more)

J.1.3.2 Number of Layers

The maximum number of layers of printed wiring boards shall be specified for each classification in detail specification.
For type III printed wiring boards, build-up layer, core layer, and the maximum number of layers for each of these types shall be specified in detail specification.

J.2. Applicable Documents etc.

J.2.1 Applicable Documents

The applicable documents shall be as follows and as specified in paragraph 2.1 of this specification.

a) JERG-0-043 Standards for Surface Mount Soldering Process in Space Application
b) JIS C 6481 Test methods of copper-clad laminates for printed wiring boards
c) IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design
d) IPC-TM-650 Test Methods Manual

J.2.2 Reference Documents

The reference documents shall be as follows and as specified in paragraph 2.2 of this specification.

a) JERG-0-054 Standards for BGA/CGA Soldering Process in Space Application
b) JIS C 6012 Qualification and Performance Specification for Rigid Printed Boards

J.3. Requirements

J.3.1 Qualification Coverage

Qualification shall be valid for printed wiring boards that are produced by the manufacturing line that conforms to materials, designs, constructions, ratings and performance specified in paragraphs J.3.2 through J.3.11. The qualification coverage shall be fully represented by samples that have passed the qualification test.
Qualification tests shall be conducted for each classification.
Products with fewer total layers and less thickness than the qualified sample units are considered qualified.
For surface plating and solder coating types, qualification tests shall be conducted using samples with solder coating or ENEPIGEG. The qualification coverage shall be represented by samples that have passed the qualification tests and the qualification coverage may include electrolytic nickel plating and electrolytic gold plating. Only solder resist inks used for qualification tests are considered qualified.
If necessary, additional qualification coverage shall be specified in the detail specification.

J.3.2 Materials

The materials for types II and III printed wiring boards shall be as follows. The materials for type I printed wiring boards shall be in accordance with the applicable appendixes, except for copper inlay.
Details shall be specified in the detail specification.

J.3.2.1 Copper-Clad Laminate, Prepreg and Copper foil

The copper-clad laminate, prepreg and copper foil laminated to prepreg, which are specified in paragraph J.2.1, shall be as specified in the drawing.
The nominal thickness of the base material shall be no less than 0.05mm.
The thickness of the copper foil shall be as specified in Table J-3 and the type of copper foil shall be specified in the detail specification. ([1])

Table J-3. Thickness of Copper Foil (Nominal)

Unit: μm

Layer	Classification	Copper foil thickness
External layer	With SVH and LVH	9 minimum
	Without SVH and LVH	18 minimum
Internal layer	With SVH, IVH and LVH	9 minimum
	Without SVH, IVH and LVH	18 minimum

Note ([1]): The standards required to materials used in the printed wiring boards shall be specified in the detail specification. The detailed information about base materials (such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the Application Data Sheet (hereinafter referred to as “ADS”).

J.3.2.2 High Thermal Conductive Materials for Build-up Layers (Type III Printed Wiring Boards only)

High thermal conductive materials for build-up layers shall be as specified in the drawing.
The copper foil laminated to prepreg on the outermost layer shall be as specified in the drawing.
Thermal conductivity of high thermal conductive materials for build-up layers shall be equal to or more than 1W/m・K. The detailed information about base materials (such as type of resin, glass-transition temperature, dielectric constant, and dielectric dissipation factor) shall be specified in the ADS.
For directional data, in-plane and out-of-plane directions shall be shown separately. Details shall be specified in the ADS.

J.3.2.3 Via Hole Filling Materials (Filling Resin)

The filling materials for SVH, IVH and small through hole shall be resin. The filling materials for LVH shall be resin or copper-plating.

J.3.2.4 Solder Resist Ink

The solder resist applied on the printed wiring boards shall conform to Class H of IPC-SM-840 or the equivalent.
Thermal conductivity of solder resist shall be specified in the ADS.

J.3.2.5 Marking Ink

The marking shall be conducted using ink that will not easily be erased by any solvent. The marking shall not adversely affect any function, performance or reliability of the printed wiring boards.

J.3.2.6 Plating

Electroless and electrolytic copper plating shall be applied to all through holes, LVH and for cap plating. Solder coating or ENEPIGEG plating shall be applied to the surface of the solder joint. For any areas other than the solder joints, electrolytic nickel gold plating may be applied if necessary.

J.3.2.6.1 Electroless Copper Plating

The electroless copper plating shall be applied as a preceding process of electrolytic copper plating to form a conductive layer over the insulating material.

J.3.2.6.2 Electrolytic Copper Plating

The electrolytic copper plating shall have a minimum purity of 99.5 %.

J.3.2.6.3 Electrolytic Gold Plating

The electrolytic gold plating shall be as specified in Table J-4. The electrolytic nickel plating specified in paragraph J.3.2.6.4 shall be applied as an undercoat. The content rate of impure metals after the electrolytic gold plating shall not exceed 0.1 % except for the metal added to increase the hardness.

Table J-4. Electrolytic Gold Plating

Item	Specification
Purity	Min. 99.7 %
KNOOP hardness	91 to 129 (inclusive)

J.3.2.6.4 Electrolytic Nickel Plating

The electrolytic nickel plating shall conform to SAE-AMS-QQ-N-290 or the equivalent.

J.3.2.6.5 Solder Coating

The solder used for solder coating shall contain 50 to 70 % tin.

J.3.2.6.6 ENEPIGEG (Electroless Nickel / Electroless Palladium / Immersion Gold / Electroless Gold)

For ENEPIGEG plating, electroless nickel plating is applied as an undercoat on the copper circuit, electroless palladium plating is applied on the undercoat, and then electroless gold plating is applied on the electroless palladium plating. ([1])

Note ([1]): Thick palladium / gold plating may cause cracks due to the effects of IMC (intermetallic compound) layer or solidification shrinkage process when mounting insert components or components with large thermal capacities (citing from JERG-1-009).

J.3.2.7 Copper Inlay

Copper inlay materials for high heat radiation shall be pure copper (purity shall be 99% or more). Details of the copper inlay (standards and hardness (with or without heat treatment)) shall be specified in the ADS.

J.3.3 Design and Construction

Design and construction for types I, II and III printed wiring boards shall be as follows. Design and construction for type I printed wiring boards shall be in accordance with the applicable appendixes, except for copper inlay embedding.

J.3.3.1 Manufacturing Drawings and Artwork Master (or Original Production Master)

Manufacturing drawings of printed wiring boards shall be prepared in accordance with this paragraph.
The manufacturing drawings and artwork masters (or original production masters) shall be approved by the purchaser. In the event of conflict between the manufacturing drawings and artwork masters (or original production masters), the manufacturing drawings shall take precedence.

J.3.3.2 Connector for Printed Wiring Boards

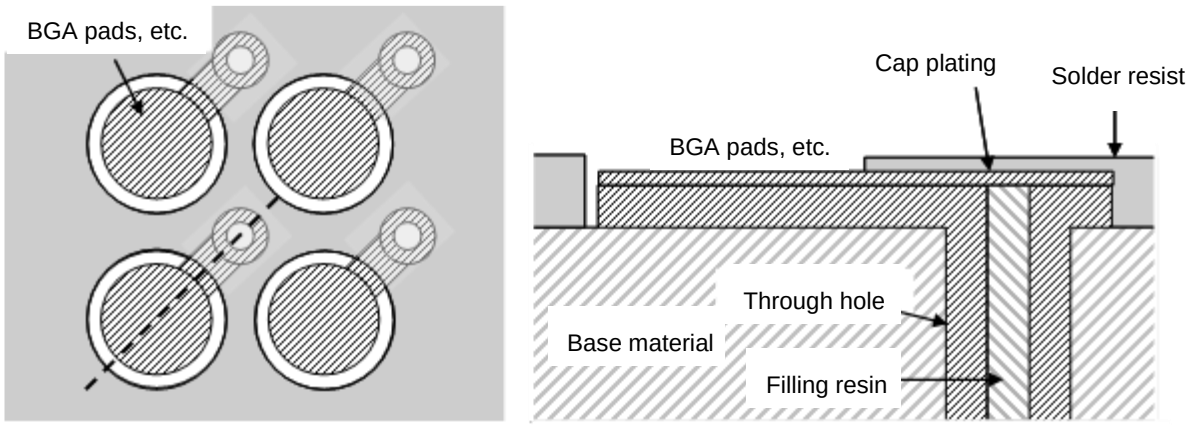
A direct connector (card edge connector) shall not be used for printed wiring boards.

J.3.3.3 Interlayer Connection

Connection between conductive patterns in different layers of the printed wiring boards shall be provided by LVH, small via holes, IVH, SVH or through holes. When through holes including copper inlay are used for signal and other conduction purposes, the intended use of the through holes shall be specified in the manufacturing drawings.

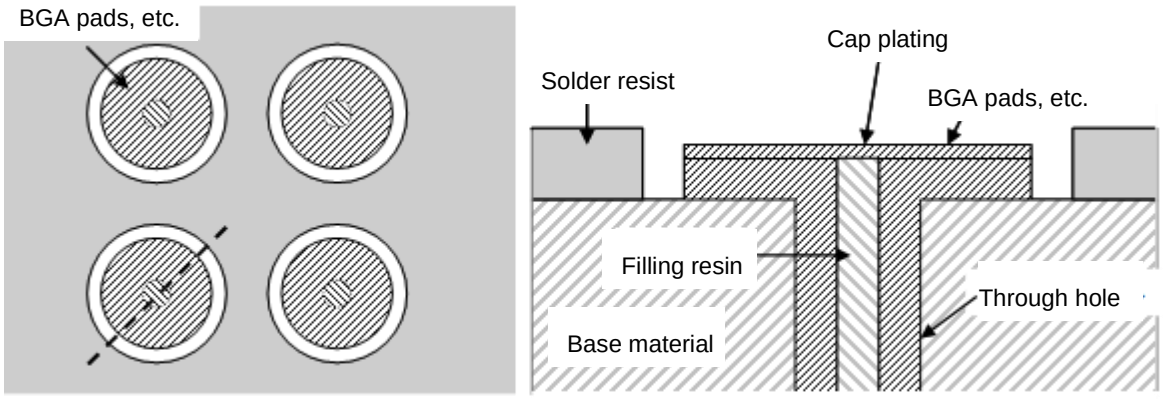
J.3.3.4 Connection Method for Area Array Packaging Pads

The connection method for contact pads of area array packages such as BGA pads (hereinafter referred to as “BGA pads, etc.”) shall be made by Dog-Bone construction or Via-in-Pad (hereinafter referred to as “VIP”) construction.
Dog-Bone construction is to connect small via hole by drawing the circuit out of the contact pads such as BGA pads as shown in Figure J-2. The small via hole shall be filled with resin and closed by plating (cap plating). LVH shall be filled with copper plating or filled with resin and closed by cap plating.
VIP construction is the construction where cap plating as BGA pad is directly on top of the LVH filled with copper plating or resin and closed by cap plating, or SVH or small via hole filled with resin and closed by cap plating as shown in Figure J-3.



External view　　Cross-section view of dashed line

Figure J-2. External and Cross-Section View of Dog-Bone Construction



External view　　Cross-section view of dashed line

Figure J-3. External and Cross-Section View of Via-in-Pad Construction

J.3.3.5 Build-up Layer (Type III Printed Wiring Boards Only)

The number of build-up layers on top and back sides of the printed wiring boards shall be identical.
Connection between layers of build-up layers shall be through staggered via or stacked via construction and shall be specified in the detail specification.
Skip via shall not be used.
Details are shown in Figure J-4.

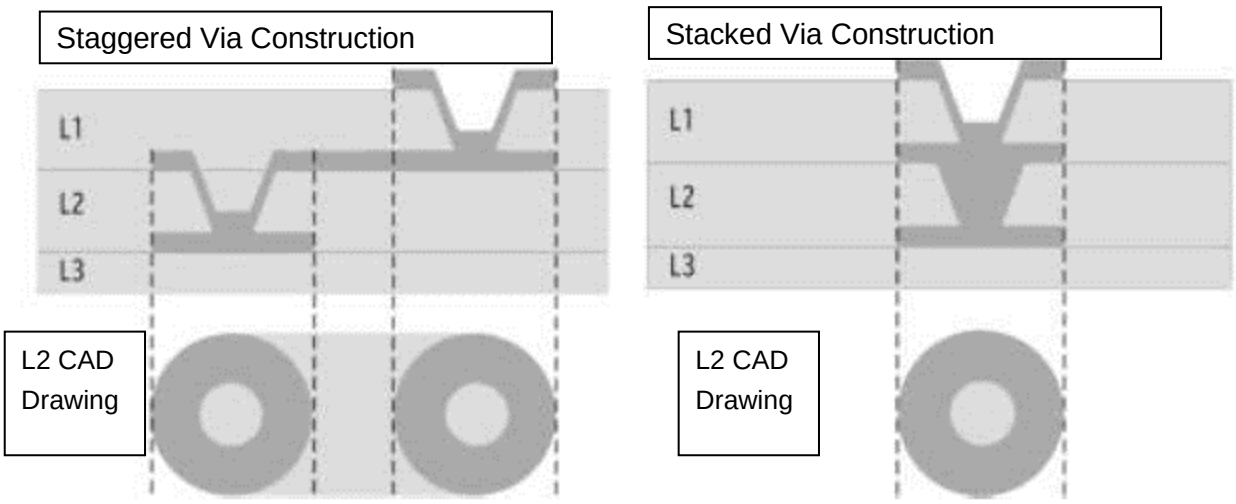


Figure J-4. External and Cross-Section View of Laser Via Construction (Staggered and Stacked Construction)

J.3.3.6 Through Hole Diameter

The minimum hole diameter for small via hole, IVH and SVH shall be φ0.20mm as a drill hole. When the lands of via hole are used as BGA pads, etc., the drill hole for via hole shall be φ0.20mm as a maximum.

J.3.3.7 LVH (Type III Printed Wiring Boards Only)

The minimum hole diameter Y for LVH shall be φ0.15mm. Aspect ratio, with or without taper construction and laser processing method (such as direct laser and conformal mask) shall be specified in the detail specification for a detail of the LVH construction.
Note ([1]): Land diameter is specified in paragraph J.3.3.12.

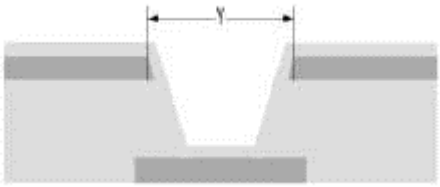


Figure J-5. Cross-Section View of LVH (Stacked Construction)

J.3.3.8 Copper Inlay Embedding

The location where copper inlay is embedded shall be specified in the manufacturing drawing. Embeddable shapes of the copper inlay and other design information shall be specified in the detail specification.

J.3.3.9 Filling Resin for Through Hole

The small via hole to be filled with via filling materials and LVH of outer layers to be filled with via filling materials shall be specified in the manufacturing drawing.
The small via holes, SVH and LVH applied to VIP construction shall be filled with via filling materials.

J.3.3.10 Conductor Width and Thickness

The minimum design value for conductor width shall be as specified in Table J-5.
The conductor width and thickness shall be designed in consideration of the allowable current (current capacity) calculated from the temperature rise due to the conductor cross section area and the current flowing through the conductor.
Figures J-6, J-7, J-8, and J-9 shall be used as a reference for the relationship between the cross section area and allowable current of the conductor, and this shall apply to conductors on both internal and external layers under vacuum and space environmental conditions.
When the conductor thickness for BGA pads, etc. should be specified, consult with manufacturers of printed wiring boards to specify the thickness in the manufacturing drawing.

Table J-5. Conductor Width (Design Value)

Unit:mm

Layer	Conductor thickness	Minimum conductor width
External	All	0.10
Internal	More than 35µm	0.10
	35µm or less	0.07

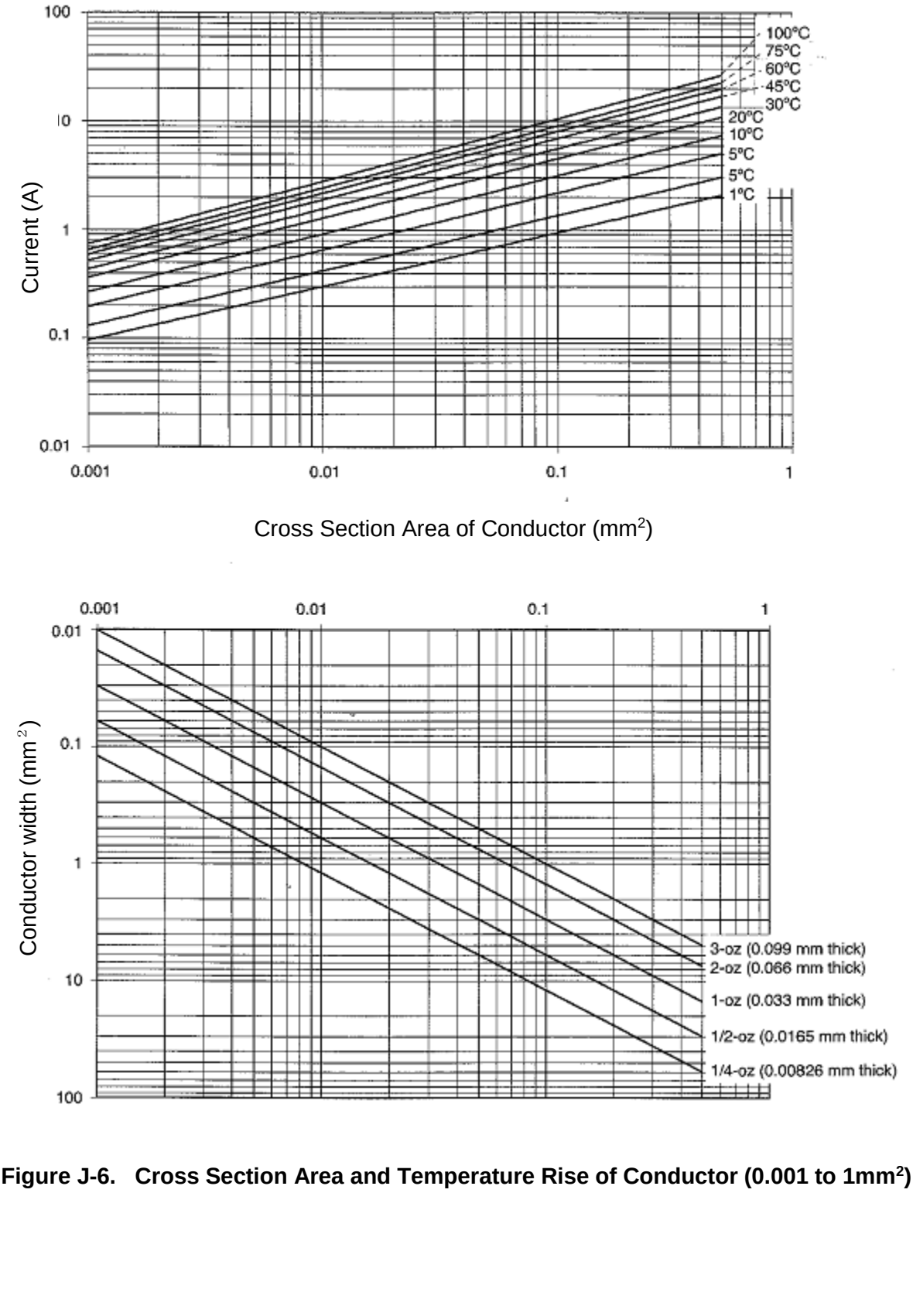


Figure J-6. Cross Section Area and Temperature Rise of Conductor (0.001 to 1mm^2)

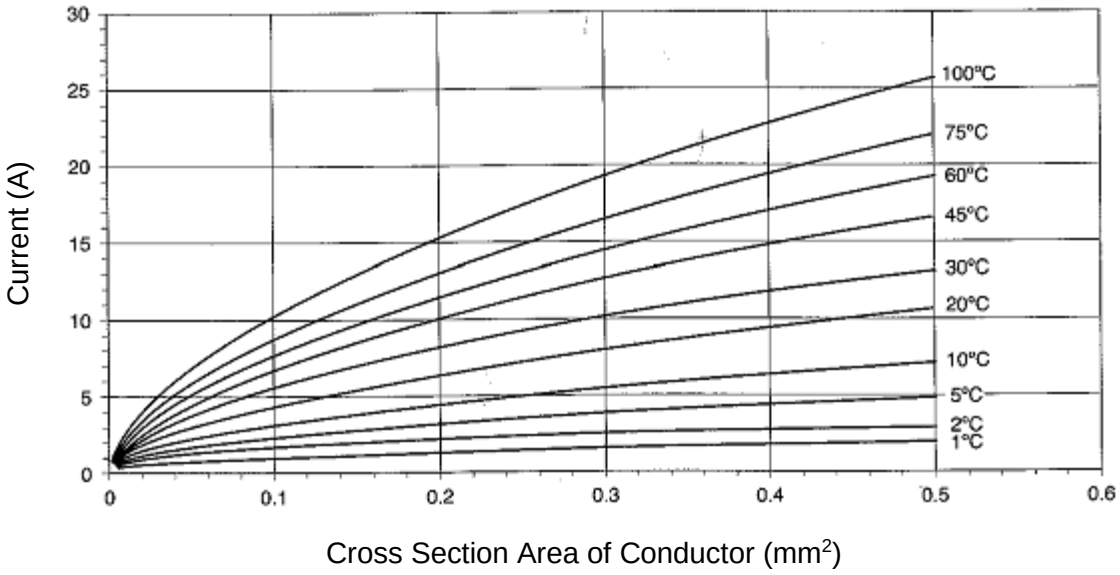


Figure J-7. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.5mm²)

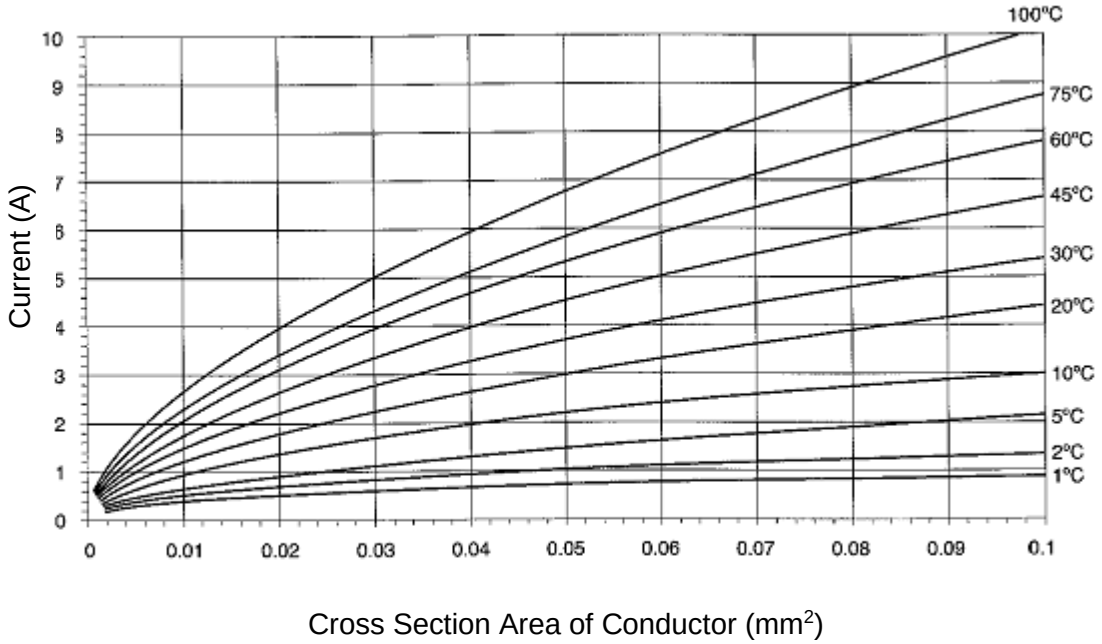


Figure J-8. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.1mm²)

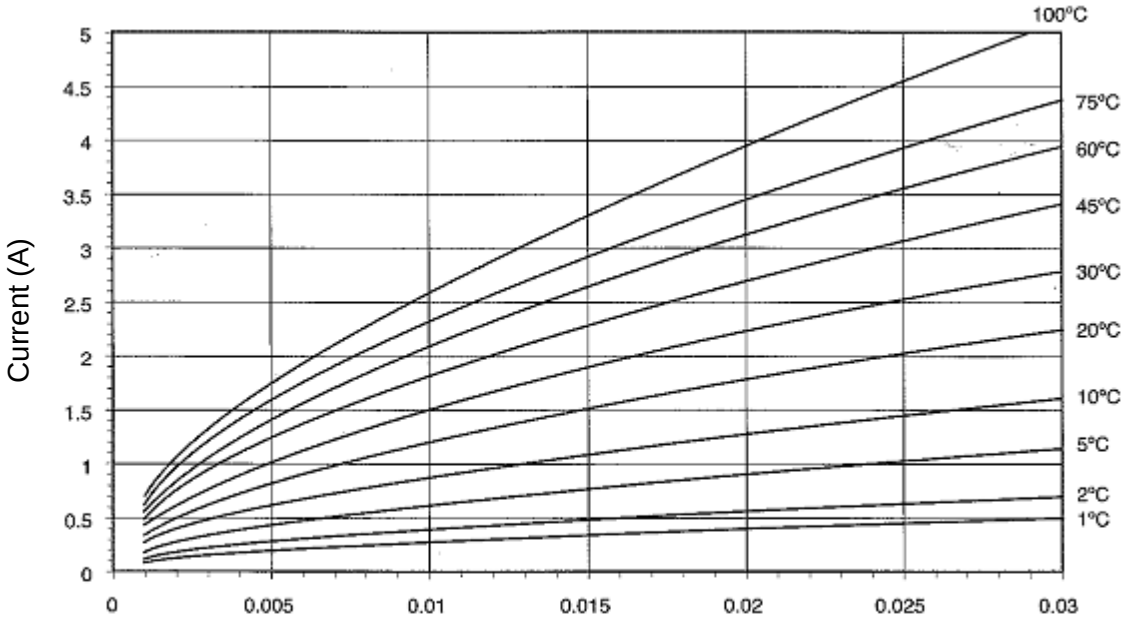


Figure J-9. Cross Section Area of Conductor and Temperature Rise (0.001 to 0.03mm^2)

J.3.3.11 Conductor Spacing

The minimum design value of conductor spacing shall be as specified in Table J-6. The specific conductor spacing that depends on the voltage applied between conductors shall be as specified in Table J-7.

Table J-6. Conductor Spacing (Design Value)

Unit:mm

Layer	Conductor thickness	Minimum conductor spacing
External	All	0.14
Internal	More than 35μm	0.15
	35μm or less	0.08

Table J-7. Conductor Spacing for Printed Wiring Boards

Unit: mm

Voltage applied between conductors, DC or AC_{p-p} (V)	Minimum conductor spacing	
	External layer	Internal layer
0 to 50	0.14	0.08
51 to 100	0.14	0.10
101 - 300	0.40	0.20
301 - 500	0.80	0.25
501 or higher	(0.003xV)	(0.0025xV)

J.3.3.12 Land Diameter

The minimum design value of land diameter shall be as specified in Table J-8 (see Figure J-10). Non-functional land ([1]) may not be provided when required to maintain conductor spacing and electrical characteristics.
For through holes with embedded copper inlay, presence/absence of non-functional land shall be specified in the detail specification.

Table J-8. Land Diameter

Unit: mm

Hole	Minimum land diameter([2])
SVH and small via holes	ϕ (Drill diameter + 0.25)
LVH	Detail specification
Through holes with embedded copper inlay	Detail specification
Through holes other than the above	ϕ (Finished hole diameter + 0.5)
Non-plated through holes	ϕ (Drill diameter + 1.1)

Notes:
([1]) Non-functional land (or inner layer unconnected land) is the land without inner layer connection.
([2]) The minimum diameter of lands other than round shaped lands shall be the measure of the length “A” shown in Figure J-10.

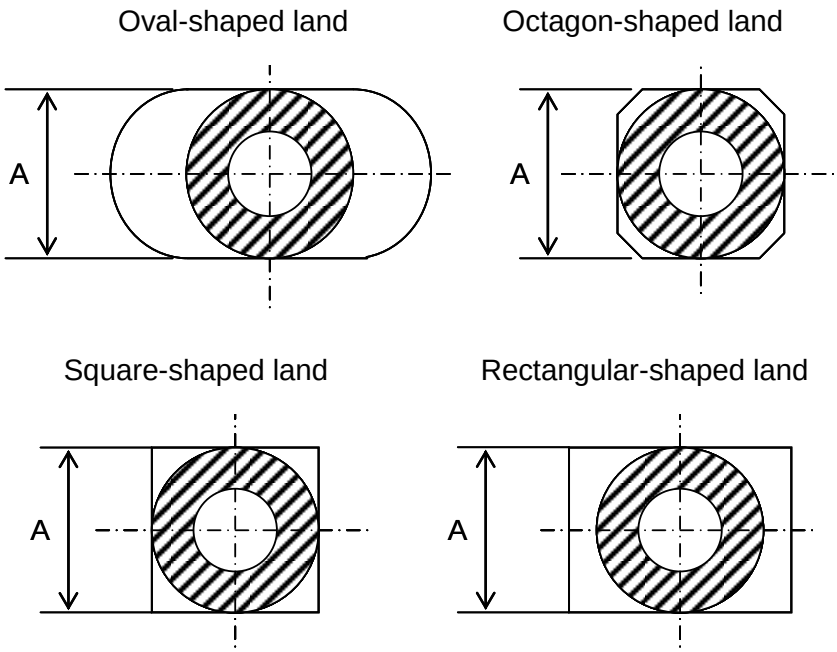


Figure J-10. Measurements of Minimum Diameter of Lands Other than Round Shaped Lands (A)

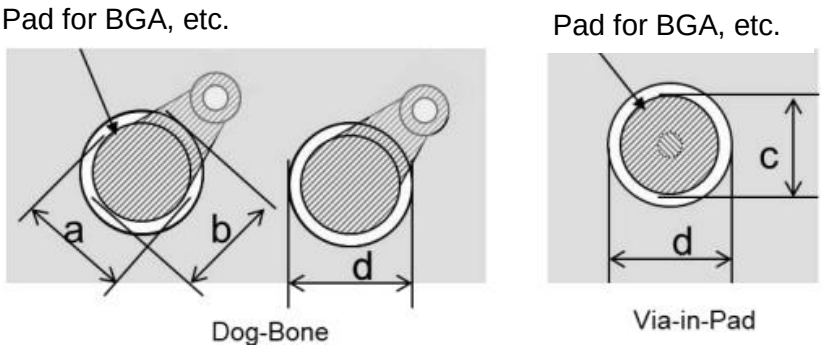
J.3.3.13 Pads for BGA, etc.

The sizes of the pads for BGA, etc. for each section shown in Table J-9 shall be specified.

Table J-9. Dimensions of BGA Pads, etc.

Unit: mm

Section		
Pad size (Bottom of conductor)	Dog-Bone	Pad (see Figure J-11 a)
		Fan-out direction (see Figure J-11 b)
	Via-in-Pad (see Figure J-11 c)	
Size of solder resist opening (Resist surface)	Dog-Bone (see Figure J-11 d)	
	Via-in-Pad (see Figure J-11 d)	
Total board thickness	Total board thickness including conductor and solder resist	

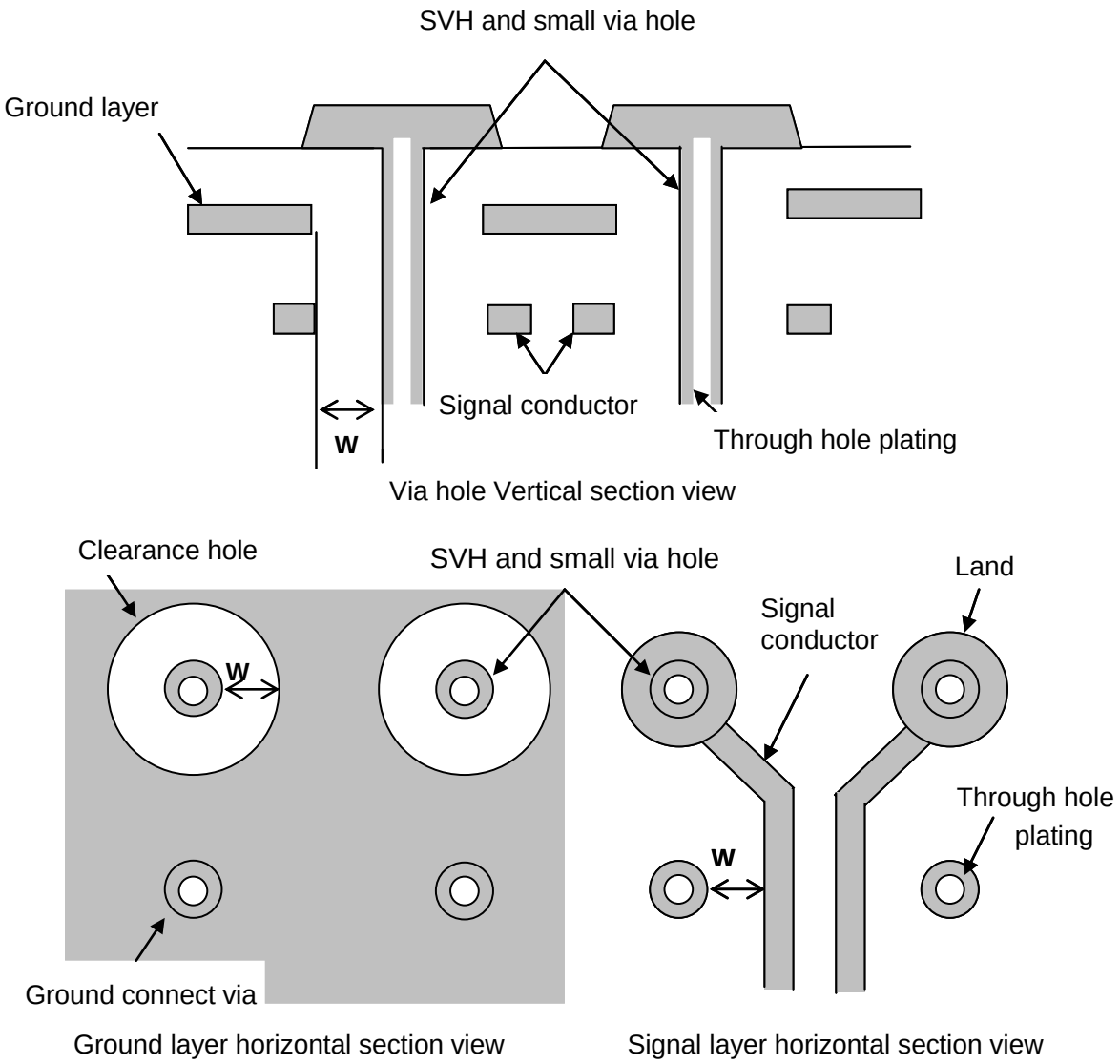


a: Pad size in Dog-bone construction b: Fan-out pad size c: Pad size in Via-in-Pad
d: Size of solder resist opening

Figure J-11. Measurements of Pads for BGA, etc.

J.3.3.14 Internal Layer Clearance

The distance (internal layer clearance) from the hole wall of SVH and small via hole to the conductor nearby shall be as specified in Figure J-12.



W= Internal layer clearance ≥ 0.28mm

Figure J-12. Cross Section View of Via Holes

J.3.3.15 Clearance of Through Holes with Embedded Copper Inlay

The distances from the hole wall of the through holes with embedded copper inlay to the conductor nearby (Figure J-13 a), to the hole wall of the through hole nearby (Figure J-13 b), to the hole wall of the another through holes with embedded copper inlay (Figure J-13 c) and to the edge of the printed wiring boards (Figure J-13 d) shall be as shown in Figure J-13 and these distances shall be specified in the detail specification.

When these distances are affected by the size of copper inlay, worst case values of these distances for the size of copper inlay shall be specified.

a: Distance between hole wall of the through holes with copper inlay and conductor nearby

b: Distance between hole wall of the through holes with copper inlay and through hole nearby

c: Distance between hole wall of the through holes with copper inlay and hole wall of the another through hole with copper inlay

d: Distance between hole wall of the through holes with copper inlay and edge of the printed wiring boards

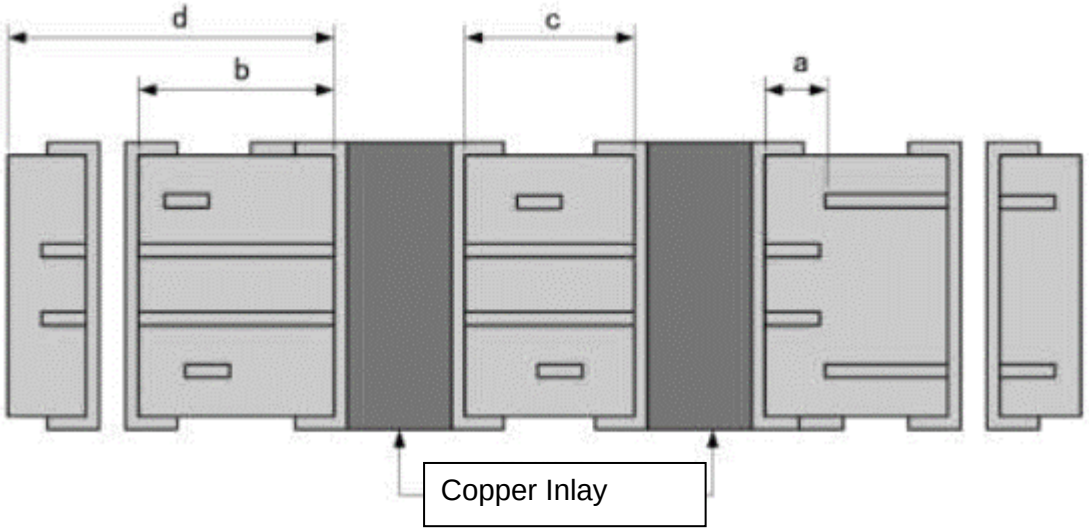


Figure J-13. Cross Section View of Through Holes in which Copper Inlay is Press-fitted

J.3.3.16 Surface Finish Plating

The thickness of the surface finish plating and solder coating specified in the manufacturing drawing shall be in accordance with Table J-10. The electrolytic Nickel plating shall be applied as an undercoat of electrolytic gold plating, and shall not be used for the surface finish. If more strict requirements than the ones specified in Table J-10 are necessary, consult with manufacturer and specify on the manufacturing drawing.

Table J-10. Thickness of Surface Finish Plating

Unit: μm

Plating material	Surface plating thickness	
Electrolytic gold	1.3 to 4.0	
Electrolytic nickel	5 as a minimum	
Solder coating	Thickness is not specified. However, the coating shall comply with solderability requirements (J.3.10.2).	
ENEPIGEG(Electroless Nickel / Electroless Palladium / Immersion Gold / Electroless Gold)	EN: Electroless nickel plating ([1])	3.00 to 8.00
	EP: Electroless palladium plating ([1])	0.05 to 0.20
	IG+EG: Immersion gold and electroless gold plating ([1])	0.10 to 0.40

Note ([1]): Shall conform to drawings and other specifications. Unless otherwise specified, this table shall apply.

J.3.3.17 Solder Resist

The solder resist application shall be specified except for the land, pads (incl. Via-in-Pad), and the small via holes without resin filling.
The lands of small via hole and SVH in the dog-bone construction shall be coated with solder resist.
Whether or not the solder resist is necessary for the lands of small via holes with resin filling and SVH except for the pads for BGA, etc. shall be specified in the manufacturing drawing.
The minimum distance from the edge of the board to the solder resist shall be 0.3mm.
Solder resist is basically not applied to the through holes with copper inlay due to thermal design requirements, however solder resist may be formed as necessary for parts mounting and other applications.

J.3.3.18 Sideplating on Outer Perimeter of the Board

The sideplating on outer perimeter of the board (hereinafter referred to as “Sideplating”) shall be specified in the manufacturing drawing if applied.
The detailed design of the sideplating shall be specified in detail specification.

J.3.3.19 Characteristic Impedance

The characteristic impedance of the printed wiring boards shall be specified in the manufacturing drawing if applied.

J.3.3.20 Operating Temperature Range

Printed wiring boards shall operate within the temperature range of the thermal shock (II) test (paragraph J.3.11.1.2) and within -65 to +125°C.

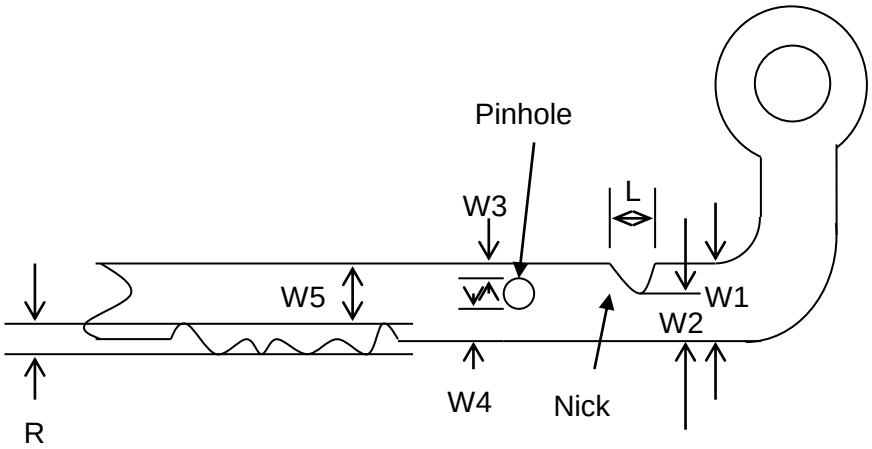
J.3.4 Externals, Dimensions, Marking and Others

J.3.4.1 Externals of Conductor, Base Material, Solder Resist and Copper Inlay

J.3.4.1.1 Conductor

a) Conductive pattern
The conductive patterns shall conform to the approved or provided artwork master (or original production master).

b) Conductor
The conductors including sideplating shall contain no tears, cracks, lifting, or separation. Any combination of edge roughness, nicks, pinholes or scratches exposing the insulation board shall not reduce the conductor width to less than 80 % of the minimum finished conductor width. The length of any defect shall not exceed the conductor width (design width of the conductor). The number of defects exceeding 0.05mm in width shall not be more than one per conductor or per unit area of 100×100mm on the printed wiring boards. The roughness at vertical conductor edges shall meet the conductor width tolerance (see Figure J-14).
The tolerances of conductor width and conductor spacing shall be as specified in Table J-11.
The nicks and pinholes on the ground surface and power supply surface shall not exceed 1.0mm in the maximum length and 4 pieces per 625cm^2 in number.



W1 ≥ (Minimum finished conductor width)
W2 ≥ 0.80 × (Minimum finished conductor width)
W3 + W4 ≥ 0.80 ×Minimum finished conductor width)
W5 ≥ Minimum conductor width
L = Length of defect

Figure J-14. Acceptance Criteria for Conductor Defects

Table J-11. Tolerance of Conductor Width and Conductor Spacing

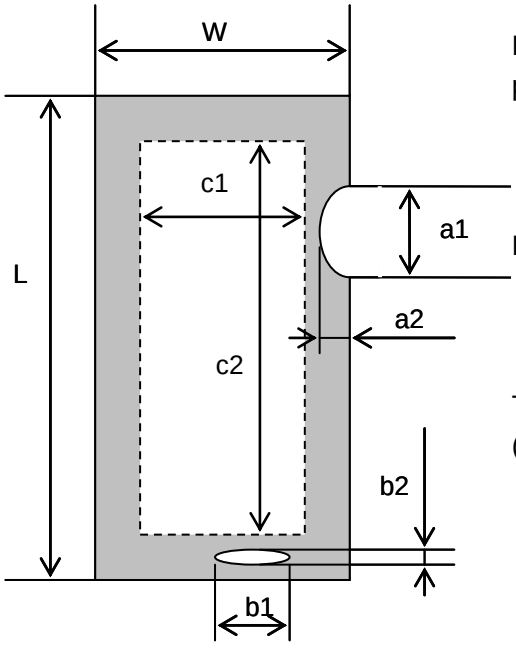
Unit: mm

Dimension		Tolerance
Conductor width	0.07 to less than 0.13	+0.05 -0.03
	0.13 to less than 0.20	±0.05
	0.20 to less than 0.50	±0.10
	0.50 or more	±20% of conductor width
Conductor spacing	Less than 0.10	0.05 as a minimum
	0.10 to less than 0.14	0.06 as a minimum
	0.14 or more	0.10 as a minimum
	The positive side tolerance is not specified for all design value.	

c) Rectangular surface mount pad

The defects such as nicks, dent and pinholes along the external edge of the pad shall not exceed 20% of the length or the width of the pad. The defects inside the pad shall not exceed 10% of the length or the width of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center to the 80% of the mount pad length and width (see Figure J-15).

The pad length and width shall be based on the design value.



Defects along the external edge of the pad
a1 ≤ L X 0.2
a2 ≤ W X 0.2

Defects inside the pad
b1 ≤ L X 0.1
b2 ≤ W X 0.1

The area where no defect is allowed (from the center of the pad)
c1 = W X 0.8
c2 = L X 0.8

Figure J-15. Acceptance Criteria for Defects on the Rectangular Surface Mount Pad

d) Mounting Pad for BGA, etc.
The defects such as nicks, dent and pinholes along the edge of the pad shall not exceed 10% of the diameter of the pad expanding in a radial direction of the land center. The defects inside the pad shall not exceed 20% of the circumference of the pad. There shall not be any defects, except for the probe mark from the electrical test, in the area from the center of the pad diameter to the 80% of the pad (see Figure J-16).
The pad diameter shall be based on the design value.

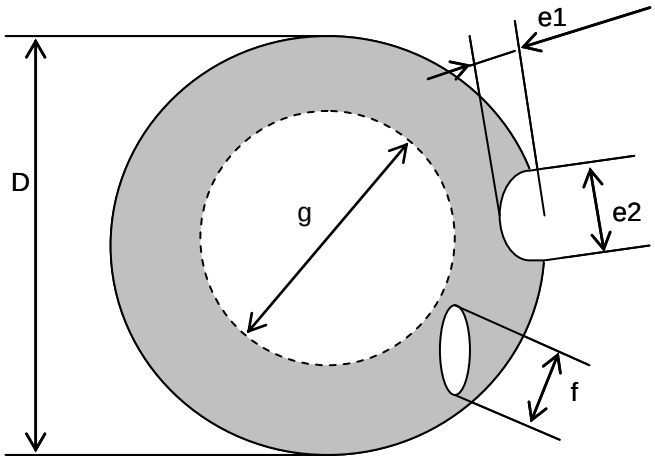


Figure J-16. Acceptance Criteria for Defects on the Mount Pad such as BGA

e) Probe mark from Electrical test
The probe mark from the electrical test shall be covered with solder coating and shall be permitted unless the undercoating copper plating is exposed. At the ENEPIGEG plating pad section and terminal section finished with electrolytic gold plating, undercoating nickel plating shall not be exposed.

f) Between conductors
The surface of a insulation plate between conductors shall be free from adhesion of any residual conductor or foreign inclusion.

g) Solder coating
The solder coating shall be free from pinholes or pits, and completely cover conductors. However, the copper exposure on sideplating side is permitted.

h) Electrolytic nickel and electrolytic gold plating
The electrolytic nickel and electrolytic gold plating shall be free from pinholes or pits, and completely cover conductors surfaces. However, the copper exposure on the conductor side is permitted.

i) ENEPIGEG (Electroless Nickel / Electroless Palladium / Immersion Gold / Electroless Gold)
ENEPIGEG shall be free from pinholes or pits, and completely cover conductor surfaces.

J.3.4.1.2 Base Materials

a) Edges of printed wiring board and non-plated through hole
Printed wiring boards shall not exhibit nicks, cracks or separation at their edges. This provision shall not apply to separate parts of a split board.
Crazing and haloing along the edges of printed wiring board shall be permitted, when the spacing between the crazing or haloing and an adjacent conductor is equal to or greater than the minimum conductor spacing specified on drawings or 1.6mm, whichever is smaller.

b) Surface of printed wiring boards
The surface of printed wiring boards shall not exhibit separation around holes. Each layer and base material shall not exhibit delamination. Measling and crazing underneath the surface of the board shall not be permitted.

J.3.4.1.3 Solder Resist

a) The cured solder resist shall be free from tackiness, blistering and delamination.
b) Significant visual damage such as a thin spot, separation, roughness on the surface, uneven color and exposed residual conductor shall not be permitted.
c) Unless otherwise specified, scratches and pinholes shall be acceptable, provided that the conductors are covered with solder resist.
d) The solder resist shall not encroach onto lands for mounting parts.
e) The application range and misalignment of solder resist and conductive patterns shall meet the provisions of manufacturing drawings.
f) Unless otherwise specified on the manufacturing drawings, adjacent conductor shall not be exposed in the solder resist opening area.
g) In the Dog-Bone construction, solder resist shall completely cover the land of small via hole and SVH.

J.3.4.1.4 Copper Inlay

a) Dents of the edge of copper inlay shall be acceptable, provided that the dents meet requirements specified in paragraph J.3.4.2.
b) Edge of the copper inlay shall be free from burrs that protrude from the surface of the copper inlay.
c) Surface of the copper inlay shall be free from scratches and dents such that copper protrudes from the surface of the copper inlay. Area of the scratches and dents that copper does not protrude from the surface of the copper inlay shall not exceed 5% of the area of the copper inlay and depths of the scratches and dents shall meet the requirements specified in paragraph J.3.4.2.

J.3.4.2 Dimensions

The dimensions of each part of the printed wiring boards shall be as specified on manufacturing drawings. Unless otherwise specified, dimensional tolerance shall be in accordance with the requirements specified in Table J-12.

Sizes of the finished hole diameter of SVH, IVH, LVH and small via holes are not specified.
Since tolerances are displayed differently for each type of the convexity tolerances of copper inlay and manufacturer-specific criteria for the convexity tolerances of copper inlay exist, description specified in the detail specification shall be added as note.

Table J-12. Dimensional Tolerance

Unit: mm

Item	Dimensional tolerance
Outline dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 in excess of 100
Finished hole diameter	The tolerance of all hole diameters shall be $^{+0.10}_{-0.15}$. However, the tolerance of finished diameters of SVH, IVH, LVH and small via holes is not specified.
Undercut	Undercut at each edge of conductors shall not exceed the total thickness of the copper foil and plated copper.
Unevenness of copper inlay	Unevenness of copper inlay shall not exceed ±0.1 including flatness, based on the lands of through holes in which copper inlay will be embedded.

J.3.4.2.1 Dimensions of BGA Pads, etc.

Unless otherwise specified, the dimension tolerance for BGA pads, etc. shall be in accordance with the requirements specified in Table J-13.

Table J-13. Dimensions for BGA Pads, etc.

Unit. (mm)

Item			Tolerance
Pad size (conductor bottom size)	Dog-Bone	Pad (Figure J-11 a)	±0.05
		Fan-out direction (Figure J-11 b)	±0.075
	Via-in-Pad (Figure J-11 c)		±0.05
Solder resist opening diameter (resist surface)	Dog-Bone (Figure J-11 d)		±0.05
	Via-in-Pad (Figure J-11 d)		±0.05
Accurate alignment	Length of row of BGA pads		±0.05
Pad thickness (conductor thickness)			±0.01
Total board thickness (incl. solder resist)			±8%
Co-planarity (flatness): Normal state			0.05mm or less for diagonal diameter of BGA pads

J.3.4.3 Marking

The marking shall be produced with the marking inks or laser marking specified in paragraph J.3.2.5, by copper etching. The marking shall remain legible and shall not adversely affect any function, performance or reliability of printed wiring boards. Unless otherwise specified, the following shall be marked on each printed wiring board. If marking on the printed wiring boards is impossible, the marking may be placed on a tag.

a) Part number
b) Year and month manufactured
c) Manufacturer's name or its identification code
d) Product serial number(1) or lot number

Note: (1) Product serial number shall be provided so that the complete manufacturing process can be traced.

J.3.4.3.1 Marking on Split Board

If any separable part (equivalent to a single wiring board) of a split board is not usable, it shall be clearly marked that the part cannot be used. This marking shall be made by a method such that it does not easily vanish by any solvent.

J.3.4.4 Structural Integrity

J.3.4.4.1 Through Holes

When printed wiring boards are tested as specified in paragraph J.4.5.5.1, the following requirements for through holes (including through holes with copper inlay), small via holes, sideplating, SVH, IVH and LVH shall be satisfied (see Figure J-17).

a) Plating shall not exhibit cracks, conductive interface separation or glass fiber protrusion, and shall be continuously smooth from the land.

b) Protrusion of plating caused by burr and nodules shall not reduce the hole diameter in through holes below its lower limit specified on manufacturing drawings.

c) Partial pits of plating shall not exceed 10% of the plating thickness specified in paragraph J.3.4.4.7.

d) Resin recession at the boundary section between hole wall and plated-through hole shall be permitted, provided the maximum depth as measured from the surface of the plated-through holes does not exceed 80μm, and the resin recession on any side of the plated-through hole does not exceed 40 % of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated. Resin recession of LVH shall not be permitted.

e) The pits of plating caused by negative etchback shall be permitted, provided that the negative etchback satisfies the requirements specified in paragraph J.3.4.4.6. This requirement is not applied to LVH.

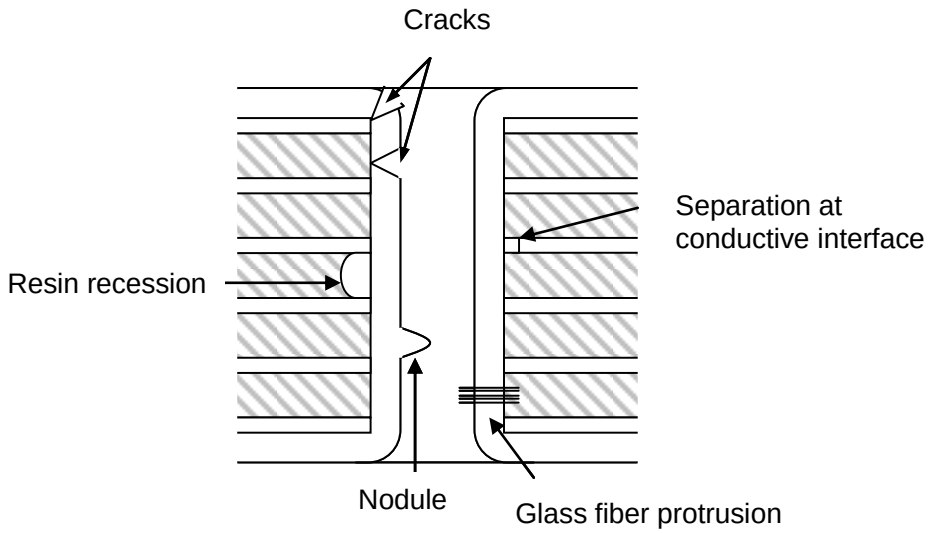


Figure J-17. Through Hole Defects

J.3.4.4.2 Through Holes with Copper Inlay Press-fitted

When printed wiring boards are tested as specified in paragraph J.4.5.1, following requirements shall be satisfied (see Figure J-17).

a) Requirements for finished through holes are specified in paragraph J.3.4.4.1 Through Holes.

b) Unless otherwise specified in the drawings, copper inlay bumps from the surface of the land shall not exceed ±0.1mm on either side of the printed wiring boards.

J.3.4.4.3 Voids

When printed wiring boards are tested as specified in paragraph J.4.5.5.2, there shall not be any plating voids, laminate voids or voids at conductor connection section (see Figure J-18).

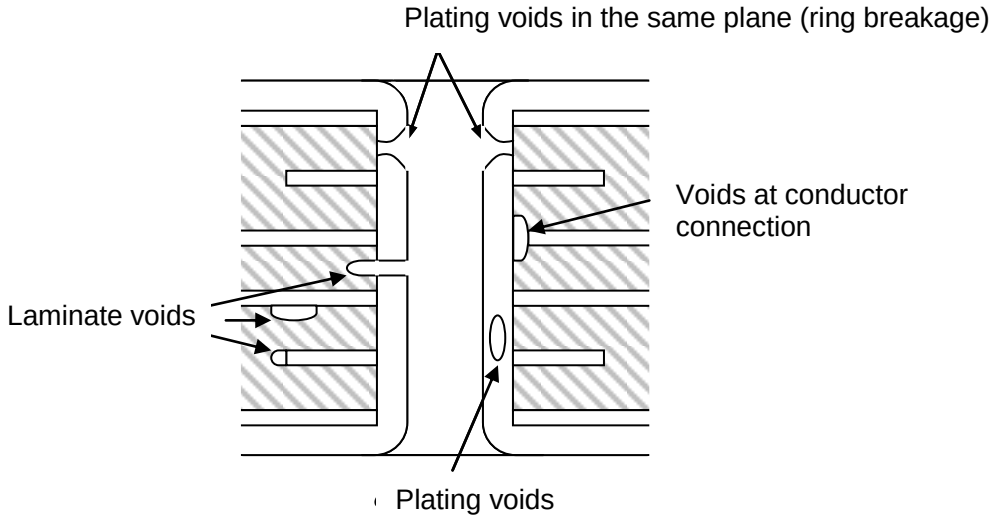


Figure J-18. Voids

J.3.4.4.4 Separation of Lands

When printed wiring boards are tested as specified in paragraph J.4.5.5.3, separation of lands shall not be permitted.

J.3.4.4.5 Cracks on Copper Foil

When printed wiring boards are tested as specified in paragraph J.4.5.5.4, there shall not be any cracks on the copper foil in the external and internal layers.

J.3.4.4.6 Inner Layer Connection

When printed wiring boards are tested as specified in paragraph J.4.5.5.5, the resin smear at the interface of the through hole wall plating and an internal conductive layer shall not be permitted. Nail heading of a conductive layer shall not exceed 50 % of the metal foil thickness (see Figure J-19). Internal layer negative etchback shall not exceed 13µm.

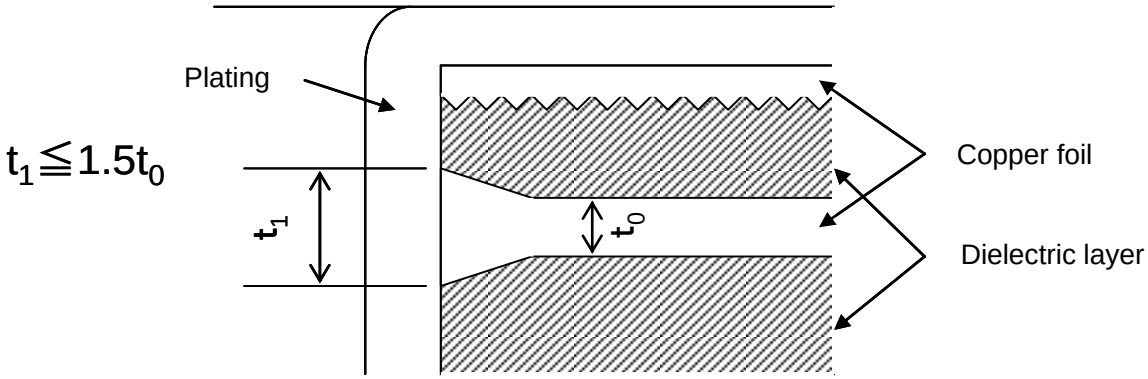


Figure J-19a. Nail Heading

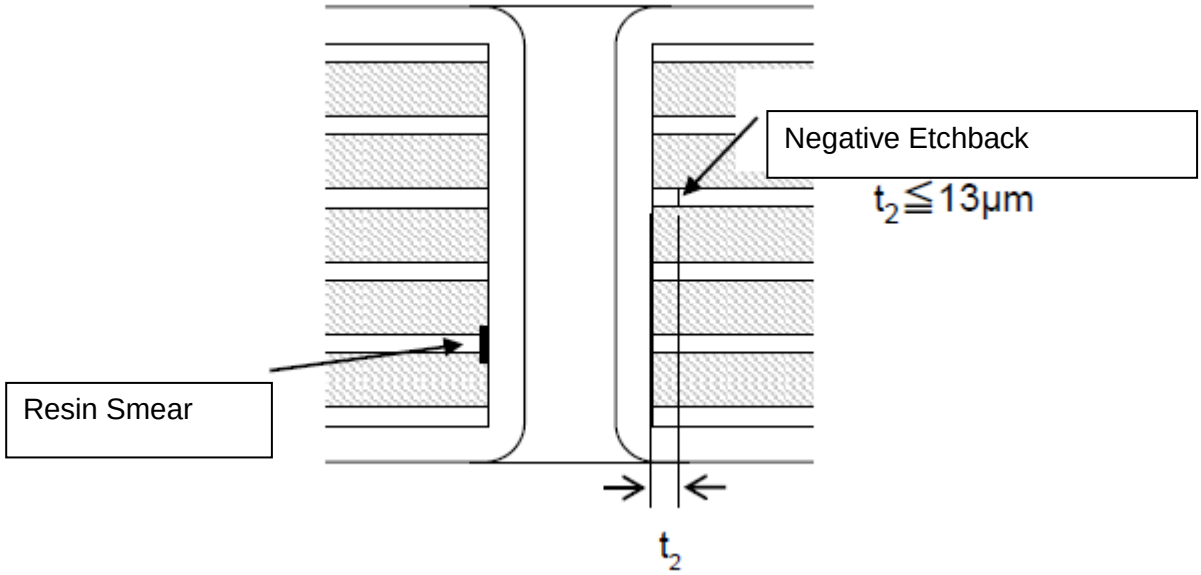


Figure J-19b. Resin Smear and Negative Etchback

Resin smear at connection between LVH and target land shall not be permitted. When viewed from a vertical cross section, target land connection shall not be less than 65% of design value of hole diameter (see Figure J-20) (applied to only type III printed wiring boards).

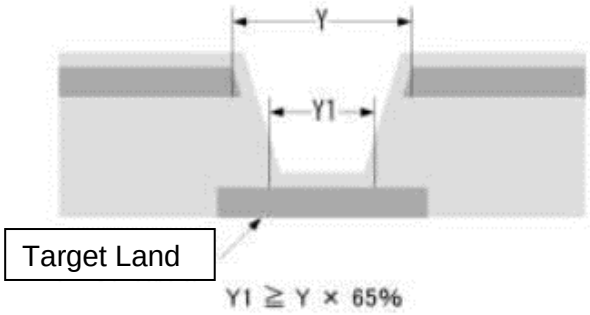


Figure J-20a. Target Land

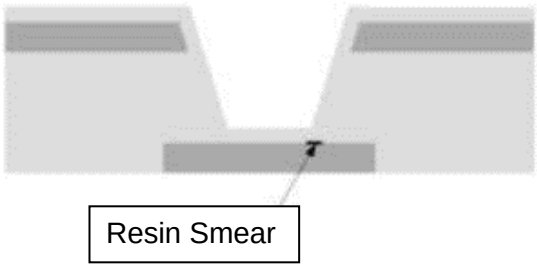


Figure J-20b. Resin Smear of LVH

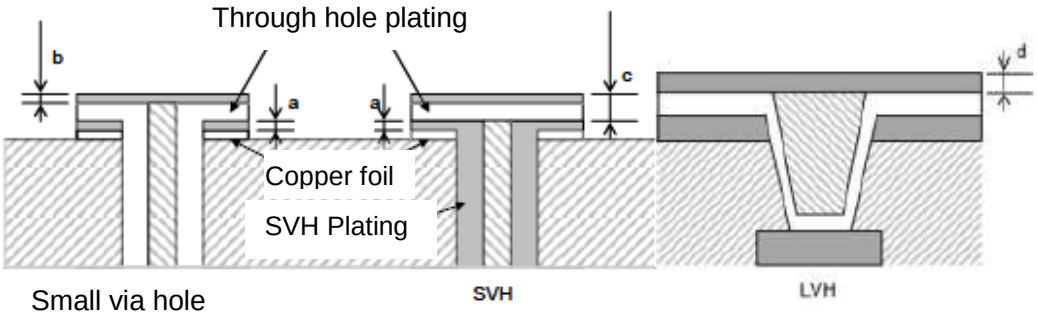
J.3.4.4.7 Plating thickness

When printed wiring boards are tested as specified in paragraph J.4.5.5.6, unless otherwise specified, the plating thickness and solder coating thickness shall meet the requirements specified in Table J-10 and Table J-14.

Table J-14. Thickness of Plating and Other

Unit: μm

Type	Surface and through hole wall thickness		
Electroless copper plating	Thickness necessary and sufficient for electrolytic copper plating in the subsequent process		
Electrolytic copper plating	Component hole		25 as a minimum
	Small via hole		25 as a minimum
	SVH and IVH		25 as a minimum
	LVH	Filled via (at the corner of the capture land)	As specified in detail specification
		Resin-filled via	As specified in detail specification
	Through holes with copper inlay press-fitted		25 as a minimum
	SVH plating on land (Figure J-21 a)		5 as a minimum
	Cap plating	Small via hole (Figure J-21 b)	As specified in detail specification
		SVH (Figure J-21 c)	As specified in detail specification
		LVH (Figure J-21 d)	As specified in detail specification
	Sideplating		25 as a minimum
Electrolytic gold plating	Shown in Table J-10		
Electrolytic nickel plating			
Solder coating			
ENEPIGEG (Electroless Nickel / Electroless Palladium / Immersion Gold / Electroless Gold)			



a: SVH plating thickness on lands
b: Cap plating thickness on small via hole
c: Cap plating thickness on SVH
d: Cap plating thickness on LVH

Figure J-21. Cap Plating Thickness

J.3.4.4.8 Laminate Cracks

When printed wiring boards are tested as specified in paragraph J.4.5.5.7, cracks on laminate shall not be permitted.

J.3.4.4.9 Delamination and Blister

When printed wiring boards are tested as specified in paragraph J.4.5.5.8, delamination and blister shall not be permitted.

J.3.4.4.10 Layer-to-layer Registraion

When printed wiring boards are tested as specified in paragraph J.4.5.5.9, the layer-to-layer registration error shall not exceed 0.15mm.

J.3.4.4.11 Conductor Width of Land (Annular Ring)

When printed wiring boards are tested as specified in paragraph J.4.5.5.10, the minimum conductor width of land of internal and external layer shall not be less than the values specified in Table J-15.

Table J-15. Conductor Width of Land

Unit: mm

Through hole type	Layer	Conductor width of land
Through hole	External	0.05
	Internal	0.025
Non-plated through hole	External	0.38
LVH	External([1])	No hole breakage
	Internal([2])	No hole breakage

Notes ([1]) External: Capture land
([2]) Internal: Target land

J.3.4.4.12 Dielectric Layer Thickness

When printed wiring boards are tested as specified in paragraph J.4.5.5.11, the dielectric layer thickness between conductive layers of a multilayer printed wiring board shall not be less than 0.08mm.

J.3.4.4.13 Adhesion between Cap Plating and Filled Resin

When printed wiring boards are tested as specified in paragraph J.4.5.5.12 and the cap plating is used as BGA pad, the gap between cap plating and filled resin shall be less than 5μm. When the cap plating is not used as BGA pad, the requirements specified in paragraph J.3.4.4.14 shall be satisfied (see Figure J-22). The above-mentioned provisions shall apply to LVH.

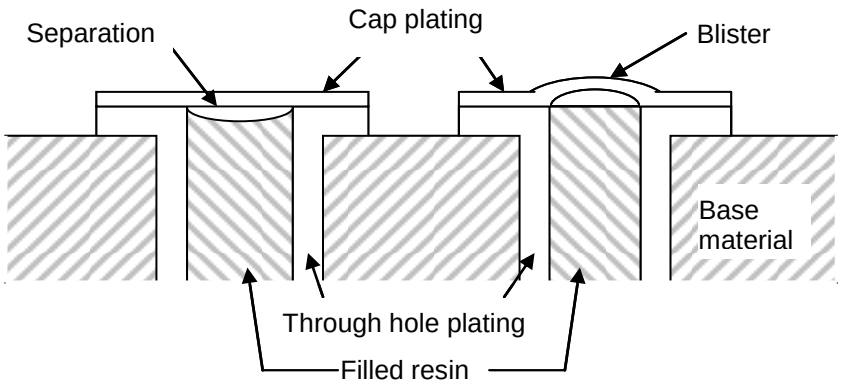


Figure J-22. Adhesion between Cap Plating and Filled Resin

J.3.4.4.14 Protrusion and Pit of Cap Plating

When printed wiring boards are tested as specified in paragraph J.4.5.5.13 and the surface of the land where the resin wasn't filled underneath is used as a reference, the protrusion and pit of the filled resin shall not be more than 50µm and 76µm, respectively (see Figure J-23).
Provisions for LVH shall be specified in the detail specification.

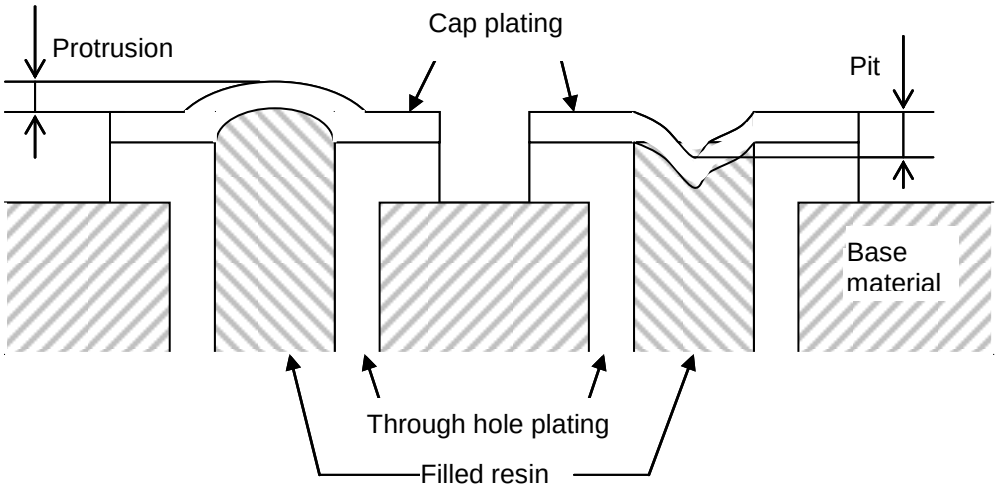


Figure J-23. Protrusion and Pit of Cap Plating

J.3.4.4.15 Filling of Resin

When printed wiring boards are tested as specified in paragraph J.4.5.5.14, the resin shall be filled a minimum of 90% of the hole volume. The pit of the surface shall satisfy the requirements specified in paragraph J.3.4.4.14 (see Figure J-24).
Provisions for LVH shall be specified in the detail specification.

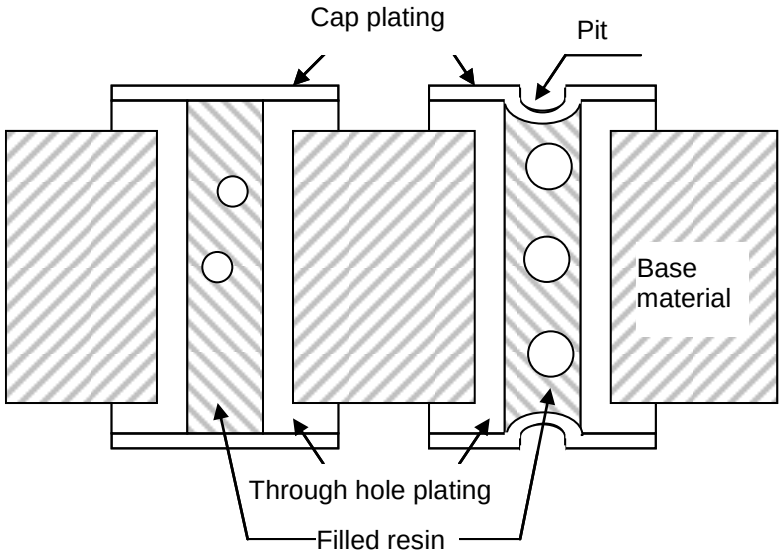


Figure J-24. Filling of Resin

J.3.4.4.16 Penetration of Target Land

Penetration of the target land of LVH shall not be permitted.

J.3.4.5 Solder Resist Thickness

When printed wiring boards are tested as specified in paragraph J.4.5.6, the solder resist thickness shall not be less than 17.5μm, measured at the center of conductors.

J.3.5 Bow and Twist

When printed wiring boards are tested as specified in paragraph J.4.5.7, the maximum limit for bow and twist shall be 0.5%, unless otherwise specified on manufacturing drawings.
For a split board, the percent bow and twist shall not exceed the value specified above, before separation.

J.3.6 Workmanship

The printed wiring boards shall exhibit no defects including fouling, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent and flux residues, which could adversely affect the function, performance or reliability of the printed wiring boards.
The detailed acceptance criteria for workmanship shall be discussed between both parties using samples that show acceptable levels, if necessary.

J.3.6.1 Repair

The insulating plates, BGA conductor pads or conductors shall not be repaired. However, the removal of an excessive conductor and an insignificant repair of solder resist may be permitted, provided that the repaired solder resist thickness shall not be more than the surrounding solder resist thickness.

J.3.7 Plating Adhesion and Overhang

When printed wiring boards are tested as specified in paragraph J.4.5.9, there shall be no separation or lifting of plating and conductors, or slivers from the conductor edges.

J.3.8 Cleanliness

When printed wiring boards are tested as specified in paragraph J.4.5.10, the resistivity of the solvent extract shall not be less than $2x10^6\Omega \cdot cm$.

J.3.9 Electrical Performance

Printed wiring board shall meet the following electrical requirements.

J.3.9.1 Dielectric Withstanding Voltage

When printed wiring boards are tested as specified in paragraph J.4.5.11.1, the printed wiring boards shall not exhibit insulation breakdown, flashover or sparkover.

J.3.9.2 Circuitry

When printed wiring boards are tested as specified in paragraph J.4.5.11.2, the printed wiring boards shall not exhibit open circuit or short-circuiting between circuit patterns.

J.3.9.3 Connection Resistance

When printed wiring boards are tested as specified in paragraph J.4.5.11.3, the resistance between two lands connecting a circuit on all conductive layers shall not exceed the value (Ri) which is calculated by the formula specified below.
When the connection resistance between all layers can not be measured at a time, the unmeasured connection resistance shall be repeatedly measured separately until all connection resistance is measured.
This requirement shall not be applied to the circuits with copper inlay.

$$Ri = 2\rho \frac{l}{W \cdot t} (m\Omega)$$

ρ: Volume resistivity at 20°C of the main metal which forms the conductor (mΩ·mm)
l: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

J.3.9.3.1 Connection Resistance of Copper Inlay

Connection resistance of copper inlay shall be tested as specified in paragraph J.4.5.11.3.1. Test results shall be evaluated using the measurement results before each test is conducted as initial values.

J.3.9.4 Characteristic Impedance

When characteristic impedance is specified in the drawing and printed wiring boards are tested as specified in paragraph J.4.5.11.4, the characteristic impedance shall be within the range specified in the manufacturing drawing. If the tolerance is not specified, the impedance shall be within ±10% of the specified value.

J.3.10 Mechanical Performance

Printed wiring boards shall meet the following mechanical requirements.

J.3.10.1 Through Hole Pull Strength

When printed wiring boards are tested as specified in paragraph J.4.5.12.1, the printed wiring boards shall meet the following requirements. This provision shall apply only to component holes.

a) Bond strength
The land shall withstand a minimum of 89.2N pull or 1380N/cm^2, whichever is smaller.

b) Conductor and land
When printed wiring boards are inspected visually as specified in paragraph J.4.5.4.1, there shall be no loosening around the through holes.

c) Microsection of through hole
When printed wiring boards are microsectioned and inspected as specified in paragraph J.4.5.5, there shall be no cracks, blistering, measling or delamination.

J.3.10.2 Solderability

When printed wiring boards are tested as specified in paragraph J.4.5.12.3, the printed wiring boards shall meet the following requirements.

a) Through hole solderability
The through hole inside wall and land surface shall exhibit proper wetting of solder. This provision shall apply to only component holes.

b) Surface conductor solderability
A minimum of 95 % of the surface conductor area shall be covered uniformly with fresh solder. The scattered existence of pinholes, dewetting or small roughened points shall be acceptable, provided that they are not concentrated in one area.

J.3.10.3 Peel Strength of Surface Conductor

When printed wiring boards are tested as specified in paragraph J.4.5.12.2, the printed wiring boards shall meet the requirements specified in the detail specification.

J.3.10.4 Extrusion Strength of Copper Inlay

When type I and II printed wiring boards are tested as specified in paragraph J.4.5.12.4, the printed wiring boards shall meet the requirements specified in the detail specification.

J.3.11 Environmental Performance

Printed wiring boards shall meet the following environmental requirements.

J.3.11.1 Thermal Shock

J.3.11.1.1 Thermal Shock (I) (applicable to qualification test)

When printed wiring boards are tested as specified in paragraph J.4.5.13.1 a), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph J.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

J.3.11.1.2 Thermal Shock (II) (Applied to Quality Conformance Inspection)

When printed wiring boards are tested as specified in paragraph J.4.5.13.1 b), there shall be no open circuit, blistering, measling, crazing or delamination. Printed wiring boards shall meet the requirements specified in paragraph J.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%.

J.3.11.1.3 Cross Section after Thermal Shock

After printed wiring boards are tested as specified in paragraph J.4.5.13.1 a) or J.4.5.13.1 b), samples prepared according to paragraph J.4.5.5.1 shall meet the requirements specified in paragraph J.3.11.4 b).

J.3.11.2 Humidity and Insulation Resistance

When printed wiring boards are tested as specified in paragraph J.4.5.13.2, there shall be no blistering, measling or delamination. The insulation resistance between conductors shall be a minimum of 500MΩ.

J.3.11.3 Hot Oil Resistance

When printed wiring boards are tested as specified in paragraph J.4.5.13.3, the change in connection resistance between circuits before and after the test shall be less than 10%.

J.3.11.4 Thermal Stress

When printed wiring boards are tested as specified in paragraph J.4.5.13.4, the printed wiring boards shall meet the following requirements.

a) Externals

There shall be no measling, cracks, separation of plating and conductors, blistering or delamination.

b) Structural Integrity
In the vertical microsection of through holes, the following requirements shall be satisfied.

1) Through hole
There shall be no corner cracks or barrel cracks.
2) Laminate void
When the conductor spacing on the same plane or between layers satisfies the minimum conductor spacing specified in the manufacturing drawings, the spacing shall not exceed 76µm.
3) Lifting of lands
Lifting of lands after thermal stress test shall be permitted.
4) Cracks on copper foil
There shall be no cracks which penetrate through the copper foil.
5) Internal layer connection
There shall be no separation between copper foil of internal layer and through hole plating, and between target land and LVH plating.
6) Laminate Cracks
After the thermal stress test, the laminate cracks between the lands of a through holes or on the lands shall not exceed 80µm, and the laminate cracks other than the ones on the land area shall not cause the spacing between adjacent conductors fall below the minimum conductor spacing.
7) Delamination and blister
There shall be no delamination and blisters.
8) Adhesion of cap plating and filled resin
The interface between cap plating and filled resin shall meet the requirements specified in paragraph J.3.4.4.13 Adhesion between Cap Plating and Filled Resin.
9) For through holes with copper inlay embedded, unevenness of the copper inlay shall meet the requirements specified in paragraph J.3.4.2.

Note: If there are any description conflicting with above requirements, quality shall be deemed to be assured by satisfying quality requirements specified in the detail specification.

J.3.11.5 Radiation Hardness

When printed wiring boards are tested as specified in paragraph J.4.5.13.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall not be less than 500MΩ. After the test, the requirements specified in paragraph J.3.9.1 shall be satisfied.

J.3.11.6 Vibration

When printed wiring boards are tested as specified in paragraph J.4.5.13.6, the printed wiring boards shall meet the requirements specified in paragraph J.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. Furthermore, the printed wiring

boards shall meet the requirements specified in paragraphs J.3.4.1.2 b) and J.3.4.1.4 and unevenness of the copper inlay shall meet the requirements specified in paragraph J.3.4.2.

J.3.11.7 Shock

When printed wiring boards are tested as specified in paragraph J.4.5.13.7, the printed wiring boards shall meet the requirements specified in paragraph J.3.9.2 at the completion of the test, and the change in connection resistance between circuits before and after the test shall be less than 10%. Furthermore, the printed wiring boards shall meet the requirements specified in paragraphs J.3.4.1.2 b) and J.3.4.1.4 and unevenness of the copper inlay shall meet the requirements specified in paragraph J.3.4.2.

J.3.12 Optional Tests

This paragraph specifies the tests that are out of the scope of requirements specified in this specification and that are not used for pass/fail decisions for qualified items. Optional tests can be conducted additionally at the user's request, however, the test method and handling of test results, etc. shall be decided between the user and the part manufacturer in advance.

J.3.12.1 IST (Interconnect Stress Test)

If requested by the user, printed wiring boards shall be tested as specified in paragraph J.4.5.14.1, and meet the requirements specified in the detail specification. This test is not applicable to copper inlay section.

J.3.12.2 Pad Strength Test

If requested by the user, printed wiring boards shall be tested as specified in paragraph J.4.5.14.2, and meet the requirements specified in the detail specification.

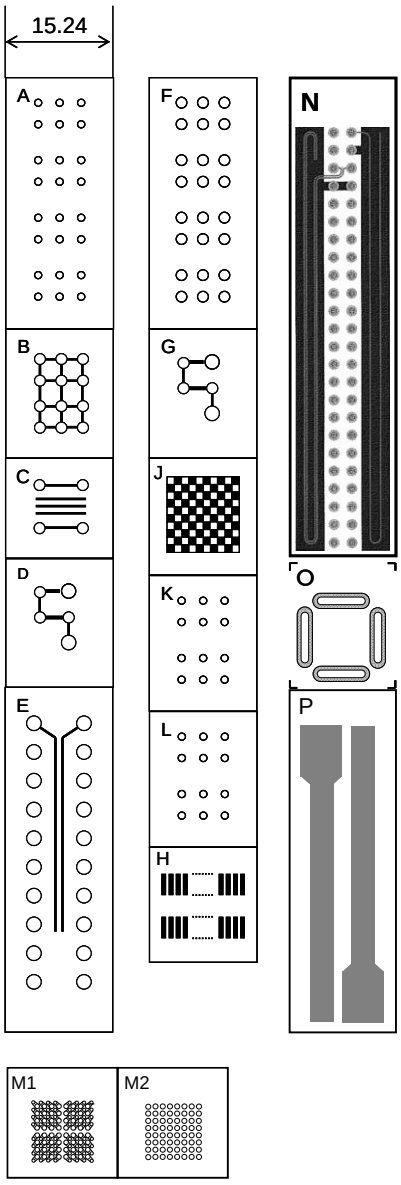
J.4. Quality Assurance Provisions

J.4.1 Test Coupon

The test coupon provided for qualification test and quality conformance inspection shall be in accordance with Figure J-25. The test coupon shall have the same construction as the product produced from the identical work board.
At least a set of the test coupon shall be assigned for each work board.

Arrangement of test coupons

Unit: mm



Notes

(1) Unless otherwise specified, the conductor width shall be 0.5±0.1mm.

(2) Test coupon A indicates the minimum hole diameter of the through hole (incl. small via hole) for the corresponding printed wiring board, and the land diameter shall be the minimum land diameter of the through holes. When applied, small via holes shall be filled with resin. The hole diameter tolerance is not specified.

(3) For test coupons B, C, E and F, the land diameter shall be 1.8±0.13mm, and the land shape shall be the typical land shape of the products. All holes shall be through holes and diameter shall be ϕ0.8mm. The hole diameter tolerance shall be the tolerance for the corresponding printed wiring board.

(4) The patterns of test coupons D and G vary depending on the number of layers and via hole (including LVH) construction. Each coupon shall be produced so as to form the same number of layers and via hole construction as those of the corresponding product, and to have a circuit continuity through all layers by via holes. Copper inlay may not be included. The hole and land diameter shall be the minimum diameter for each SVH, IVH, LVH and small via hole of the corresponding products, and the land shape shall be the typical land shape of the products. On both ends of the printed wiring board, through holes shall be formed to measure the resistance, the diameter of the land and hole shall be ϕ1.8mm and ϕ0.8mm, respectively. The hole diameter tolerance is not specified.

(5) Solder resist shall apply to the test coupons E, H, and J, only when solder resist is required for the products. The clearance spacing for the solder resist shall be the clearance diameter for the corresponding printed wiring board. If the hole diameter for the product is unknown, the land diameter shall be equal to the land diameter + 0.2mm.

(6) Test coupons K and L shall be prepared only when the corresponding products have SVH, IVH and LVH. Those coupons vary depending on the number of layers and via hole construction.
The land shall be formed only on the layers which are connected by SVH, IVH and LVH.

(7) Test coupons D, E and G are different in the number of conductors, depending on the number and construction of layers. The conductors shall be formed on all layers in accordance with this figure.

(8) The arrangement of test coupons shown in this figure is an example; a different arrangement is also acceptable.

(9) The symbols of test coupons (A to H and J to M2) shall be used for identification and not for the object of inspection. The marking method is not specified.

(10) Only when the BGA pads, etc. are required, the test coupon M1 (Dog-bone construction) or test coupon M2 (VIP construction) shall be formed in accordance with the pad construction. An example of test coupons M1 and M2 is shown to the left. See detail specification for more detailed information.

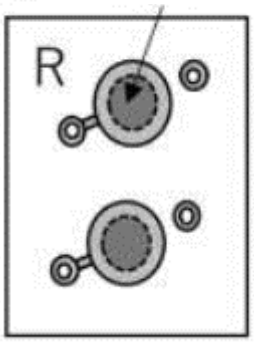
(11) Only when the characteristic impedance is required, the test coupon N shall be formed. If the characteristic impedance are assured, the other test coupon may be used.

(12) Only when the outer perimeter sideplating is required, the test coupon O shall be formed. An example of test coupons O is shown to the left. See detail specification for more detailed information.

(13) Only when the construction where copper foil is laminated on the outer layer is required, the test coupon P shall be formed.

Figure J-25. Test Coupon (1/12)

Copper Inlay

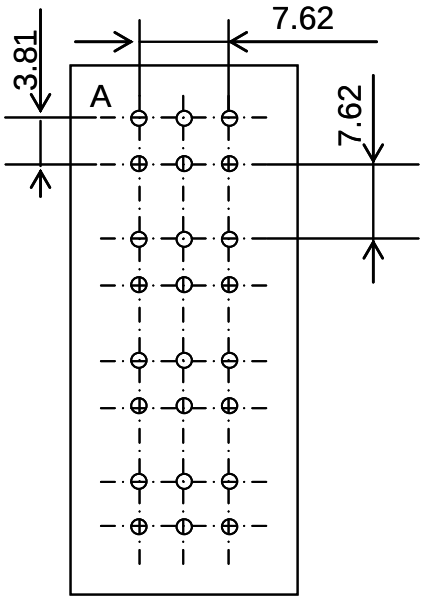


(14) For type I and II printed wiring boards, test coupon R shall be formed. Number of copper inlay shall be two.
(15) For type III printed wiring boards, test coupon S shall be formed in order to evaluate continuity between copper inlay and LVH and insulation between copper inlay and adjacent conductors. Details of test coupon S shall be as specified in the detail specification.
(16) When specified in the drawings or other documentation, IST test coupon shall be formed.

Figure J-25. Test Coupon (1/12) (Continued)

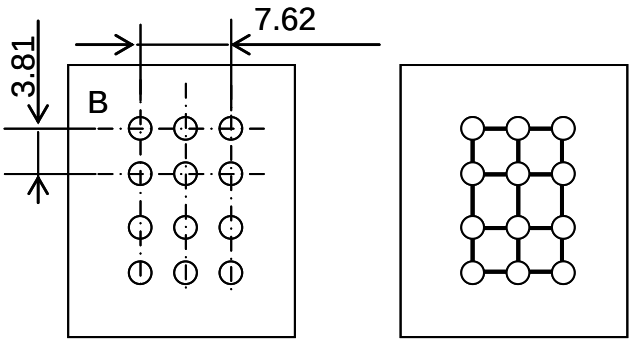
Unit: mm

Test coupon A



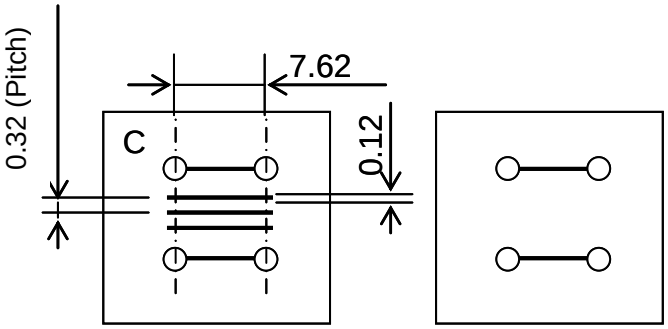
Internal and external layer

Test coupon B



External layer Internal layer

Test coupon C

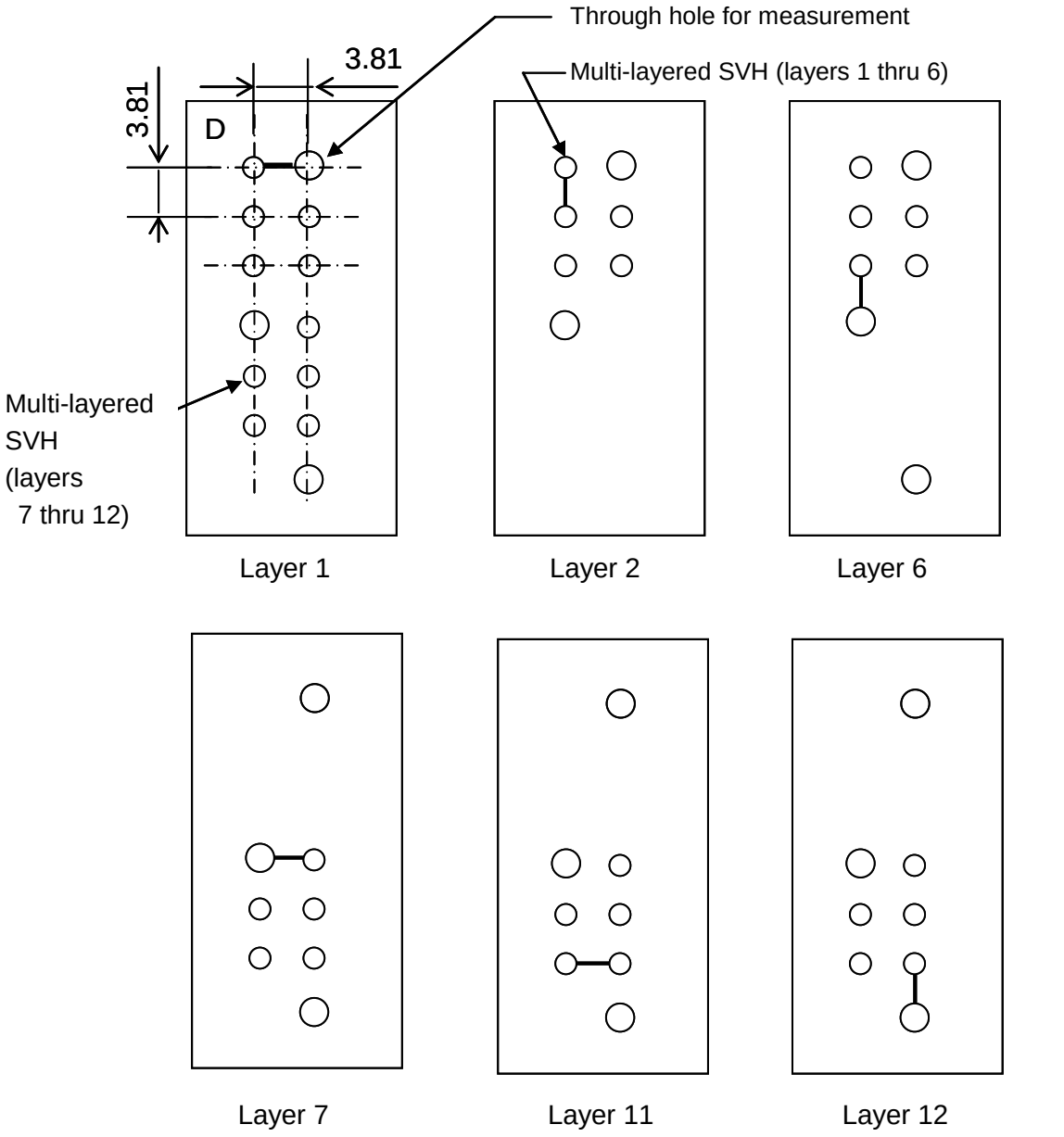


External layer Internal layer

Figure J-25. Test Coupon (2/12)

Test coupon D and G

Unit: mm

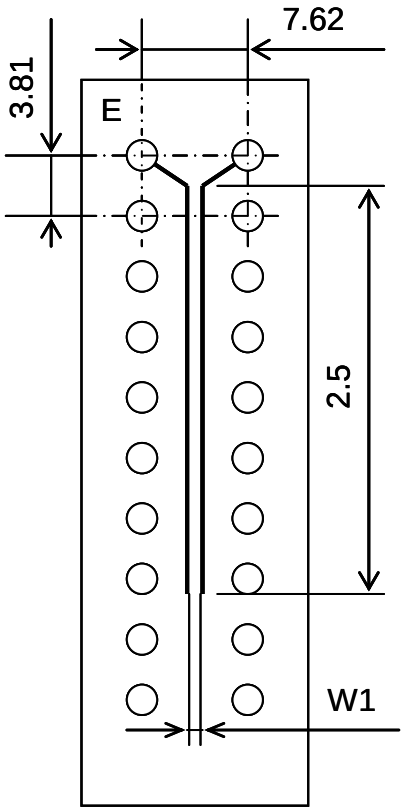


This figure shows an example of layers 1 through 6 and 7 through 12 of SVH.

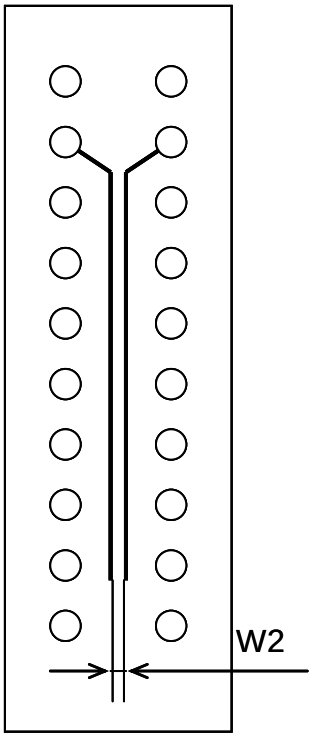
Figure J-25. Test Coupon (3/12)

Unit: mm

Test coupon E

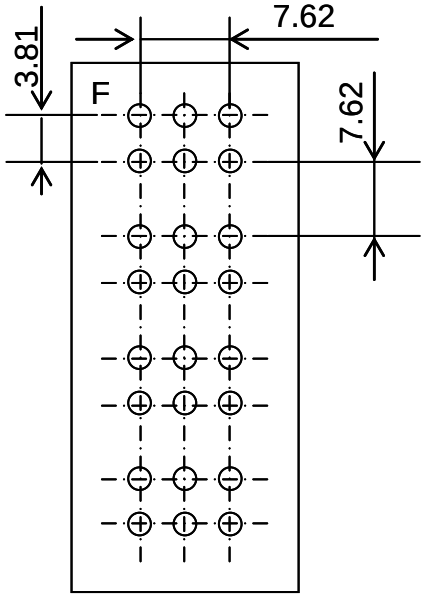


Layer 1



Layer 2

Test coupon F



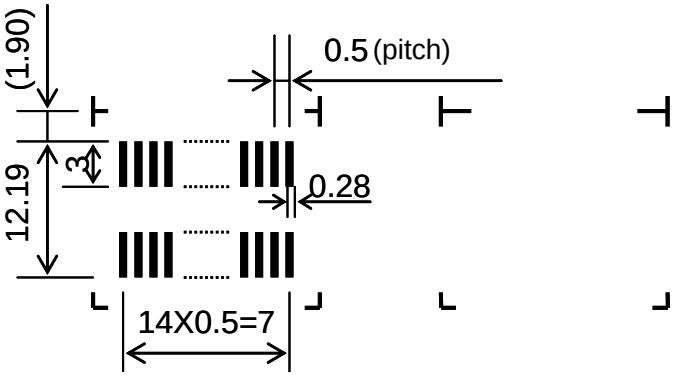
External and Internal layer

W1: Minimum conductor spacing on the external layer of the product or 0.14mm
W2: Minimum conductor spacing on the internal layer of the product or 0.08mm

Figure J-25. Test Coupon (4/12)

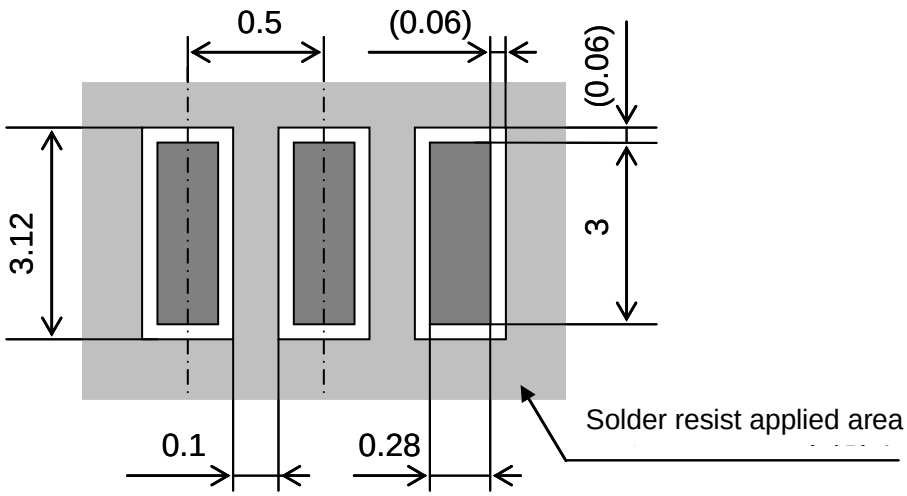
Test coupon H

Unit: mm



Number of pads: 15
(in this range)

Top surface Bottom surface (no pattern)

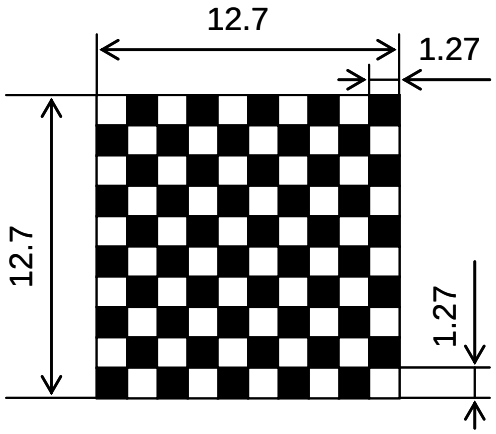


Enlarged view of pad area

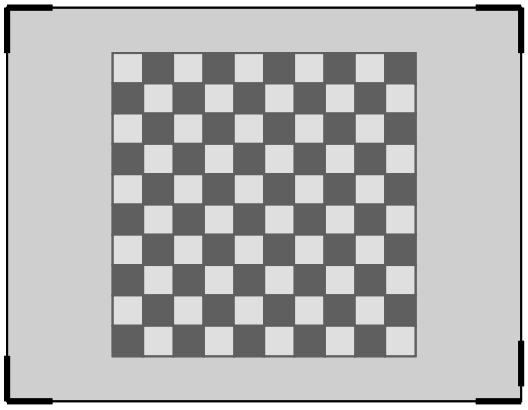
Figure J-25. Test Coupon (5/12)

Unit: mm

Test coupon J

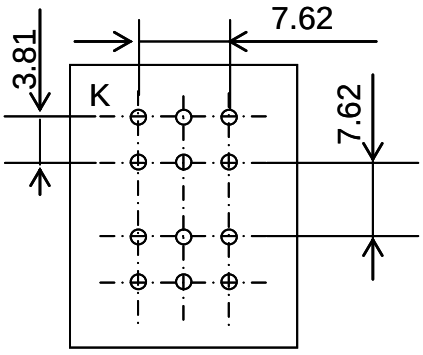


Top and bottom surface

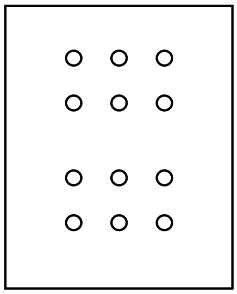


Solder resist applied area

Test coupon K and L



External layer

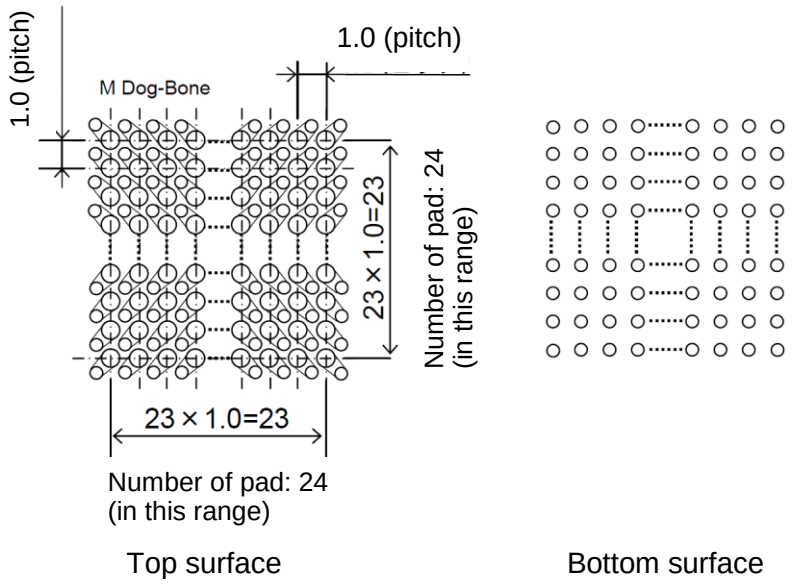


Internal layer (SVH layer)

Figure J-25. Test Coupon (6/12)

Unit: mm

Test coupon M1 (Dog-Bone construction)



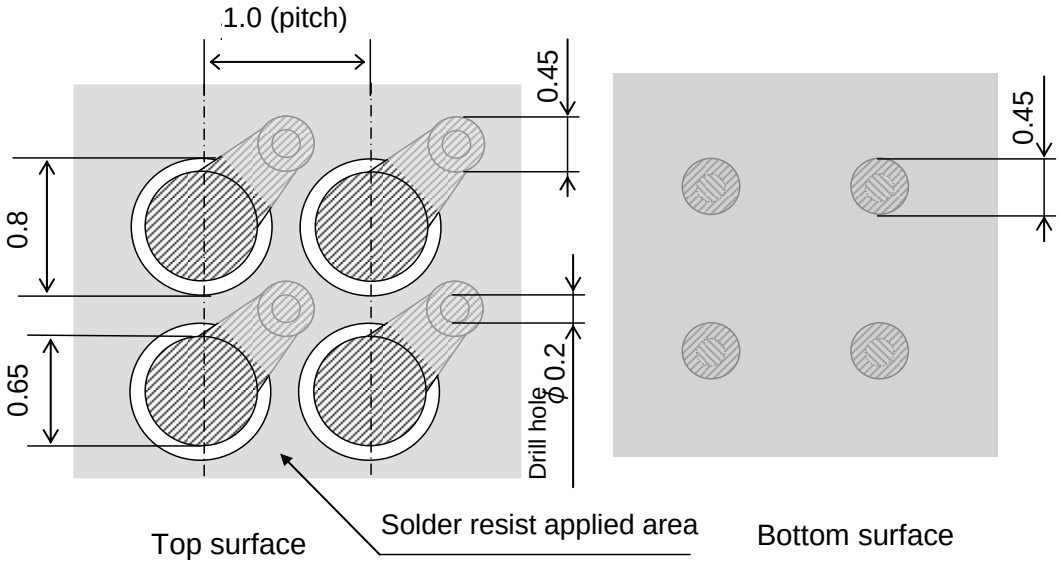


Figure J-25. Test Coupon (Example of BGA pads) (7/12)

Unit: mm

Test coupon M2 (VIP construction)

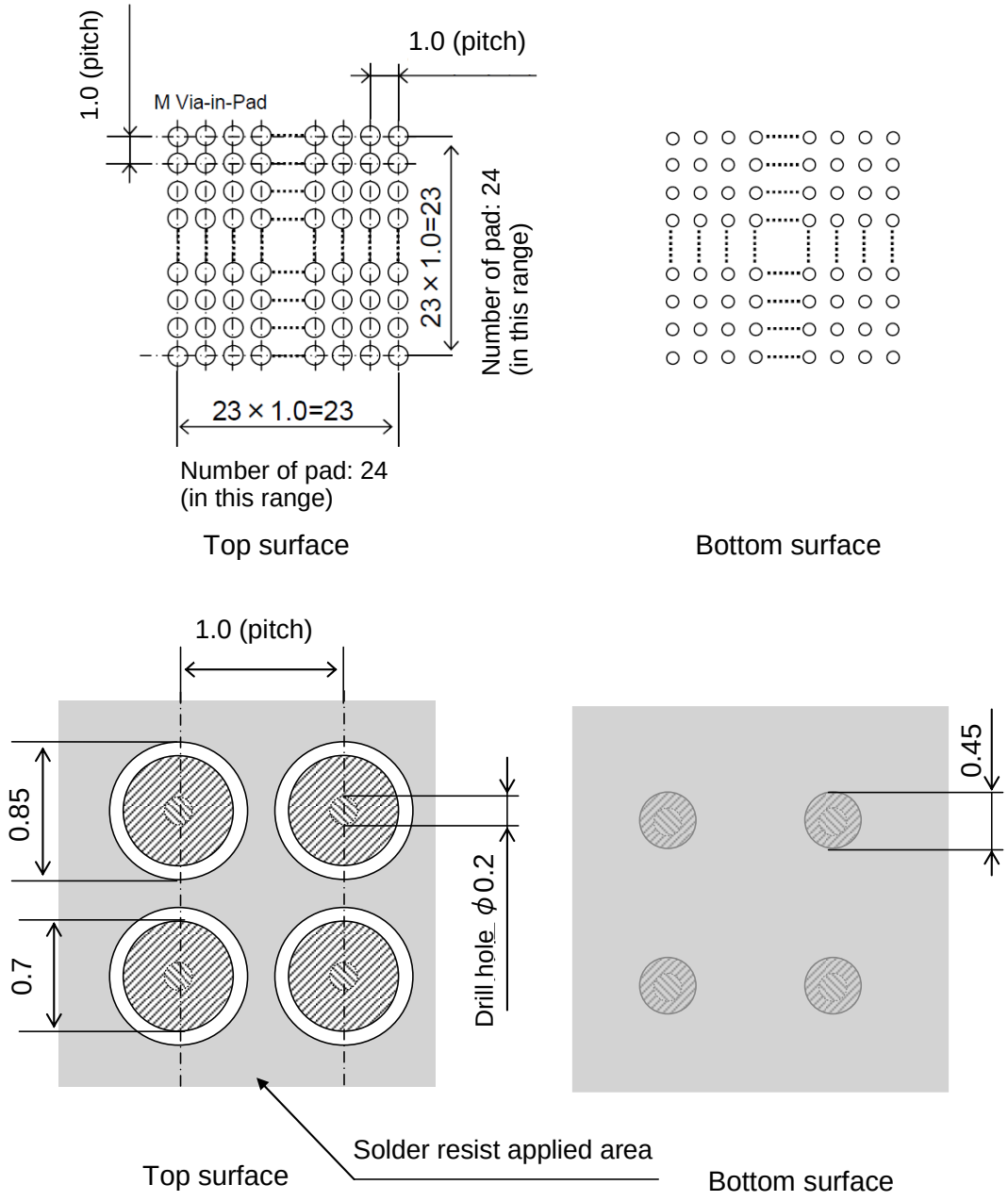
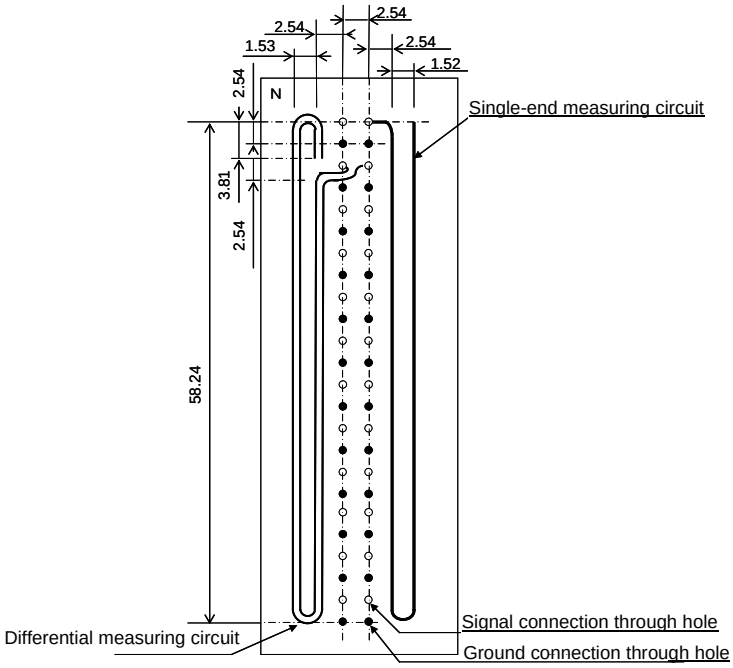


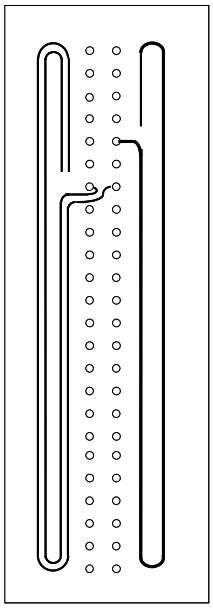
Figure J-25. Test Coupon (Example of BGA pads) (8/12)

Unit: mm

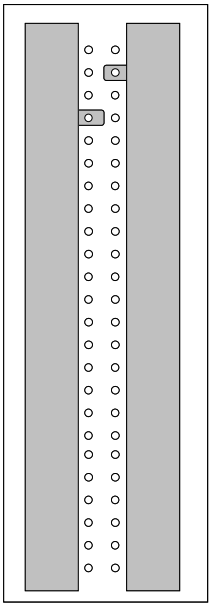
Test coupon N



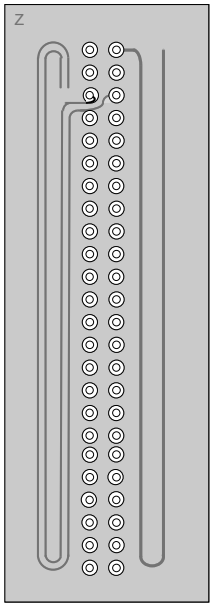
External layer



Internal layer (impedance control layer)



Internal layer (ground layer)



Solder resist applied area

Figure J-25. Test Coupon (Characteristic Impedance) (9/12)

Test coupon O

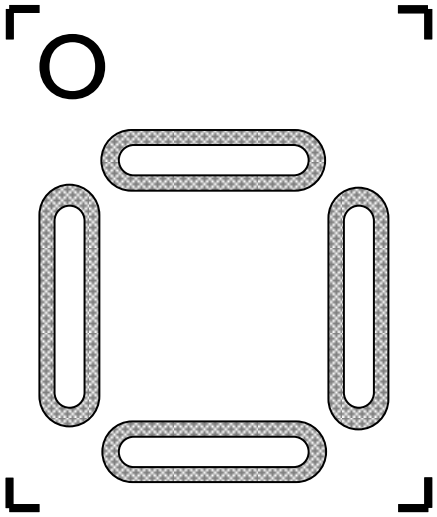
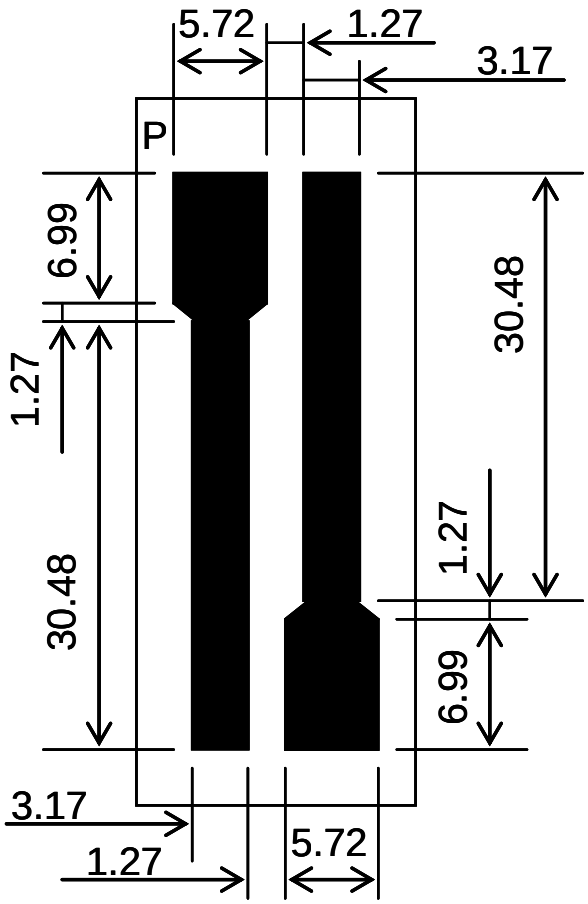


Figure J-25. Test Coupon (Outer Perimeter Sideplating) (10/12)

Unit: mm

Test coupon P



Front surface and back surface

Figure J-25. Test Coupon (Peel Strength) (11/12)

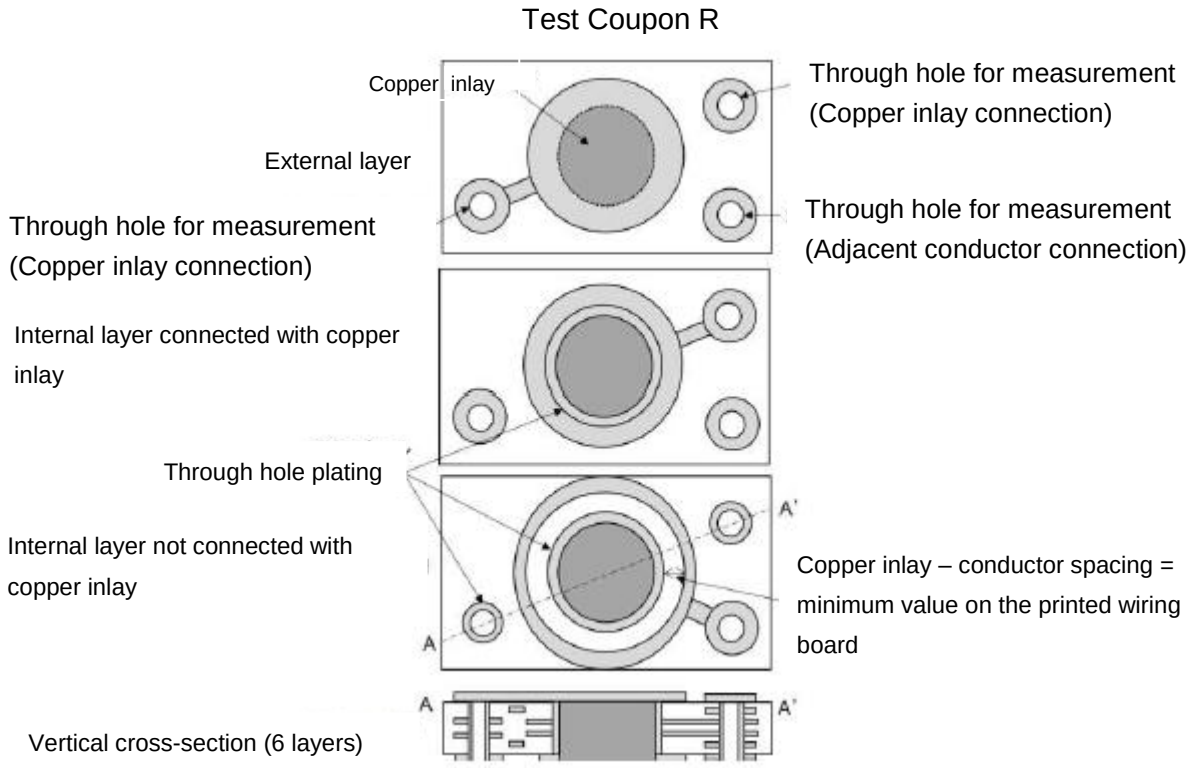


Figure J-25. Test Coupon (Extrusion Strength of Copper Inlay, Continuity and Insulation) (12/12)

J.4.2 In-Process Inspection

The in-process inspection specified in Table J-16 shall be performed per production lot and printed wiring boards shall meet the requirements of paragraphs J.3.4.1 (Externals of Conductor, Base Material, Solder Resist and Copper Inlay), J.3.4.2 (Dimensions), J.3.4.3 (Marking), J.3.8 (Cleanliness), and J.3.4.2.1 (Dimensions of BGA Pads, etc).

Table J-16. In-Process Inspection

No.	Item	Requirement paragraph	Test method paragraph	Sample size	Inspection timing
1	Externals of internal layer, dimensions and marking, etc.	J.3.4.1 J.3.4.2 J.3.4.3	J.4.5.4.1 J.4.5.4.2 J.4.5.4.3	All	After forming internal circuit and before pre-treating the laminate layer
2	Conductor of external layer Base material of external layer	J.3.4.1.1 J.3.4.1.2	J.4.5.4.1	All	After forming external circuit and before applying solder resist
3	Cleanliness	J.3.8	J.4.5.10	AQL 1.0%	After forming external circuit and before applying solder resist
4	Dimensions of BGA pads, etc.	J.3.4.2.1	J.4.5.4.2	All	After forming solder resist and before solder coating
5	Externals of copper inlay section	J.3.4.1.4	J.4.5.4.1 d)	All	After forming circuit on copper inlay press-fit layer

J.4.3 Qualification Test

J.4.3.1 Sample

Samples shall have the minimum conductor width, conductor spacing, SVH, small via hole, copper inlay, number of layers and construction sufficient enough to verify compliance with the requirements of this appendix. Samples shall consist of the production printed wiring boards and test coupons manufactured on the same work board as the production printed wiring board.
In order to qualify split boards, split board specimens shall be subjected to the qualification test. The split boards shall include at least one of deep-hole-shape slit, V-groove cut and continuous perforation.

J.4.3.2 Test Items and Number of Samples

The tests of each group shall be performed in the order listed in Table J-17. Upon completion of Group I and II tests, Group III through IX tests shall be performed using specimens allocated to the appropriate group tests. Group III through IX tests may be performed in any order regardless of group number. However, tests in each of Group III through IX shall be performed in the order listed.

Six production printed wiring boards shall be prepared for each test condition. The number of test coupons shall be as specified in Table J-17.

Table J-17. Qualification Test

Test			Requirement paragraph	Test method paragraph	Pass/fail Criteria		
					Sample size		Number of defectives permitted
Group	Order	Test item			Production printed wiring boards	Test coupon (1) (2)	
I	1	Externals of conductor, base materials, and solder resist Externals, dimensions, Dimensions Marking	J.3.4.1 J.3.4.2 J.3.4.3	J.4.5.4.1 J.4.5.4.2 J.4.5.4.3	No. 1 to No. 6	A, B, C, D, E, F, G, H, K, L, M, N, O, P, R and S	0
	2	Workmanship	J.3.6	J.4.5.8			
II	1	Plating adhesion and overhang	J.3.7	J.4.5.9	No. 1 to No. 6	C	
	2	Bow and twist	J.3.5	J.4.5.7		N/A	
III	1	Structural integrity	J.3.4.4	J.4.5.5	No. 1	A, F, K, M and O	
	2	Through hole pull strength	J.3.10.1	J.4.5.12.1		F	
	3	Solder resist thickness	J.3.4.5	J.4.5.6		J	
	4	Peel strength of surface conductor(3)	J.3.10.3	J.4.5.12.2		P	
	5	Extrusion strength of copper inlay (4)	J.3.10.4	J.4.5.12.4		R	
IV	1	Connection resistance	J.3.9.3	J.4.5.11.3	No. 2	D, R and S (5)	
	2	Hot oil resistance	J.3.11.3	J.4.5.13.3			
	3	Connection resistance	J.3.9.3	J.4.5.11.3			
V	1	Circuitry	J.3.9.2	J.4.5.11.2	No. 3	E, G, R and S(6)	
	2	Connection resistance	H.3.9.3	J.4.5.11.3			
	3	Thermal shock (I)	J.3.11.1.1	J.4.5.13.1a)			
	4	Circuitry	J.3.9.2	J.4.5.11.2			
	5	Connection resistance	J.3.9.3	J.4.5.11.3			
	6	Cross-section after thermal shock	J.3.11.1.3	J.4.5.5.1			
VI	1	Humidity and insulation resistance	J.3.11.2	J.4.5.13.2	No. 4	E, R and S (5)	
	2	Dielectric withstanding voltage	J.3.9.1	J.4.5.11.1			
VII	1	Thermal stress	J.3.11.4	J.4.5.13.4	No. 5	A, B, L M, O, R and S	
	2	Solderability	J.3.10.2	J.4.5.12.3		B and H(7)	
VIII	1	Radiation hardness	J.3.11.5	J.4.5.13.5	No.6	N/A	
IX	1	Vibration	J.3.11.6	J.4.5.13.6	As specified in J.4.5.13.6 h) and J.4.5.13.7 h).		0
	2	Shock	J.3.11.7	J.4.5.13.7			
-	-	Materials	J.3.2	J.4.5.2	N/A		N/A

Notes:

(1) The number of test coupons submitted for Group I tests shall be a summation of the test coupons for Group II through IX tests. For Group II through IX tests, one test coupon shall be provided for each coupon

type specified above. When a test coupon has failed to pass the marking test, the coupon may be replaced with a non-defective one.

(2) Test coupons and sample product shall be fabricated simultaneously. For Group III through IX tests, each test coupon shall be manufactured on the same work board as the production printed wiring boards which shall be subjected to the same group test.

(3) This test shall be performed when copper foil laminate construction is under the qualification coverage.

(4) Applied to type I and II printed wiring boards.

(5) The test coupon R shall be tested for type I and II printed wiring boards and the test coupon S shall be tested for type III printed wiring boards.

(6) Under the circuitry test, the test coupon G shall be subjected to the continuity test, test coupon E shall be subjected to the circuit shorts test, test coupon R shall be subjected to the continuity test and circuit shorts test for copper inlay of type I and II printed wiring boards, and test coupon S shall be subjected to the continuity test and circuit shorts test for copper inlay including type III LVH.

(7) The test coupon B shall have been subjected to thermal stress test prior to this test. The test coupons B and H shall be subjected to the tests for through hole solderability and surface conductor solderability, respectively.

J.4.4 Quality Conformance Inspection

J.4.4.1 Quality Conformance Inspection (Group A)

J.4.4.1.1 Sample

The quality conformance inspection shall be performed with the sample products and the test coupons. The test coupons and sample product shall be manufactured simultaneously.
Even though any part of a split board fails an inspection in the manufacturing process and is marked with rejection, the board may be included in an inspection lot. However, in order not to adversely affect the inspection result, the part marked with rejection shall not be used as a specimen.
A “split board” means a board constructed of parts of the same patterns or parts of different patterns.

J.4.4.1.2 Inspection Items and Sample Size

Test items and test order of Group A inspection shall be in accordance with Table J-18. The inspections within each group shall be performed in the order listed.
One test coupon shall be provided for each of Group IV and V test.

Table J-18. Quality Conformance Inspection (Group A)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria		
					Sample size		
Group	Order	Inspection item			Production printed wiring boards	Test coupon	Number of defectives permitted
I	1	Design and construction	J.3.3	J.4.5.3	100%	N/A	0
	2	Externals of conductor, base materials, and solder resist	J.3.4.1	J.4.5.4.1			
		Dimensions	J.3.4.2	J.4.5.4.2			
		Marking	J.3.4.3	J.4.5.4.3			
	3	Workmanship	J.3.6	J.4.5.8			
	4	Characteristic impedance	J.3.3.19	J.4.5.11.4	100%	N(1)	
II	1	Bow and twist	J.3.5	J.4.5.7	100%	N/A	
III	1	Circuitry	J.3.9.2	J.4.5.11.2	100%	N/A	
IV	1	Thermal stress	J.3.11.4	J.4.5.13.4	N/A	A, F, K(2), M(3) , O(4), R and S(5)	
V	1	Solderability	J.3.10.2	J.4.5.12.3	N/A	F and H(6)	

Notes:

(1) Test coupon N shall be inspected when characteristic impedance is required.

(2) Test coupon A shall be inspected only when the product is provided with small via holes. Test coupons K shall be inspected only when the product is provided with SVH.

(3) Test coupon M shall be inspected when the products is provided with pads such as BGA pads.

(4) Test coupon O shall be inspected when the sideplating is required.

(5) Test coupon R shall be inspected for type I and II printed wiring boards and the test coupon S shall be inspected for type III printed wiring boards.

(6) Test coupons F and H shall be subjected to the tests for through hole solderability and surface conductor solderability, respectively.

J.4.4.2 Quality Conformance Inspection (Group B)

J.4.4.2.1 Sample

Test coupons for Group B inspection shall be manufactured at the same time as those for Group A inspection and selected from the lot which passed Group A inspection.

J.4.4.2.2 Inspection Items and Sample Size

Test items and test order of Group B inspection shall be as specified in Table J-19.
The inspections within each group shall be performed in the order listed.
One test coupon shall be subjected to each of test Groups.

Table J-19. Quality Conformance Inspection (Group B)

Inspection			Requirement paragraph	Test method paragraph	Pass/fail criteria	
Group	Order	Inspection item			Test coupon	Quantity of allowable defects
I	1	Plating adhesion and overhang	J.3.7	J.4.5.9	C	0
II	1	Through hole pull strength	J.3.10.1	J.4.5.12.1	F	
III	1	Connection resistance	J.3.9.3	J.4.5.11.3	D, R and S(1)	
	2	Hot oil resistance	J.3.11.3	J.4.5.13.3		
	3	Connection resistance	J.3.9.3	J.4.5.11.3		
IV	1	Circuitry	J.3.9.2	J.4.5.11.2	E, G, R and S(2)	
	2	Connection resistance	J.3.9.3	J.4.5.11.3		
	3	Thermal shock (II)	J.3.11.1.2	J.4.5.13.1b)		
	4	Circuitry	J.3.9.2	J.4.5.11.2		
	5	Connection resistance	J.3.9.3	J.4.5.11.3		
	6	Cross-section after thermal shock	J.3.11.1.3	J.4.5.5.1		
V	1	Humidity and insulation resistance	J.3.11.2	J.4.5.13.2	E, R and S(1)	
	2	Dielectric withstanding voltage	J.3.9.1	J.4.5.11.1		
VI	1	Peel strength of surface conductor	J.3.10.3	J.4.5.12.2	P(3)	
	2	Extrusion strength of copper inlay(4)	J.3.10.4	J.4.5.12.4	R	

Notes:

(1) Test coupon R shall be inspected for type I and II printed wiring boards and the test coupon S shall be inspected for type III printed wiring boards.

(2) Under the circuitry test, the test coupon G shall be subjected to the continuity test, test coupon E shall be subjected to the circuit shorts test, test coupon R shall be subjected to the continuity and circuit shorts test of copper inlay of type I and II printed wiring boards and test coupon S shall be subjected to the continuity and circuit shorts test of copper inlay including LVH of type III printed wiring boards.

(3) Peel strength of surface conductor is performed when copper foil laminate construction is used. If copper foil laminate construction is in qualification coverage and group B inspection is performed on a sample without this construction, the inspection shall be performed again on the first lot of the products with this construction.

(4) Applied to type I and II printed wiring boards.

J.4.5 Methods for Test and Inspection

J.4.5.1 Condition of Test and Inspection

Conditions for test and inspection shall be as specified in paragraph 4.2 of MIL-STD-202. The base condition shall be kept at a temperature of 15°C to 35°C, a relative humidity of 45% to 75%, and a luminance of 750 lx as a minimum.

J.4.5.2 Materials

The copper clad laminates, prepreg and copper foil shall be verified with the documents which prove that the materials meet the applicable standards per used material lot. The other materials shall be verified with the documents which prove that the materials meet the requirements at the qualification test.

J.4.5.3 Design and Construction

The manufacturing drawings or the artwork master shall be in compliance with the scope of the general specification and detail specification. Products shall be in compliance with manufacturing drawings.

J.4.5.4 Externals, Dimensions, Marking and Others

J.4.5.4.1 Externals of Conductor, Base Material, Solder Resist and Copper Inlay

External inspection shall be performed with 4X to 10X magnifier.

a) Conductors
For conductive pattern inspection, Automatic Optical Inspection machine (AOI) can be used. Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

b) Base Materials
Pass or fail shall be determined by using an optical measuring instrument with sufficient accuracy.

c) Solder Resist
Pass or fail shall be determined by using 10X magnifier.

d) Copper Inlay Section
Pass or fail shall be determined by using 4X magnifier.

J.4.5.4.2 Dimensions

Dimensions shall be measured by using a measuring instrument with sufficient accuracy.

a) Dimensions of BGA pads, etc.

The dimensions of printed wiring boards with BGA pads, etc. shall be measured as follows. For the board with multiple BGA pads, the BGA pad with the largest area shall be selected for measurement. If all the BGA pad areas are the same size, any one of the pad shall be selected for measurement. The detailed measurement sections shall be shown in Figure J-26.

1) Dimension of pads such as BGA pads. and solder resist opening diameter
Each section of grid corner (outer) and the center area (inner) shall be measured by an optical measuring instrument.

2) Position accuracy for pads such as BGA pads.
The directions of X and Y axes of circumference for BGA pads shall be measured with a 2-dimension end-measuring machine or an equivalent measuring instrument sufficient enough for measurement.

3) Height from the base material for pads such as BGA pads. (pad thickness)

Each section of grid corner (outer) and the center area (inner) of BGA pad shall be measured by the focal depth method using a metallograph or by an optical measuring instrument.

4) Total board thickness for pads such as BGA pads.
For the total board thickness including solder coating and solder resist, the center section of BGA pad shall be measured by using a micrometer.

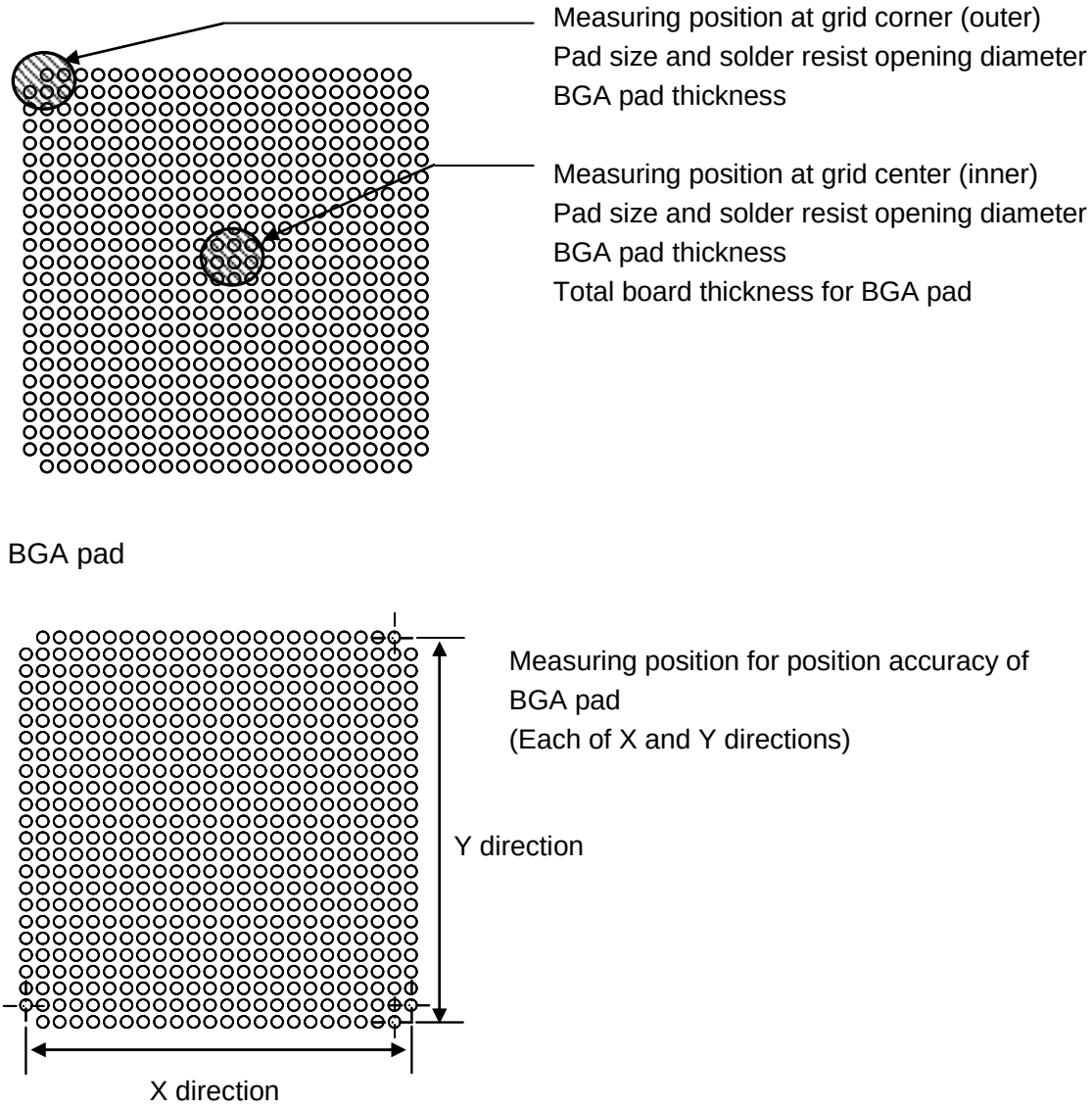


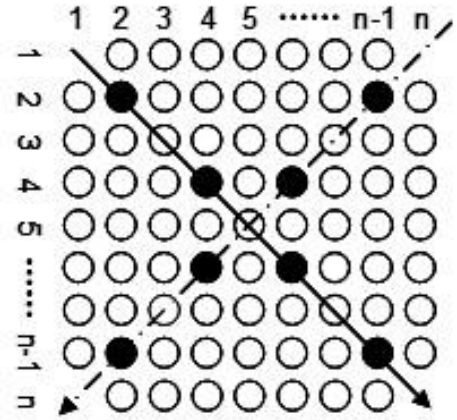
Figure J-26. Measuring Points for Pads such as BGA Pads

5) Co-Planarity

The height of the pad surface for the diagonal direction of the BGA pad shall be measured by using a 3-dimension measuring instrument. At least half of the pads in number on the diagonal line shall be measured. The pad for two diagonal directions shall be measured.

Co-planarity shall be shown as the relative height from the lowest point of the pad measured as a reference. (See Figure J-27)

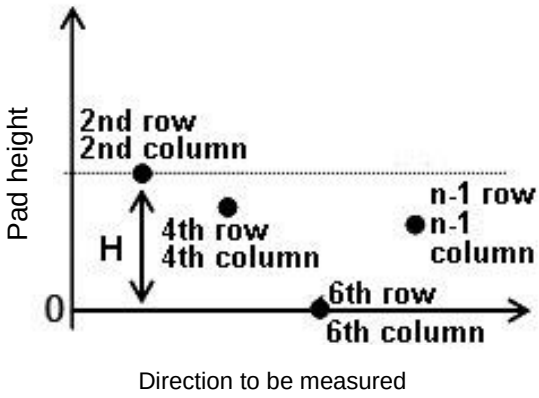
Directions of the pad to be measured



Direction 1 Direction 2

●: Pad to be measured

Co-planarity



H: Co-planarity (at max.)

Figure J-27. Measuring of Co-Planarity

6) Unevenness of copper inlay

For construction I and III, unevenness of the copper inlay shall be measured with reference to the land of through hole to be copper inlay press-fitted. The unevenness shall be measured using a 3-dimension measuring instrument with sufficient accuracy for measurement or measuring instrument with equivalent accuracy

J.4.5.4.3 Marking

Marking shall be inspected visually (naked eyed inspection).

J.4.5.5 Structural Integrity

J.4.5.5.1 Through Holes

a) Vertical microsection

The printed wiring board specimen shall be cut in the vertical plane near the center of a hole. The sample shall be encapsulated in resin and polished to expose the center of the hole.

At least three plated-through holes shall be inspected for each work board. The through holes for the vertical microsection may be prepared outside of the effective product area on the work board. For measurement of layer to layer registration and land conductor width, the hole to be measured shall be far from the starting point of drilling.

The vertical microsection shall be inspected at a magnification of 50X to 100X. If there are any questionable results, the higher magnification shall be used to

inspect the specimen. Pass/fail shall be determined at 100X magnification. Soft etching to clarify the borderline of copper plating and copper foil shall not be conducted at the observation of internal connection and resin smear.

b) Horizontal microsection

b) Multilayer boards with through holes shall be encapsulated in resin and polished. A conductive layer shall be polished in the parallel direction to expose the conductive layer.
The integrity of the through hole (internal connection in horizontal direction) shall be inspected at a magnification of 50 to 100X. If there are any questionable results, the higher magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.
Soft etching shall not be conducted on the microsection surface.

J.4.5.5.2 Voids

The microsection prepared in paragraph J.4.5.5.1 a) shall be inspected for any void at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.3 Lifting of Lands

Lands shall be inspected for any lifting by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.4 Cracks on Copper Foil

Copper foil shall be inspected for any crack by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.5 Internal Layer Connection

Internal layer connection shall be inspected by using the microsection prepared in paragraphs J.4.5.5.1 a) and b) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.6 Plating Thickness

Plating thickness shall be inspected by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 200X as a minimum. Plating thickness shall be the average value of three measurements for a plated through hole. If any of the measured value is significantly different from the other values, the value shall not be used for calculating the average.
Cap plating thickness shall be measured at the thinnest area of a hole.

J.4.5.5.7 Laminate Cracks

Laminate shall be inspected for any crack by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.8 Delamination and Blister

The microsection prepared in paragraph J.4.5.5.1 a) shall be inspected for any delamination and blister at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.9 Layer-to-layer registration

The layer-to-layer registration shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 25X to 100X. The misregistration shall be measured around the hole in the direction parallel to the board length and the vertical direction. The microsections for inspection of layer-to-layer misregistration shall be prepared by cutting the multi-layer printed wiring board in the direction parallel to the board length for at least one hole and the vertical direction for another one hole as a minimum. (See Figure J-28)

J.4.5.5.10 Land Conductor Width (Annular ring)

The land conductor width (annular ring) shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 25X to 100X. The measurement of the annular ring on an external layer shall be from the surface of the plated hole to the outer edge of the annular ring on the surface of the printed wiring board. The annular ring on an internal layer shall be measured by the distance from the drilled hole wall to the edge of the land (see Figure J-28).

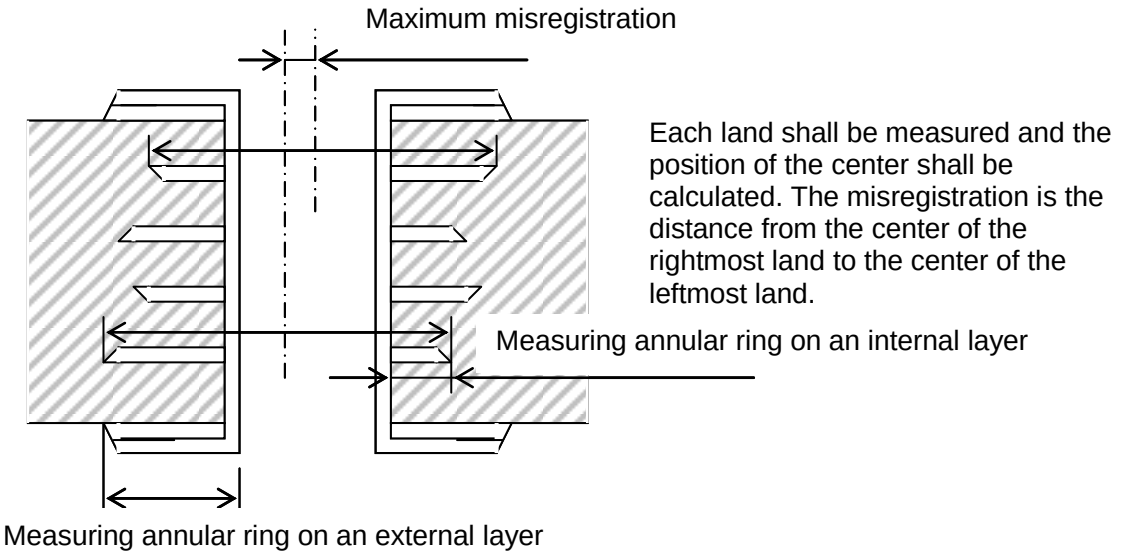


Figure J-28. Measurement of Layer-to-Layer Misregistration and Annular Ring

J.4.5.5.11 Insulation Layer Thickness

Insulation Layer Thickness shall be measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X.

J.4.5.5.12 Adhesion of Cap Plating and Filled Resin

Adhesion of cap plating and filled resin shall be observed and measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X to 100X. If there are any questionable results, the larger magnification shall be used to inspect the specimen. Pass/fail shall be determined at 100X magnification.

J.4.5.5.13 Protrusion and Pit of Cap Plating

Protrusion and pit of cap plating shall be observed and measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 50X as a minimum.

J.4.5.5.14 Filling of Resin

Filled resin shall be observed and measured by using the microsection prepared in paragraph J.4.5.5.1 a) at a magnification of 25X to 50X.

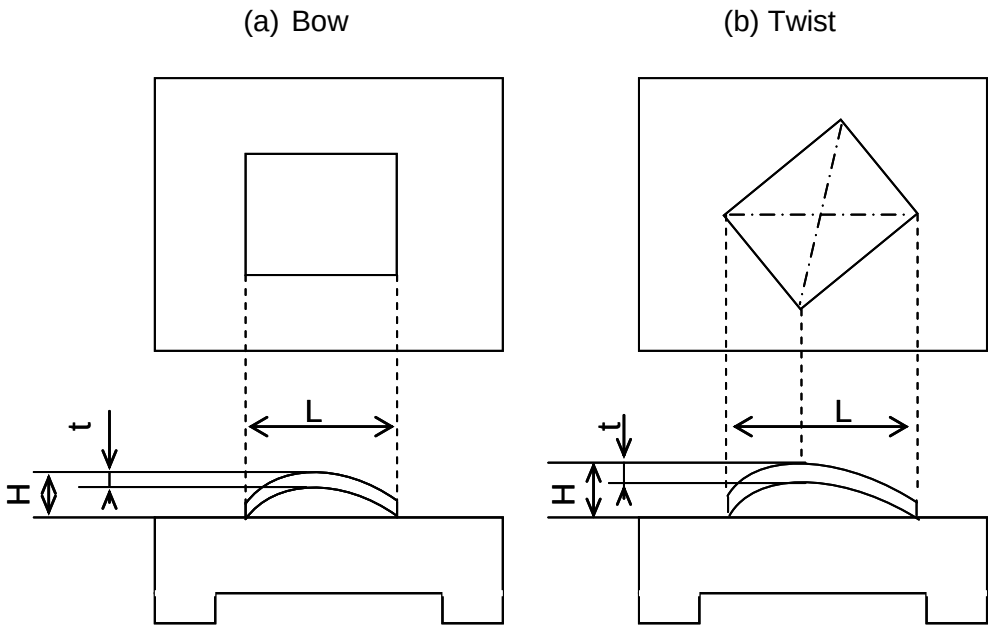
J.4.5.6 Solder Resist Thickness

Solder resist shall be cut vertically near the conductor and encapsulated in resin and polished to expose the center of the conductor. The solder resist thickness shall be measured at a magnification of 200X as a minimum.

J.4.5.7 Bow and Twist

The printed wiring board specimen shall be placed horizontally on a reference plate with its convex side facing upward, and the distance between the reference plate and the highest point of the printed wiring board shall be measured (see Figure J-29).The percent bow and twist shall be calculated by the following formula.

$$\text{Percent bow and twist} = \frac{H\text{-}t}{L} \times 100\ (\%)$$



H = Height from the reference plate (mm)
t = Thickness of the printed wiring board (mm)
L = Length of the side or diagonal line (mm)

Figure J-29. Measurement of Bow and Twist

J.4.5.8 Workmanship

The workmanship of the printed wiring boards shall be inspected at a magnification of 4X to 10X.

J.4.5.9 Plating Adhesion and Overhang

A strip of pressure sensitive tape (12.7mm wide and a minimum of 50mm long), conforming to type 1, class A of A-A-113, or JIS-Z-1522, shall be placed across the surface of a conductive pattern, and pressed firmly to the conductor, eliminating air bubbles. A tab shall be left for pulling. The tape shall be pulled with a snap pull at an angle of approximately 90 degrees to the printed wiring board. The tape shall be applied to, and removed from three different locations on each board tested. Fresh tape shall be used for each pull. If overhang metal breaks off and adheres to the tape, it is an evidence of slivers, but not a plating adhesion failure.

J.4.5.10 Cleanliness

A funnel of proper size shall be positioned over an electrolytic beaker. The printed wiring board shall be suspended within the funnel. A wash solution of 75 % by volume of isopropyl alcohol and 25 % by volume of distilled water shall be prepared. The wash solution shall have a resistivity not less than $6x10^6\Omega \cdot cm$. The wash solution shall be poured onto both sides of the printed wiring board from the top until 100ml of the wash solution is collected from each board surface of $6.5cm^2$ (including both sides of the board). The time required for the wash activity shall be a minimum of one minute. The resistivity of the collected wash solution in the beaker shall be measured with a conductivity bridge or other instrument of equivalent range and accuracy.
The alternate test methods specified in Table J-20 may be used to perform the cleanliness test.

Table J-20. Equivalent Measuring Method

Method	Resistivity ($\times 10^6\Omega \cdot cm$)	Equivalent factor	Equivalents of sodium chloride ($\mu g/cm^2$)
Conductivity bridge	2	1	1.56
Omega Meter(1)	2	1.39	2.2

Note: (1) Alpha Metals Incorporated, “Omega Meter”

J.4.5.11 Electrical Performance

The electrical performance tests shall be performed as follows.

J.4.5.11.1 Dielectric Withstanding Voltage

The dielectric withstanding voltage test shall be performed in accordance with the Test Method 301 of MIL-STD-202. The following conditions shall apply.

a) Test voltage: $500V_{AC}$ peak or $500V_{DC}$
b) Duration: 30 seconds
c) Points of application: Between conductive patterns of each layer and the electrically isolated pattern of each adjacent layer.

J.4.5.11.2 Circuitry

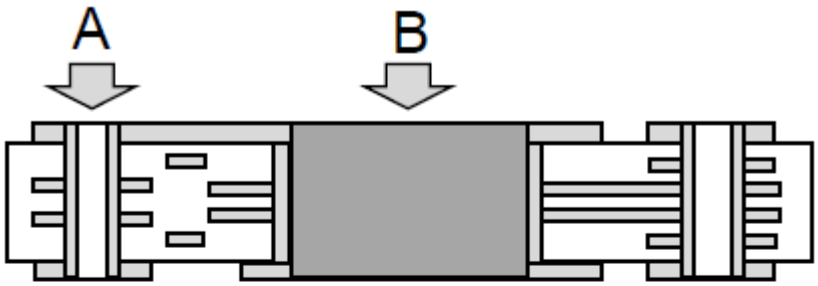
a) Continuity
A current of 2A as a maximum shall be flown through each circuit or a group of interconnected circuits to verify connectivity
b) Circuit shorts
A voltage of $250V_{DC}$ shall be applied between all common terminals of each conductive pattern and all adjacent common terminals of each conductive pattern to verify non-existence of short-circuiting.

J.4.5.11.3 Connection Resistance

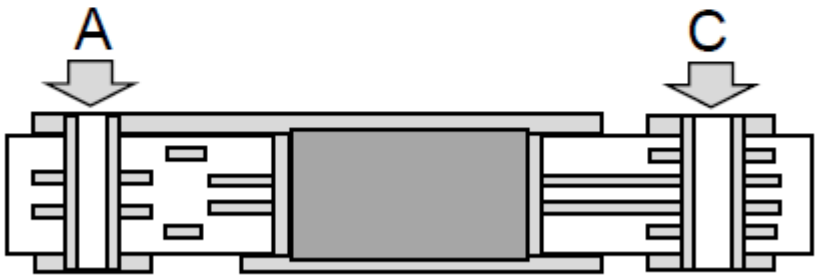
The resistance between the through hole terminals shall be measured by using a measuring instrument of four-terminal method capable of measuring a resistance below 0.5 mΩ.

J.4.5.11.3.1 Connection Resistance of Copper Inlay

The connection resistance of types I and II printed wiring boards shall be measured at following points in accordance with paragraph J.4.5.11.3. For construction without plating after press-fitting of copper inlay, the connection resistance between through hole (A) for measurement and exposed copper inlay (B) shall be measured. For construction with plating after press-fitting of copper inlay, the connection resistance between through hole (A) for measurement and through hole (C) for measurement through copper inlay shall be measured. In both cases, if measured connection resistance value is less than or equal to measurable value, only the continuity may be evaluated.



Without Plating after Press-fitting of Copper Inlay: Vertical Microsection (Example: 6 Layers)



With Plating after Press-fitting of Copper Inlay: Vertical Microsection (Example: 6 Layers)

Figure J-30. Measuring Points for Copper Inlay

J.4.5.11.4 Characteristic Impedance

The characteristic impedance shall be measured in accordance with paragraph 2.5.5.7 of IPC-TM-650.

J.4.5.12 Mechanical Performance

The mechanical performance tests shall be performed as follows.

J.4.5.12.1 Through Hole Pull Strength

A conductor shall be cut with a sharp knife at a minimum of 6mm from the land, peeled and pulled toward the land, and shall be cut off by applying the sharp knife at the joining point of the conductor and land without degrading the land adherence strength.
Then, a lead wire sufficient in length for installing a tensile tester shall be inserted in the hole and soldered. After that, a cycle of solder removal and resoldering by using a soldering iron shall be performed.

a) A lead wire shall be soldered in to the through hole.
b) The lead wire shall be removed from the through hole (solder removal).
c) A lead wire shall be resoldered in to the through hole.
d) The lead wire shall be removed from the through hole (solder removal).
e) A lead wire shall be resoldered in to the through hole.

The edge of the lead shall not be clinched. The lead wire shall be taken off completely during the solder removal and replaced with a new one when resoldering. The soldering iron shall be used at 15 to 60W and adjusted to develop the tip temperature of 232 to 260°C. The lead wire shall be heated by the solder iron without bringing its tip into contact with the conductor of the printed wiring board. The heating time shall be limited to the required minimum.
Upon completion of e) resoldering, the lead wire shall be installed on a tensile tester at room temperature, and be pulled at the rate of 50mm per minute forward and vertically with the land until the pull strength reaches the requirement (L) or any failure occurs. Breaking off or pulling out the lead wire shall not be regarded as a failure, and a new lead wire shall be soldered and pulled. The pull strength shall be calculated by the following formula.

$$L \geq 1380 \times \frac{\pi \left\{ (d_2)^2 - (d_1)^2 \right\}}{4}$$

L = Pull strength (N)
d_1 = Hole diameter (cm)
d_2 = Land diameter (cm)

J.4.5.12.2 Peel Strength of Surface Conductor

The peel strength of surface conductor is performed in accordance with Paragraph 2.4.8 of IPC-TM-650 and as follows.

a) Normal state
   Test condition A shall be applied.
b) After Thermal stress
   Test condition B shall be applied.

J.4.5.12.3 Solderability

a) Through hole solderability
   The wetting of solder shall be inspected using a microsection sample subjected to the inspection specified in paragraph J.4.5.5.1.
b) Surface conductor solderability and sideplating
   After the specimen is dipped into the flux specified in Test Method 208 of MIL-STD-202, the flux shall be drained for 60 seconds. Solder compliant with the Test Method 208 of MIL-STD-202 shall be melted in a bath and stirred with a clean stainless steel paddle. It shall be confirmed that the temperature is in the range between 226 and 238°C. The solder slug and burnt flux shall be removed from the molten solder surface immediately before the specimen immersion. The specimen shall be put vertically into the solder bath at a rate of 25±6mm per second, kept in the bath for 4±0.5 seconds and raised at a rate of 25±6mm per second. After the pull-up, the specimen shall be kept in the vertical state in the air, until the solder is solidified. No quick cooling shall be permitted. The condition of solder on the conductive surface shall be inspected after the solder is solidified.

J.4.5.12.4 Extrusion Strength of Copper Inlay

The test methods for extrusion strength of copper inlay shall be specified in the detail specification.

J.4.5.13 Environmental Performance

The environmental performance tests shall be performed as follows.

J.4.5.13.1 Thermal Shock

The thermal shock test shall be performed in accordance with Test Method 107 of MIL-STD-202. The following conditions shall apply.

a) Thermal shock (I) (applicable to qualification test)
   The test shall be performed under the test condition B. However, the lowest temperature shall be -30°C and the number of cycle shall be 1200 cycles. The time for steps 2 and 4 shall be within 2 minutes each.
   Reflow soldering of total heating process in accordance with JERG-0-043 shall be performed three times as a pre-treatment of the printed wiring board. The resistance shall be measured and recorded before and after the reflow in order

to confirm there is no effect by the reflow. The heating condition shall be as follows.

1) Heating condition: 200°C min. for 45 seconds min.
2) Peak temperature: 230°C min.

b) Thermal shock (II) (applicable to quality conformance inspection)
The test shall be performed under the test condition B-3 (-65°C to +125°C). The time for step 2 and 4 shall be within 2 minutes each.

J.4.5.13.2 Humidity and Insulation Resistance

a) Humidity resistance
The first 6 steps in Test Method 106 of MIL-STD-202 shall be performed for 10 cycles, and the polarization voltage of 100V±10V_{DC} shall be applied to all layers during the test. Upon completion of step 6 of the final cycle, the specimen shall be taken out of the bath and dried immediately by blowing air at 25±5°C and evaluated.

b) Insulation resistance
The test shall be performed in accordance with the test condition B, Test Method 302 of MIL-STD-202. The voltage shall be applied for 1 minute.

J.4.5.13.3 Hot Oil Resistance

The specimen shall be dried at 120±5°C for 2 hours and then cooled to room temperature. After that, the specimen shall be immersed in oil or wax at 260±5°C for 5 seconds and cooled to room temperature. This Immersion and cooling shall be performed for 10 cycles.

J.4.5.13.4 Thermal Stress

The specimen shall be dried for 2 hours at 121 to 149°C. Then, the specimen shall be placed on a ceramic plate in a desiccator, and cooled down. The specimen shall then be fluxed in accordance with the detail specification and floated in a solder bath of composition Sn 63±5 % maintained at 288±5°C for a period of 10 seconds. The specimen shall be placed on a piece of insulator to be cooled. After a check for any defects on the external surface, the sample shall be inspected for the structural integrity using the microsection prepared in accordance with paragraph J.4.5.5.1. Solder temperature shall be measured at a probe depth not to exceed 50mm from the molten surface of the solder. Evaluation specimen of Adhesion of cap plating and filled resin (paragraph J.3.4.4.13) shall be floated in a solder bath for a period of 10 seconds and cooled down. This floating and cooling shall be performed three times.

J.4.5.13.5 Radiation Hardness

The gamma ray irradiation shall be performed by using cobalt 60 at a rate of 0.5×10^4Gy to 1×10^4Gy per hour to the specimen in open air, until the total dose amounts to 1×10^4Gy. After the irradiation, the specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of dielectric withstanding voltage and insulation resistance shall be

performed in accordance with paragraphs J.4.5.11.1 and J.4.5.13.2 b), respectively. The insulation resistance shall be measured using the same circuit for the dielectric withstanding voltage test.

J.4.5.13.6 Vibration

Vibration test shall be performed in accordance with Method 214 of MIL-STD-202. Following conditions shall be applied to the vibration tests.

a) Mounting method
Printed wiring board shall be secured to the jig (mounting section: (ϕ 6mm), lifting height: (10mm to 20mm) / rigid studs are acceptable) on the appropriate test axis with specified torque.

b) Measurement before test
Interrupted or shorted circuits shall be checked in accordance with paragraph J.4.5.11.2 and the connection resistance shall be measured in accordance with paragraph J.4.5.11.3. Unevenness of copper inlay shall be measured in accordance with paragraph J.4.5.4.2 b).

c) Test condition: II-H
Frequency range: 50Hz to 2,000Hz
Total RMS acceleration: 34.02 Grms

d) Vibration direction: Three-direction

e) Number of tests and duration
Each vibration test duration shall be 15 minutes once per direction; total of 45 minutes for 3 directions.

f) Measurement after test
Interrupted or shorted circuits shall be checked in accordance with paragraph J.4.5.11.2 and the connection resistance shall be measured in accordance with paragraph J.4.5.11.3. Unevenness of copper inlay shall be measured in accordance with paragraph J.4.5.4.2 b).

g) Visual inspection after test
Printed wiring board shall be inspected at a magnification of 4X to 10X.

h) Design of test board for evaluation
Design of test board for evaluation shall be as follows.
- External dimensions: 100mm, mounting pitch: 90mm, mounting hole diameter: ϕ 3.5mmx4P, board thickness: 1.6mm
- Copper inlay shall be located at the center of the board (Size of copper inlay shall be the maximum size in the qualification range)

J.4.5.13.7 Shock

Shock test shall be performed in accordance with Method 213 of MIL-STD-202. Following conditions shall be applied to the vibration tests.

a) Mounting method
Printed wiring board shall be secured to the jig (mounting section: (ϕ 6mm), lifting height: (10mm to 2mm) / rigid studs are acceptable) on the appropriate test axis with specified torque.

b) Measurement before test
Interrupted or shorted circuits shall be checked in accordance with paragraph J.4.5.11.2 and the connection resistance shall be measured in accordance with

paragraph J.4.5.11.3. Unevenness of copper inlay shall be measured in accordance with paragraph J.4.5.4.2 b).

c) Test condition: F (1500G, 0.5m/s, half-sine wave)

d) Shock test direction: Three-direction

e) Number of tests
Number of shock test shall be 3 times per direction; total of 9 times for 3 directions.

f) Measurement after test
Interrupted or shorted circuits shall be checked in accordance with paragraph J.4.5.11.2 and the connection resistance shall be measured in accordance with paragraph J.4.5.11.3. Unevenness of copper inlay shall be measured in accordance with paragraph J.4.5.4.2 b).

g) Visual inspection after test
Printed wiring board shall be inspected at a magnification of 4X to 10X.

h) Design of test board for evaluation
Design of test board for evaluation shall be as follows.
- External dimensions: 100mm, mounting pitch: 90mm, mounting hole diameter: ϕ 3.5mmx4P, board thickness: 1.6mm
- Copper inlay shall be located at the center of the board (Size of copper inlay shall be the maximum size in the qualification range)

J.4.5.14 Optional Tests

J.4.5.14.1 IST (Interconnect Stress Test)

IST is performed to evaluate connection reliability (acceleration correlation evaluation) of pattern wirings and through holes. Test methods shall be specified in the detail specification.
When the IST cannot be performed, the reason shall be specified in the detail specification.

J.4.5.14.2 Pad Strength Test

For the pads requiring strength verification, pad strength test is performed by ball shear test and ball pull test. Test methods shall be specified in the detail specification.
When the pad strength test cannot be performed, the reason shall be specified in the detail specification.