COMMON PARTS/MATERIALS, SPACE USE,

APPLICATION DATA SHEET FOR

Part Description	FINE PITCH PRINTED WIRING BOARDS, GLASS BASE WOVEN EPOXY RESIN BASE MATERIAL, HIGH RELIABILITY, SPACE USE
Part Number and Type	JAXA2140/B701GF　III10
Applicable Specification	JAXA-QTS-2140 JAXA-QTS-2140/B701

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Prepared and Established by MEIKO ELECTRONICS Co., LTD.

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

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Record of Revisions

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MUS-4595

Revision History

Rev.	Date	Description
0	23 Jan. 2026	Original.
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Contents

MUS-4595

COMMON PARTS/MATERIALS, SPACE USE, APPLICATION DATA SHEET FOR

1. GENERAL

1.1 Scope

This Application Data Sheet provides detailed information necessary for part users for selection, design, and usage etc. of JAXA qualified parts to be installed in the applications.
Users are responsible for their decisions on part selection and usage.

1.2 Applicable Documents

Unless otherwise specified, the documents listed below form a part of this data sheet to the extent specified herein.

JAXA-QTS-2140	Printed Wiring Boards, High Reliability, Space Use, General Specification for
JAXA-QTS-2140/B701	Fine Pitch Printed Wiring Boards, Glass Base Woven Epoxy Resin Base Material, High Reliability, Space Use, Detail Specification for

1.3 Reference Documents

Not applicable.

2. SUMMARY OF PRODUCTS

2.1 Externals and Dimensions

Externals and dimensions of the printed wiring board are specified in the drawing designed by the users. There are no such things as standard externals or dimensions of the printed wiring board.

2.2 Mass

Mass is dependent on the dimension and thickness of the printed wiring board. There are no such things as standard mass of the printed wiring board.

2.3 Element Construction including Small-Diameter Via Holes

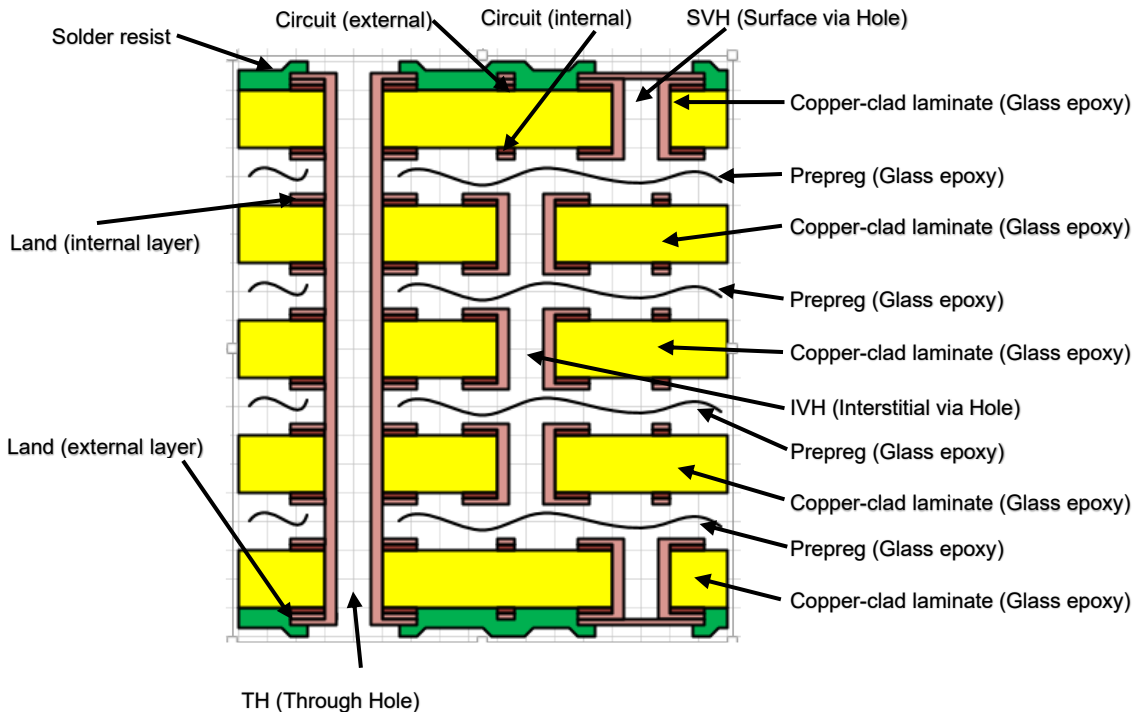


Figure 1. IVH Printed Wiring Board Cross-Section (Example: 10 Layers)

Materials shall be a halogen-free, FR-4.1, R-1566 (copper-clad laminate) and R-1551 (prepreg) supplied by Panasonic Corporation.
Glass base woven epoxy resin Tg (DSC method): 148 °C

2.4 Qualification Coverage

Qualification coverage is shown in Table 1. Qualification Coverage.

Table 1. Qualification Coverage

Specification		Standard 10 layers
Base material		GF epoxy (R1566)
Applicable standard for the base material		IPC-4101
Maximum number of layers	Through-holes	10 layers
	SVH/IVH	2 layers / 2 layers
Maximum number of lamination cycles		1 cycle
Maximum board thickness		1.8 mm
Minimum drill diameter	Through-holes	ø 0.35 mm
	SVH/IVH	ø 0.2 mm
Minimum plating thickness	Through-holes	30 μm
	SVH/IVH	15 μm
Conductor width		0.13 mm as a minimum
Conductor spacing		0.18 mm as a minimum
Conductor keep-out area from board edge		0.3 mm as a minimum
Solder resist ink		Equivalent to IPC-SM-840, class H
Surface treatment		Solder leveler

3. USAGE

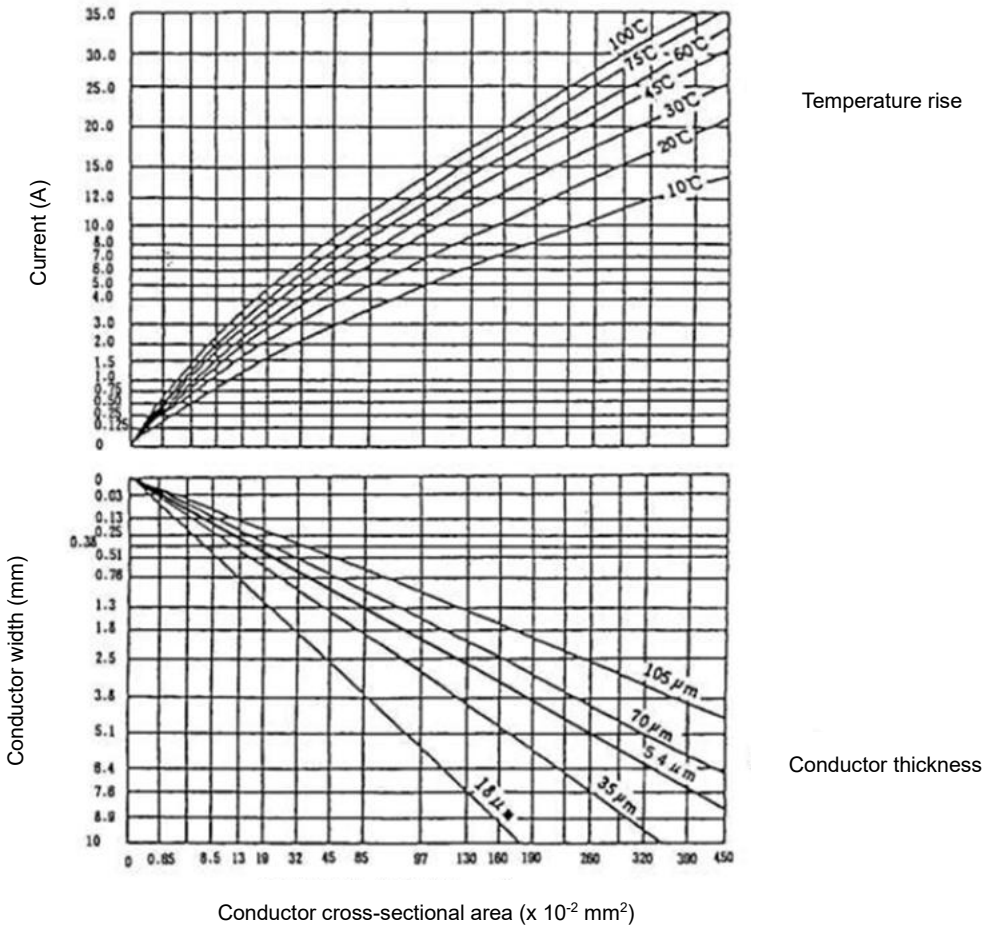
3.1 Operating Temperature Range

Operating temperature range: -65 °C to +125 °C.

3.2 Caution in Circuit Design

3.2.1 Conductor Width

The design value for the conductor width shall be greater than or equal to 0.13 mm. The conductor width of the external layer and internal layer shall be designed in accordance with Figures 2 and 3.



Remarks:

(1) This chart has been prepared as an aid in estimating relationships among the conductor cross-sectional area, conductor current, and temperature rise above ambient. It is assumed that the conductor surface area is relatively small compared to the surface area of the adjacent insulating layer. The allowable current in this chart includes a 10% margin considering tolerances in etching accuracy, conductor thickness, conductor width, and conductor cross section.

(2) Additional 15 % margin for the allowable current is preferable under the following conditions.
a) When the insulation layer thickness is less than 0.8 mm.
b) When the conductor thickness is greater than or equal to 105 μm.

(3) In general, the allowable temperature rise is defined as the difference between the maximum operating temperature of the printed wiring board and the maximum ambient temperature in the location where the printed wiring board will be used.

(4) For single conductor applications, this chart may be used for determining conductor widths, conductor cross-sectional area and allowable current (current-carrying capacity) for temperature rise.

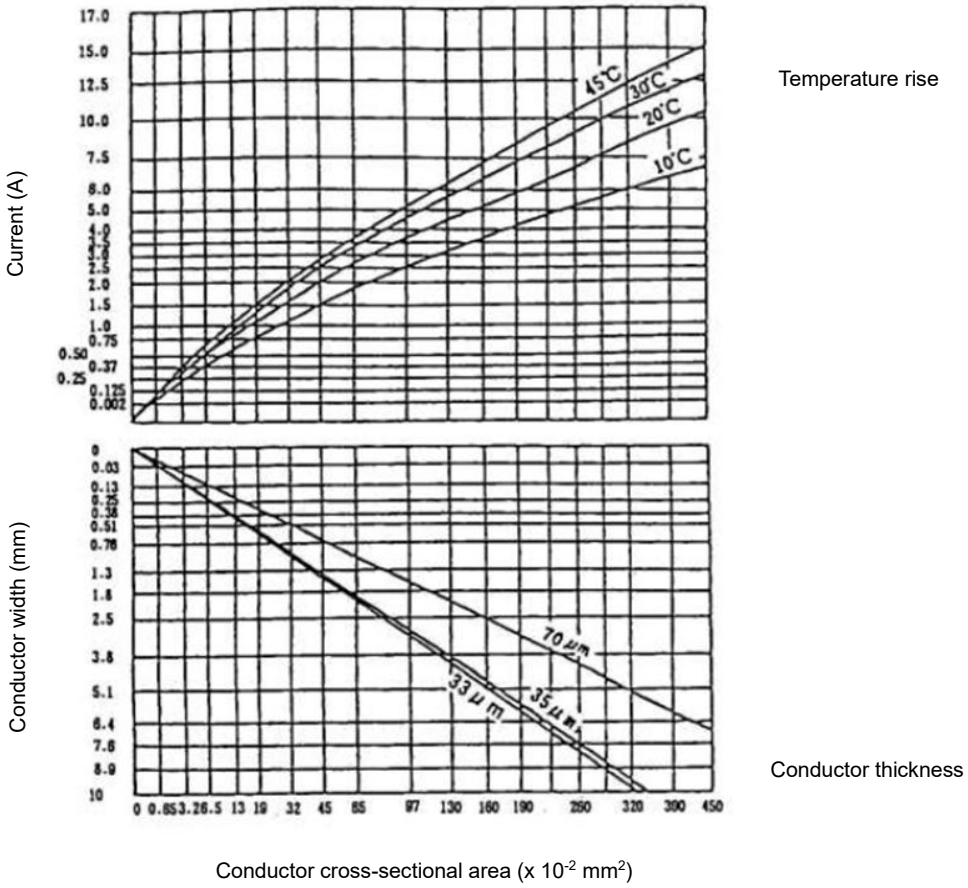
(5) For groups of similar parallel conductors that are closely spaced, the temperature rise shall be determined from the equivalent cross-sectional area and equivalent current.

(6) Heating effects due to heat-generating parts are not considered in this chart.

(7) The conductor thickness does not include plating thickness of metals other than copper.

(8) The 54 μm line shall apply to an external layer with SVH.

Figure 2. Conductor Width (External Layer)



Remarks:
(1) The remarks for Figure 2, except for (8), shall apply to Figure 3.
(2) For the internal layer comprising SVH and the internal layer comprising IVH, a line of 33 μm shall be applied.
(*) If 12 μm copper foil is to be applied to the internal layer of SVH, consult with the manufacturer in advance.

Figure 3. Conductor Width (Internal Layer)

3.2.2 Copper Foil

Table 2. Copper Foil Thickness

	with SVH	with IVH	without SVH or IVH
External layer	9 μm as a minimum	-	18 μm as a minimum
Internal layer	12 μm as a minimum	18 μm as a minimum	35 μm as a minimum

3.2.3 Conductor Spacing

Table 3. Conductor Spacing

Voltage between conductors (DC or AC (peak)) (V)	Minimum conductor spacing (mm)	
	External layer	Internal layer
0 to 100	0.18	0.18
101 to 300	0.48	0.30
310 to 500	0.86	0.35
greater than or equal to 501	(0.003 x V)+0.1	(0.003 x V)+0.1

3.2.4 Interlayer Connection

All interlayer connections shall be implemented using through-holes, including small-diameter vias (minimum drill diameter: ø 0.35 mm), IVHs (minimum drill diameter: ø 0.2 mm), and SVHs (minimum drill diameter: ø 0.2 mm).

3.2.5 Land Diameter

Table 4. Land Diameter

Hole Classification	Minimum Land Diameter (mm)
IVH and SVH, and small via holes	ø (Drill diameter + 0.4 mm) *Minimum land diameter of small via hole is ø 0.76 mm.
Plated-through holes other than above	ø (Finished through hole diameter + 0.5 mm)
Non-plated-through holes	ø (Drill diameter + 1.1 mm)

To ensure the safety of conductor connections, teardrops shall be provided on both internal and external layers. The shape is for reference only, as it may vary depending on the routing configuration.

Table 5. Tear Drop

Tear Drop: T mm	T mm ≥ L mm

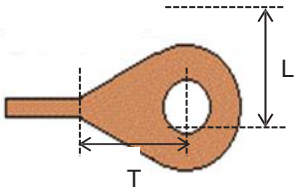


Figure 4. Tear Drop

3.2.6 Thermal Land

Table 6. Thermal Land

A	B	C
A ≥ Dr + 0.40 mm	B ≥ 0.15 mm	C ≥ 0.10 mm

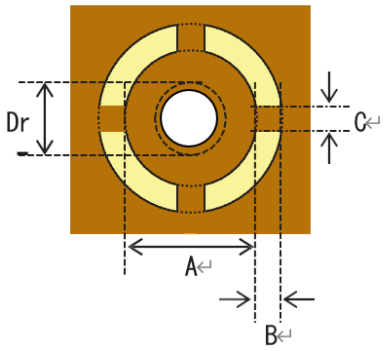


Figure 5. Thermal Land

3.2.7 Plating Thickness

Table 7. Plating Thickness

Plating type	Plating thickness at the surface and through hole	
Electroless copper plating	Necessary and sufficient thickness for electrolytic copper plating in the next process.	
Electrolytic copper plating	Parts hole	25 μm as a minimum.
	Small via hole	30 μm as a minimum.
	IVH and SVH	15 μm as a minimum.
Electrolytic gold plating	Not used.	
Electrolytic nickel plating	Not used.	
Solder coating	Thickness shall not be specified. However, the coating shall meet the requirements for solderability.	

3.2.8 Dimensional Tolerance

Table 8. Dimensional Tolerance

Unit: mm

Item	Tolerance
External dimensions	±0.3 for the dimension of 100 or smaller, and additional 0.05 for every 50 more than 100.
Finished hole diameter	The tolerance of all hole diameters shall be +0.10, -0.15. However, the tolerance of finished diameters of IVH, SVH and small via holes shall not be specified.
Conductor width	0.13 or more and less than 0.20: ± 0.05 0.20 or more and less than 0.50: ± 0.10 0.50 or more: ± 20 % of conductor width
Conductor spacing	The conductor spacing tolerance in the case of 3 patterns between pins shall be set as -0.08, and the positive side shall not be specified. In addition, if there are two or less patterns between pins, the conductor spacing tolerance shall be set as -0.10, and the positive side shall not be specified. The minimum conductor spacing tolerance in the external layer shall be 0.13.
Board thickness	The board thickness tolerance shall be between solder resists.
Bow and twist	0.8% as a maximum

Nominal Board Thickness (T)	Tolerance
T ≤ 0.6	± 0.10
0.6 < T ≤ 1.0	± 0.15
1.0 < T ≤ 1.2	± 0.17
1.2 < T ≤ 1.6	± 0.19

3.2.9 Design Value of Solder Resist

The solder resist opening size shall be defined as follows.

- Opening size of parts hole: land diameter + 0.2 mm
- Small via hole: drill diameter + 0.1 mm
- SVH: land surface shall be coated with solder resist.
- For surface-mount pads, the solder resist opening shall provide a standard clearance of 0.1 mm around the pad, with a minimum clearance of 0.075 mm.

Note: If the minimum value other than specified above is to be used, consult with the manufacturer in advance.
When increasing the solder resist clearance from the conductor pattern, care shall be taken to ensure sufficient solder resist width between adjacent pads to prevent solder bridge.

3.2.10 Marking of Part Number

In principle, part number shall be marked on printed wiring board as specified in the applicable specification.

Part number example: JAXA 2140/B701 GF III 10

JAXA 2140/B	: Applicable specification
701	: Individual identification for Meiko Electronics
GF	: Glass base woven epoxy resin
III	: Multilayer
10	: Number of layers

3.2.11 SVH

SVH shall not be used as a part mounting pad.

3.2.12 Location Layout of Mount Pads

It is recommended to place solder resist between the mounting pads.

For spacing of less than 0.25 mm between adjacent mounting pads, solder resist shall be provided between the pads, or the part layout shall be arranged to avoid mixing pad orientations in vertical, horizontal, and diagonal directions.

3.2.13 Connectors

Direct printed wiring board connectors shall not be used.

3.3 Recommended Mounting Method

3.3.1 Soldering

For flow soldering, a soldering temperature of 240 °C (+0 °C, -5 °C) and a soldering time of 3 ± 0.5 seconds are preferable.

For reflow soldering, it is preferable to follow the heat resistance of the parts and the recommended conditions for the solder paste use.

For manual soldering, it is preferable to follow the temperature ratings of the parts and the recommended conditions for the solder wire used.

Storage during the assembly process shall be avoided as much as possible, and the processing shall proceed to the next step without delay.

3.3.2 Baking

Baking is not required under normal use conditions.

4. CHARACTERISTICS UNDER NORMAL OPERATING CONDITIONS

4.1 Electric Characteristics

The conductor resistance (R_i) of conductive pattern shall be determined using the following equation.

$$\mathbf{R_i} = \mathbf{2\rho\frac{\ell}{W \times t}}\ (\mathbf{m\Omega})$$

where:

ρ: Volume resistivity at 20 °C of the primary metal forming the conductor (mΩ • mm)

$\rho = 1.72 \times 10^{-2}$ (mΩ • mm) (Volume resistivity at 20 °C of copper)
ℓ: Distance between lands (mm)
W: Conductor width (mm)
t: Conductor thickness (mm)

4.2 Mechanical Characteristics

Terminal pull strength shall be as follows.
The terminal pull strength shall be greater than or equal to 89.2 N or 1380 N/cm^2, whichever is smaller. The pull strength shall be determined using the following equation.

$$L \geq 1380 \times \frac{\pi\{(d2)^2 - (d1)^2\}}{4}$$

where:
L: Terminal pull strength (N)
d1: Hole diameter (cm)
d2: Land diameter (cm)

4.3 Thermal Characteristics

The temperature dependence (R_x) $(m\Omega)$ of the conductor resistance of the conductor pattern shall be determined using the following equation.

$$R_x = R_c\{1 + 0.00377\,(T_x - 20)\}$$

where:
R_c : Conductor resistance of conductor at 20 °C $(m\Omega)$
T_x : Temperature (°C)

4.4 Dielectric Withstanding Voltage

A dielectric withstanding voltage of 1000 V AC (peak) or 1000 V DC shall be applied for 30 seconds. No insulation breakdown, such as flashover or sparkover, shall occur.

4.5 Solderability

a) Hole solderability
The through-hole wall and land surface shall exhibit proper solder wettability.
b) Surface solderability
A minimum of 95 percent of the conductor surface area shall be covered uniformly with solder. Pinholes, dewetting and small rough areas shall not be concentrated in a single location.

5. CHARACTERISTICS UNDER VARIOUS OPERATING CONDITIONS

No data.

6. ENVIRONMENTAL LIMITS

6.1 Test Items of Environmental Limits

a) Thermal shock
b) Humidity and insulation resistance
c) Hot oil resistance
d) Thermal stress
e) Radiation hardness
f) Outgassing

6.2 Design Specification for Samples

Table 9. Design Specification for Samples

No.	Item	Specification
1	Material	As specified in appendix B of JAXA-QTS-2140. Glass base woven epoxy resin
2	Board thickness	1.6 mm and 1.8 mm
3	Number of layers	6 layers and 10 layers
4	Through hole	IVH and SVH: Drill diameter: ø 0.2 mm, plating thickness: 15 μm Small via hole: Drill diameter: ø 0.35 mm, plating thickness: 30 μm Part hole: Drill diameter: ø 0.8 mm, plating thickness: 30 μm
5	Conductor	Width: 0.13 mm, Spacing: 0.18 mm
6	Pattern	As specified in appendix B of JAXA-QTS-2140.

Note: Samples manufactured in Kanagawa factory were prepared with design specification: 10-layer, 1.8 mm board thickness. Samples manufactured in Kahoku factory were prepared with two types of design specifications: 6-layer, 1.6 mm board thickness and a 10-layer, 1.8 mm board thickness.

6.3 Thermal Shock

6.3.1 Test Method

1) Thermal shock test shall be performed in accordance with method 107 of MIL-STD-202.
2) The connection resistance between the circuits of the sample shall be measured before the test.
3) The samples shall be tested under the conditions shown in Table 10. Temperature.

Table 10. Temperature of Thermal Shock

Step	Temperature (°C)	Duration (minutes)
1	-30	30
2	25	2 as a maximum
3	125	30
4	25	2 as a maximum

4) Steps 1 to 4 shall be defined as one cycle, and 1000 cycles shall be performed.
5) After completion of 1000 cycles, the samples shall be visually inspected, and the inter-circuit connection resistance shall be measured to determine the rate of change in resistance.

6.3.2 Acceptance Criteria

1) After completion of the test, no open circuit, blistering, measling, crazing, or delamination shall be observed.
2) After completion of the test, no open circuit or short circuit between circuits shall be observed.
3) The rate of change in inter-circuit connection resistance before and after the test shall be less than 10 %.

6.3.3 Test Results

1) Visual inspection
   After completion of the test, visual inspection confirmed that no defects such as open circuits, blistering, measling, crazing, or delamination were observed in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).
2) Open circuit and short circuit
   After completion of the test, no defects such as open circuit and short circuit were observed in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).
   Open and short circuit results are as shown in Tables 11 to 13 and meet the requirements.

Table 11. Open and Short Circuit Results for Kanagawa Factory Samples (10-Layer, 1.8 mm) after Thermal Shock Test

Number of Layer	Open and Short Circuit Results
L1	No
L2	No
L3	No
L4	No
L5	No
L6	No
L7	No
L8	No
L9	No
L10	No

Table 12. Open and Short Circuit Results for Kahoku Factory Samples (6-Layer, 1.6 mm) after Thermal Shock Test

Number of Layer	Open and Short Circuit Results
L1	No
L2	No
L3	No
L4	No
L5	No
L6	No

Table 13. Open and Short Circuit Results for Kahoku Factory Samples (10-Layer, 1.8 mm) after Thermal Shock Test

Number of Layer	Open and Short Circuit Results
L1	No
L2	No
L3	No
L4	No
L5	No
L6	No
L7	No
L8	No
L9	No
L10	No

3) The rate of change in connection resistance
The rate of change in connection resistance for Kanagawa factory samples (10-Layer, 1.8 mm) is -1.04 % and meets the requirements.
The rate of change in connection resistance for Kahoku factory samples (6-Layer, 1.6 mm) is 0.40 % and meets the requirements.
The rate of change in connection resistance for Kahoku factory samples (10-Layer, 1.8 mm) is 0.80 % and meets the requirements.

6.4 Humidity and Insulation Resistance

6.4.1 Test Method

1) Humidity and insulation resistance testing shall be performed in accordance with method 106 of MIL-STD-202, for 10 cycles using the first six stages.
2) During testing, a voltage of 100 V ± 10 V DC shall be applied to all layers.
3) After completion of 10 cycles, the samples shall be removed from the test chamber and dried in air at 25 °C ± 5 °C.
4) Insulation resistance shall be measured in accordance with method 301 of MIL-STD-202.

6.4.2 Acceptance Criteria

1) After completion of the test, no blistering, measling, or delamination shall be observed.
2) After completion of the test, insulation resistance between conductors shall be not less than 500 MΩ.

6.4.3 Test Results

1) Visual inspection

After completion of the test, visual inspection confirmed that no defects such as open circuits, blistering, measling, crazing, or delamination were observed in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).

2) Insulation resistance

After completion of the test, insulation resistance was measured in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm). Test results are as shown in Tables 14 to 19 and meet the requirements.

Table 14. Insulation Resistance between Patterns for Kanagawa Factory Samples (10-Layer, 1.8 mm) after Humidity Resistance Test

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13
L7	1.00E+13
L8	1.00E+13
L9	1.00E+13
L10	1.00E+13

Table 15. Dielectric Withstanding Voltage for Kanagawa Factory Samples (10-Layer, 1.8 mm) after Humidity Resistance Test

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects
L6 – L7	No defects
L7 – L8	No defects
L8 – L9	No defects
L9 – L10	No defects

Table 16. Insulation Resistance between Patterns for Kahoku Factory Samples (6-Layer, 1.6 mm) after Humidity Resistance Test

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13

Table 17. Dielectric Withstanding Voltage for Kahoku Factory Samples (6-Layer, 1.6 mm) after Humidity Resistance Test

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects

Table 18. Insulation Resistance between Patterns for Kahoku Factory Samples (10-Layer, 1.8 mm) after Humidity Resistance Test

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13
L7	1.00E+13
L8	1.00E+13
L9	1.00E+13
L10	1.00E+13

Table 19. Dielectric Withstanding Voltage for Kahoku Factory Samples (10-Layer, 1.8 mm) after Humidity Resistance Testing

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects
L6 – L7	No defects
L7 – L8	No defects
L8 – L9	No defects
L9 – L10	No defects

6.5 Hot Oil Resistance

6.5.1 Test Method

1) The samples shall be dried at 120 ± 5 °C for 2 hours and cooled to room temperature.
2) The samples shall be immersed in oil at 260 ± 5 °C for 5 seconds and then cooled to room temperature. This sequence shall constitute one cycle, and 10 cycles shall be performed.
3) After completion of 10 cycles, the connection resistance shall be measured.

6.5.2 Acceptance Criteria

1) The rate of change in inter-circuit connection resistance before and after the test shall be less than 10 %.

6.5.3 Test Results

1) The rate of change in resistance for Kanagawa factory samples (10-layer, 1.8 mm) before and after 10-cycle test is a maximum of 0.08 % and meets the requirements.
2) The rate of change in resistance for Kahoku factory samples (6-layer, 1.6 mm) before and after 10-cycle test is a maximum of 1.32 % and meets the requirements.
3) The rate of change in resistance for Kahoku factory samples (10-layer, 1.8 mm) before and after 10-cycle test is a maximum of 1.32 % and meets the requirements.

6.6 Thermal Stress

6.6.1 Test Method

1) The samples shall be held at 121 °C to 149 °C for 2 hours to remove moisture.
2) The samples shall be placed on a ceramic plate in a desiccator and cooled to room temperature.
3) Flux shall be applied, and the samples shall be floated on the surface of a solder bath [Sn: 63 % ± 0.5 %, Sb: 0.20 %, Bi: 0.10 %, Cd: 0.002 %, Cu: 0.08 %, Au: 0.05 %, In: 0.10 %, Ag: 0.10 %, Al: 0.001 %, As: 0.03 %, Fe: 0.02 %, Ni: 0.01%, Zn: 0.001 %, Pb: balance, temperature: 288 °C ± 5 °C] for 10 seconds.
4) The samples shall be placed on an insulating plate and cooled to room temperature.
5) The samples shall be visually inspected for any defects.
6) The samples shall be cut perpendicular to the board surface near the center of the hole, embedded in resin, and polished so that the center of the hole is exposed on the cross-sectional surface.
7) Cross-sectional observation shall be performed.

6.6.2 Acceptance Criteria

1) After completion of the test, no measling, cracks, separation between plating and conductors, blistering, or delamination shall be observed.

2) No cracks shall be observed in the internal layer copper foil in cross-sectional observation.
3) In cross-sectional observation, when laminate voids within the same layer or between layers meet the minimum conductor spacing specified in the manufacturing drawings, the maximum length shall be no greater than 76 μm.

6.6.3 Test Results

1) Visual inspection
After completion of the test, visual inspection confirmed that no defects such as measling, cracks, separation between plating and conductors, crazing, or delamination were observed in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).
2) Cross-sectional observation
After completion of the test, no cracks and laminate voids were observed in internal layer copper foil in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).

6.7 Radiation Hardness

6.7.1 Test Methods

1) The samples shall be irradiated with gamma rays (Cobalt-60) in air at a rate of 0.5×10^4 Gy to 1×10^4 Gy per one hour until the total radiation dose reaches 1×10^4 Gy.
2) The samples shall be visually inspected for any deterioration.
3) Dielectric withstanding voltage and insulation resistance shall be measured.

6.7.2 Acceptance Criteria

1) After completion of the test, no measling, delamination, or weave texture defects shall be observed.
2) After completion of the test, insulation resistance between conductors shall be at least 500 MΩ.
3) After completion of the test, a voltage of 1000 V AC (peak) or 1000 V DC shall be applied for 30 seconds in accordance with method 301 of MIL-STD-202. No insulation breakdown, such as flashover or sparkover, shall occur.

6.7.3 Test Results

1) Visual inspection
After completion of the test, visual inspection confirmed that no defects such as measling, delamination, or weave texture were observed in all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm).
2) Dielectric withstanding voltage
After completion of the dielectric withstanding voltage testing, insulation resistance between patterns and layers for all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm) are as shown in Tables 20 to 25. The test results meet the

requirements, and no insulation breakdown, such as flashover or sparkover, was observed.

Table 20. Insulation Resistance between Patterns at each Layer for Kanagawa Factory Samples (10-Layer, 1.8 mm)

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13
L7	1.00E+13
L8	1.00E+13
L9	1.00E+13
L10	1.00E+13

Table 21. Inter-Layer Dielectric withstanding Voltage at each Layer for Kanagawa Factory Samples (10-Layer, 1.8 mm)

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects
L6 – L7	No defects
L7 – L8	No defects
L8 – L9	No defects
L9 – L10	No defects

Table 22. Insulation Resistance between Patterns at each Layer for Kahoku Factory Samples (6-Layer, 1.6 mm)

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13

Table 23. Inter-Layer Dielectric withstanding Voltage at each Layer for Kahoku Factory Samples (6-Layer, 1.6 mm)

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects

Table 24. Insulation Resistance between Patterns at each Layer for Kahoku Factory Samples (10-Layer, 1.8 mm)

Number of Layer	Insulation Resistance Results (MΩ)
L1	1.00E+13
L2	1.00E+13
L3	1.00E+13
L4	1.00E+13
L5	1.00E+13
L6	1.00E+13
L7	1.00E+13
L8	1.00E+13
L9	1.00E+13
L10	1.00E+13

Table 25. Inter-Layer Dielectric withstanding Voltage at each Layer for Kahoku Factory Samples (10-Layer, 1.8 mm)

Number of Layer	Visual Inspection Results
L1 – L2	No defects
L2 – L3	No defects
L3 – L4	No defects
L4 – L5	No defects
L5 – L6	No defects
L6 – L7	No defects
L7 – L8	No defects
L8 – L9	No defects
L9 – L10	No defects

6.8 Outgassing

6.8.1 Test Method

Outgassing shall be measured in accordance with ASTM E595.

Note: Samples for outgassing measurement were prepared to represent outgassing from the actual product and were tested at the product level (including solder resist, marking ink, etc.), rather than at the individual material level.

6.8.2 Acceptance Criteria

In the selection of materials for space applications, the criteria of "TML ≤ 1.0 % and CVCM ≤ 0.1 %," which have been traditionally used for material screening, shall not be used as the sole basis for evaluation. Instead, the impact of outgassing shall be assessed and determined at the system level, considering the use environment, the quantity of materials used, and the positional relationship between contamination sources and sensitive surfaces.

a) TML (Total Mass Loss)
b) CVCM (Collected Volatile Condensable Materials)
c) WVR (Water Vapor Regained)

6.8.3 Test Results

Outgassing measurement results for all samples from the Kanagawa factory (10-layer, 1.8 mm) and the Kahoku factory (6-layer, 1.6 mm and 10-layer, 1.8 mm) are as shown in Tables 26 to 28. The measurement results meet the requirements.

Table 26. Outgassing Test Results for Kanagawa Factory Samples (10-Layer, 1.8 mm)

TML (%)	CVCM (%)	WVR (%)
0.3292	0.004	0.081

Table 27. Outgassing Test Results for Kahoku Factory Samples (6-Layer, 1.6 mm)

TML (%)	CVCM (%)	WVR (%)
0.251	0.002	0.087

Table 28. Outgassing Test Results for Kahoku Factory Samples (10-Layer, 1.8 mm)

TML (%)	CVCM (%)	WVR (%)
0.262	0.001	0.086

7. RELIABILITY

7.1 Possible Failure Modes

The possible failure modes are as follows.

1) Open circuit
   a) External layer conductor open circuits
   b) Internal layer conductor open circuits
   c) Through-hole open circuits (including IVH and SVH open circuits)
   d) Internal layer interconnection open circuit
2) Short Circuit
   a) Short circuit
   b) Insulation failure
3) Land breakdown
4) Separation of conductor
5) Separation of plating
6) Bow and twist
7) Delamination
8) Insufficient solderability

8. STORAGE CONDITIONS

1) Ambient temperature: 0 °C to 30 °C
2) Relative humidity: 70 % RH as a maximum
3) Others
   To maintain the quality of printed wiring boards, storage under the following conditions shall be avoided.
   a) Storage in areas exposed to acids or alkalis.
   b) Storage in areas exposed to direct sunlight.
   c) Storage for more than one week after opening of the package.
   d) Storage during the assembly process.
   e) Storage under conditions where condensation or similar effects may adversely affect the boards.

9. NOTES

1) If the soldering temperature is excessively high, blistering of the base material and copper foil may occur. Therefore, proper control of temperature and time shall be ensured. For special assembly processes, mounting verification using prototype printed wiring boards shall be performed in advance.
2) Printed wiring boards may be susceptible to measling or blistering during high-temperature processing in part assembly due to moisture absorption. Therefore, the storage conditions specified in paragraph 8 shall be strictly followed.
3) To avoid degradation of solder wettability and solder wicking characteristics, printed wiring boards shall not be handled with bare hands after opening the package.

4) After opening under atmospheric conditions of 30 °C and 60 % RH or lower, the allowable storage period before part assembly shall be within 72 hours for printed wiring boards including SVH and IVH, and within 30 days for through-hole boards.

10. OTHERS

Contact information

Inquiries regarding application data sheets shall be directed to the head office. Orders received from customers are managed by the head office and production is arranged with each factory. Manufacturing and shipment are carried out by the respective factories, and after shipment, inquiries shall be handled by the shipping factory.

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