JAXA-ADS-2040/M105C

# COMMON PARTS/MATERIALS, SPACE USE, APPLICATION DATA SHEET FOR

| | |
|---|---|
| Part Description | CAPACITORS, MINIATURE, HIGH-CAPACITY, SURFACE MOUNT, FINE CERAMIC DIELECTRIC |
| Part Number and Type | J2040/M105 |
| Applicable Specification | JAXA-QTS-2040<br>JAXA-QTS-2040/M105 |

September 2025

Prepared and Established by Fukui Murata Manufacturing Co., Ltd.

Issued by Japan Aerospace Exploration Agency

This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users.  If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

The release date of the English version of this data sheet: 12 March 2026

## Record of revisions

| Rev. | Date | Description |
|---|---|---|
| NC | 8 May. 2012 | Original |
| A | 28 Nov. 2019 | Reflected the change of document by Fukui Murata Manufacturing Co., Ltd. Document No: JMCG0-0020-R (Rev. A) |
| B | 21 Oct. 2022 | Reflected the change of document by Fukui Murata Manufacturing Co., Ltd. Document No: JMCG0-0020-R (Rev. B) |
| C | 10 Sept. 2025 | Reflected the change of document by Fukui Murata Manufacturing Co., Ltd. Document No: JMCG0-0020-R (Rev. C) |
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No. JMCG0-0020-R

Revision history

| Rev. | Date | Description |
|---|---|---|
| NC | 8 May 2012 | Original |
| A | 28 Nov. 2019 | · Paragraph 2.1 Externals and Dimensions<br>Changed the dimensions L, W, T, G and S to the proper values in order to reduce the selection effort by correcting the dimensions.<br>· Paragraph 2.3<br>Changed the description of terminal finish S from “Sn60Pb37Ag3 solder coating over Ni plating” to “Replacement solder coating for terminal finish “Y”” in line with the detail specification.<br>· Paragraph 8 Storage condition<br>Specified the lower limit of the storage temperature and of the humidity in line with the detail specification.<br>· Contact<br>Updated the division from AS Capacitor Product Engineering Section II to Products Planning Section 1, Product Engineering Department, Capacitor Division, and telephone number from +81-778-21-8409 to +81-778-21-8371 due to internal organization change. |
| B | 21 Oct. 2022 | · Cover page<br>Changed Part number and type from JAXA2040 to J2040 in line with expression in JAXA-QTS-2040/M105.<br>· Paragraph 2, Summary of products (para. 2.1. Externals and dimensions a)Externals)<br>Added the picture and scale of J2040/M105-1005X7SB104KR. The picture was added for additional product type by requalification, and scale is to show clear contrast in size.<br>· Paragraph 2, Summary of products (para. 2.1. Externals and dimensions b)Dimensions and mass)<br>Added J2040/M105-1005X7SB104KR for additional lineup by requalification.<br>· Paragraph 2, Summary of products (para. 2.3. Terminal finish)<br>Changed description of terminal finish “Y” in line with the expression in JAXA-QTS-2040/M105.<br>· Paragraph 2, Summary of products (para. 2.3. Terminal finish)<br>Added the description of terminal finish “R” for additional lineup by requalification.<br>· Paragraph 3. Usage (para. 3.1 Ratings): Added J2040/M105-1005X7SB104KR and changed element thickness to dielectric thickness in the table due to additional lineup by requalification and bringing the term in line with supplementary table 1 of JAXA-QTS-2040/M105.<br>· Paragraph 3. Usage (para. 3.4 Recommended mounting methods)<br>Added size 1005 to the table for additional lineup by requalification.<br>· Paragraph 4 Characteristics under normal conditions<br>Changed JAXA2040 to J2040 in characteristics, sample, table, and part number in line with the expression in the detail specification JAXA-QTS-2040/M105.<br>· Paragraph 4 Characteristics under normal conditions<br>Added 5.J2040/M105-1005X7SB104KR for additional lineup by requalification.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Added 5.J2040/M105-1005X7SB104KR in capacitance for additional lineup by requalification. Also changes were made to dielectric dissipation factor, dielectric withstanding voltage, insulation resistance(25°C), insulation resistance(+125°C), impedance/ESR-frequency characteristics, ripple temperature characteristics, board bending, solderability, resistance to soldering heat, random vibration, shock, thermal shock and immersion cycling, moisture resistance, humidity, steady-state, low voltage, voltage-temperature characteristics, thermal shock (I), life, shear, direct voltage breakdown, and failure rate that appear thereafter. |

Revision history

| Rev. | Date | Description |
|---|---|---|
|  |  | · Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Changed V to Vrms in capacitance in line with paragraph M.4.4.7.1, Appendix M of JAXA-QTS-2040.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Set significant figure one digit less than the standard value in No. 1 data of capacitance to properly express the significant figure.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Set significant figure one digit less than the standard value in dielectric dissipation factor to properly express the significant figure. Also the dielectric dissipation factors that appear thereinafter were changed.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Added the defective number/sample size table for results in dielectric withstanding voltage to unify the expression of defective number/sample size.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Changed the y-axis title of the graph to Log IR [-] in insulation resistance(+25°C) since there is no unit for the logarithm of insulation resistance. Also the insulation resistance(+25°C) and (+125°C) that appear thereinafter were changed.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Changed Insulation resistance (+25°C) to logarithmic value in Ω instead of MΩ since it is common to express the logarithm value of insulation resistance in Ω. Also the insulation resistance(+25°C) and (+125°C) that appear thereinafter were changed.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Set significant figure one digit more than the standard value in Insulation resistance (+25°C) to properly express the significant figure. Also the insulation resistance(+25°C) and (+125°C) that appear thereinafter were changed.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.1 Electrical characteristics)<br>Changed Ripple temperature characteristics to Ripple heating characteristics for more appropriate expression.<br>· Paragraph 4 Characteristics under normal conditions (paragraph 4.2 Mechanical and thermal characteristics)<br>Set significant figure one digit less than the standard value in capacitance change rate for board bending to properly express the significant figure. Also the capacitance change rates that appear thereinafter were changed.<br>· Paragraph 5 Characteristics under various operating environmental conditions<br>Changed thermal shock (I) to thermal shock in Drifting in Thermal shock (I) in line with paragraph M.3.10.3, Appendix M of JAXA-QTS-2040.<br>· Paragraph 5 Characteristics under various operating environmental conditions<br>Changed IR to Insulation resistance in Drifting in Thermal shock (I) to unify the expression.<br>· Paragraph 6 Environmental limit (paragraph 6.1 Shear)<br>Added the description about the solder filet thickness being less than 1/2 (size 1005 or smaller) in a) for additional lineup by requalification.<br>· Paragraph 6 Environmental limit (paragraph 6.1 Shear)<br>Divided shear mode symbol D into D1 and D2 in b) test method in line with paragraph M.4.4.8.1, Appendix M of JAXA-QTS-2040.<br>· Paragraph 6 Environmental limit (paragraph 6.2 Direct voltage breakdown)<br>Deleted safety factor to prevent from misleading in use. |

Revision history

| Rev. | Date | Description |
|---|---|---|
| | | · Paragraph 9 Notes (paragraph 9.3 Note for Tin whisker)<br>Added terminal finish “R” due to additional “R” products by requalification.<br>· Paragraph 10 Others<br>Changed contact information to Products Planning Section 1, Product Engineering Department, Ceramic Capacitor Division due to organization change. |
| C | 10 Sept. 2025 | · Corrected parts numbers in paragraphs 4 through 6 as follows;.<br>From J2040/M105-3216X7RA226KS to J2040/M105-3216X7RA226MS.<br>From J2040/M105-3225X7RB226KS to J2040/M105-3225X7RB226MS.<br>Reason: The parts with capacitance tolerance "M" , not "K", were used as samples.<br>· Paragraph 3. Usage<br>Revised the rating description format in paragraph 3.1 to match the format used in the ADS for the N2040/L104 model type.<br>Accordingly, the dielectric thickness information was deleted.<br>Reason: The dielectric thickness is not required in the ADS, and the format is to be standardized with the L104 description.<br>· Paragraph 4.1<br>Added DC Bias Characteristics to the electrical characteristics.<br>Reason: To indicate that in high dielectric constant type MLCCs, capacitance may vary from the nominal value when a DC voltage is applied.<br>· Paragraph 4.1<br>Added AC Voltage Characteristics to the electrical characteristics.<br>Reason: To indicate that in high dielectric constant type MLCCs, capacitance may vary from the nominal value when an AC voltage is applied.<br>· Paragraph 6.3 Thermal Shock + PCBT (Pressure Cooker Bias Test)<br>Changed the part number in item b) from the former Murata part number to the new Murata part number as follows;<br>From GRK42-6X7R226K6.3 to GCM31CR70J226K.<br>· Paragraph 8. Storage Conditions<br>Revised some expressions<br>Reason: To unify the terminology with other paragraphs.<br>· Paragraph 9. Notes<br>Added to specify the use of resin coating materials with high sulfur gas barrier properties in item d) of paragraph 9.2.1.<br>Reason: Dendrite formation may occur in environments containing sulfur-based gases.<br>· Paragraph 9. Notes<br>Added reference data on the relationship between resin coating, life test conditions, and dendrite formation to paragraph 9.2.2.<br>Reason: The reference data indicates that without a resin coating, dendrite formation tends to occur as the ambient temperature increases, while with a resin coating, dendrite formation was suppressed even under high-temperature conditions.<br>· Paragraph 9. Notes<br>Added DC bias characteristics in paragraph 9.4 and AC voltage characteristics in paragraph 9.5.<br>Reason: To clarify that in high dielectric constant type MLCCs, the capacitance may vary from its nominal value depending on the applied DC bias or AC voltage. |

## Contents

No. JMCG0-0020-R

# COMMON PARTS/MATERIALS, SPACE USE, APPLICATION DATA SHEET FOR

## 1. GENERAL

### 1.1 Scope

This Application Data Sheet details additional general information necessary for parts selection and/or equipment design that is not contained in JAXA-QML. Users are encouraged to look into other information sources for specific applications, and responsible for their decisions on part selection and usage.

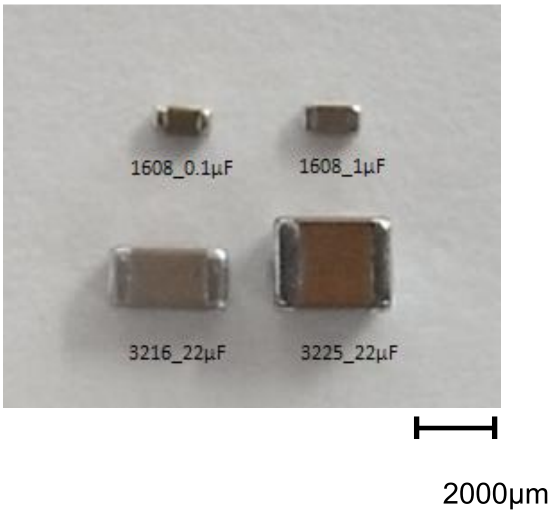
### 1.2 Applicable Documents

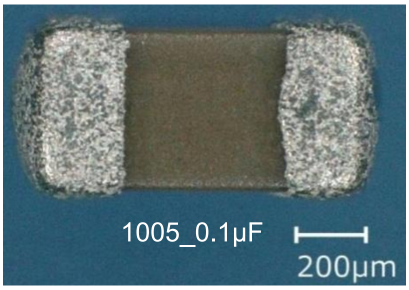
| | | |
|---|---|---|
| (a) | JAXA-QTS-2040 | Capacitors, Fixed, High Reliability, Space Use, General Specification For |
| (b) | JAXA-QTS-2040/M105 | Capacitors, Miniature, High-Capacity, Surface Mount, Fine Ceramic Dielectric, (J2040/M105), High Reliability, Space Use, Detail Specification For |

## 2. SUMMARY OF PRODUCTS

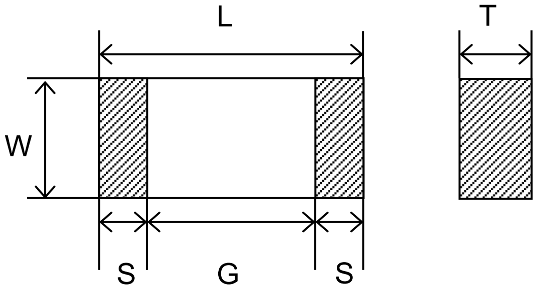
### 2.1 Externals and Dimensions

a) Externals





b) Dimensions and Mass

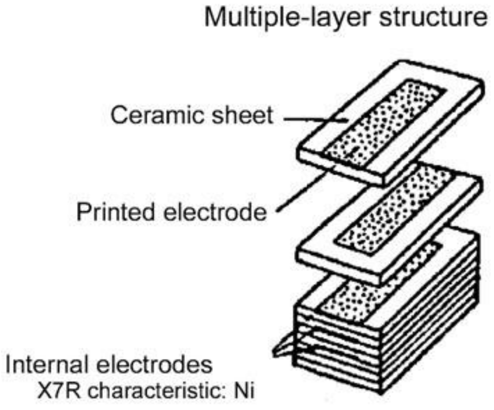


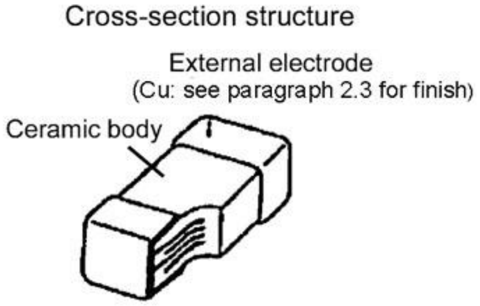
**Outline of the Capacitor**

Unit: mm

| Symbol / Style | L | | W | | T | | G | S | Mass (mg) |
|---|---|---|---|---|---|---|---|---|---|
| | Max | Min | Max | Min | Max | Min | | | |
| 1005 | 1.10 | 0.90 | 0.60 | 0.40 | 0.60 | 0.40 | 0.3 min. | 0.1 to 0.4 | 1.6 |
| 1608 | 1.80 | 1.50 | 1.00 | 0.70 | 1.00 | 0.70 | 0.5 min. | 0.2 to 0.6 | 7 |
| 3216 | 3.60 | 3.05 | 1.90 | 1.45 | 1.90 | 1.50 | 1.2 min. | 0.3 min. | 55 |
| 3225 | 3.60 | 2.90 | 2.80 | 2.30 | 2.80 | 2.30 | 1.0 min. | 0.3 min. | 130 |

## 2.2 Element Construction





## 2.3 Terminal Finish

| Symbol | Terminal finish |
|---|---|
| Y | Ni and Sn plating over underlying metal |
| S | Replacement solder coating for terminal finish “Y” |
| R | Resin electrode, Ni plating, Sn plating, and solder (SnPb) plating over underlying metal |

## 2.4 Failure Rate Level

The product satisfies S level (0.001%/1000HR). See paragraph 7.1 for details.

## 3. USAGE

### 3.1 Ratings

| Item | JAXA-QTS-2040 Applicable paragraph | Note |
|---|---|---|
| Voltage－Temperature Characteristics | M.1.3.2 | X7R X7S |
| Nominal capacitance range | M.1.3.4 | 0.1μF to 22μF |
| Rated voltage | M.1.3.3 | 3.5V, 8V, 25V |
| Operating temperature range | M.1.3.2 | -55°C to +125°C |
| Capacitance tolerance | M.1.3.5 | K, M |

### 3.2 Recommended Operating Conditions

Ambient temperature: -55 to +75°C

### 3.3 Notes for Circuit Design

Capacitors with X7R characteristics are suitable for use as bypass and coupling capacitors in high frequency circuits. The capacitors shall be used under the rated voltage within the operating temperature range.

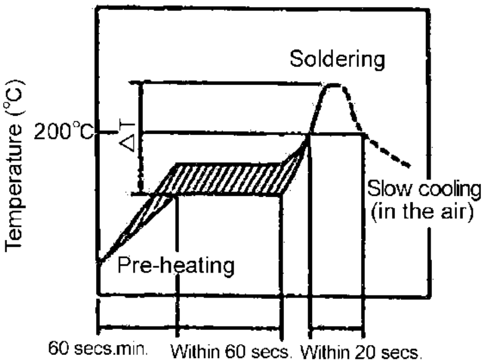
### 3.4 Recommended Mounting Methods

a) Fluxes shall be selected from those of rosin types with chlorine concentration of 0.2wt% as a maximum.
b) Solders shall be selected from those of Sn-Pb types with Sn:Pb ratio of 6:4 or 5:5.
c) Preheating shall be performed prior to soldering to control the temperature differences as shown in the table below. If the temperature difference exceeds the limit, cracks could occur on the ceramic element and reduce the insulation resistance, which could lead to insulation failures and/or short-circuiting.

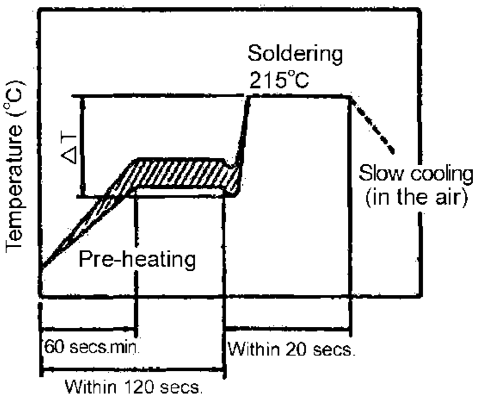
| Chip size | Temperature difference ($\Delta T$) |
|---|---|
| 1005, 1608 | Up to 190°C |
| 3216, 3225 | Up to 130°C |

d) Recommended Soldering Conditions
Reflow soldering

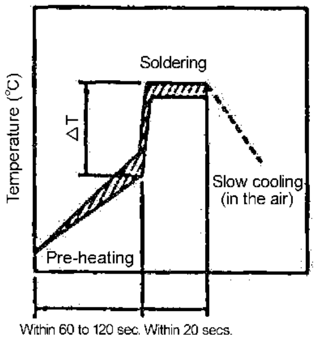
Infrared reflow soldering



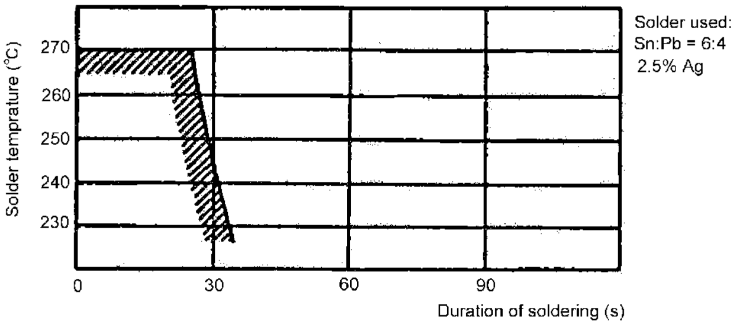
Vapor reflow soldering



·Iron soldering



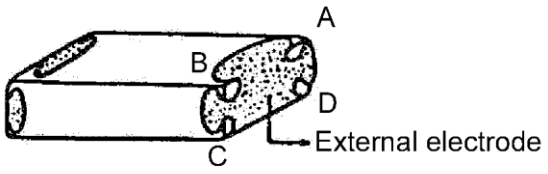
e) Allowable soldering temperatures and durations



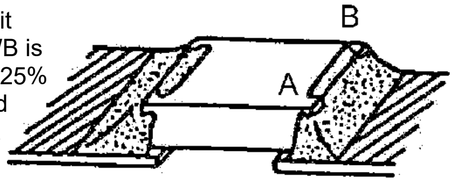
When soldering is repeated, note that the allowable duration is a total of soldering durations. When soldering is performed with different method(s), the allowable duration is a total of normalized soldering durations which offset different soldering conditions.

f) If soldering took a long time, verify with a magnifier that dissolution of the electrodes shall not exceed a maximum of 25% of the perimeter of A-B-C-D face.

Single unit



Unit soldered on PWB



As the edge of unit soldered on a PWB is partially invisible, 25% shall be measured within visible area (side A-B).

g) Limit the solder amount (fillet height) between 0.30 and 0.50T (T: thickness of the capacitor) and mount on an Alumina board or glass epoxy board (FR-4). Verify that the solder joint is firmly secured to the board. When 3225 size capacitor is mounted on an Alumina board, limit the solder amount between 0.15T and 0.25T. Minimize the solder quantity. Check the compatibility with the boards (compatibility of Coefficient of Thermal Expansion (CTE) ) prior to use.
CTE (as an example)
Ceramics: 11ppm/°C
Alumina: 7ppm/°C
FR-4: less than Tg: 16ppm/°C, more than Tg: 15ppm/°C, (Tg=140 to 150°C)

h) After soldering the capacitors shall be left in room temperature for slow cooling.

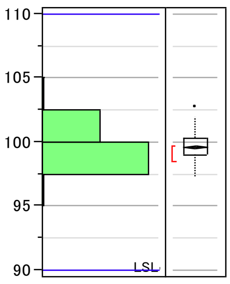
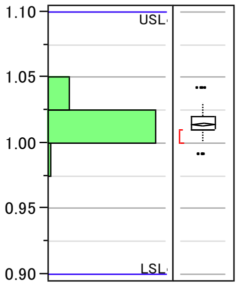
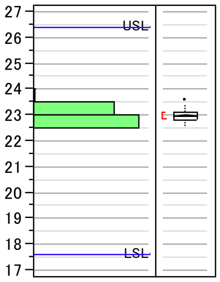
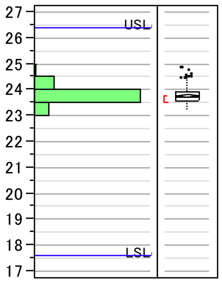
## 4. CHARACTERISTICS UNDER NORMAL CONDITIONS

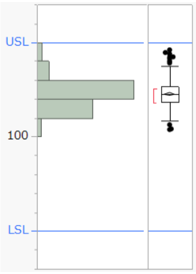
Sample

| No | Part number | Size | Characteristics | Rate voltage (V) | Capacitance (μF) |
|---|---|---|---|---|---|
| 1. | J2040/M105-1608X7RC104KS | 1608 | X7R | 25 | 0.1 |
| 2. | J2040/M105-1608X7RB105KS | 1608 | X7R | 8 | 1 |
| 3. | J2040/M105-3216X7RA226MS | 3216 | X7R | 3.5 | 22 |
| 4. | J2040/M105-3225X7RB226MS | 3225 | X7R | 8 | 22 |
| 5. | J2040/M105-1005X7SB104KR | 1005 | X7S | 8 | 0.1 |

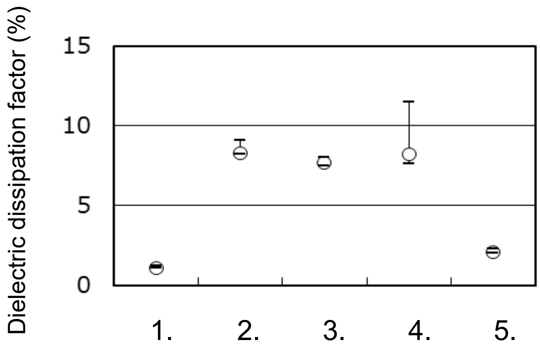
### 4.1 Electrical Characteristics

[Capacitance]

| No. | 1. | 2. | 3. | 4. |
|---|---|---|---|---|
| Sample size | 245 | 245 | 245 | 245 |
| Measuring condition | 1kHz 1.0V$_{\mathrm{rms}}$ | 1kHz 1.0 V$_{\mathrm{rms}}$ | 120Hz 0.5 V$_{\mathrm{rms}}$ | 120Hz 0.5 V$_{\mathrm{rms}}$ |
| Limit | 90 to 110 μF | 0.9 to1.1 μF | 17.6 to 26.4 μF | 17.6 to 26.4 μF |
|  |  |  |  |  |
| Ave | 99.61 | 1.010 | 22.970 | 23.770 |
| Max | 102.6 | 1.04 | 23.52 | 24.80 |
| Min | 97.3 | 0.99 | 22.51 | 23.14 |

| No. | 5. |  |  |  |
|---|---|---|---|---|
| Sample size | 241 |  |  |  |
| Measuring condition | 1kHz 1.0 V$_{\mathrm{rms}}$ |  |  |  |
| Limit | 90 to 110 μF |  |  |  |
|  |  |  |  |  |
| Ave | 104.54 |  |  |  |
| Max | 109.2 |  |  |  |
| Min | 100.8 |  |  |  |

[Dissipation factor]

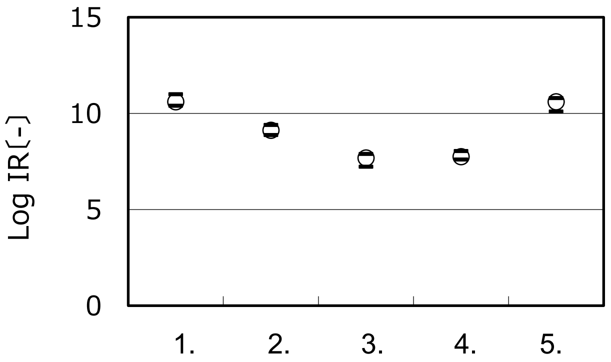


| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 245 | 245 | 245 | 245 | 241 |
| Limit | 15% as a maximum | | | | |
| Ave | 1.14 | 8.33 | 7.66 | 8.15 | 2.13 |
| Max | 1.2 | 9.1 | 8.0 | 11.5 | 2.3 |
| Min | 1.1 | 8.2 | 7.5 | 7.6 | 2.0 |

[Dielectric withstanding voltage] (250%WV, 5s±1s as a minimum)

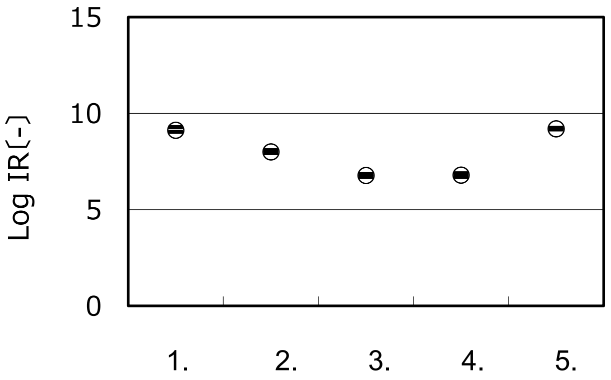
| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| No. of defective/ Sample size | 0/245 | 0/245 | 0/245 | 0/245 | 0/241 |

[Insulation resistance] (+25°C)



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 245 | 245 | 245 | 245 | 241 |
| Limit | 9.0≦ | 8.0≦ | 6.7≦ | 6.7≦ | 8.7≦ |
| Ave | 10.61 | 9.120 | 7.680 | 7.740 | 10.59 |
| Max | 11.0 | 9.40 | 7.89 | 8.04 | 10.8 |
| Min | 10.4 | 8.88 | 7.23 | 7.60 | 10.1 |

[Insulation resistance] (+125°C)

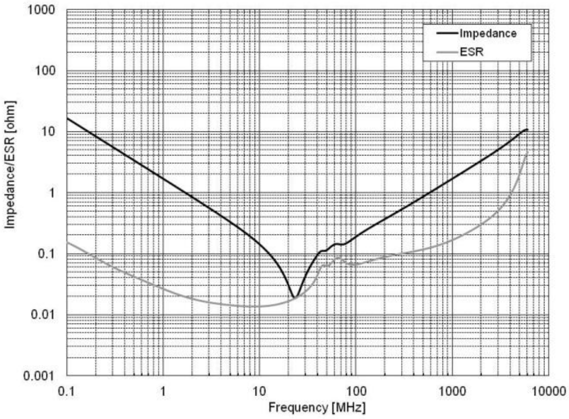


| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 245 | 245 | 245 | 245 | 241 |
| Limit | 8.0≦ | 7.0≦ | 5.7≦ | 5.7≦ | 7.7≦ |
| Ave | 9.120 | 8.000 | 6.780 | 6.790 | 9.199 |
| Max | 9.29 | 8.09 | 6.85 | 6.89 | 9.26 |
| Min | 9.05 | 7.94 | 6.71 | 6.71 | 9.17 |

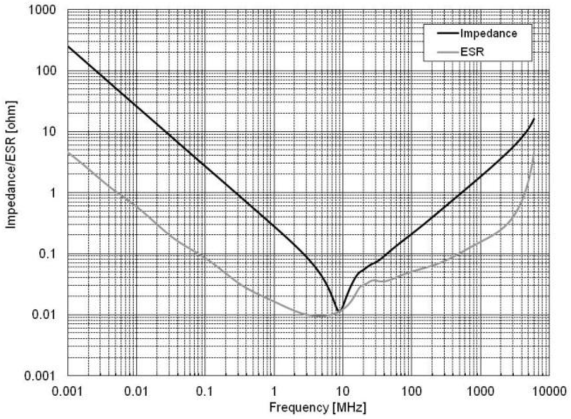
No. JMCG0-0020-R

[Impedance / ESR - Frequency characteristics]

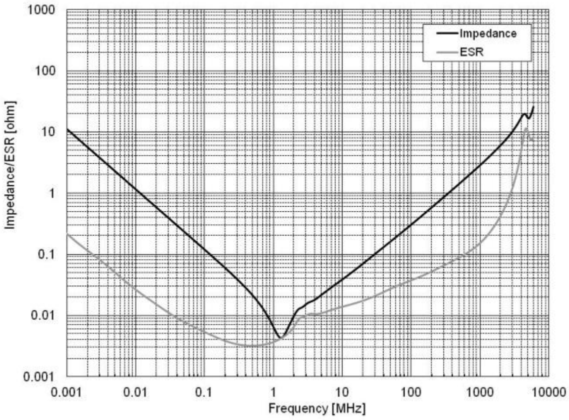
1. 1608X7RC104KS



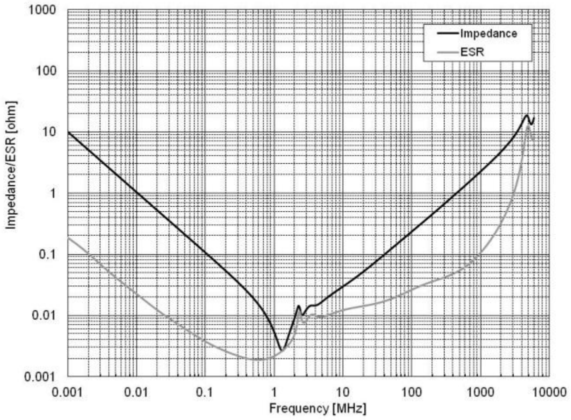
2.1608X7RB105KS



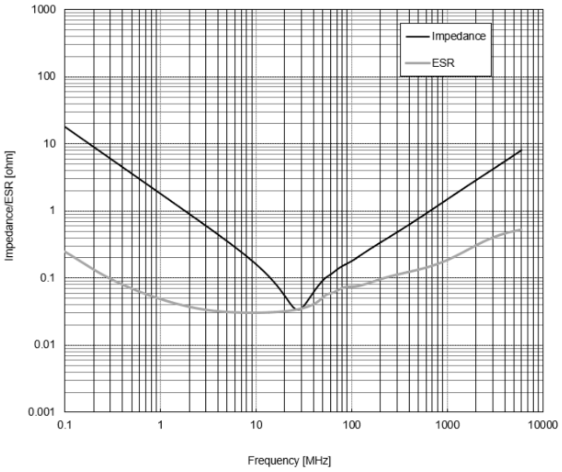
3. 3216X7RA226MS



4.3225X7RB226MS

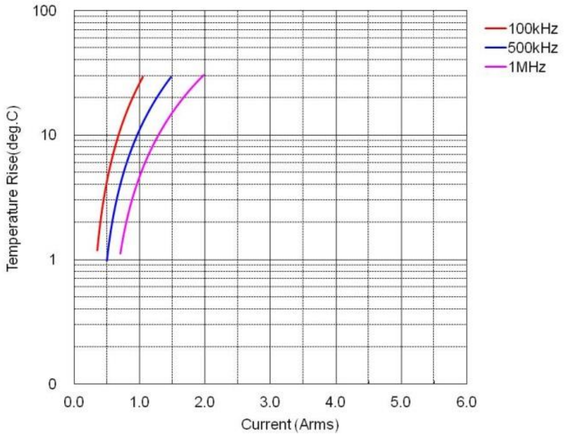


5.1005X7SB104KR

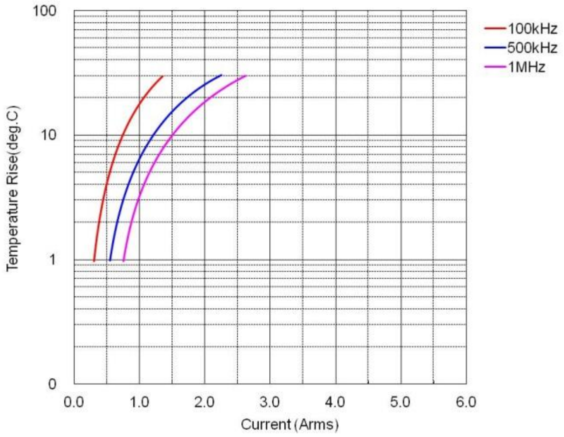


[Ripple temperature characteristics]

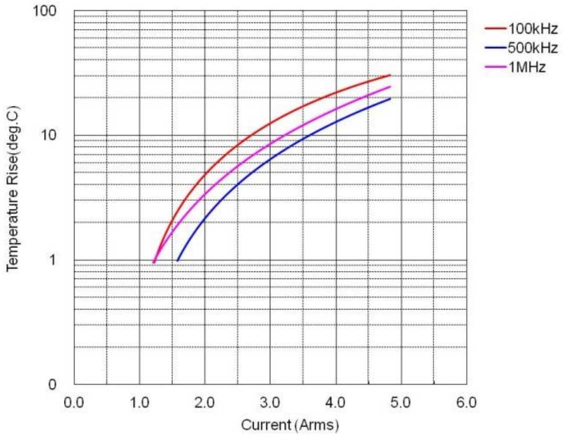
1. 1608X7RC104KS



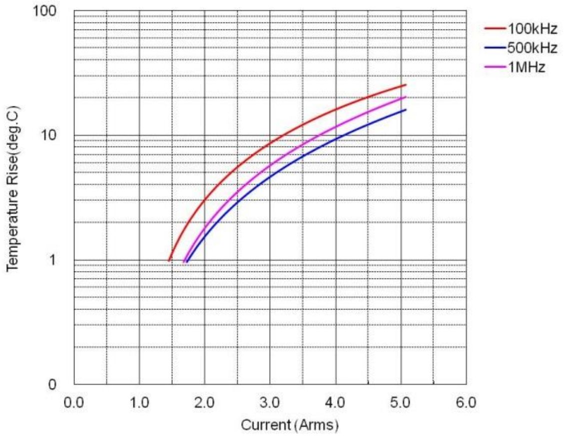
2. 1608X7RB105KS



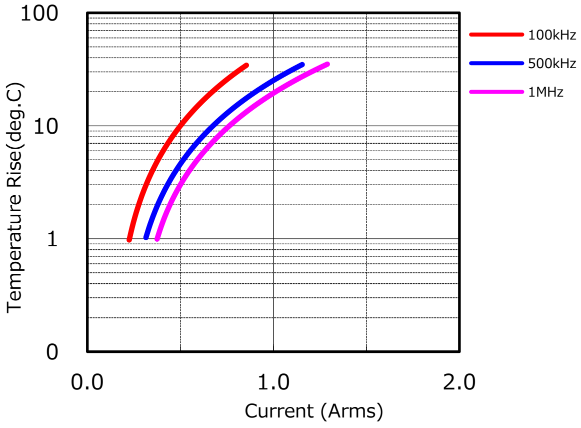
3. 3216X7RA226MS



4. 3225X7RB226MS

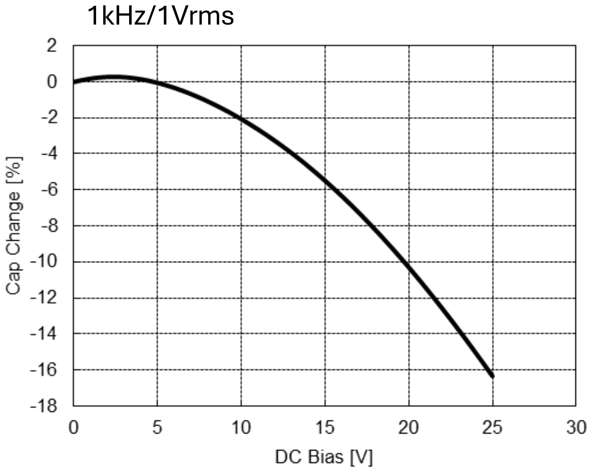


5.1005X7SB104KR

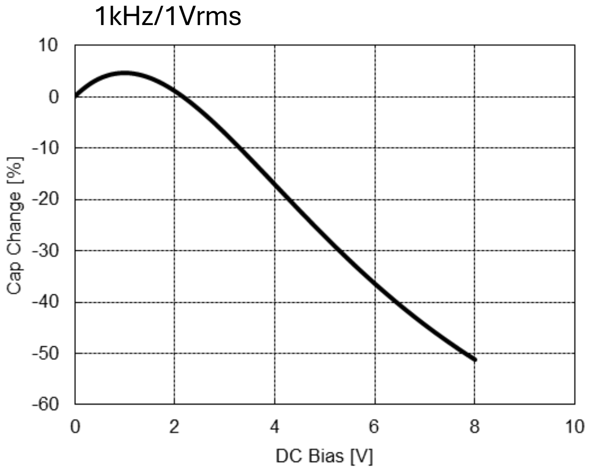


〔DC Bias Characteristics〕

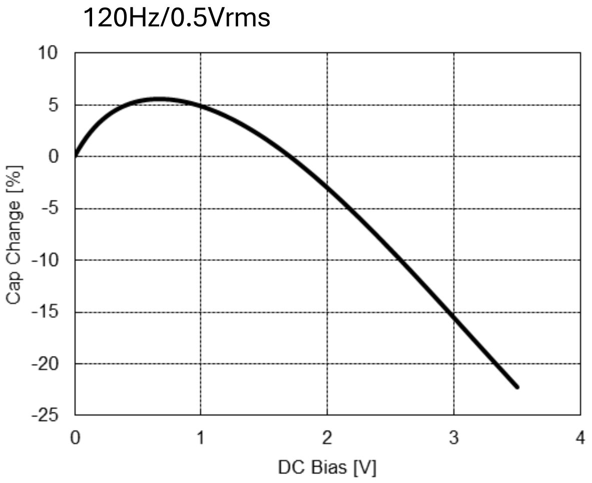
1.1608X7RC104KS



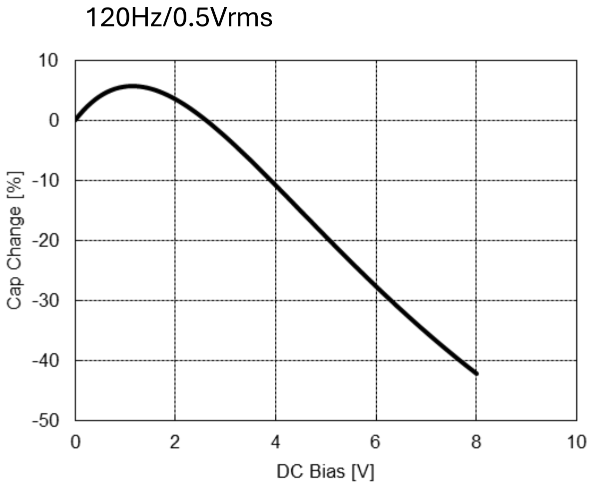
2.1608X7RB105KS



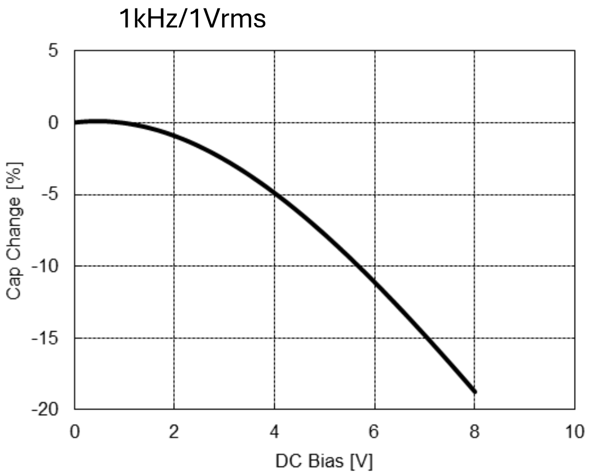
3.3216X7RA226MS



4.3225X7RB226MS

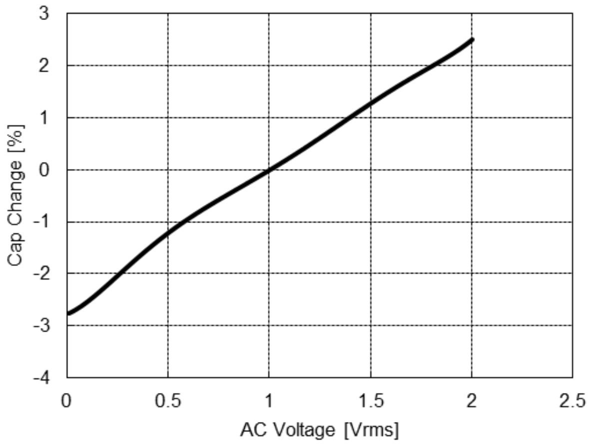


5.1005X7SB104KR

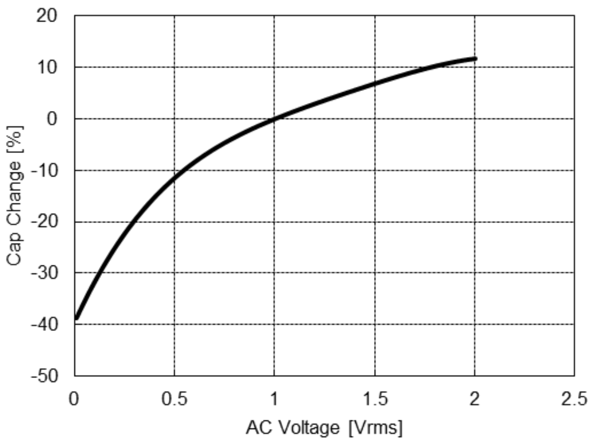


## 〔AC Voltage Characteristics〕

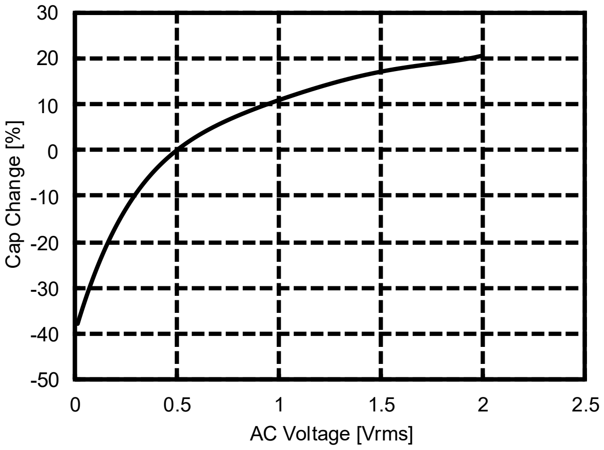
### 1.1608X7RC104KS



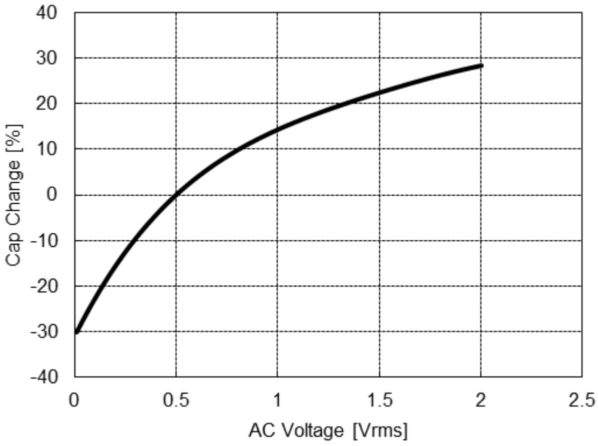
### 2.1608X7RB105KS



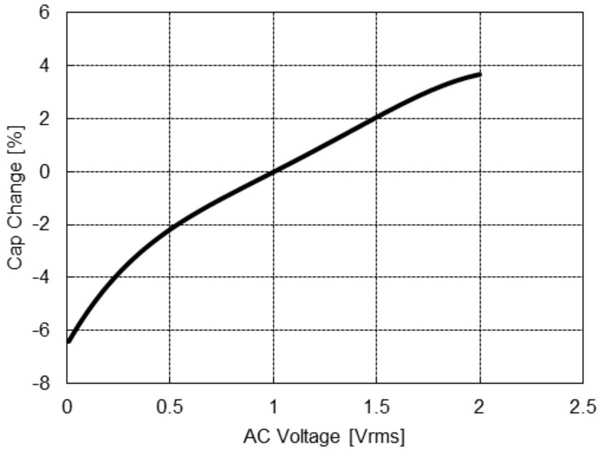
### 3.3216X7RA226MS



### 4.3225X7RB226MS



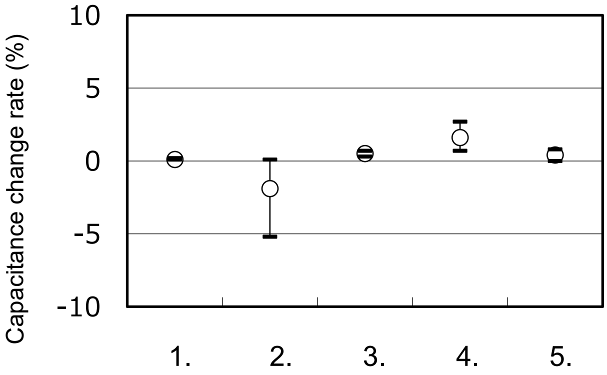
### 5.1005X7SB104KR



## 4.2 Mechanical and Thermal Characteristics

[Substrate bending]
Flexure: 1mm, Duration: 5±1 seconds

[Capacitance change rate]



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 3 | 3 | 3 | 3 | 3 |
| Limit | Within ±10% | | | | |
| Ave | 0.13 | -1.87 | 0.54 | 1.63 | 0.40 |
| Max | 0.2 | 0.1 | 0.7 | 2.7 | 0.8 |
| Min | 0.1 | -5.2 | 0.3 | 0.7 | 0.0 |

[Solderability]
Solder temperature: 230±5°C, Immersion duration: 5±0.5 seconds

[Externals]

| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| No. of defective/ Sample size | 0/4 | 0/4 | 0/4 | 0/4 | 0/4 |

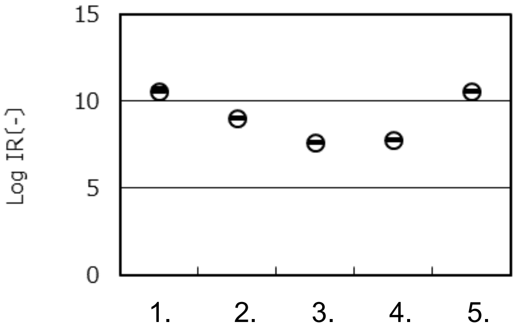
[Resistance to soldering heat]

Solder temperature: 260±5°C,  Immersion duration: 10±1 seconds

[Externals]

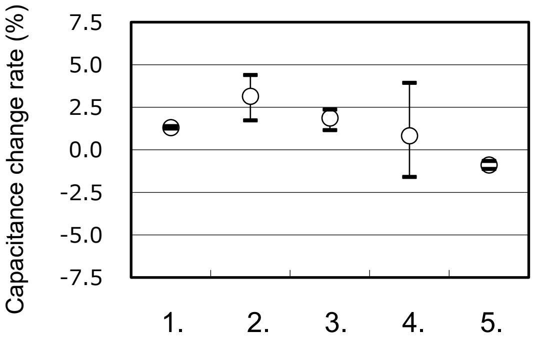
| No | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| No. of defective/ Sample size | 0/4 | 0/4 | 0/4 | 0/4 | 0/4 |

[Insulation resistance] (+25°C)



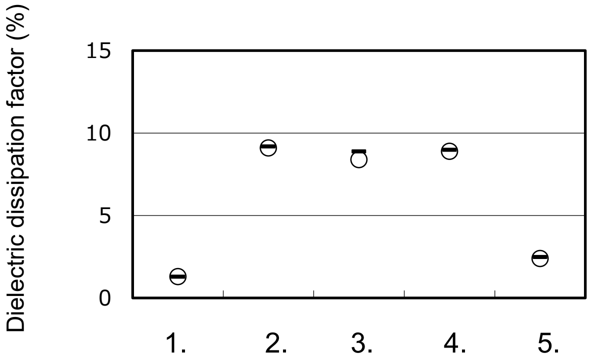
| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 4 | 4 | 4 | 4 | 4 |
| Limit | 9.0≦ | 8.0≦ | 6.7≦ | 6.7≦ | 8.7≦ |
| Ave | 10.65 | 9.045 | 7.605 | 7.790 | 10.56 |
| Max | 10.7 | 9.06 | 7.61 | 7.80 | 10.6 |
| Min | 10.6 | 9.03 | 7.60 | 7.78 | 10.5 |

[Capacitance change rate]



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 4 | 4 | 4 | 4 | 4 |
| Limit | Within ±7.5% | | | | |
| Ave | 1.310 | 3.150 | 1.870 | 0.830 | -0.887 |
| Max | 1.40 | 4.41 | 2.38 | 3.95 | -0.64 |
| Min | 1.26 | 1.74 | 1.17 | -1.58 | -1.11 |

[Dissipation factor]



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 4 | 4 | 4 | 4 | 4 |
| Limit | 15% as a maximum | | | | |
| Ave | 1.27 | 9.13 | 8.41 | 8.92 | 2.44 |
| Max | 1.3 | 9.2 | 8.9 | 9.0 | 2.5 |
| Min | 1.2 | 9.1 | 8.2 | 8.7 | 2.4 |

[Random vibration]
1WV x 125% Frequency range: 50 to 2000Hz, Overall effective acceleration: 53.79Grms
Direction and duration of vibration: 3 min. each direction (total of 9 min.) of three angles which are perpendicular to each other.

| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| No. of Defective/ Sample size | 0/10 | 0/10 | 0/10 | 0/10 | 0/10 |

*Shall not have any intermittent contact, open or short-circuitry of 0.1ms or more.

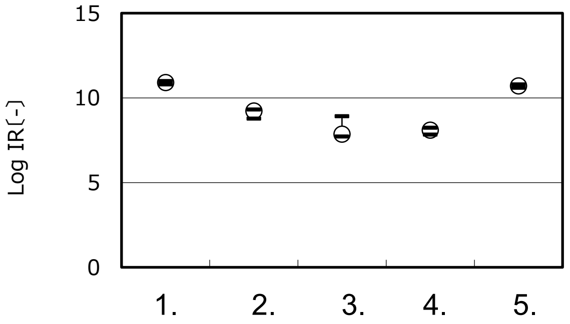
[Shock]
Maximum acceleration: 14.71km/s$^2$, Normal duration: 0.5ms, Waveform: half-wave sine wave, Rate change: 4.69m/s, All effect acceleration: 1500g’s

| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| No. of Defective/ Sample size | 0/10 | 0/10 | 0/10 | 0/10 | 0/10 |

*Shall not have any intermittent contact, open or short-circuitry of 0.1ms or more.

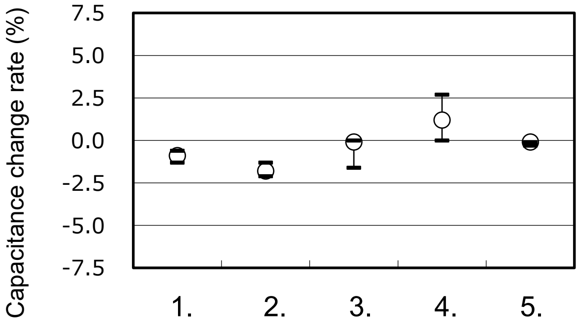
[Thermal shock and Immersion cycle]
Thermal shock: -55 to 125°C, 250 cycles
Immersion cycle: 65°C fresh water ↔ 25°C saturated saline, 2 cycles

[Insulation resistance] (25°C)



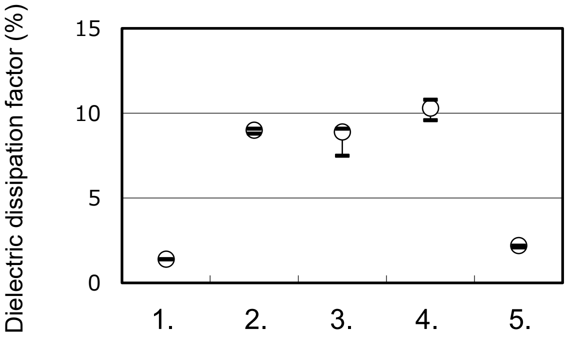
| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 18 | 18 | 18 | 18 | 18 |
| Limit | 8.7≦ | 7.7≦ | 6.4≦ | 6.4≦ | 8.4≦ |
| Ave | 10.90 | 9.220 | 7.860 | 8.092 | 10.68 |
| Max | 11.0 | 9.32 | 8.92 | 8.24 | 10.8 |
| Min | 10.8 | 8.78 | 7.72 | 7.84 | 10.6 |

[Capacitance change rate]



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 18 | 18 | 18 | 18 | 18 |
| Limit | Within ±10% | | | | |
| Ave | -0.89 | -1.78 | -0.13 | 1.15 | -0.14 |
| Max | -0.6 | -1.3 | 0.0 | 2.7 | -0.1 |
| Min | -1.3 | -2.1 | -1.6 | 0.0 | -0.3 |

[Dissipation factor]

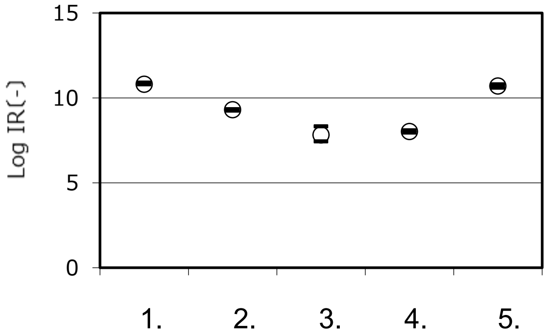


| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 18 | 18 | 18 | 18 | 18 |
| Limit | 15% as a maximum | | | | |
| Ave | 1.41 | 9.01 | 8.91 | 10.25 | 2.15 |
| Max | 1.4 | 9.1 | 9.1 | 10.8 | 2.2 |
| Min | 1.4 | 8.8 | 7.5 | 9.6 | 2.1 |

[Moisture resistance]

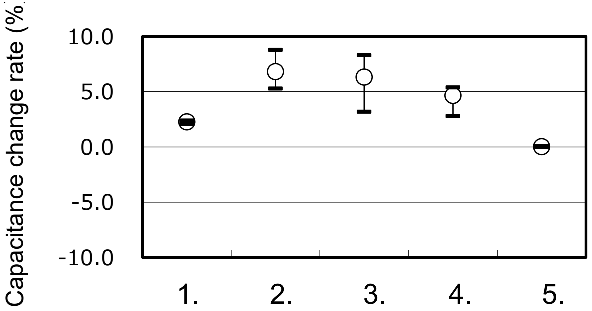
MIL-STD-202 TM106 20 times in a row

[Insulation resistance] (+25°C)



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 12 | 12 | 12 | 12 | 12 |
| Limit | 8.7≦ | 7.7≦ | 6.4≦ | 6.4≦ | 8.4≦ |
| Ave | 10.82 | 9.300 | 7.821 | 8.019 | 10.74 |
| Max | 10.9 | 9.34 | 8.33 | 8.09 | 10.8 |
| Min | 10.8 | 9.25 | 7.44 | 7.96 | 10.6 |

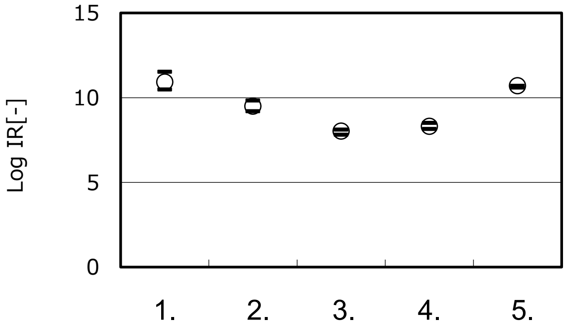
[Capacitance change rate]



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 12 | 12 | 12 | 12 | 12 |
| Limit | Within ±10% | | | | |
| Ave | 2.27 | 6.82 | 6.32 | 4.66 | 0.02 |
| Max | 2.4 | 8.8 | 8.3 | 5.4 | 0.1 |
| Min | 2.1 | 5.3 | 3.2 | 2.8 | 0.0 |

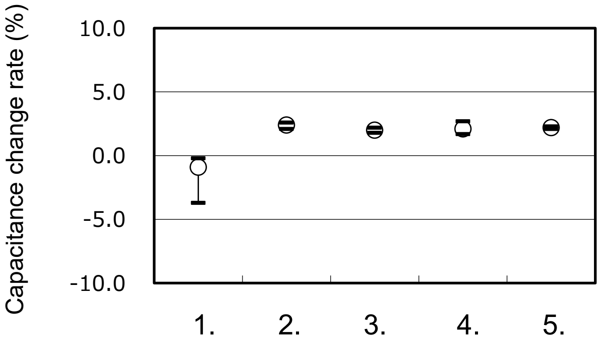
[Humidity, Steady-State, Low voltage]
85°C, 85%RH, DC1.3V, 240h

[Insulation resistance] (+25°C)



| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 12 | 12 | 12 | 12 | 12 |
| Limit | 9.0≦ | 8.0≦ | 6.7≦ | 6.7≦ | 8.7≦ |
| Ave | 10.90 | 9.500 | 8.030 | 8.310 | 10.65 |
| Max | 11.5 | 9.84 | 8.12 | 8.52 | 10.7 |
| Min | 10.5 | 9.20 | 7.82 | 8.16 | 10.6 |

[Capacitance change rate]

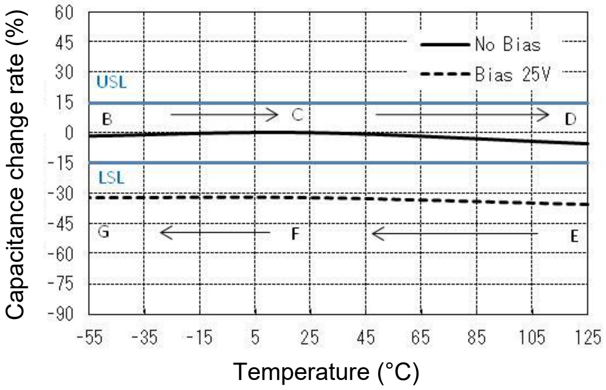


| No. | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 12 | 12 | 12 | 12 | 12 |
| Limit | Within ±10% | | | | |
| Ave | -0.88 | 2.43 | 1.97 | 2.08 | 2.18 |
| Max | -0.2 | 2.6 | 2.2 | 2.7 | 2.3 |
| Min | -3.7 | 2.1 | 1.8 | 1.7 | 2.1 |

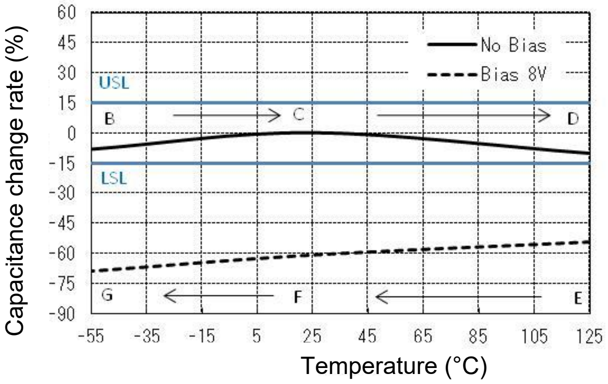
## 5. CHARACTERISTICS UNDER VARIOUS OPERATING ENVIRONMENTAL CONDITIONS

[Voltage – Temperature characteristics] (Sample size: 4 pieces)

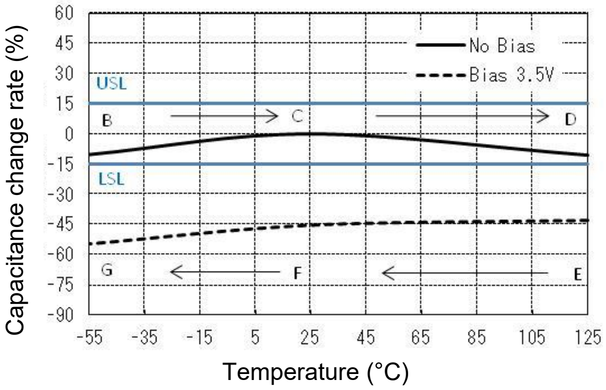
1.1608X7RC104KS



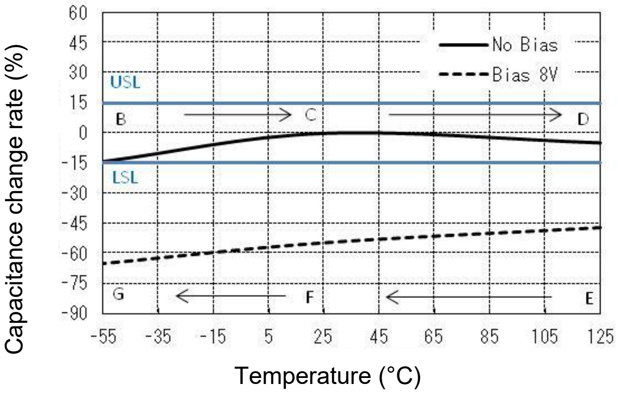
2.1608X7RB105KS



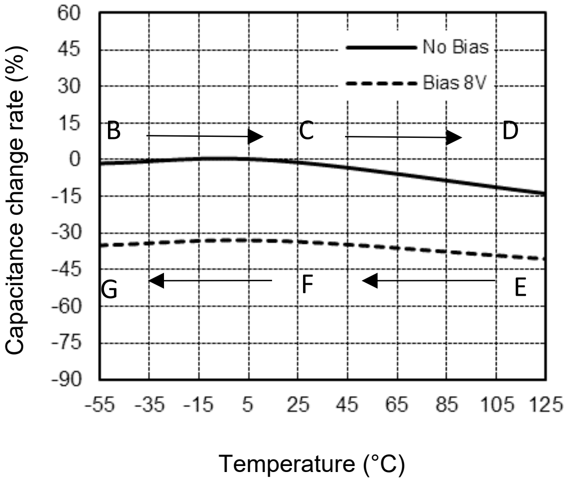
3. 3216X7RA226MS



4.3225X7RB226MS



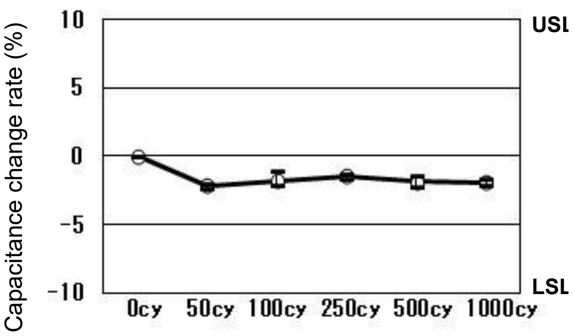
5.1005X7SB104KR



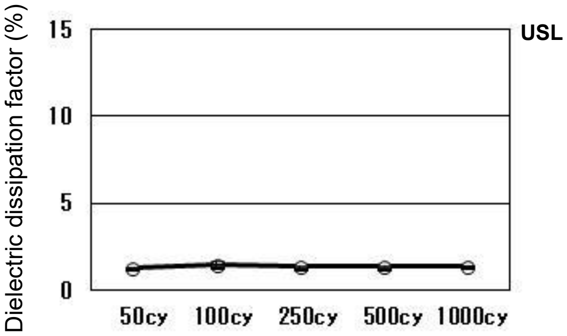
[Drifting in Thermal shock (I)] (Sample size: 18 pieces)

1.1608X7RC104KS

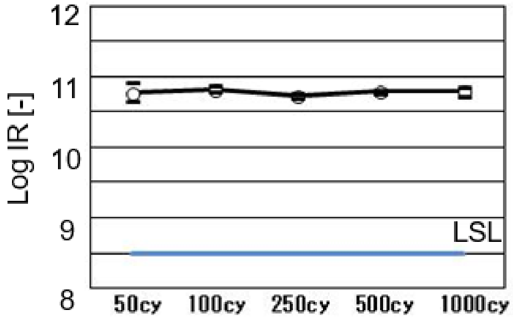
[Capacitance change rate]



[DF]

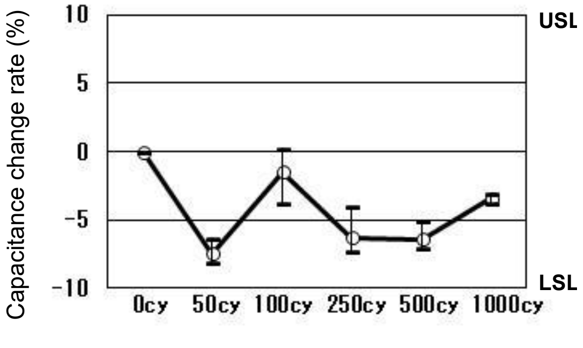


[IR] (+25°C)

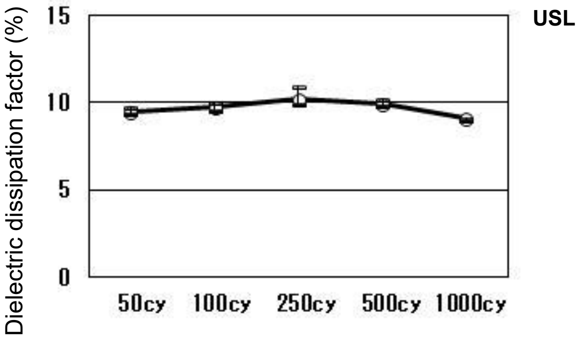


2.1608X7RB105KS

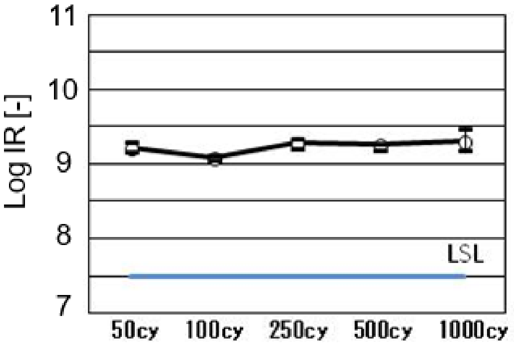
[Capacitance change rate]



[DF]

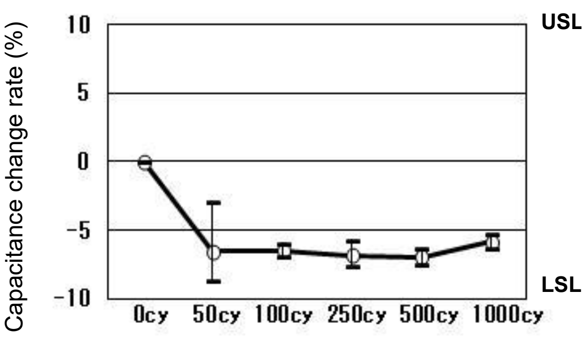


[IR] (+25°C)

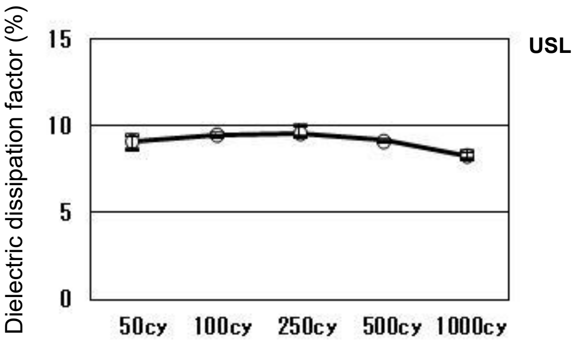


### 3.3216X7RA226MS

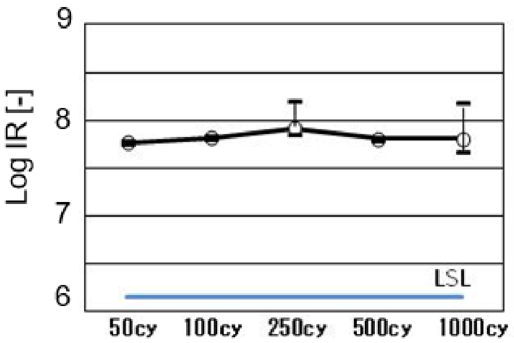
[Capacitance change rate]



[DF]

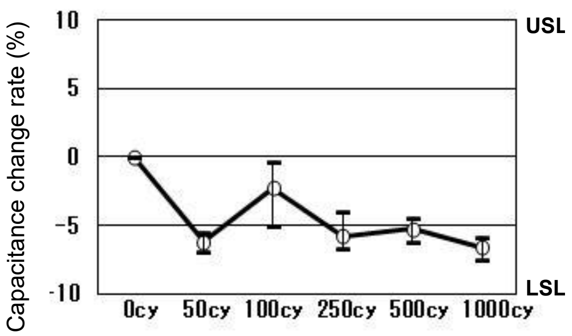


[IR] (+25°C)

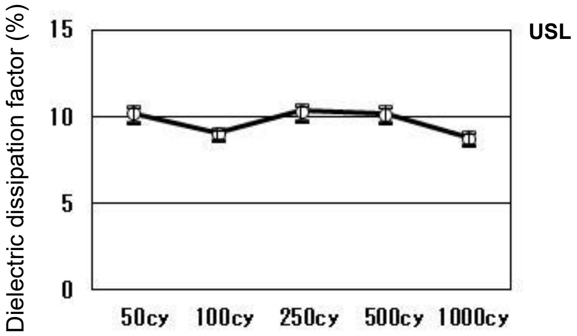


### 4. 3225X7RB226MS

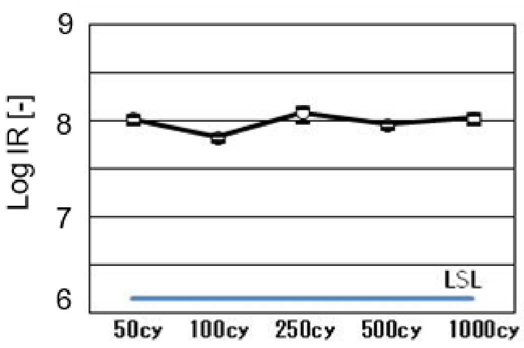
[Capacitance change rate]



[DF]

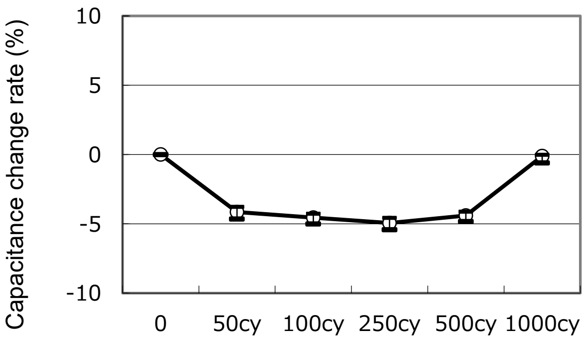


[IR] (+25°C)

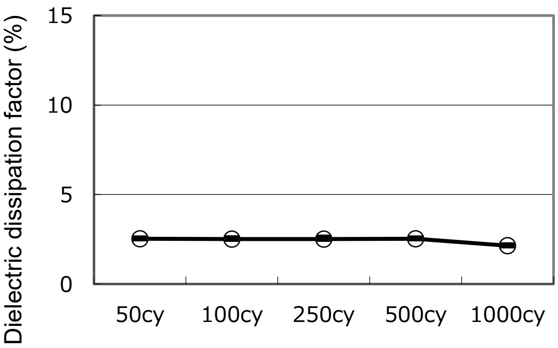


5.1005X7SB104KR

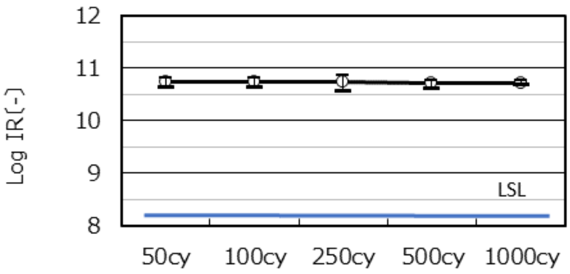
[Capacitance change rate]



[DF]



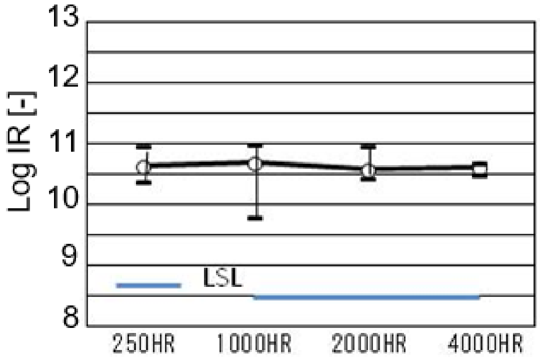
[IR] (+25°C)



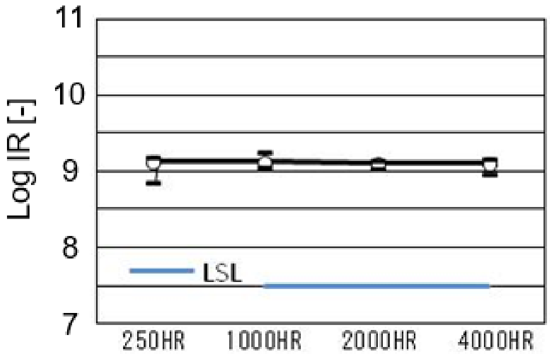
[Drifting in Life test] (Sample size: 123 pieces)

1.1608X7RC104KS

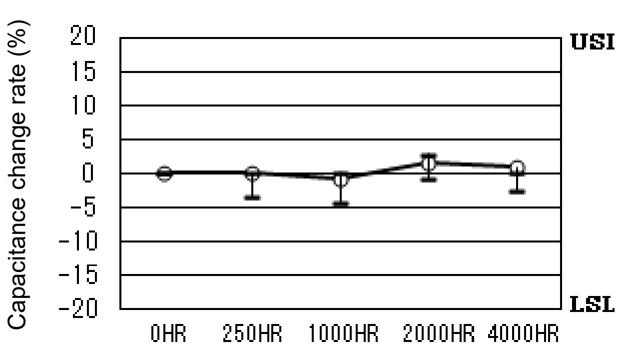
[IR] (+25°C)



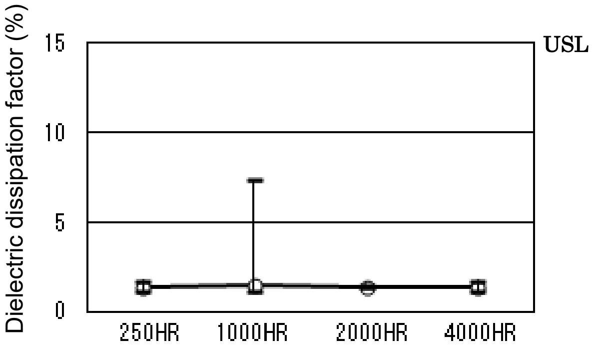
[IR] (+125°C)



[Capacitance change rate]

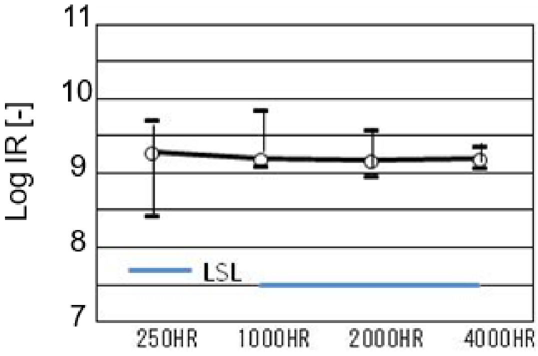


[DF]

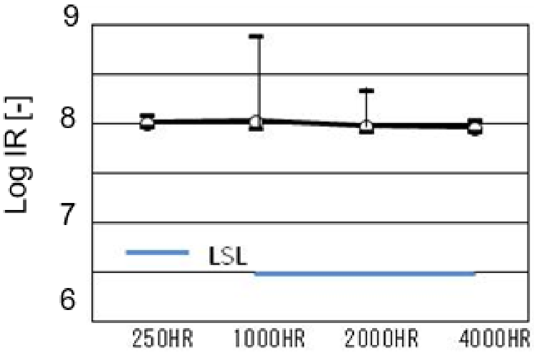


2. 1608X7RB105KS

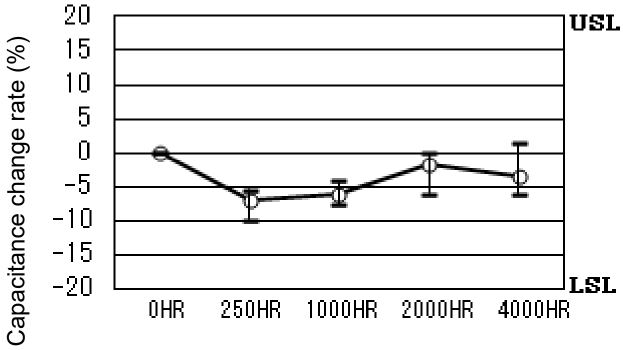
[IR] (+25°C)



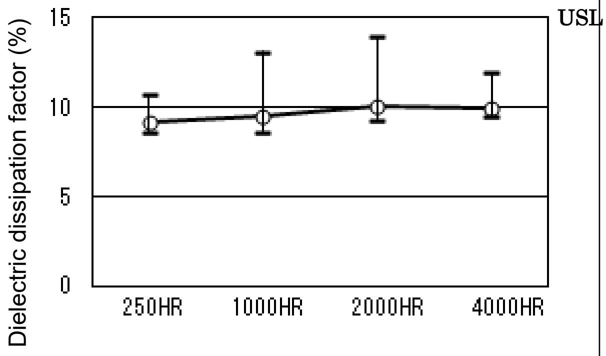
[IR] (+125°C)



[Capacitance change rate]

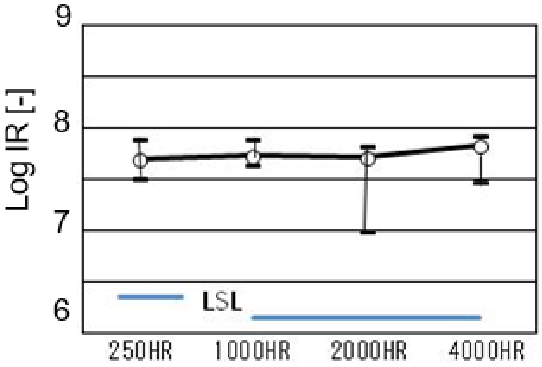


[DF]

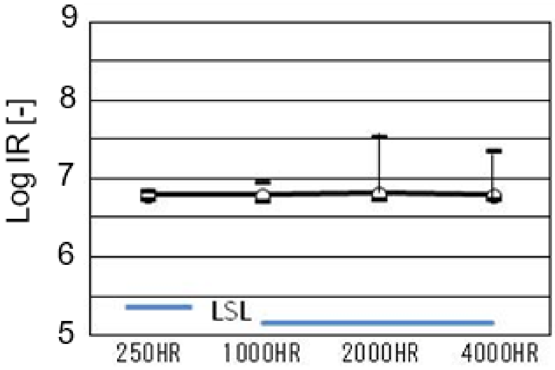


3. 3216X7RA226MS

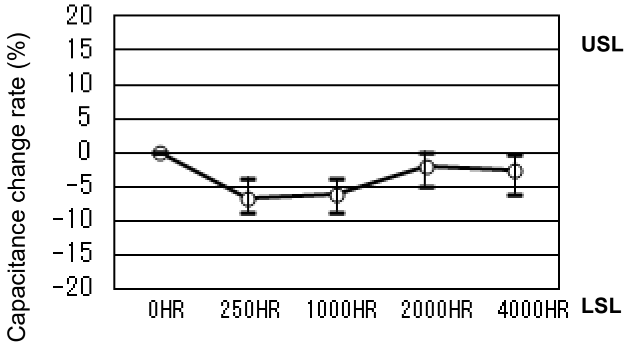
[IR] (+25°C)



[IR] (+125°C)



[Capacitance change rate]



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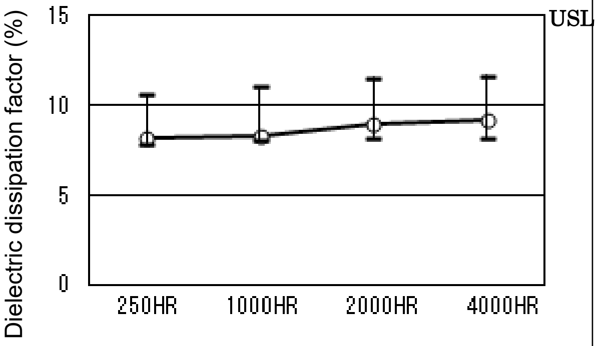
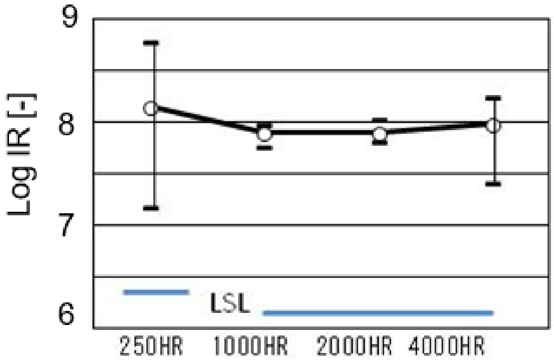
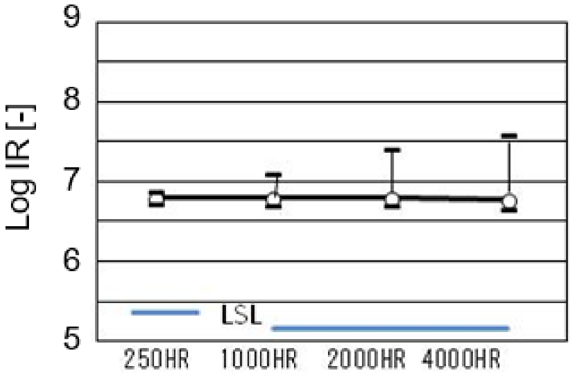


4.3225X7RB226MS

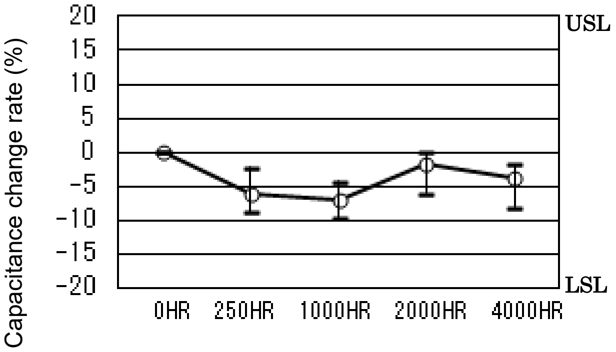
[IR] (+25°C)



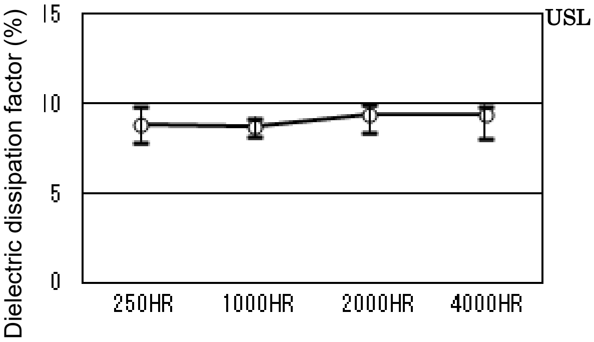
[IR] (+125°C)



[Capacitance change rate]

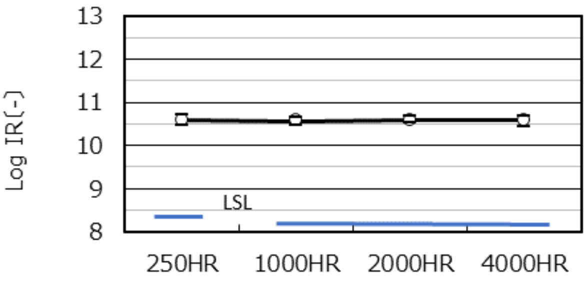


[DF]

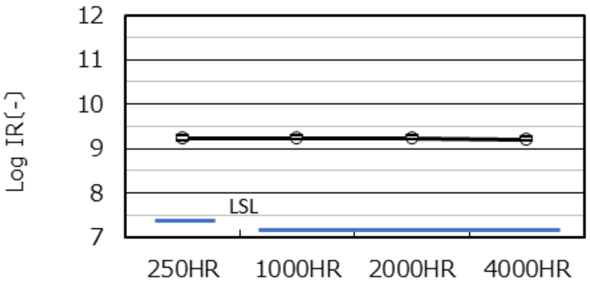


5.1005X7SB104KR

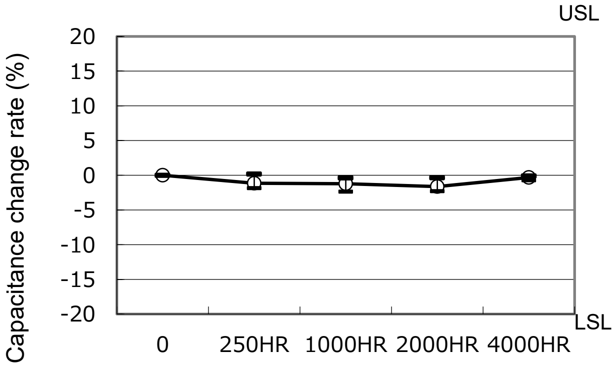
[IR] (+25°C)



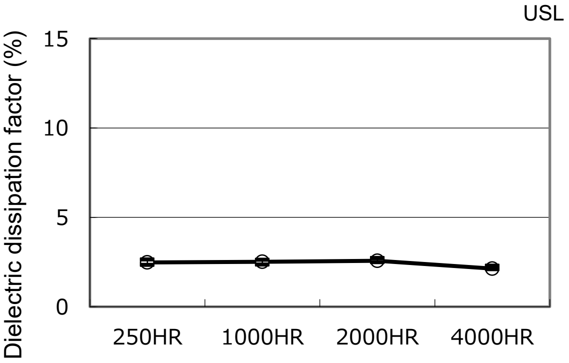
[IR] (+125°C)



[Capacitance change rate]



[DF]



## 6. ENVIRONMENTAL LIMITS

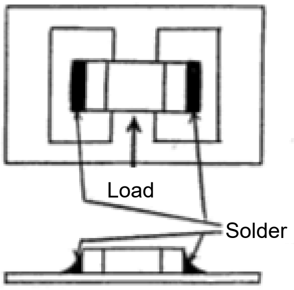
### 6.1 Shear (Destructive)

a) Mounting method

The capacitor was mounted on the test jig shown in the figure below (thickness of 0.635mm±0.05mm or thicker, with a minimum of 95% of Alumina substrate) by the reflow soldering method with Sn60/Pb40 solder. The thickness was adjusted to be between 0.30 and 0.50T (where T = Thickness of the capacitor) for the capacitor with the solder filet thickness of 1005 through 3216, and to be between 0.15 and 0.25T for the capacitor with the filet thickness of 3225 size.

b) Test method

The load was applied to the direction of the arrow in the figure below with the velocity of 30mm/min ± 6mm/min.



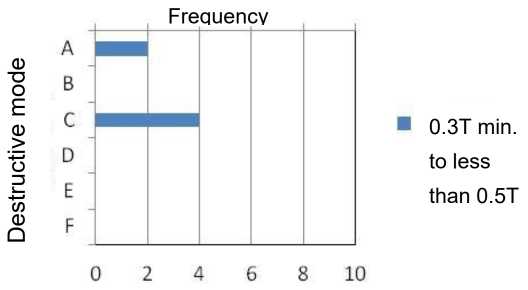
Test jig

| Symbol | Shear mode |
|---|---|
| A | Sheared ceramic |
| B | Separation between ceramic and terminal electrodes |
| C | Sheared solder |
| D1 | Detachment of solder joint (from part surface) |
| D2 | Detachment of solder joint (from board surface) |
| E | Peeling of the land on test board |
| F | Others |

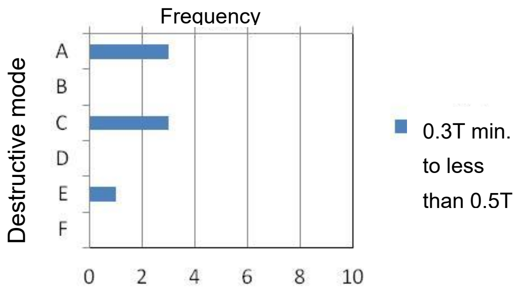
c) Results

[Destructive Mode]

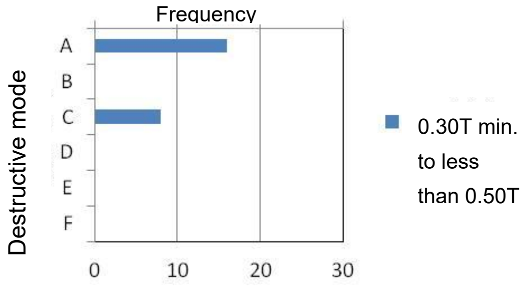
1.1608X7RC104KS



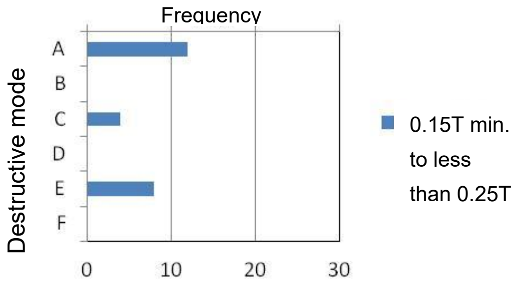
2.1608X7RB105KS



3.3216X7RA226MS



4.3225X7RB226MS



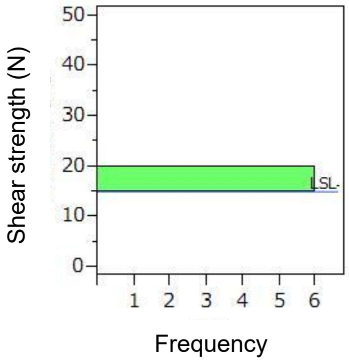
〔piece〕

| | Shear mode symbol | | | | | | |
|---|---|---|---|---|---|---|---|
| Sample | A | B | C | D1 | D2 | E | F |
| 5.1005X7SB104KS | 6 | 0 | 0 | 0 | 0 | 0 | 0 |

[Breakdown strength]

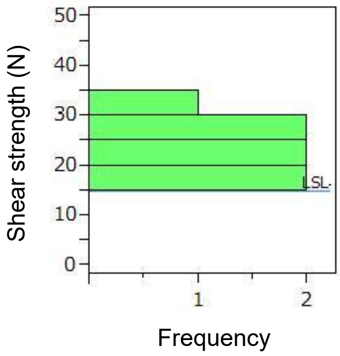
1.1608X7RC104KS (Min. Shear strength: 15N)

0.3T min. to less than 0.5T



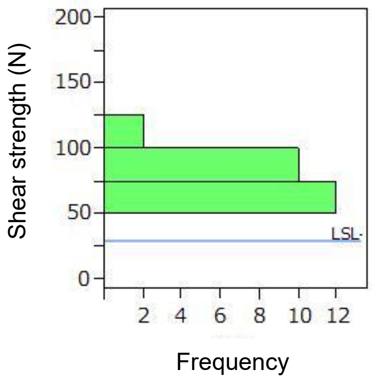
2.1608X7RB105KS (Min. Shear strength: 15N)

0.3T min. to less than 0.5T



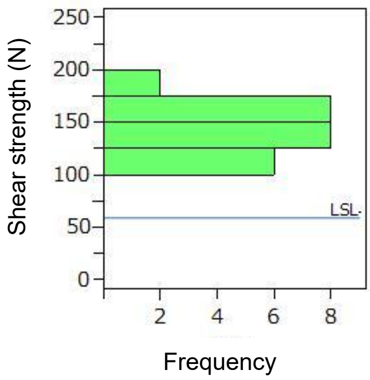
3.3216X7RA226MS (Min. Shear strength: 30N)

0.3T min. to less than 0.5T



4.3225X7RB226MS (Min. Shear strength: 60N)

0.15T min. to less than 0.25T



〔N〕

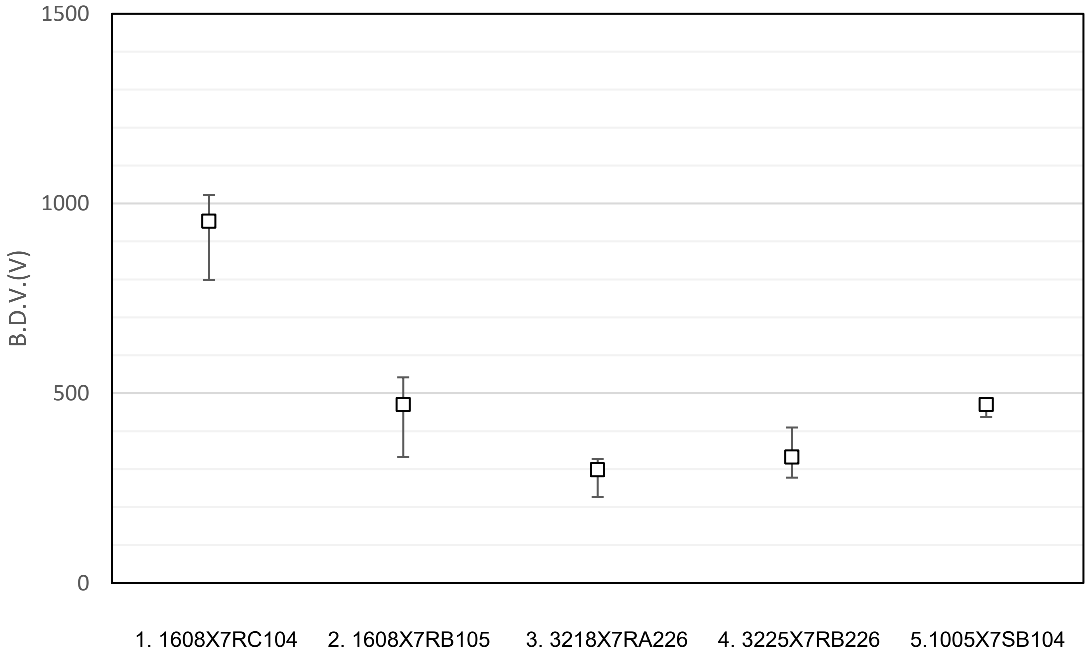
| Sample | Std. | Ave | Max | Min |
|---|---|---|---|---|
| 5.1005X7SB104KS | 5 | 16.42 | 18.9 | 14.1 |

## 6.2 Direct Voltage Breakdown

a) Test method:
Applied voltage was raised by the rate of 12.5V/sec.

b) Sample size: 10 pieces each

c) Results:



〔V〕

| No | 1. | 2. | 3. | 4. | 5. |
|---|---|---|---|---|---|
| Sample size | 10 | 10 | 10 | 10 | 10 |
| Ave | 953 | 470 | 298 | 334 | 470 |
| Max | 1020 | 540 | 330 | 410 | 480 |
| Min | 800 | 330 | 230 | 280 | 440 |

### 6.3 Thermal Shock + PCBT (Pressure cooker Bias Test) (Reference)

The Limit evaluation test by 2000 cycles of thermal shock + PCBT was performed on the chip capacitor for automotive mounted on FR-4.

a) Mount method

The capacitor was mounted on the copper-clad laminate board for glass woven base epoxy resin printed wiring board (thickness: 1.6±0.2mm) by solder reflow method with SAC305 solder.

Solder filet thickness shall be shown in Table 1.

b) Sample and sample size

GCM31CR70J226K (size: 3216, rated value: 22μF, 6.3V)

Unit: piece

| Test item | Sample size | |
|---|---|---|
| | Lot A | Lot B |
| Thermal shock + DPA | 9 | 9 |
| Thermal shock + PCBT | 23 | 23 |

c) Test condition

1) Thermal shock (air)

Test temperature: -55 to +125°C
Soak time: 30 minutes each
Test cycle: 2000 cycles
Limit temperature transition time: within 5 minutes

2) PCBT

Test temperature: +125°C
Relative humidity: 95%RH
Test atomosphere: 2 atomosphere
Applied voltage: Rated voltage
Test duration: 144 hours

d) Results

After the completion of thermal shock test, small crack was found in the external ceramic part of the capacitor. However, the depth of the crack was less than 30μm and it did not reack at the internal electrode. (See images 2 and 3)
During PCBT, the insulation resistance was stabilized at 1MΩ or more and it is confirmed that the reliability of the capacitor was not affected by the small crack.

**Table 1. Filet Thickness (1)**

| No. | Lot A | | | Lot B | | |
|---|---|---|---|---|---|---|
| | Solder filet thickness (mm) | T dimension ratio (2) | Note | Solder filet thickness (mm) | T dimension ratio (2) | Note |
| 1 | 1.195 | 0.650 | See image 2 | 1.314 | 0.714 | |
| 2 | 1.123 | 0.610 | | 1.275 | 0.693 | |
| 3 | 1.203 | 0.654 | | 1.231 | 0.669 | |
| 4 | 1.336 | 0.726 | | 1.219 | 0.662 | See image 3 |
| 5 | 1.063 | 0.578 | | 1.069 | 0.581 | |
| 6 | 1.207 | 0.656 | | 1.051 | 0.571 | |
| 7 | 1.098 | 0.597 | | 1.175 | 0.639 | |
| 8 | 1.189 | 0.646 | See image 1 | 1.211 | 0.658 | |
| 9 | 1.165 | 0.633 | | 1.255 | 0.682 | |
| 10 | 1.266 | 0.688 | | 1.192 | 0.648 | |
| 11 | 1.251 | 0.680 | | 1.131 | 0.615 | |
| 12 | 1.218 | 0.662 | | 1.228 | 0.668 | |
| 13 | 1.252 | 0.680 | | 1.255 | 0.682 | |
| 14 | 1.049 | 0.570 | | 1.264 | 0.687 | |
| 15 | 1.077 | 0.585 | | 1.271 | 0.691 | |
| 16 | 1.279 | 0.695 | | 1.195 | 0.649 | |
| 17 | 1.257 | 0.683 | | 1.281 | 0.696 | |
| 18 | 1.252 | 0.680 | | 1.313 | 0.713 | |
| Ave | 1.193 | 0.649 | | 1.218 | 0.662 | |
| Max | 1.336 | 0.726 | | 1.314 | 0.714 | |
| Min | 1.049 | 0.570 | | 1.051 | 0.571 | |

Notes: (1) The filet thicknesses on 18 samples of PCBT were measured.
(2) The ratio of the solder filet thickness to the thickness of the capacitor (T dimension)

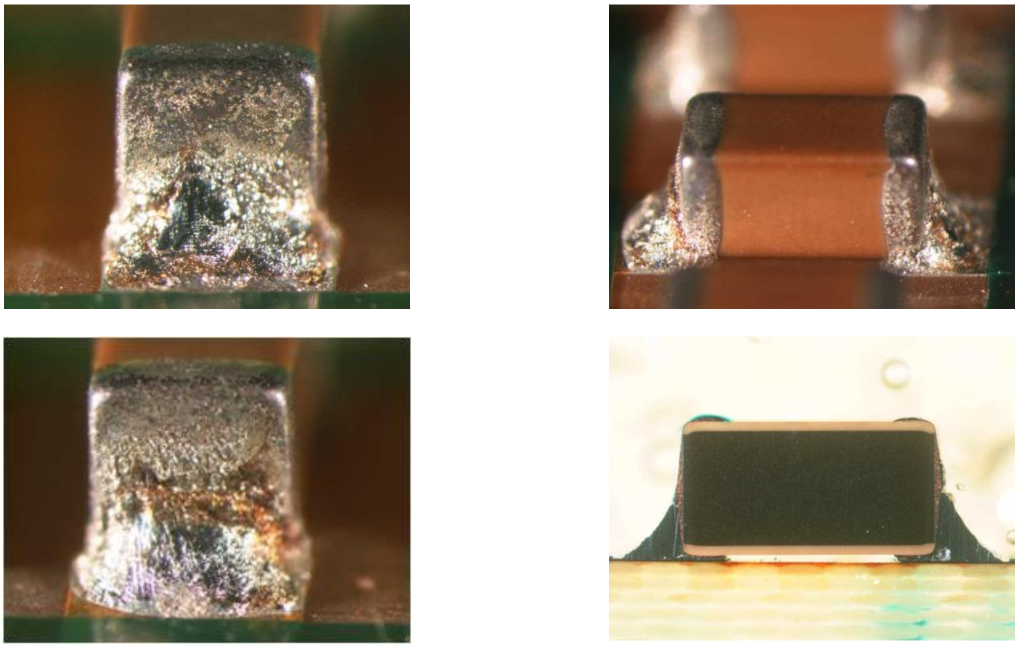
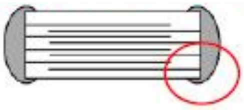


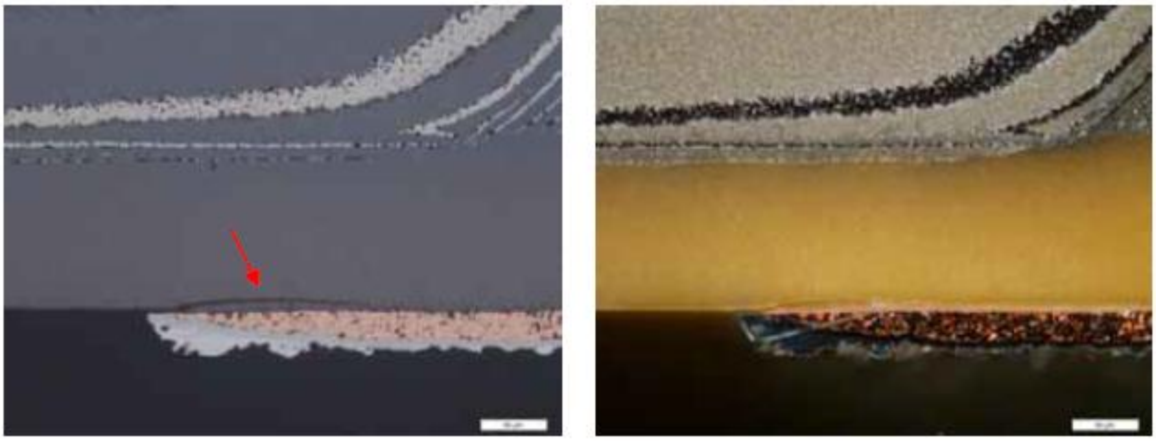
**Image 1. The Mount State of the Capacitor (No. 8 in Lot A)**

→ Center of sample No. 1



Bright field image

Dark field image



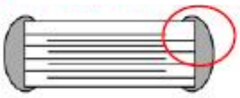
Bright field image

Dark field image

**Image 2. Occurrence of Small Crack (No. 1 of Lot A)**

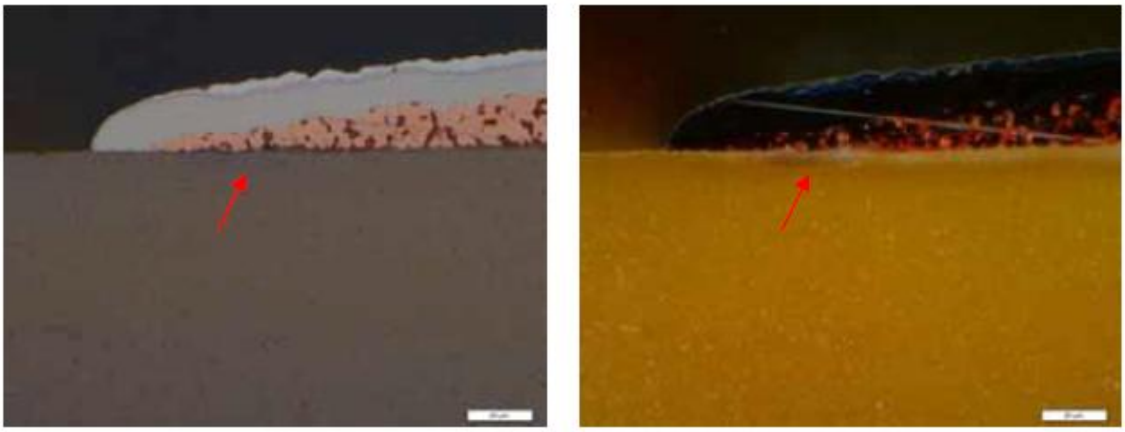
Lot B: An example of small crack images

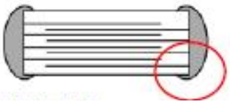
→ Center of sample No. 4



Bright field image

Dark field image





Bright field image

Dark field image

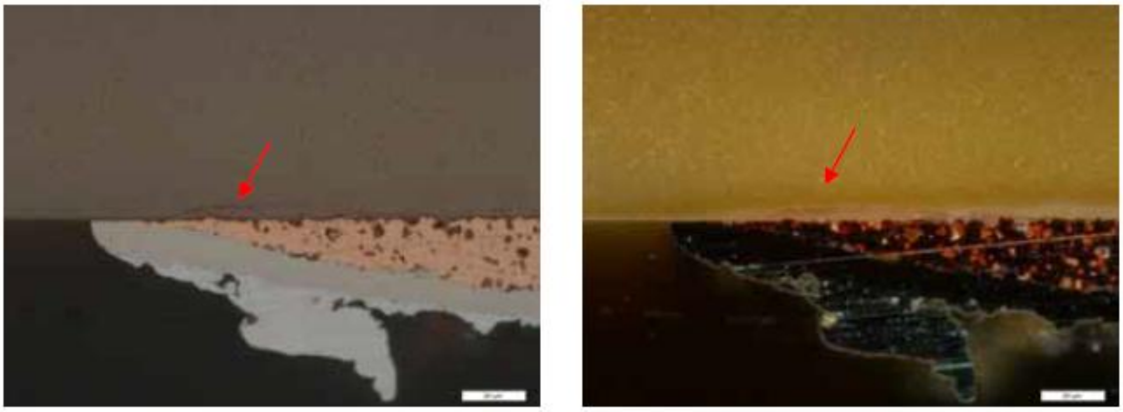


**Image 3. Occurance of Small Crack (No. 4 of Lot B)**

## 7. RELIABILITY

### 7.1 Failure Rates

a) Life test condition and results

| Sample name | | Rating condition (125°C, 1.5WV) | | |
|---|---|---|---|---|
| | | Sample size | Test duration | No. of defectives |
| 1. | 1608X7RC104KS | 123 | 4000 | 0 |
| 2. | 1608X7RB105KS | 123 | 4000 | 0 |
| 3. | 3216X7RA226MS | 123 | 4000 | 0 |
| 4. | 3225X7RB226MS | 123 | 4000 | 0 |
| 5. | 1005X7SB104KR | 123 | 4000 | 0 |

b) Calculation of failure rate

| Sample name | | Component hour (25°C, WV conversion) | Failure rate (Fit) |
|---|---|---|---|
| 1. | 1608X7RC104KS | 3,123,746,087 | 0.294 |
| 2. | 1608X7RB105KS | 3,123,746,087 | 0.294 |
| 3. | 3216X7RA226MS | 3,123,746,087 | 0.294 |
| 4. | 3225X7RB226MS | 3,123,746,087 | 0.294 |
| 5. | 1005X7SB104KR | 3,123,746,087 | 0.294 |

[Remarks]

1. Failure criteria
   Insulation resistance, externals, capacitance change, dielectric dissipation factor (Specifications: As specified in JAXA-QTS-2040)
2. Voltage is accelerated by 4.5 power rule and temperature is accelerated by 10°C rule for converting to the application of rated voltage at 25°C.
3. In the case of no defects, the failure rate shall be as follows. (reliability level: 60%)
   $\lambda = 0.917 / T$ where $\lambda$ : Failure rate
   T : Component hour
   As a result of the calculation, the values in the table above satisfy S level (0.001% / 1000HR = Less than 10Fit)

### 7.2 Possible Failure Modes

Insulation resistance degradation
High capacitance change rate
High dielectric dissipation factor
Decreased solder joint strength
Occurrence of cracks

## 8. STORAGE CONDITIONS

Observe the followings when the products are stored. Special cautions should be used about discoloration of terminal electrodes due to moisture and/or noxious fumes, which deteriorates solderability.

a) Do not open the most internal package (heat sealed plastic bag). If opened, re-heat seal the package immediately or place the product in a desiccator with a drying agent.

b) Keep the storage environments at ambient temperatures of between 5 and 40°C and humidity of between 20 and 70%RH.

c) Keep the storage atmosphere free of noxious gases including sulfur and chlorine.

d) Use high dielectric constant type capacitor as soon as possible as their capacitance gradually decrease due to aging.

## 9. NOTES

### 9.1 Note for Cleaning

Ultrasonic cleaning shall be conducted with chamber output 20W/l as a maximum for 5 minutes as a maximum.

### 9.2 Notes for Resin Coating

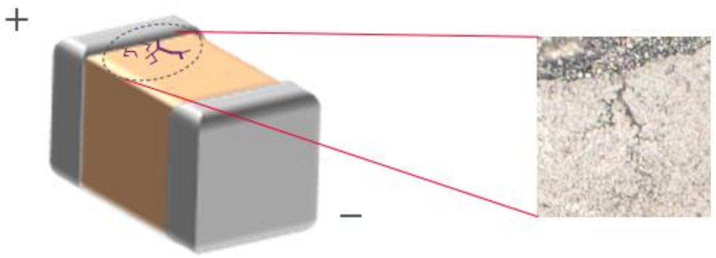
### 9.2.1 Notes

a) Perform resin coating with a moisture-proof material for external insulation after the capacitor is mounted. Use a coating material of the minimum coefficient of thermal expansion.

b) If an improper resin is used, capacitance reduction, degradation of insulation resistance or short-circuiting may be caused due to cracks in the ceramic element and/or detachment of terminal electrodes.

c) If any problem is expected as a result of resin coating, change the coating material or perform buffer coating between the capacitor and the resin with a silicone resin.

d) In environments containing sulfur-based gases, sulfur may react with the silver (Ag) component in the resin electrode, which can lead to dendrite formation between the terminal electrodes. Please use a resin coating material with high sulfur gas barrier properties.



**Locations of Dendrite Formation and Representative Photograph**

### 9.2.2 Relationship between Resin Coating, Life Test Conditions, and Dendrite Formation (Reference)

#### 9.2.2.1 Relationship between Life Test Conditions and Dendrite Formation (Without Resin Coating)

a) Samples and Quantity
1005X7SB104KR (with solder plating, series name: GSX): 18 pieces for each condition
1005X7SB104KJ (without solder plating, series name: GSJ): 18 pieces for each condition

b) Test Conditions
Test temperature: Three levels (85 / 105 / 125°C)
Applied voltage: Three levels (4 / 8 / 12V)
Test duration: 8,000 hours

c) Results
In tests conducted at 105°C or below and under 4V, no dendrite formation was observed up to 8,000 hours, regardless of the presence or absence of the solder plating layer.
At 125°C, dendrites were observed even at 4V. At 12V, connection between terminal electrodes occurred at 6,360 hours. The test was continued until 8,000 hours, and the electrical characteristics (capacitance, dissipation factor, and insulation resistance) remained within the specification range, with no degradation caused by the dendrites.

| Solder plated | | Yes | No |
|---|---|---|---|
| Temperature (°C) | Voltage (V) | GSX | GSJ |
| 85 | 4 | Not occurred | Not occurred |
| 105 | 4 | Not occurred | — |
| 125 | 4 | Occurred | Occurred |
| | 8 | Occurred | — |
| | 12 | Occurred | Occurred |

#### 9.2.2.2 Transition of Electrical Characteristics During Life Test (Without Resin Coating)

a) Samples and Quantity
1005X7SB104KR (with solder plating, series name: GSX): 18 pieces

b) Test Conditions
Test temperature: 125°C
Applied voltage: 12V
Test duration: 8,000 hours

c) Results
Shown on the following page.

Insulation Resistance Transition

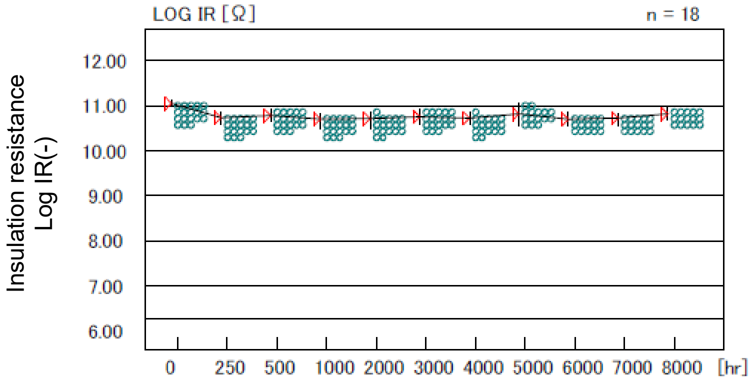


**Table. Change in Log(IR) of the Chip with Dendrite Bridging Between Terminal Electrodes at 6,360 Hours**

| Duration hr | 1000 | 4000 | 5000 | 6000 | 7000 | 8000 |
|---|---|---|---|---|---|---|
| Log IR | 10.65 | 10.67 | 10.85 | 10.56 | 10.56 | 10.74 |

Even after 7,000 and 8,000 hours following dendrite-induced bridging between the terminal electrodes, the insulation resistance met the specification, and no degradation trend was observed.

### 9.2.2.3 Relationship Between Life Test Conditions and Dendrite Formation (With Resin Coating)

a) Samples and Quantity
1005X7SB104KR (with solder plating, GSX series): 18 pieces for each condition

b) Test Conditions
Test temperature: Two levels (105 / 125°C)
Applied voltage: Two levels (4 / 12V)

c) Results
Even under test conditions of 125°C and 12V, no dendrite formation was observed up to 4,000 hours.
After the test, the coating layer was removed and the surface of the element was inspected; no dendrites were detected.

**Table Result of Dendrite Observation After Life Test**

| | | Parylene | | | Uralene |
|---|---|---|---|---|---|
| Temperature (°C) | Voltage (V) | 15um | 25um | 35um | |
| 105 | 4 | Not occurred | Not occurred | Not occurred | Not occurred |
| 125 | 12 | Not occurred | Not occurred | Not occurred | Not occurred |

### 9.3 Note for Tin Whisker

The tin whisker will occur on the products with the terminal finish "Y" in this application data sheet due to the tin plated finish on the external electrodes. Nodule whiskers around

30μm were observed as a result of the thermal shock test (at -30 to +100°C for 1,000 cycles) in the development test. Use caution about tin whisker growth in using terminal finish “Y” products. Whiskers do not grow on terminal finishes “S” and “R”.

### 9.4 DC Bias Characteristics

High-dielectric-constant type capacitors exhibit capacitance variation when a DC voltage is applied.
Before use, select capacitors after considering this DC voltage characteristic.
Since the capacitors use dielectric ceramics that have voltage dependency, the capacitance may greatly vary when the applied DC voltage is high.
In order to ensure the required capacitance, please confirm the following points:

(1) Check that the capacitance variation due to the applied voltage is within the allowable range, or that the application is not affected by such variation.
(2) The DC voltage characteristic shows that, even when the applied voltage is below the rated voltage, the capacitance change rate increases (decreases in value) as the applied voltage increases.
When using high-dielectric-constant capacitors in circuits such as time constant circuits, which require precise capacitance with a narrow tolerance, fully take into account the voltage characteristics, and carefully verify all characteristics under actual operating conditions and in the actual equipment.

### 9.5 AC Voltage Characteristics

High-dielectric-constant capacitors exhibit capacitance variation due to the applied AC voltage.
Before use, select capacitors after considering this AC voltage characteristic.

### 9.6 Others

To cut a PWB populated with capacitors, use a dedicated jig instead of manual cut to prevent breakage due to mechanical shocks.

## 10. OTHERS

For any questions with this data sheet, please contact:
Product Planning Section 1, Product Engineering Department, Sales Promotion Department, Ceramic Capacitor Division,
Fukui Murata Manufacturing Co., Ltd.
Address: 13-1, Okamoto-cho, Echizen-shi, Fukui 915-8601 Japan
Telephone: +81-778-21-8371