COMMON PARTS/MATERIALS, SPACE USE, APPLICATION DATA SHEET FOR

Part Description	Integrated Circuits, Multi-Core Processor, SOI-SOC, CMOS, Monolithic Silicon, High Reliability, Space Use
Part Number and Type	JAXA2010/20101XZR
Applicable Specification	JAXA-QTS-2010 JAXA-QTS-2010/201

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This document is the English version of JAXA QTS/ADS which was originally written and authorized in Japanese and carefully translated into English for international users. If any question arises as to the context or detailed description, it is strongly recommended to verify against the latest official Japanese version.

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Record of revisions

Revision	Date	Description
NC	28 July 2025	Original issued in accordance with VET25310 Revision NC issued by Mitsubishi Heavy Industries, Ltd.
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Revision history

Revision	Date	Description
NC	28 July 2025	Original
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COMMON PARTS/MATERIALS, SPACE USE,
APPLICATION DATA SHEET FOR

1. GENERAL

1.1 Scope

This Application Data Sheet details additional detail information necessary for parts selection and/or equipment design that is not contained in JAXA QML. Users are encouraged to look into other information sources for specific applications, and responsible for their decisions on parts selection and usage.

1.2 Applicable Documents

The documents listed below shall form a part of this document to the extent specified herein. Following revision numbers and/or letter shall be applied.

a)	VET25310	Integrated Circuits, Multi-Core Processor, SOI-SOC, CMOS, Monolithic Silicon, High Reliability, Space Use, Detail Specification for
b)	JAXA-QTS-2010D	Integrated Circuits, High Reliability, Space Use, General Specification for
c)	JAXA-QTS-2000F	Common Parts/Materials, Space Use, General Specification for
d)	MIL-STD-883L	Test Methods Standard – Microcircuits
e)	JERG-0-043E	Standard for Surface Mount Soldering Process for Space Use
f)	JESD22-B115A	SOLDER BALL PULL
g)	JEDEC JESD22-A115C	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM)
h)	ANSI/ESDA/JEDEC JS-002-2018	ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level
i)	J-STD-002E	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

1.3 Reference Documents

(None)

2. SUMMARY OF PRODUCT

2.1 Summary

The functions and performance of the IC specified in this specification are shown in Table 2.1-1.

Table 2.1-1. Functions and Performances (1/3)

Item	Specification	Construction	Summary
Processor core	Renesas RXv3	2 cores	- Operation frequency: 160MHz (Temperature: +125°C, operation voltage: 1.11V, worst path) - Operation frequency: 190MHz (Temperature:+25°C, operation voltage: 1.2V, worst path) - Double-precision FPU support (customized for next-generation MPU)
Core peripheral functions	DMAC (DMA controller)	CPU0：4ch CPU1：4ch	- Equivalent to RX64M product (DMACAa) by Renesas
	DTC (Date transfer controller)	CPU0：1ch CPU1：1ch	- Equivalent to RX64M product (DTCa) by Renesas
	EXDMAC (EXDMA controller)	CPU0：2ch CPU1：－	- Equivalent to RX64M product (EXDMACa) by Renesas - External bus transfer only - However, the following functions are excluded: (1) Transfer to SDRAM (2) Control via external pins (EDREQ and EDACK)
	BSC (Bus controller)	CPU0：1ch CPU1：－	- Equivalent to RX64M product (BSC) by Renesas
	ICU (Interrupt controller)	CPU0：1ch CPU1：1ch	- Renesas RX64M equivalent product (ICUA)
High-speed communication I/F	SpaceWire (SpaceWire communication function)	CPU0/1 shared: 6ch	- Refer to Table 2.1-2. - Support for SpaceWire/RAMP, SpaceWire-PTP and RAW packet
	Ethernet (EthernetAVB communication function)	CPU0/1 shared: 2ch	- Refer to Table 2.1-2.
Low-speed communication I/F	MIL-STD-1553B (MIL-STD-1553B communication function)	CPU0/1 shared: 2ch	- Refer to Table 2.1-2.
	CAN (CAN communication function)	CPU0: 1ch CPU1: 1ch	- Refer to Table 2.1-2.
	Multifunction serial (SCI)	CPU0: Max. 2ch CPU1: Max. 2ch	- Refer to Table 2.1-2. - Shared pins with GPIO
	SPI (SPI communication function)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 2.1-2. - Shared pins with GPIO
	I2C (I2C communication function)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 2.1-2. - Shared pins with GPIO

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Table 2.1-1. Function and Performances (2/3)

Item	Specification	Construction	Summary
Universal I/O	GPIO (Universal input and output)	CPU0/1 shared: Max. 76ch	- Refer to Table 2.1-2. - Shared pins with PWM, SPI, I2C, SCI, TMR and CMTW
	PWM (GPT) (Universal PWM timer)	CPU0: Max. 4ch CPU1: Max. 4ch	- Refer to Table 2.1-2. - Shared pins with GPIO
Timer	TMR (8bit timer)	CPU0: Max. 1ch CPU1: Max. 1ch	- Refer to Table 2.1-2. - Shared pins with GPIO
	OS timer (16/32bit compare match timer)	CPU0: 3ch CPU1: 3ch CPU0/1 shared 2ch	- Refer to Table 2.1-2.
	CMTW (16/32bit compare match timer)	CPU0: Max. 2ch CPU1: Max. 2ch	- Refer to Table 2.1-2. - Shared pins with GPIO
	WDTA (Watchdog timer)	CPU0: 1ch CPU1: 1ch	- Refer to Table 2.1-2.
Processing support	CRC (CRC processing circuit)	CPU0 : 1ch CPU1 : 1ch	- Refer to Table 2.1-2.
	DOC (Data processing circuit)	CPU0 : 1ch CPU1 : 1ch	- Refer to Table 2.1-2.
Internal memory (1)	Code RAM	CPU0/1 shared: 4MByte	- Implemented accelerator and memory scrubber
	Shared memory	CPU0/1 shared: 2MByte	- Implemented accelerator and memory scrubber
	Local RAM	CPU0: 64kByte CPU1: 64kByte	- Implemented memory scrubber (option)
External memory (1)	Universal external bus controller	CPU0: 1ch CPU1: -	- Equivalent to RX64M product (CSC) by Renesas
	SDRAM controller	CPU0: 1ch CPU1: -	- RX64M product (SDRAMC) by Renesas with the following modifications. (1) Added error correction functions (capable of correcting multi-bit errors using Reed-Solomon codes). Note that the function may be enabled or disabled. (2) Expanded the address space to a maximum of 512MB. - Throughput between external SDRAM and internal memory: Minimum 100Mbps
Debug I/F	-	-	- Compatible with Renesas original emulators (E1 emulator).
Boot function	-	-	- After reset, CPU0 acquires the fixed address of the CS1 area as a vector and executes the program. - The following addresses may be switched by configuring the MODE pin (external terminal). (1) CS1 base address (2) 2Mbyte offset (3) 4Mbyte offset
Security		CPU0: 1ch CPU1: 1ch	- Implemented the functions shown in Table 2.1-3. - Supports the equivalent of TSL 1.3 authentication methods.

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Table 2.1-1. Functions and Performances (3/3)

Item	Specification	Construction	Summary
Power consumption	Maximum 1W	-	- Temperature: +25°C, operation voltage: 1.2V, except for external I/O power consumption. - Total power consumption of the MPU (when using 2 cores).
	1.8W (Worst case) (For reference)	-	- Simulation results under worst-case power consumption conditions (manufacturing process: fast corner, temperature: +125°C, VDD voltage: 1.29V, VCCQ voltage: 3.6V, toggle rate: 10%, operating frequency: 160MHz, including I/O power consumption). - Total power consumption of the MPU (when using 2 cores).
Radiation hardness	TID hardness	-	- 100krad (Si)
	SEL hardness	-	- Minimum threshold LET: 75 MeV/(mg/cm^2) (Tj = +125°C)
	SEU hardness	Logic section (Flip-Flop)	- Minimum threshold LET: 40 MeV/(mg/cm^2) - Maximum saturated cross section (Flip-Flop): 2 x 10^{-9} (cm^2/cell)
		Local RAM	- Minimum threshold LET: 40 MeV/(mg/cm^2) (2) (3) - Maximum saturated cross section: 2 x 10^{-9} (cm^2/bit)
		Code RAM and shared memory	- Based on the saturated cross section (9.96x10^{-10}(cm^2/bit)), the Scrubbing Period (4) was calculated from the target threshold LET for each orbit. - The target threshold LET for each orbit and Scrubbing Period are shown in (5).
Package	CBGA, 572-pin		Dimension (nominal): 26mm x 26mm

Notes:

(1) This area may be used for program storage. However, an accelerator for external memory access has not been implemented.

(2) The LET value when the saturated cross section is 1/100th of the saturated cross section without SEU countermeasure.

(3) The value without scrubbing. The ICs have EDAC and scrubbing functions.

(4) The Scrubbing Period is defined as the amount of time required to read, modify and write all memory within the specified range

(5) Refer to the following table.

No.	Target LET Threshold (6) for Each Orbit	Scrubbing Period
1	Equivalent to a LET threshold of ≥ 25 MeV/(mg/cm^2) in the ISS orbit (7)	327680 (seconds)
2	Equivalent to a LET threshold of ≥ 25 MeV/(mg/cm^2) in the GEO orbit (7)	1310 (seconds)

(6) Defined as the results of calculating the LET threshold (the LET value when the saturated cross section is 1/100th of the saturated cross section without SEU countermeasure) using the saturated cross section.

(7) The calculation conditions for orbital flux when calculating the Scrubbing Period are shown below.

- Aluminum shielding thickness: 2.54mm
- Solar activity: Solar min.

Table 2.1-2. List of Peripheral IP Addresses

IP name	Overview	CPU 0		CPU 1		IP specification
		unit	ch	unit	ch	
SpW Engine	SpaceWire communication function	6	6	Shared with CPU0		
SpW Router	SpaceWire Router	2	6	Shared with CPU0		
MIL-STD-1553B	MIL-STD-1553B communication function	2	2	Shared with CPU0		
GPIO	Universal input and output	1	76	Shared with CPU0		
Ethernet (for DualUse)	EthernetAVB communication function	2	2	Shared with CPU0		- Equivalent to RZA1H (EthernetAVB) by Renesas
PWM (GPT)	Universal PWM timer	1	4	1	4	- Equivalent to RX64M product (GPTa) by Renesas
SPI	SPI communication function	1	1	1	1	- Equivalent to RX64M product (RSPIa) by Renesas
Multifunction serial (SCI)	Serial communication function	2	2	2	2	- Equivalent to RX64M product (SCIg) by Renesas
CRC	CRC processing unit	1	1	1	1	- Equivalent to RX64M product (CRC) by Renesas
DOC	Data processing unit	1	1	1	1	- Equivalent to RX64M product (DOC) by Renesas
WDTA	Watchdog timer	1	1	1	1	- Equivalent to RX64M product (WDTA) by Renesas
OS timer	16/32 bit compare match timer	5 (1)	5 (1)	5 (1)	5 (1)	- Equivalent to RX64M product (CMTW) by Renesas Note (1): Two of the five channels share CPU0/CPU1.
CMTW	16/32 bit compare match timer	2	2	2	2	- Equivalent to RX64M product (CMTW) by Renesas
TMR	8bit timer	1	1	1	1	- Equivalent to RX64M product (TMR) by Renesas
CAN	CAN communication function	1	1	1	1	- Equivalent to RX64M product (CAN) by Renesas
I2C(RIIC)	I2C communication function	1	1	1	1	- Equivalent to RX64M product (RIICa) by Renesas
CPG	Clock source circuit	1	1	-	-	

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Table 2.1-3. Security Functions and Cryptographic Performances

Major Function Item	Minor Function Item	Function Summary
Encryption and decryption function	Data encryption function	Function for encrypting data and generating signature and authentication codes
	Encrypted communication function	Function for keeping the contents of communication data confidential from third parties
	Classified information management function	Function for restricting access to confidential information
Falsification prevention and detection function	Destination authentication function	Function for inhibiting communication with unknown parties
	Software authentication function	Function for inhibiting the operation of unauthorized software
	Countermeasures for flaw exploitation attacks	Function for preventing leakage of confidential information due to out of specification operation
Cryptographic Performance		
Security level indicator: 128-bit security		

2.2 Externals and Dimensions

The package configuration and dimensions are shown in Figure 2-1. The marking details are specified in Figure 2-2.

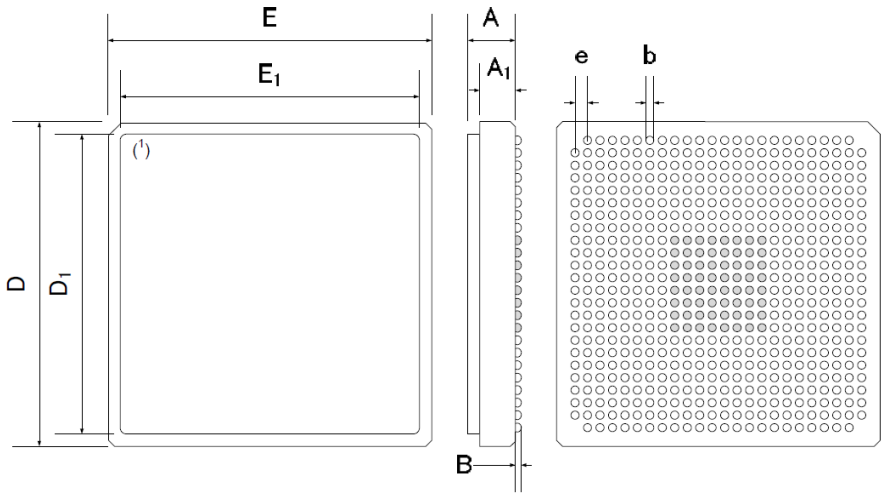
2.3 Mass

Mass (Reference value): 7.6g to 12.0g (Typ. 9.7g) (1)

Note (1): Design values were calculated based on mass variations in the ceramic package and other components. For reference, the mass variation (actual results) for three assembly lots is 9.5g to 9.8g.

2.4 Element Construction

Type of the IC is a hermetically sealed Ball Grid Array type, incorporating a single CMOS die within a ceramic package, sealed with a Fe-Ni-Co alloy lid using seam welding. The element construction is shown in Figure 2-3.



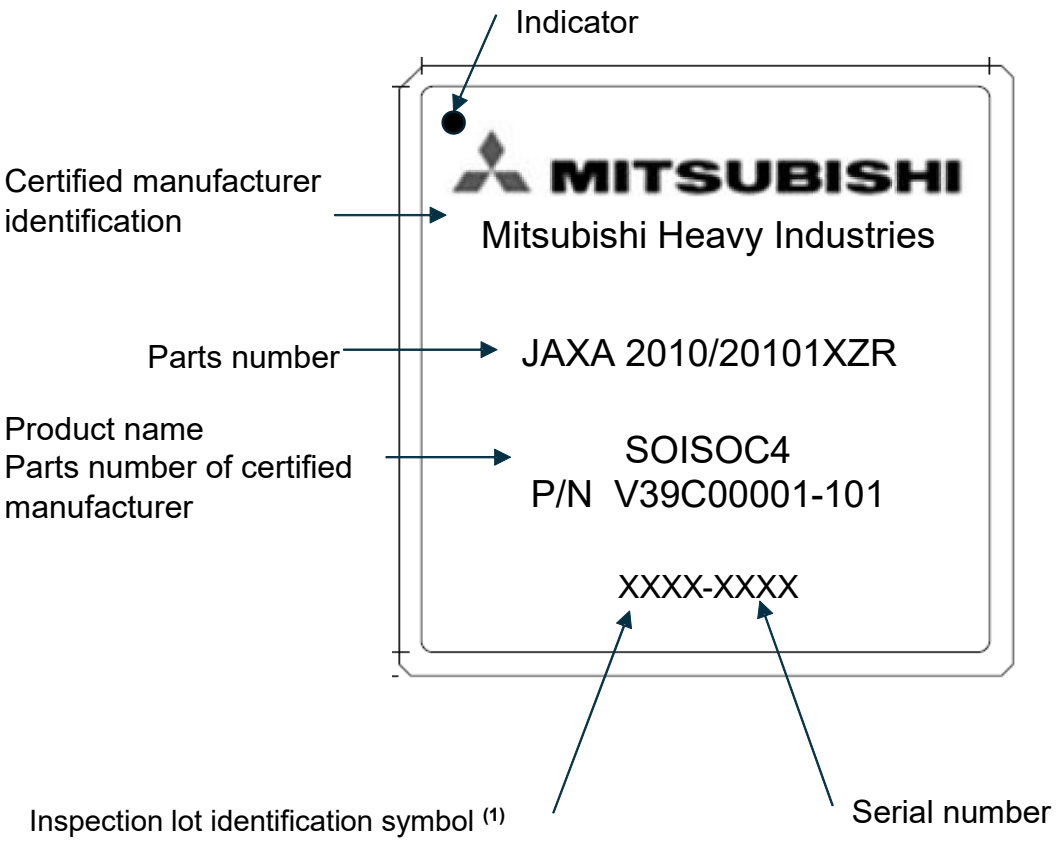
- Package material: Ceramic, Fe-Ni-Co alloy
- Solder terminal material: Sn10/Pb90 (central 8x8 solder balls),
  Sn63/Pb37 (perimeter solder balls)

Unit: mm

Symbol	Dimensions		Notes
	Min.	Max.	
A	3.45	4.15	
A_1	2.55	3.15	
B	0.40	0.60	
b	0.60	0.80	(2)
D	25.80	26.20	
D_1	24.00	24.40	(3)
E	25.80	26.20	
E_1	24.00	24.40	(3)
e	1.00 standard		(2)

Notes:
(1) Indicator area
(2) Shall be applied to all terminals.
(3) Lid misalignment and seam ring brazing shall be included.

Figure 2-1. Package Configuration

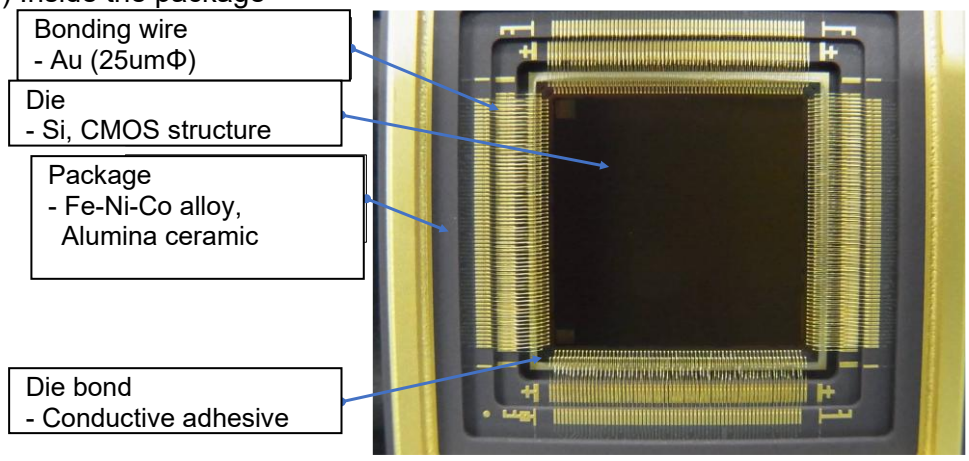


Note: (1) Four-digit numbers consisting of the las two digits of the year and two digits for the month in which assembly began shall be printed. For example, for assembly in June 2023, “2306” shall be printed.

Figure 2-2. Marking

(a) IC Surface

(b) Inside the package



(c) IC back surface

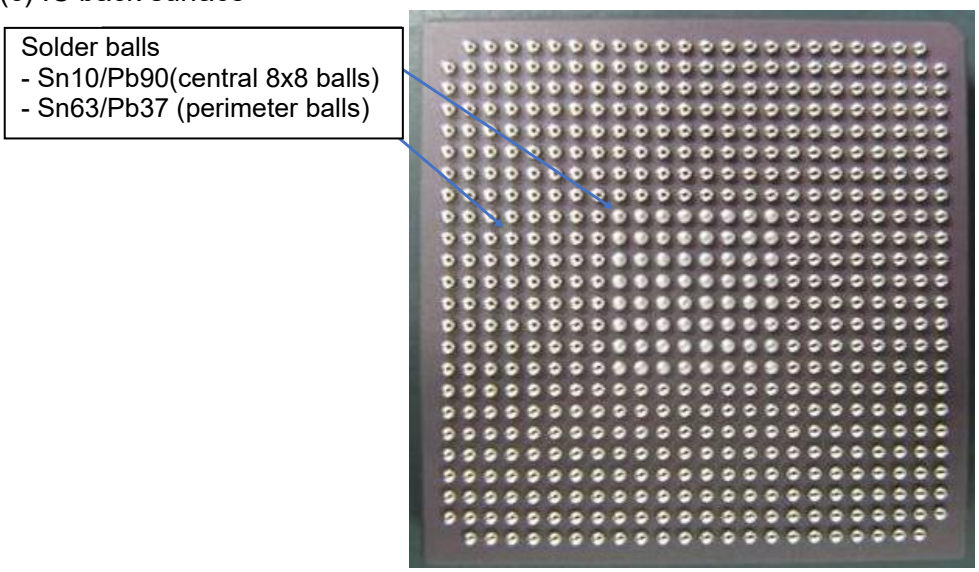


Figure 2-3. Element Construction Summary

3. USAGE

3.1 Absolute Maximum Ratings

Absolute maximum ratings are shown in Table 3-1.

Table 3-1. Absolute Maximum Ratings

Item		Symbol	Min.	Max	Unit
Power supply voltage		V_{CCQ}	-0.3	4.6	V
		V_{DD}	-0.3	1.4	V
Input voltage ([1])		V_{in}	-0.3	V_{CCQ} +0.3	V
Output voltage		V_O	-0.3	V_{CCQ} +0.3	V
Output current	8mA buffer	$I_{O(8mA)}$	-90	86	mA
	24mA buffer	$I_{O(24mA)}$	-266	267	mA
Storage temperature		T_{stg}	-55	+150	°C
Junction temperature		T_j	-40	+125	°C

Note: ([1]) Shall not exceed +4.6V.

3.2 Recommended Operating Conditions

Recommended operating conditions are shown in Table 3-2.

Table 3-2. Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max	Unit
Power supply voltage range		V_{CCQ}	3.0	3.3	3.6	V
		V_{DD}	1.11	1.2	1.29	V
High level input voltage		V_{IH}	0.7 x V_{CCQ}	-	VCCQ + 0.3	V
Low level input voltage		V_{IL}	-0.3	-	0.2 x V_{CCQ}	V
Operating board surface temperature		T_b([1])	-37([5])	-	+120	°C
Operating junction temperature		T_j ([2])	-40([6])	-	+125	°C
External clock frequency	When the PLL on the chip is used	f_{extclk}	-	20	-	MHz
	When the PLL on the chip is not used		-	100	-	MHz

Notes:

[(1)] Defined as the temperature at the board surface (directly beneath the chip edge).

[(2)] T_J is calculated as follows.

$T_J = T_b + \theta_{j\text{-}b} \times P_D$

Where,

T_b: Operating board surface temperature (°C)

$\theta_{j\text{-}b}$: Standard thermal resistance between the junction and board (1.8°C/W) (3)

P_D: Power dissipation (1.8W) (4)

(3) Defined as the thermal resistance calculated in the simulation between “the junction and board surface (directly beneath the chip edge)”. Simulation results of thermal resistance are shown in Table 3-3.

For reference, the thermal resistance $\Theta_{j\text{-}c}$ calculated in the simulation between “the junction and case (seal ring section)” is 7.1°C/W. Thermal design shall be performed to ensure that the absolute maximum rating T_{jmax} is not exceeded.

(4) Simulation results under the worst-case power consumption conditions (manufacturing process: fast corner, temperature: 125°C, V_{DD}: 1.29V, V_{CCQ}: 3.6V, toggle rate: 10%, operation frequency: 160MHz, including I/O power consumption).

(5) Specified as the upper limit value for the test conditions of the package.

(6) Specified as the upper limit value for the test conditions of the wafer.

Table 3-3. Thermal Resistance

Items		Thermal resistance	Unit
Junction – Board surface	Center of the chip	0.8	°C/W
	Edge of the chip	1.8	°C/W
Junction –top surface of seal ring		7.1	°C/W

3.3 Precautions for Circuit Design

(None).

3.4 Recommended Installation Method

For circuit design, it is recommended to design with sufficient margin relative to the absolute maximum ratings. It is preferable to operate within the recommended operating range.

4. PERFORMANCE CHARACTERISTICS IN NORMAL CONDITIONS

4.1 Electrical Characteristics

a) Electrical characteristics
For electrical characteristics, DC characteristics are shown in Table 4-1. AC characteristics are shown in Table 4-2.

b) System block diagram
The system block diagram is shown in Figure 4-40.

c) Pin configuration
The pin configuration is shown in Figure 4-41 and Table 4-3.

Table 4-1. Electrical Characteristics (DC Characteristics)
(VCCQ=3.3±0.3V、VDD=1.2±0.09V、Tb=-37°C to +120°C)

Items		Symbol	Min.	Max	Unit	Conditions
Input voltage		V_{IL}	-	0.2 x VCCQ	V	-
		V_{IH}	0.7 x VCCQ	-	V	-
Input leak		I_{IL}	-0.6	0.6	uA	-
		I_{IH}	-0.6	0.6	uA	-
Output voltage	8mA buffer	$V_{OL(8mA)}$	-	0.4	V	I_{OL}=8mA
	24mA buffer	$V_{OL(24mA)}$	-	0.4	V	I_{OL}=24mA
	8mA buffer	$V_{OH(8mA)}$	0.8 x VCCQ	-	V	I_{OH}=8mA
	24mA buffer	$V_{OH(24mA)}$	0.8 x VCCQ	-	V	I_{OH}=24mA

Table 4-2. Electrical Characteristics (AC characteristics) (1/13) (Power-on Sequence)
(VCCQ=3.3±0.3V, VDD=1.2±0.09V, Tb=-37°C to +120°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Timing chart (3)
External signal (EXT_CLK) clock cycle	t_{cyc}	-	50(1) 10(2)	-	ns ns	Figures 4-1 and 4-2
Reset release time (Time from power supply voltage stabilization to reset release)	t_{PLL_RST}	1	-	-	ms	
External signal (PLL_SEL) hold time	t_{PLL_SEL}	3	-	-	t_{cyc}	
PLL lock up time	t_{PLL_LUP}	-	-	50	us	
Internal reset release time	t_{RST}	-	1024	-	t_{cyc}	

Notes: (1) When the internal PLL is used.
(2) When the internal PLL is not used.
(3) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Table 4-2. Electrical Characteristics (AC characteristics) (2/13) (CS Function)

(VCCQ=3.3±0.3V, VDD=1.2±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart(1)
Address delay time	t_{AD}	2.8	15.4	ns	Figures 4-3 to 4-8
Byte control delay time	t_{BCD}	2.8	15.4	ns	
CS# delay time	t_{CSD}	2.8	15.4	ns	
ALE delay time	t_{ALED}	2.8	15.4	ns	
RD# delay time	t_{RSD}	2.8	15.4	ns	
Read-data setup time	t_{RDS}	12.78	-	ns	
Read-data hold time	t_{RDH}	3	-	ns	
WR# delay time	t_{WRD}	2.8	15.4	ns	
Write-data delay time	t_{WDD}	1.7	15.4	ns	
Write-data hold time	t_{WDH}	2.8	-	ns	
WAIT# setup time	t_{WTS}	12.78	-	ns	Figure 4-9
WAIT# hold time	t_{WTH}	3	-	ns	
Address delay time 2 (SDRAM)	t_{AD2}	2.8	15.4	ns	Figures 4-10 to 4-12
CS# delay time 2 (SDRAM)	t_{CSD2}	2.8	15.4	ns	
DQM delay time (SDRAM)	t_{DQMD}	2.8	15.4	ns	
CKE delay time (SDRAM)	t_{CKED}	2.8	15.4	ns	
Read-data setup time 2 (SDRAM)	t_{RDS2}	12.78	-	ns	
Read-data hold time 2 (SDRAM)	t_{RDH2}	3	-	ns	
Write-data delay time 2 (SDRAM)	t_{WDD2}	1.7	15.4	ns	
Write-data hold time 2 (SDRAM)	t_{WDH2}	2.8	-	ns	
WE# delay time (SDRAM)	t_{WED}	2.8	15.4	ns	
RAS# delay time (SDRAM)	t_{RASD}	2.8	15.4	ns	
CAS# delay time (SDRAM)	t_{CASD}	2.8	15.4	ns	

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Table 4-2. Electrical Characteristics (AC characteristics) (3/13) (SYSTEM Function)

(VCCQ=3.3±0.3V、VDD=1.2±0.09V、Tb=-37°C to +120°C)

Item	Symbol	Min.	Max.	Unit	Timing chart (1)
NMI pulse width	t_{NMIOUT}	200	-	ns	Figure 4-13
IRQ pulse width	t_{IRQOUT}	200	-	ns	Figure 4-14

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 4-2. Electrical Characteristics (AC characteristics) (4/13) (JTAG Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart(1)
TCK clock high-level pulse width	t_{TCKH}	45	-	ns	Figure 4-15
TCK clock low-level pulse width	t_{TCKL}	45	-	ns	
TCK clock rise time	t_{TCKr}	-	5	ns	
TCK clock fall time	t_{TCKf}	-	5	ns	
TRST# pulse width	(t_{TRSTW})	20	-	ns	Figure 4-16
TMS setup time	t_{TMSS}	20	-	ns	Figure 4-17
TMS hold time	t_{TMSH}	20	-	ns	
TDI setup time	t_{TDIS}	20	-	ns	
TDI hold time	t_{TDIH}	20	-	ns	
TDO data delay time	t_{TDOD}	0	40	ns	

Note: (1) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 4-2. Electrical Characteristics (AC characteristics) (5/13) (Ethernet Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart(1)
ET_TXCLK cycle time	t_{Tcyc}	40	-	ns	Figures 4-18 to 4-22
ET_TXCLK high level width	t_{TCKWH}	0.35×t_{Tcyc}	-	ns	
ET_TXCLK low level width	t_{TCKWL}	0.35×t_{Tcyc}	-	ns	
EX_TXEN output delay time	t_{TEND}	0	25	ns	
ET_TXD[3:0] output delay time	t_{TDD}	0	25	ns	
ET_RXCLC cycle time	t_{Rcyc}	40	-	ns	
ET_RXCLK high level width	t_{RCKWH}	0.35×t_{Rcyc}	-	ns	
ET_RXCLK low level width	t_{RCKWL}	0.35×t_{Rcyc}	-	ns	
ET_RXDV setup time	t_{RDVS}	10	-	ns	
ET_RXDV hold time	t_{RDVH}	10	-	ns	
ET_RXD[3:0] setup time	t_{RDDS}	10	-	ns	
ET_RXD[3:0] hold time	t_{RDDH}	10	-	ns	
ET_RXER setup time	t_{RERS}	10	-	ns	
ET_RXER hold time	t_{RERH}	10	-	ns	
AVB_GPTP_EXTERN cycle time	t_{Gcyc}	40	-	ns	
AVB_GPTP_EXTERN high level width	t_{GCKWH}	0.35×t_{Gcyc}	-	ns	
AVB_GPTP_EXTERN low level width	t_{GCKWL}	0.35×t_{Gcyc}	-	ns	
AVP_CAPTURE high level width	t_{CAPWH}	2×t_{Gcyc}	-	ns	
ET_CRS setup time	t_{CAPWH}	2×t_{Ccyc}		ns	Figure 4-23
ET_CRS hold time	t_{CRSs}	10	-	ns	
ET_COL setup time	t_{CRSh}	10	-	ns	Figure 4-24
ET_COL hold time	t_{COLs}	10	-	ns	

Note: (1) The timing voltage threshold of t_{Tcyc}, t_{Rcyc} and t_{Gcyc} shall be set to "V_{CCQ} × 0.5".
Other timing voltage thresholds shall be "V_{OH}=0.7xV_{CCQ}, V_{OL}=0.3xV_{CCQ}, V_{IH}=0.7xV_{CCQ} and V_{IL}=0.3xV_{CCQ}".

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Table 4-2. Electrical Characteristics (AC characteristics) (6/13) (GPT Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart(2)
Input capture input pulse width (single edge designation)	t_{GTICW1}	3	-	t_{PAcyc} (1)	Figure 4-25
Input capture input pulse width (both edges designation)	t_{GTICW2}	5	-	t_{PAcyc} (1)	
External trigger input pulse width (single edge designation)	t_{OTETW1}	1.5	-	t_{PAcyc} (1)	Figure 4-26
External trigger input pulse width (both edges designation)	t_{OTETW2}	2.5	-	t_{PAcyc} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Table 4-2. Electrical Characteristics (AC characteristics) (7/13) (TMR Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart(2)
Timer clock input pulse width (single edge designation)	t_{TMCWH}	1.5	-	t_{PBcyc} (1)	Figure 4-27
Timer clock input pulse width (both edges designation)	t_{TMCWL}	2.5	-	t_{PBcyc} (1)	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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Table 4-2. Electrical Characteristics (AC characteristics) (8/13) (RSPI Function(1/2))
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
RSPCK clock cycle (master)	t_{SPcyc1}	2	4096	t_{PAcyc} (1)	Figure 4-28
RSPCK clock cycle (slave)	t_{SPcyc2}	8	4096	t_{PAcyc} (1)	
RSPCK clock high level pulse width (master)	t_{SPCKWH}	(t_{SPcyc1}-t_{SPCKr}-t_{SPCKf})/2-3	-	ns	
RSPCK clock high level pulse width (slave)	t_{SPCKWH}	(t_{SPcyc2}-t_{SPCKr}-t_{SPCKf})/2	-	ns	
RSPCK clock low level pulse width (master)	t_{SPCKWL}	(t_{SPcyc1}-t_{SPCKr}-t_{SPCKf})/2-3	-	ns	
RSPCK clock low level pulse width (slave)	t_{SPCKWL}	(t_{SPcyc2}-t_{SPCKr}-t_{SPCKf})/2		ns	
RSPCK clock rise / fall time (output) (3)	t_{SPCKr}, t_{SPCKf}	-	5	ns	
RSPCK clock rise / fall time (input)	t_{SPCKr}, t_{SPCKf}	-	1	μs	
Data input setup time (master)	t_{SU}	6	-	ns	Figures 4-29 to 4-34
Data input setup time (slave)	t_{SU}	8.3-t_{PAcyc} (1)	-	ns	
Data Input Hold Time (Master, PCLKA set to divide-by-2)	t_{HF}	0	-	ns	
Data Input Hold Time (Master, PCLKA set to a value other than divide-by-2)	t_H	t_{PAcyc}	-	ns	
Data input hold time (slave)	t_H	8.3+2×t_{PAcyc} (1)	-	ns	
SS input setup time (master)	t_{LEAD}	1	8	t_{SPcyc1}	
SS input setup time (slave)	t_{LEAD}	4	-	t_{PAcyc} (1)	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples.

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Table 4-2. Electrical Characteristics (AC characteristics) (8/13) (RSPI Function(2/2))
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SS input hold time (master)	t_{LAG}	1	8	t_{SPcyc1}	Figure 4-29 to 4-34
SS input hold time (slave)	t_{LAG}	4	-	t_{PAcyc} (1)	
Data output delay time (master)	t_{OD}	-	6.3	ns	
Data output delay time (slave)	t_{OD}	-	$3\times t_{PAcyc}+20$	ns	
Data output hold time (master)	t_{OH}	0	-	ns	
Data output hold time (slave)	t_{OH}	0	-	ns	
Continuous transmission delay time (master)	t_{TD}	t_{SPcyc1} $+2\times t_{PAcyc}$	$8\times t_{SPcyc1}$ $+2\times t_{PAcyc}$	ns	
Continuous transmission delay time (slave)	t_{TD}	$4\times t_{PAcyc}$	-	ns	
MOSI rise / fall time (master) (3)	t_{Dr}, t_{Df}	-	5	ns	
MISO rise / fall time (slave)	t_{Dr}, t_{Df}	-	1	μs	
SS input rise / fall time (output) (3)	t_{SSLr}, t_{SSLf}	-	5	ns	
SS input rise / fall time (input)	t_{SSLr}, t_{SSLf}	-	1	μs	
Slave access time	t_{SA}	-	4	t_{PAcyc} (1)	Figure 4-33
Slave output release time	t_{REL}	-	3	t_{PAcyc} (1)	Figure 4-34

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples.

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Table 4-2. Electrical Characteristics (AC characteristics) (9/13) (Simple SPI Function(SCIF))
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance=73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SCK clock cycle output (master)	t_{SPcyc1}	4	65536	t_{PAcyc} (1)	Figure 4-28
SCK clock cycle input (slave)	t_{SPcyc2}	6	65536	t_{PAcyc} (1)	
SCK clock high level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock low level pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock rise time (3)	t_{SPCKr}	-	5	ns	
SCK clock fall time (3)	t_{SPCKf}	-	5	ns	
Data input setup time (master)	t_{SU}	15	-	ns	Figures 4-29 to 4-32
Data input setup time (slave)	t_{SU}	5	-	ns	
Data input hold time	t_{H}	5	-	ns	
SS input setup time	t_{LEAD}	1	-	t_{SPcyc1} t_{SPcyc2}	
SS input hold time	t_{LAG}	1	-	t_{SPcyc1} t_{SPcyc2}	
Data output delay time (master)	t_{OD}	-	5	ns	
Data output delay time (slave)	t_{OD}	-	25	ns	
Data output hold time	t_{OH}	-5	-	ns	
Data rise time (3)	t_{Dr}	-	5	ns	
Data fall time (3)	t_{Df}	-	5	ns	
SS input rise time (3)	t_{SSLr}	-	5	ns	
SS input fall time (3)	t_{SSLf}	-	5	ns	
Slave access time	t_{SA}	-	3 xt_{Pcyc} +25	t_{PAcyc} (1)	Figure 4-33
Slave output release time	t_{REL}	-	3 xt_{Pcyc} +25	t_{PAcyc} (1)	Figure 4-34

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples.

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Table 4-2. Electrical Characteristics (AC characteristics) (10/13) (Simple SPI Function(SCI))
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
SCK clock cycle output (master)	t_{SPcyc1}	4	65536	t_{PBcyc} (1)	Figure 4-28
SCK clock cycle output (slave)	t_{SPcyc2}	8	65536	t_{PBcyc} (1)	
SCK clock high level pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock low level pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc1} t_{SPcyc2}	
SCK clock rise time (3)	t_{SPCKr}	-	20	ns	
SCK clock fall time (3)	t_{SPCKf}	-	20	ns	
Data input setup time	t_{SU}	33.3	-	ns	Figures 4-49 to 4-32
Data input hold time	t_H	33.3	-	ns	
SS input setup time	t_{LEAD}	1	-	t_{SPcyc1} t_{SPcyc2}	
SS input hold time	t_{LAG}	1	-	t_{SPcyc1} t_{SPcyc2}	
Data output delay time	t_{OD}	-	33.3	ns	
Data output hold time	t_{OH}	-10	-	ns	
Data rise time (3)	t_{Dr}	-	16.6	ns	
Data fall time (3)	t_{Df}	-	16.6	ns	
SS input rise time (3)	t_{SSLr}	-	16.6	ns	
SS input fall time (3)	t_{SSLf}	-	16.6	ns	
Slave access time	t_{SA}	-	5	t_{PBcyc} (1)	Figure 4-33
Slave output release time	t_{REL}	-	5	t_{PBcyc} (1)	Figure 4-34

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples.

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Table 4-2. Electrical Characteristics (AC characteristics) (11/13) (SCIF Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input clock cycle phase-locked synchronization	t_{Scyc1}	4	-	t_{PAcyc} (1)	Figure 4-35
Input clock cycle clock synchronization	t_{Scyc2}	6	-	t_{PAcyc} (1)	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Input clock rise time	t_{SCKr}	-	5	ns	
Input clock fall time	t_{SCKf}	-	5	ns	
Output clock cycle phase-locked synchronization	t_{Scyc1}	8	-	t_{PAcyc} (1)	
Output clock cycle clock synchronization	t_{Scyc2}	4	-	t_{PAcyc} (1)	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Output clock rise time(3)	t_{SCKr}	-	5	ns	
Output clock fall time(3)	t_{SCKf}	-	5	ns	
Transmission data delay time master	t_{TXD1}	-	5	ns	Figure 4-36
Transmission data delay time slave	t_{TXD2}	-	25	ns	
Received data setup time master	t_{rxs1}	15	-	ns	
Received data setup time slave	t_{rxs2}	5	-	ns	
Received data hold time master	t_{RXH1}	5	-	ns	
Received data hold time slave	t_{RXH2}	5	-	ns	

Note: (1) t_{PAcyc}: PCLKA cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples.

Table 4-2. Electrical Characteristics (AC characteristics) (12/13) (SCI Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input clock cycle phase-locked synchronization	t_{Scyc1}	4	-	t_{PBcyc} (1)	Figure 4-37
Input clock cycle clock synchronization	t_{Scyc2}	6	-	t_{PBcyc} (1)	
Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Input clock rise time	t_{SCKr}	-	5	ns	
Input clock fall time	t_{SCKf}	-	5	ns	
Output clock cycle phase-locked synchronization	t_{Scyc1}	8	-	t_{PBcyc} (1)	
Output clock cycle clock synchronization	t_{Scyc2}	4	-	t_{PBcyc} (1)	
Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc1} t_{Scyc2}	
Output clock rise time(3)	t_{SCKr}	-	5	ns	
Output clock fall time(3)	t_{SCKf}	-	5	ns	
Transmission data delay time clock synchronization	t_{TXD}	-	28	ns	Figure 4-38
Received data setup time clock synchronization	t_{rxs}	15	-	ns	
Received data hold time clock synchronization	t_{RXH}	5	-	ns	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

Note: (3) Based on the results of the characteristic evaluation test confirming that the parameters are within process levels with sufficient margin, tests shall not be performed on all samples".

Table 4-2. Electrical Characteristics (AC characteristics) (13/13) (CMTW Function)
(V_{CCQ}=3.3V±0.3V, V_{DD}=1.2V±0.09V, Tb=-37°C to +120°C, Output load capacitance =73pF)

Item	Symbol	Min.	Max.	Unit	Timing chart (2)
Input capture input pulse width single edge designation	$t_{CMTWTICW1}$	1.5	-	t_{PBcyc} (1)	Figure 4-39
Input capture input pulse width both edges designation	$t_{CMTWTICW2}$	2.5	-	t_{PBcyc} (1)	

Note: (1) t_{PBcyc}: PCLKB cycle

Note: (2) The timing voltage threshold shall be set to "V_{CCQ} × 0.5". When different voltage threshold is applied, it shall be shown in the notes of the timing chart.

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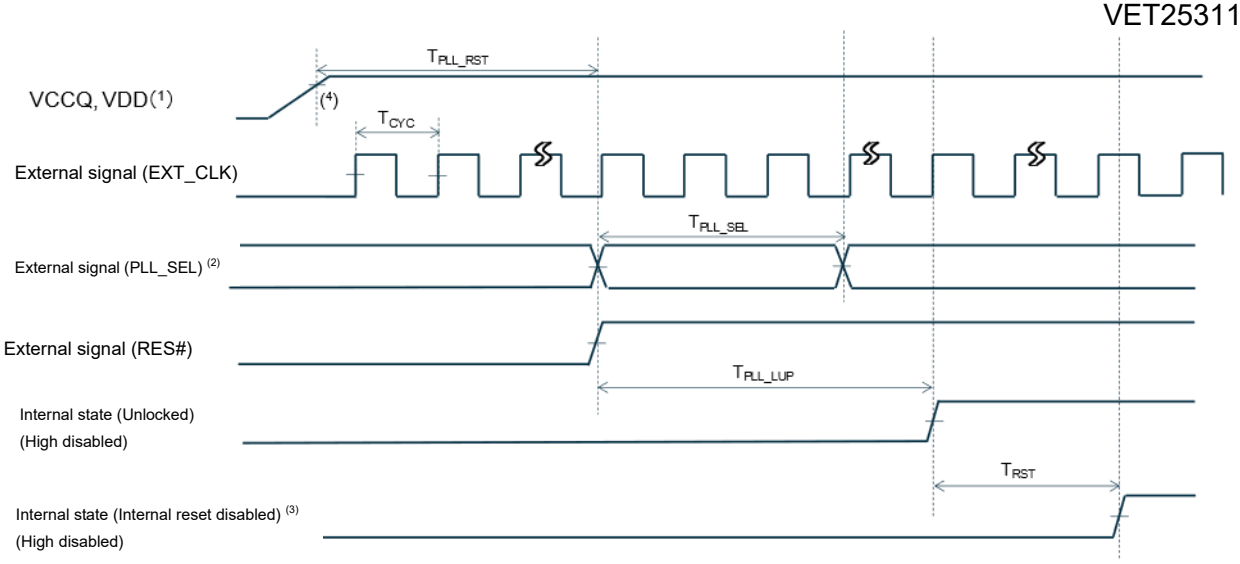


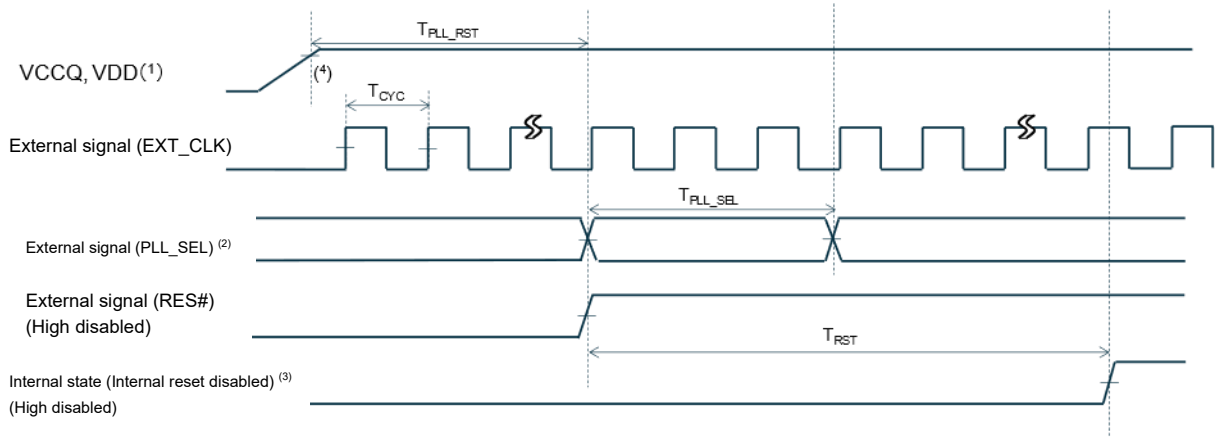
Notes (1): The recommended power-on sequence is to activate the internal logic power supply VDD (1.2V) first, followed by the I/O power supply VCCQ (3.3V), or to activate them simultaneously.

(2): The value shall be maintained for at least T_{PLL_SEL} periods after the rise of the external signal (RES#). Setting the value before the rise of the external signal (RES#) is acceptable.

(3): After internal reset is disabled, access to the CS area shall start approximately 25 internal clock cycles later.

(4): T_{PLL_RST} shall be based on the time when the power supply voltage stabilizes within the recommended operating conditions power supply voltage range specified in Table 2.

Figure 4-1. Power-on Sequence Timing (using internal PLL)



Notes (1): The recommended power-on sequence is to activate the internal logic power supply VDD (1.2V) first, followed by the I/O power supply VCCQ (3.3V), or to activate them simultaneously.

(2): The value shall be maintained for at least T_{PLL_SEL} periods after the rise of the external signal (RES#). Setting the value before the rise of the external signal (RES#) is acceptable.

(3): After internal reset is disabled, access to the CS area shall start approximately 25 internal clock cycles later.

(4): T_{PLL_SEL} shall be based on the time when the power supply voltage stabilizes within the recommended operating conditions power supply voltage range specified in Table 2.

Figure 4-2. Power-on Sequence Timing (not using internal PLL)

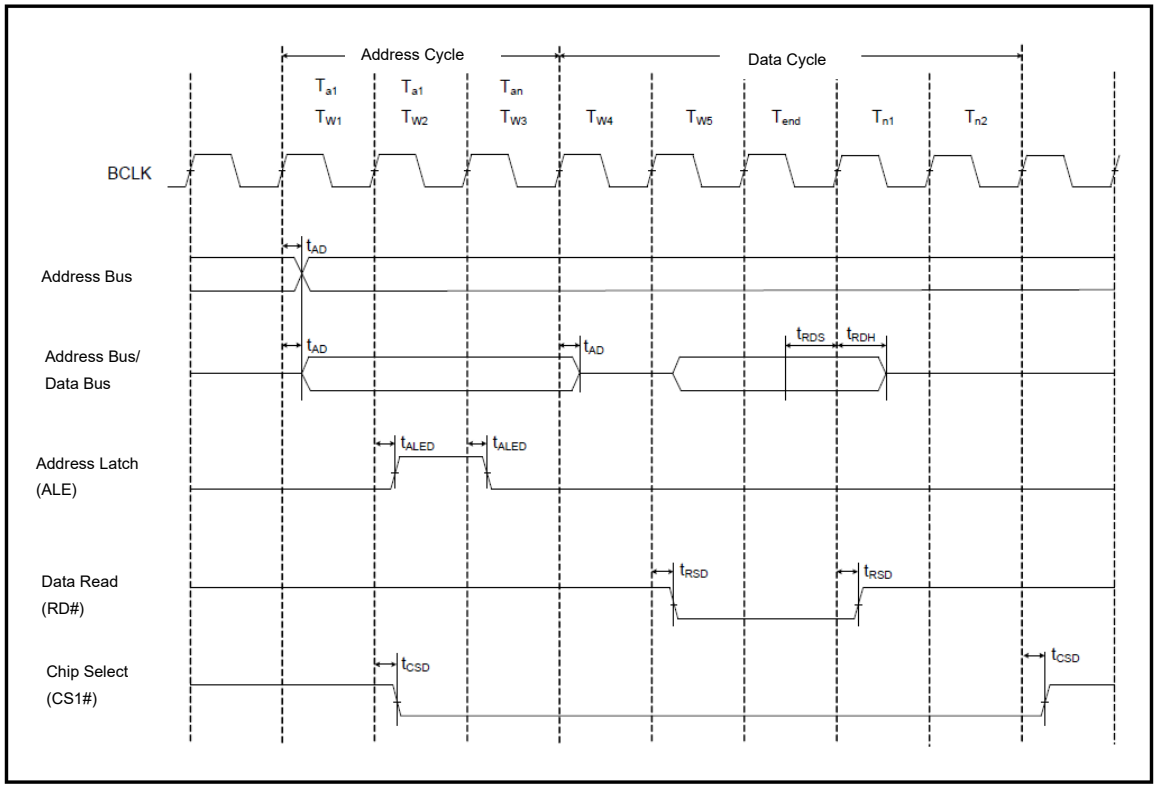


Figure 4-3. Read Access Timing of Address / Data Multiplex Bus

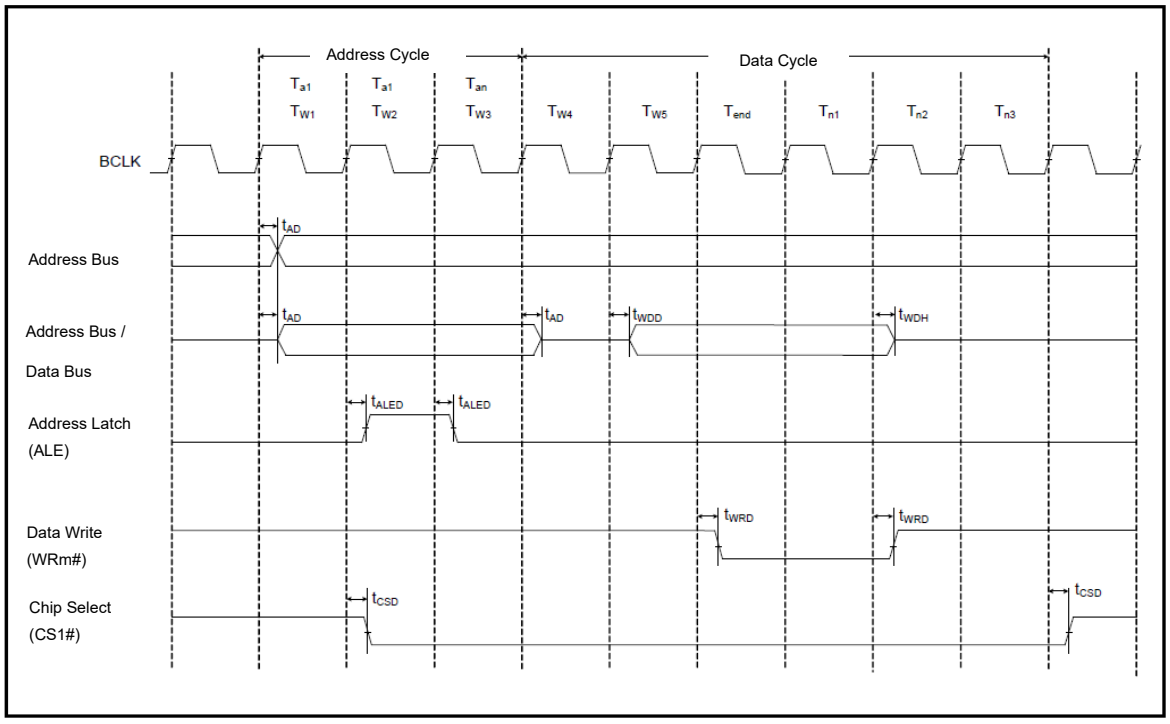


Figure 4-4. Write Access Timing of Address / Data Multiplex Bus

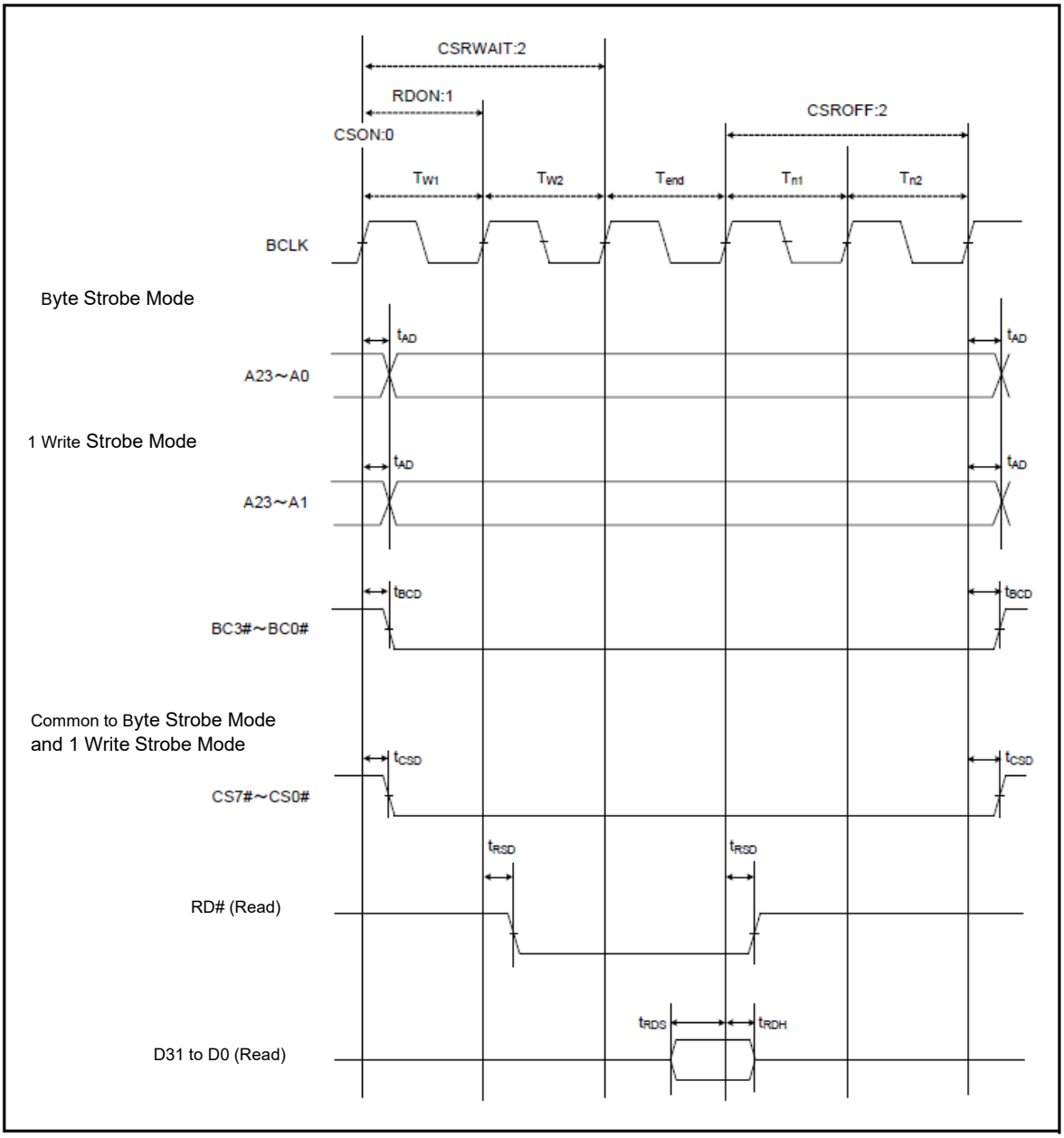
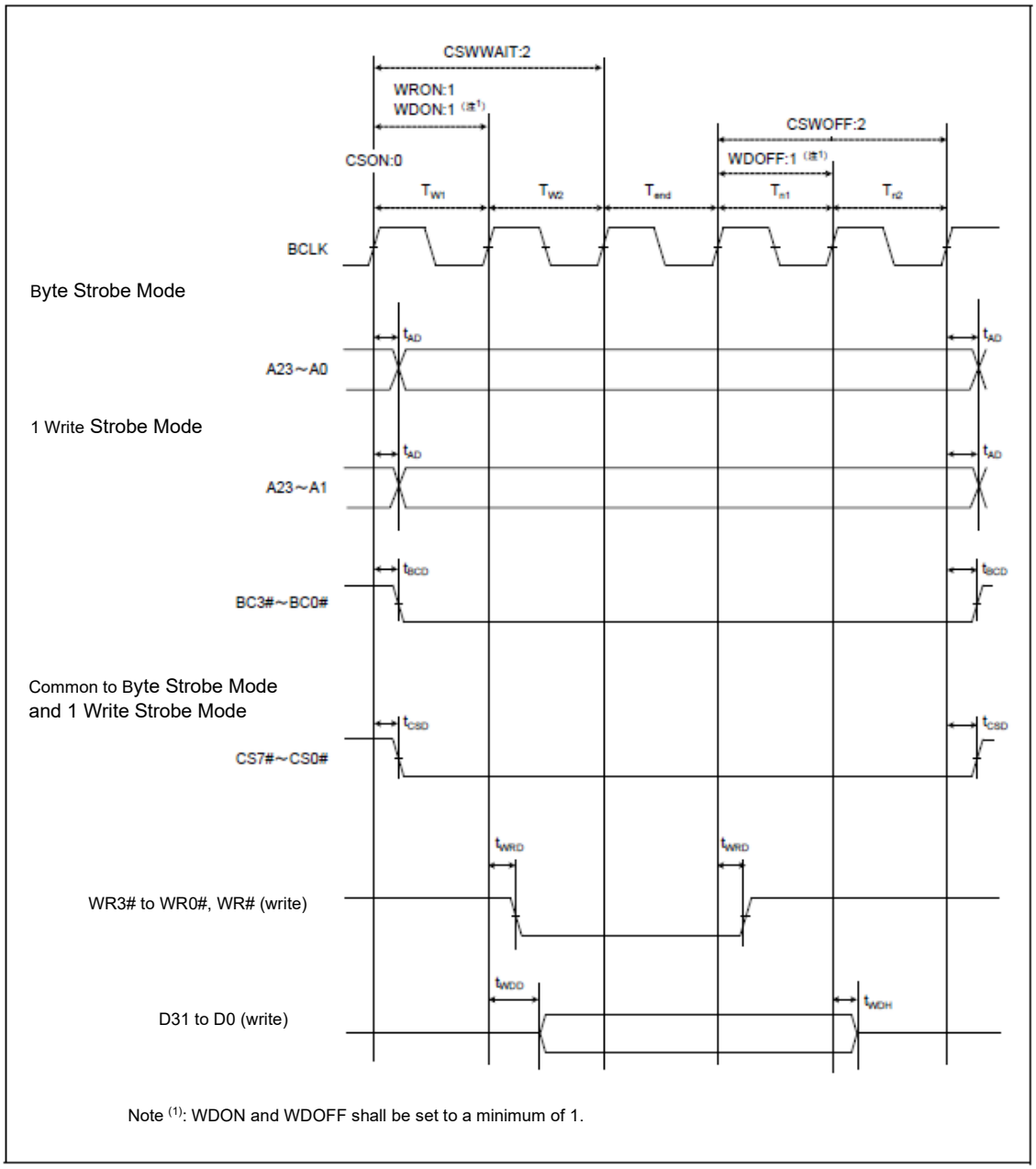


Figure 4-5. External Bus Timing / Normal Read Cycle (Bus Clock Synchronization)



Note (1): WDON and WDOFF shall be set to a minimum of 1.

Figure 4-6. External Bus Timing / Normal Write Cycle (Bus Clock Synchronization)

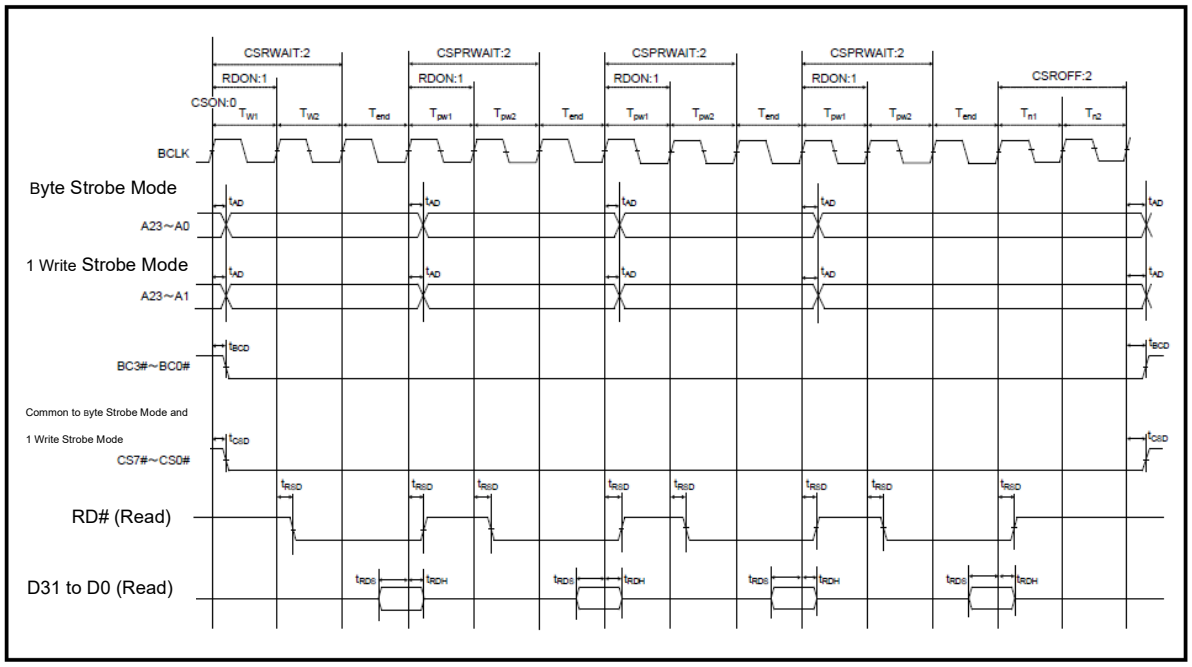


Figure 4-7. External Bus Timing / Page Read Cycle (Bus Clock Synchronization)

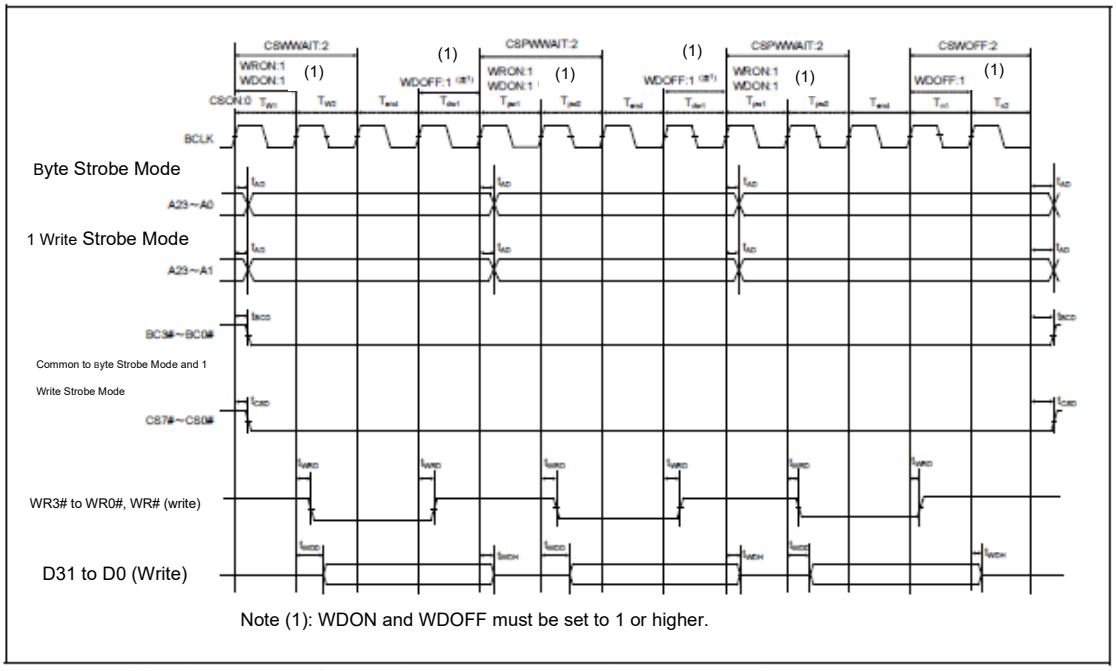


Figure 4-8. External Bus Timing / Page Write Cycle (Bus Clock Synchronization)

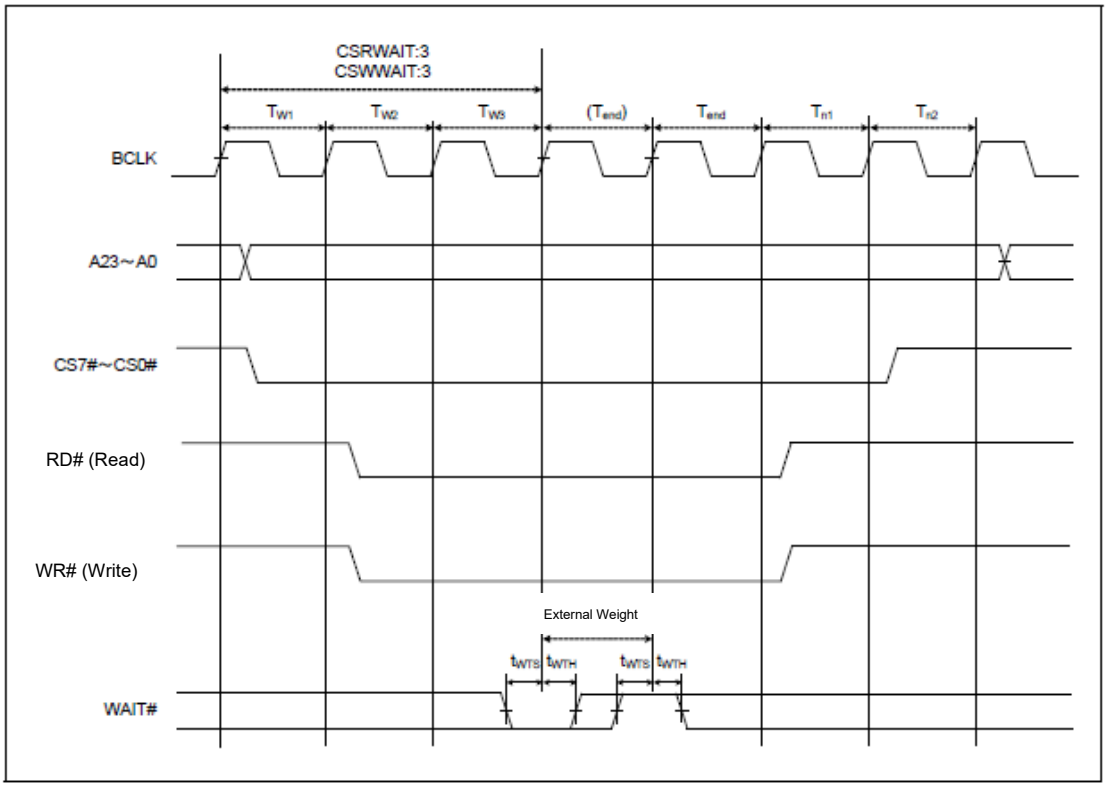
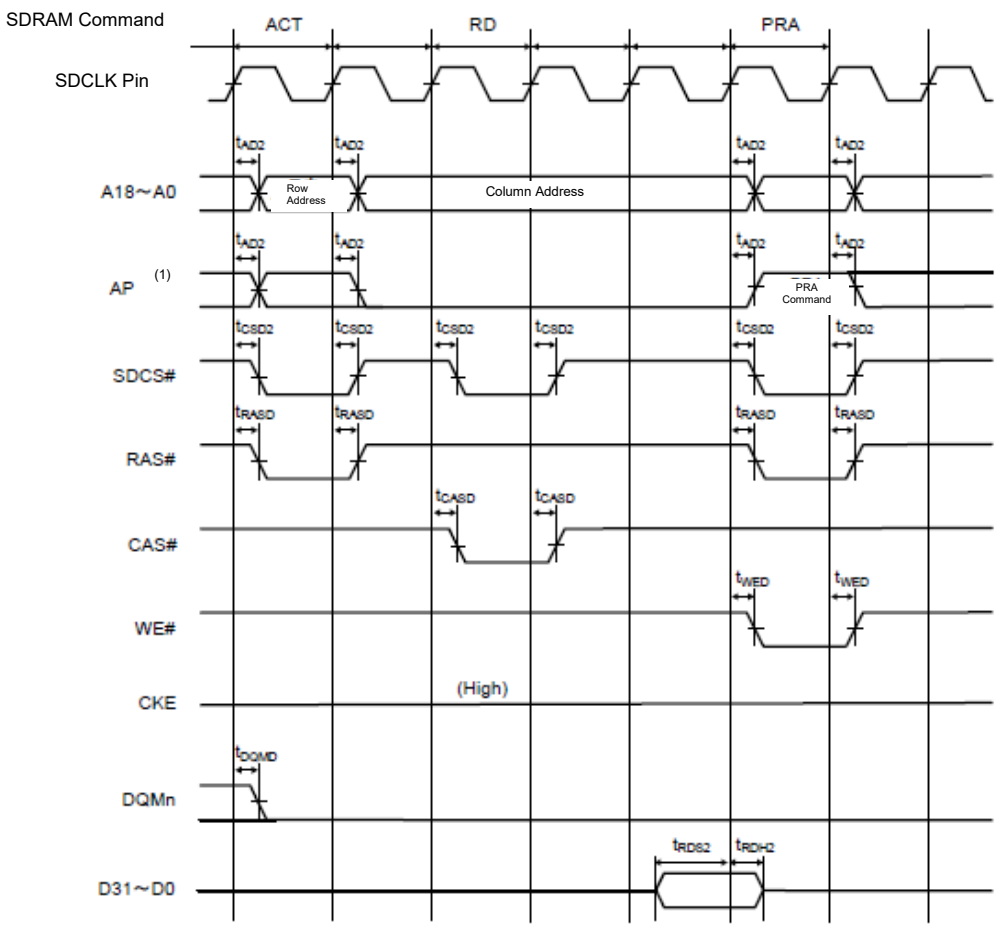
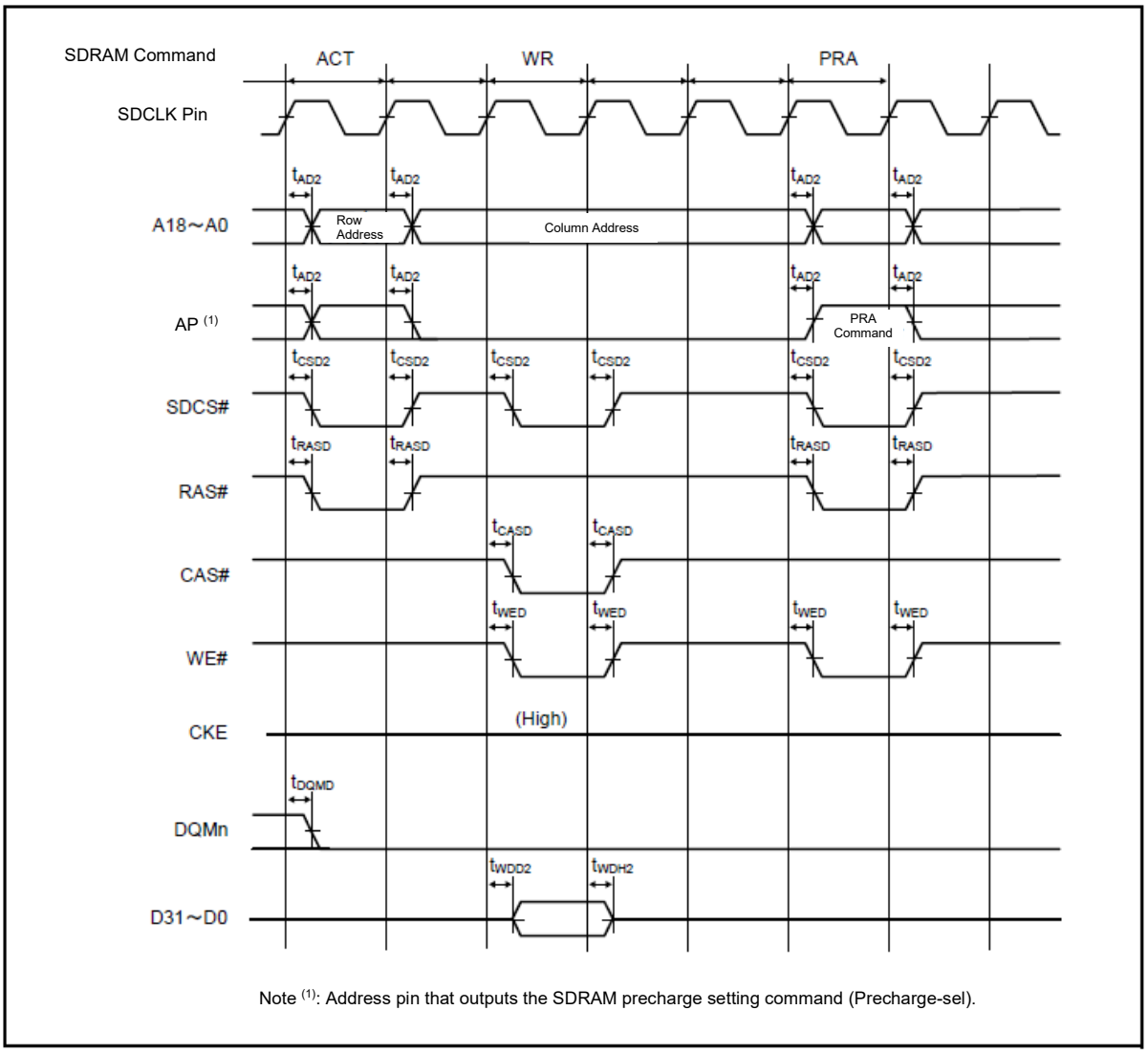


Figure 4-9. External Bus Timing / External Weight Control



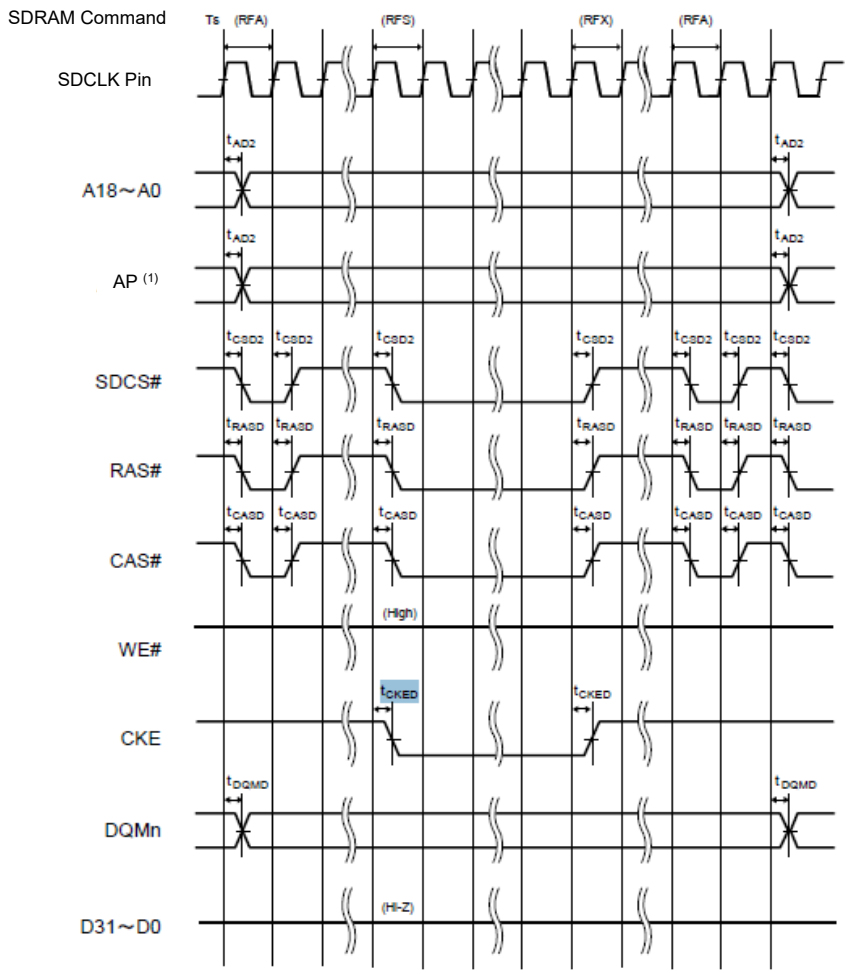
Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 4-10. SDRAM Space Single Read Bus Timing



Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 4-11. SDRAM Space Single Write Bus Timing



Note (1): Address pin that outputs the SDRAM precharge setting command (Precharge-sel).

Figure 4-12. SDRAM Space Self Refresh Bus Timing

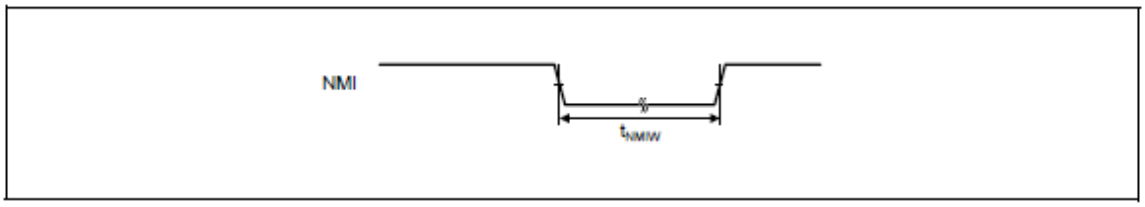


Figure 4-13. NMI Interrupt Input Timing

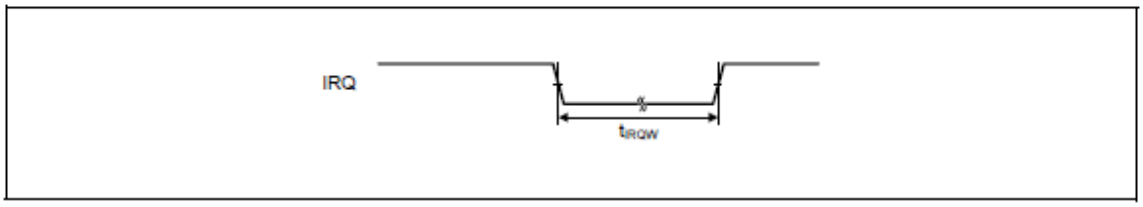


Figure 4-14. IRQ Interrupt Input Timing

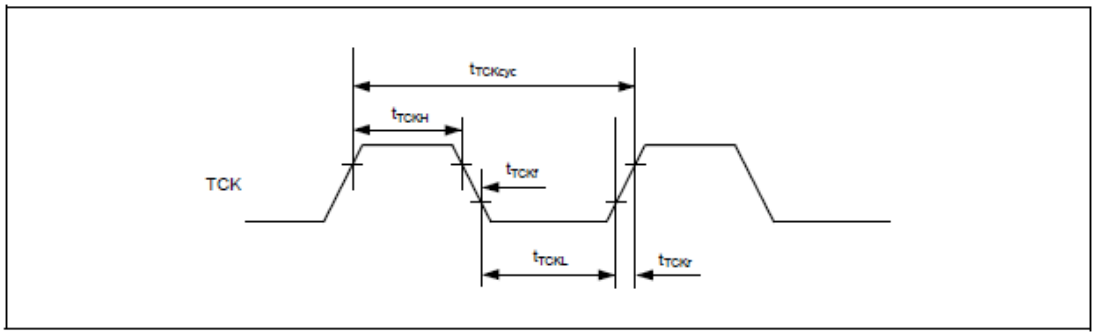


Figure 4-15. Boundary Scan TCK Timing c

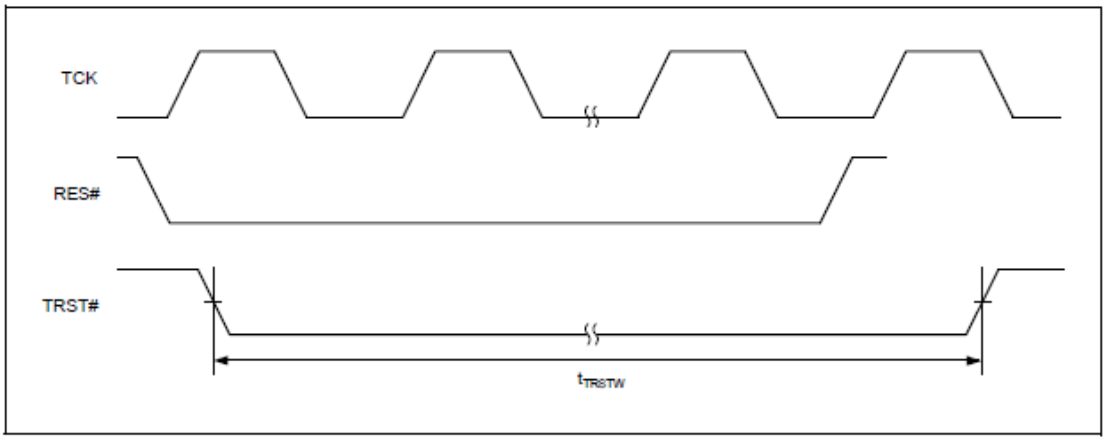


Figure 4-16. Boundary Scan TRST Timing

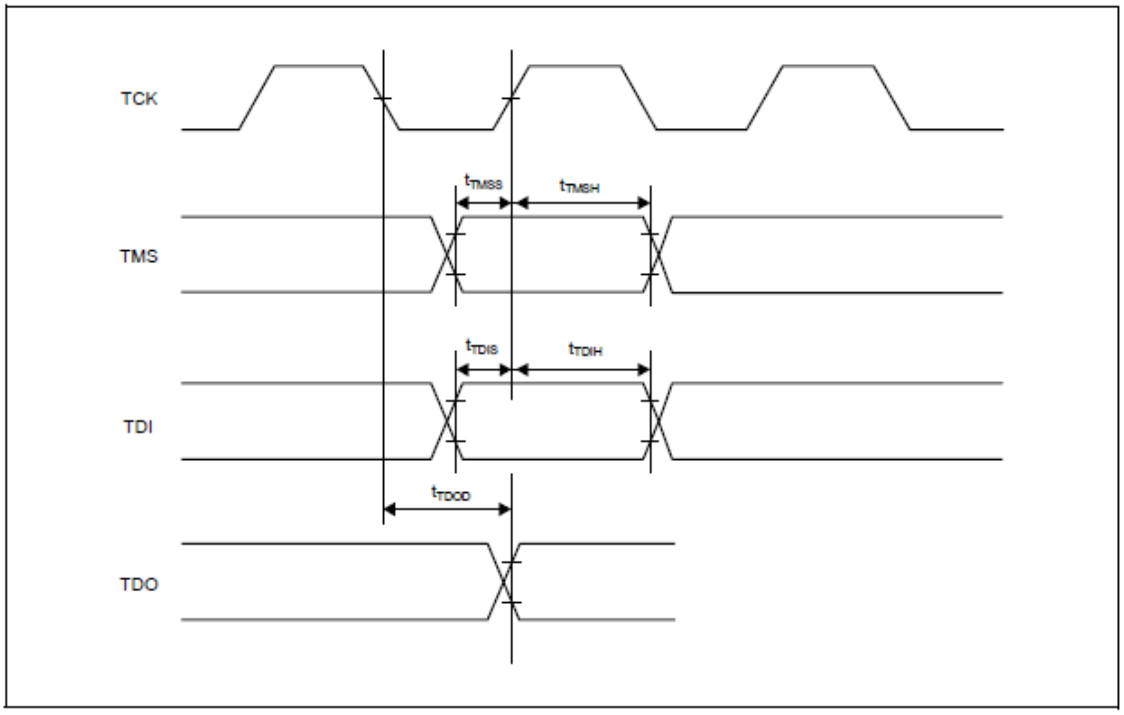


Figure 4-17. Boundary Input and Output Timing

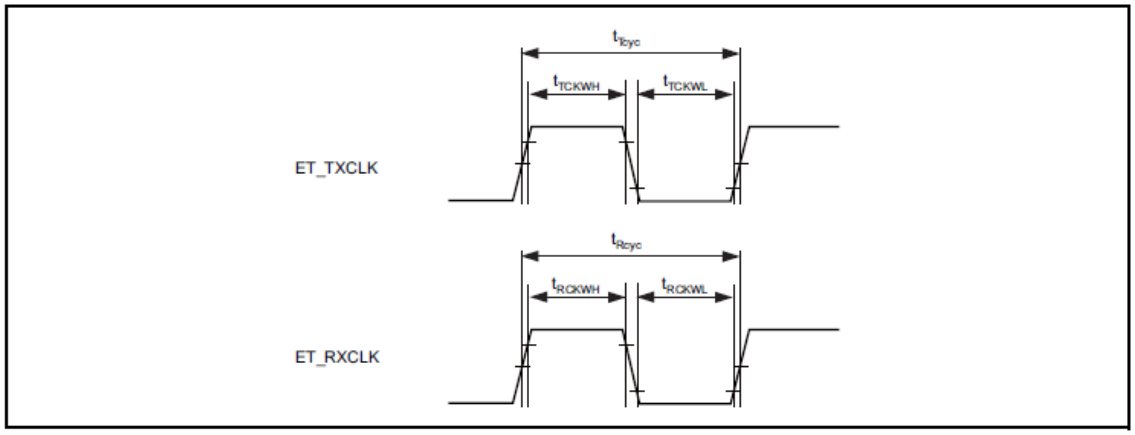


Figure 4-18. MII Clock Timing

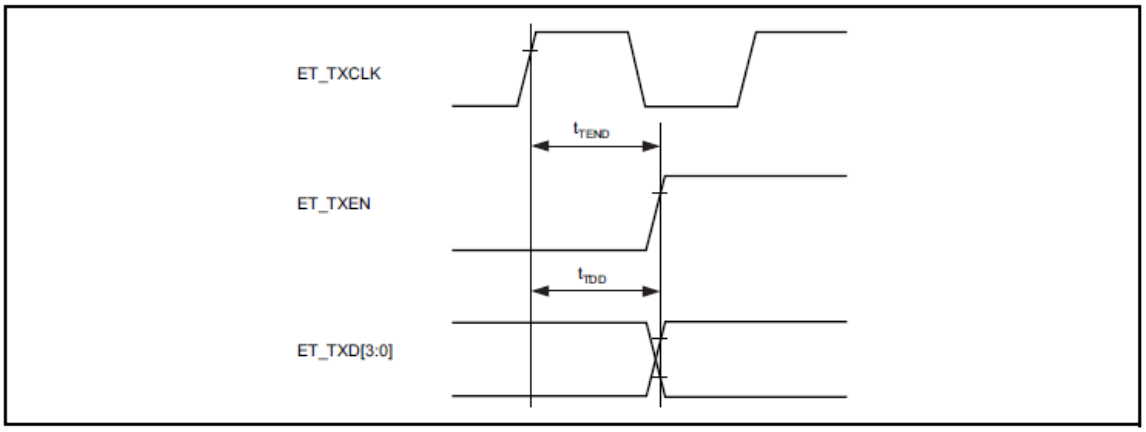


Figure 4-19. MII Transmission Data Timing

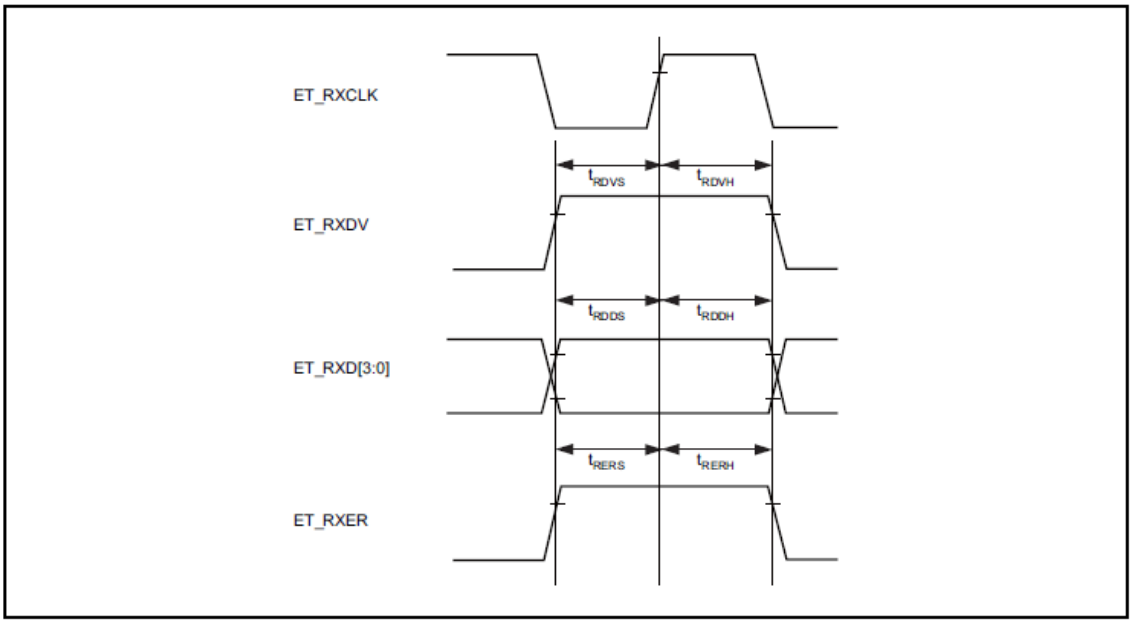


Figure 4-20. MII Receive Data Timing

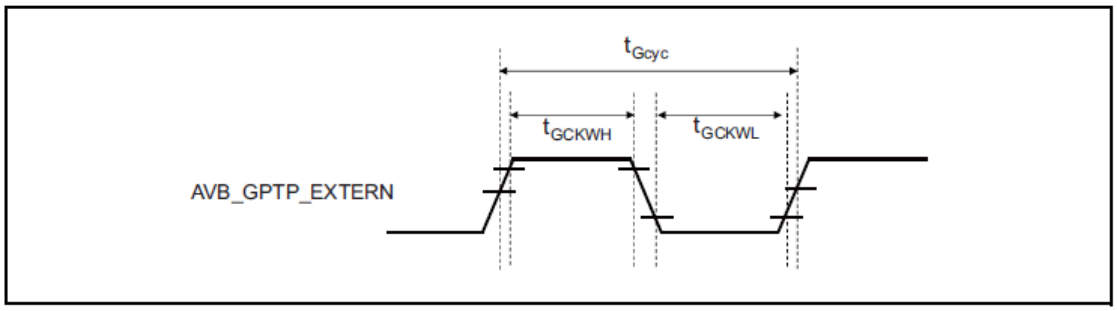


Figure 4-21. gPTP Timer External Clock Timing

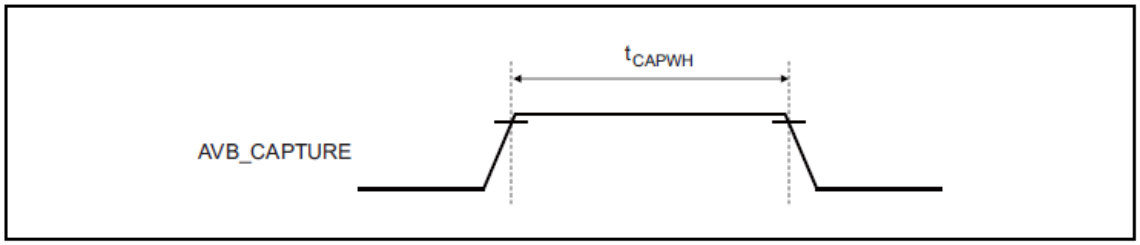


Figure 4-22. Timer Capture Signal Timing

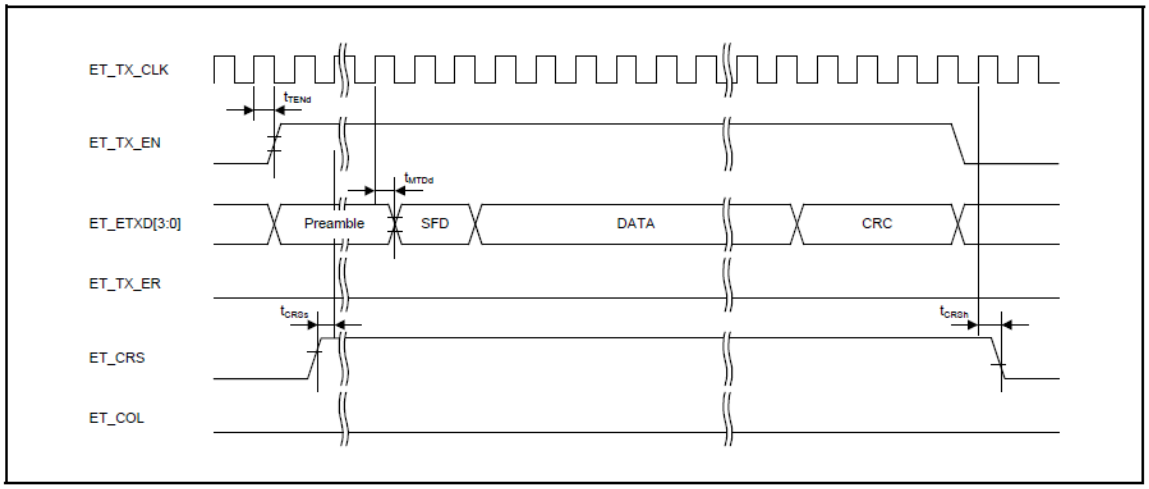


Figure 4-23. MII Transmission Timing (Normal Operation)

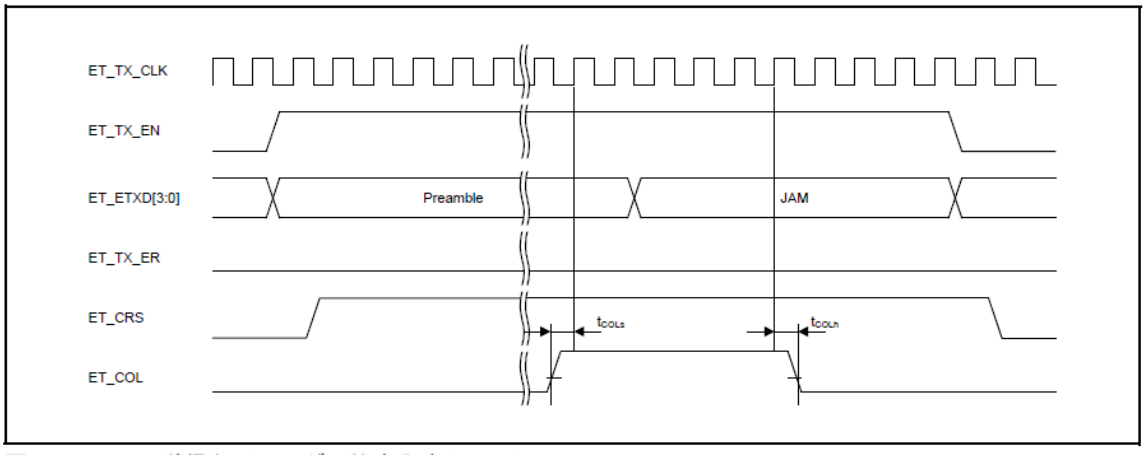


Figure 4-24. MII Transmission Timing (Collision Occurrence Case)

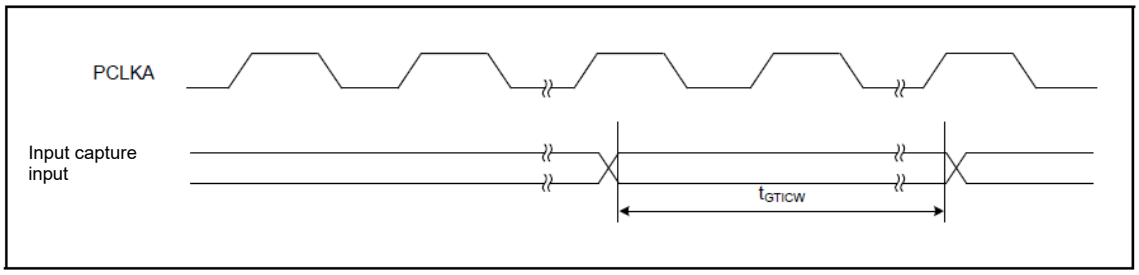


Figure 4-25. GPT Input Capture Input Timing

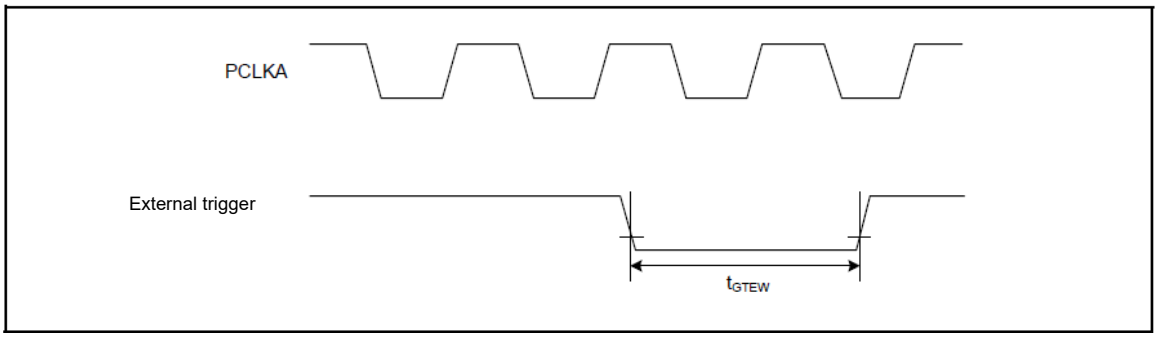


Figure 4-26. GPT External Trigger Input Timing

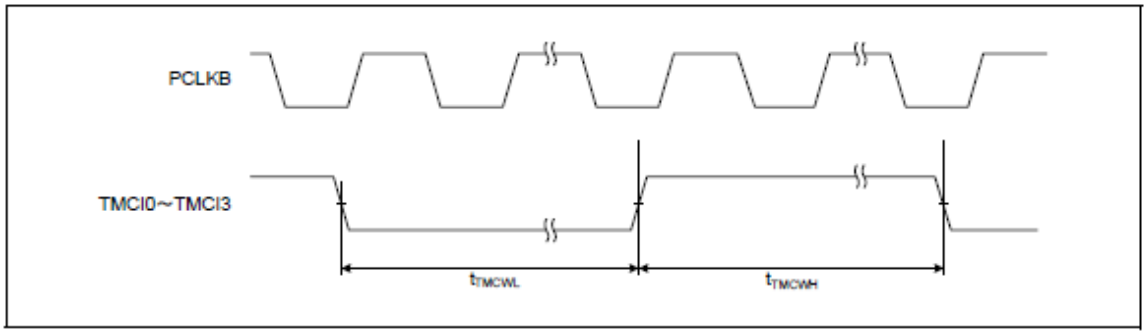


Figure 4-27. TMR Clock Input Timing

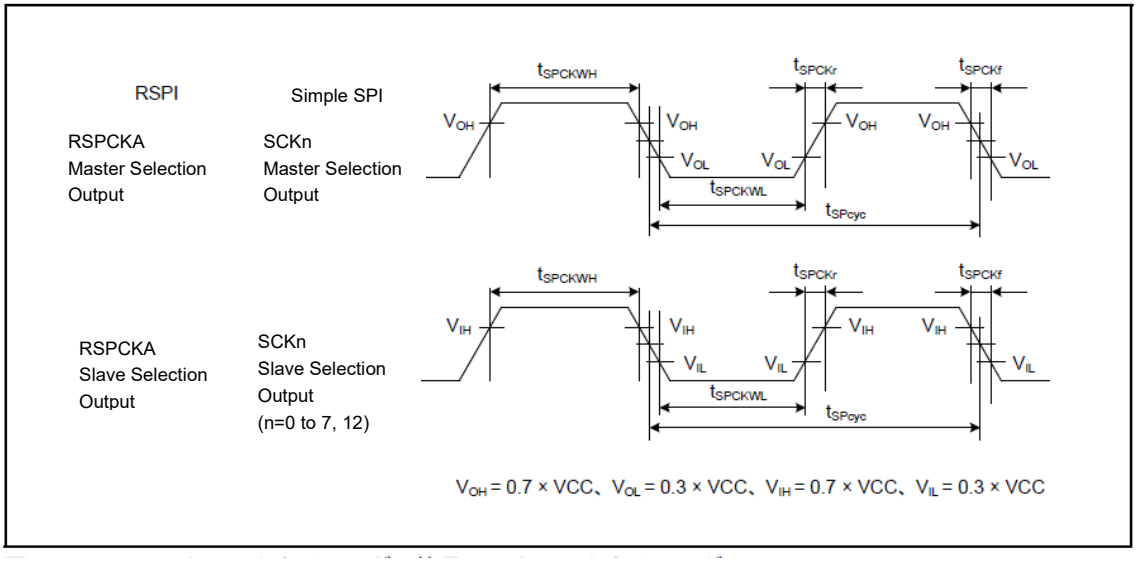


Figure 4-28. RSPI Clock Timing / Simple SPI Clock Timing

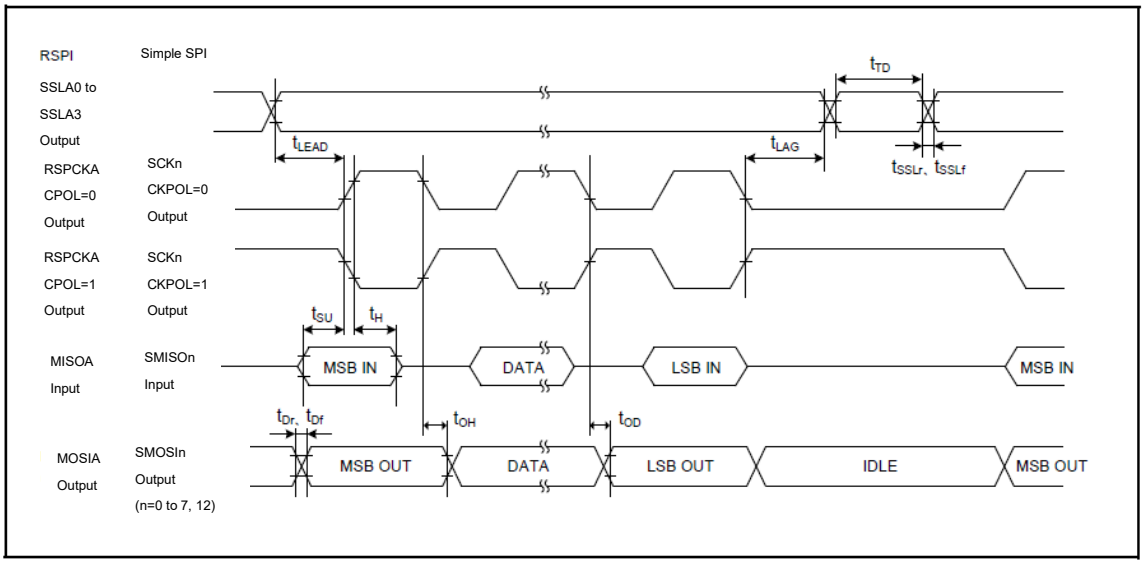


Figure 4-29. RSPI Timing (Master, CPHA=0)
(Bit rate: Set PCLK to a division other than 2) / Simple SPI Timing (Master, CKPH=1)

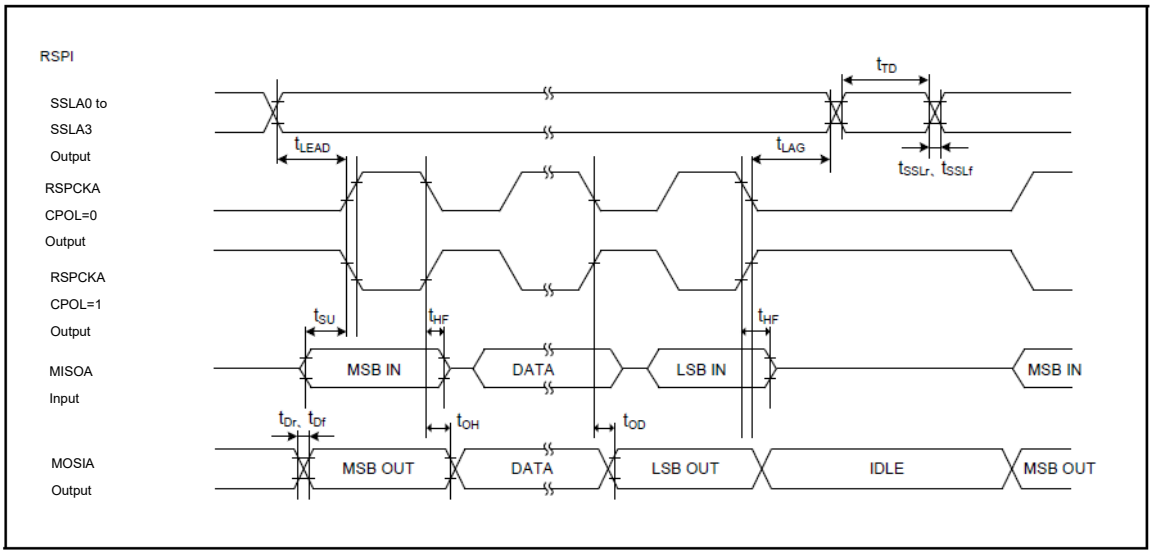


Figure 4-30. RSPI Timing (Master, CPHA=0)
(Bitrate: Set PCLK to a division of 2)

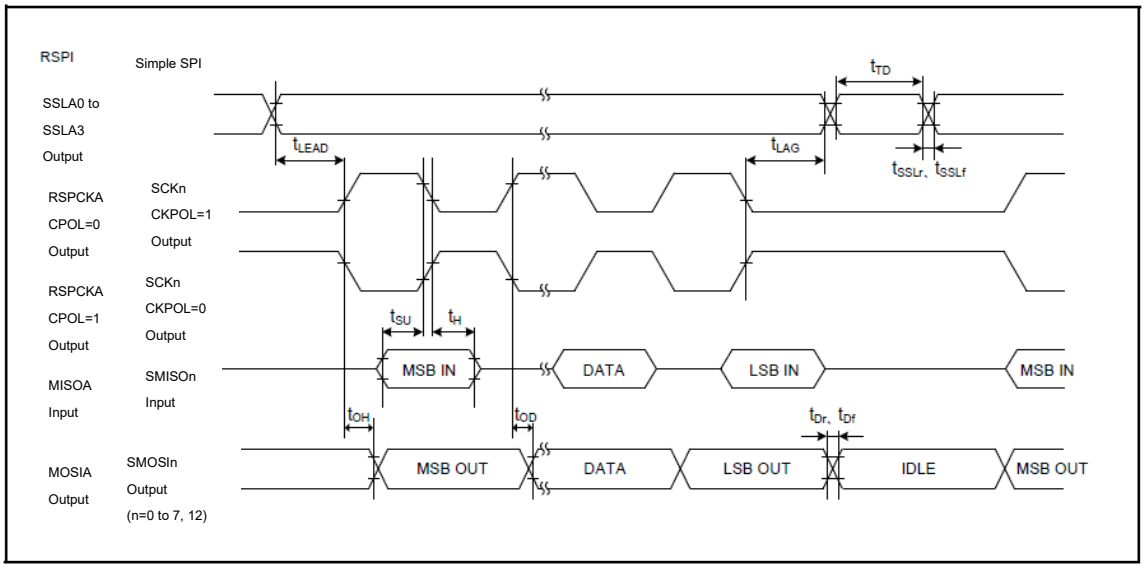


Figure 4-31. RSPI Timing (Master, CPHA=1)
(Bit rate: Set PCLK to a division other than 2) / Simple SPI Timing (Master, CKPH=1)

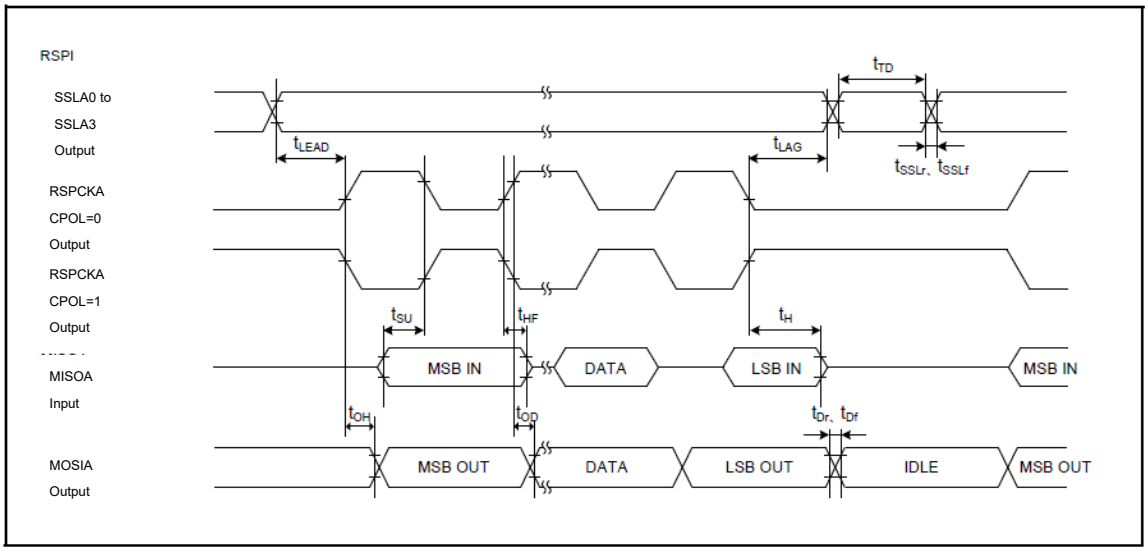


Figure 4-32. RSPI Timing (Master, CPHA=1)
(Bitrate: Set PCLK to division of 2)

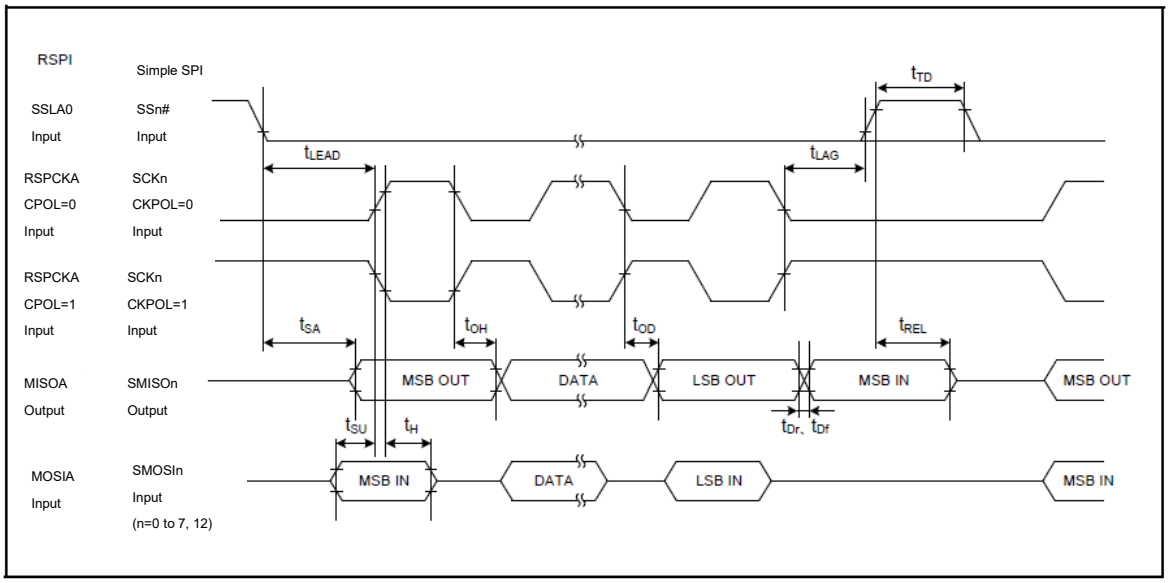


Figure 4-33. RSPI Timing (Slave, CPHA=0) / Simple SPI Timing (Slave, CKPH=1)

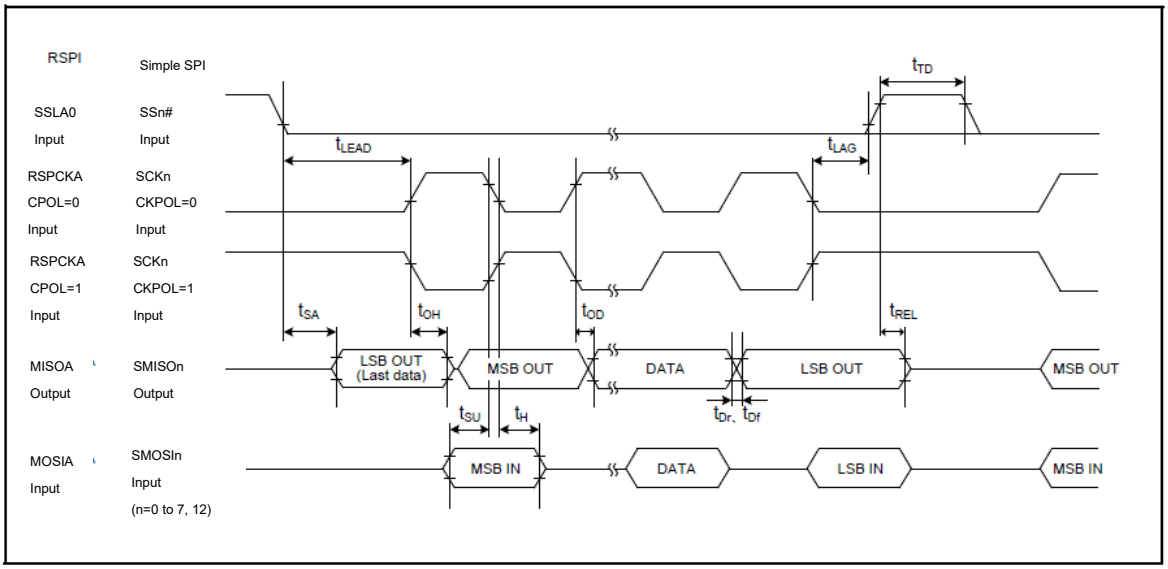


Figure 4-34. RSPI Timing (Slave, CPHA=1) / Simple SPI Timing (Slave, CKPH=0)

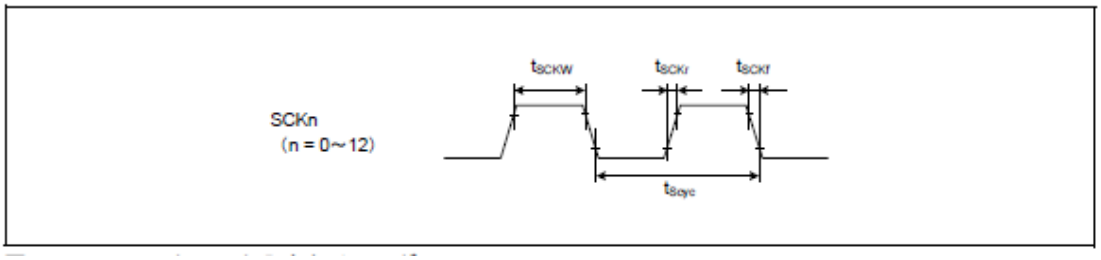


Figure 4-35. SCK Clock Input Timing

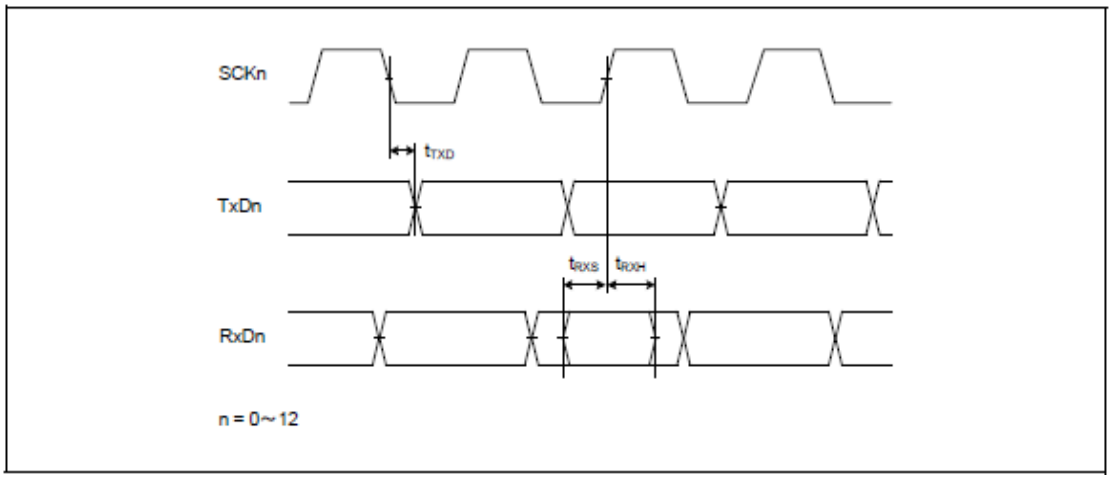


Figure 4-36. SCI Input and Output Timing / Clock-Synchronous Mode

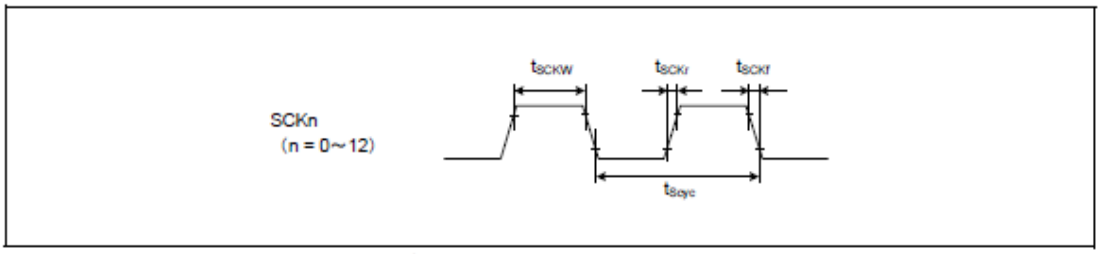


Figure 4-37. SCK Clock Input Timing

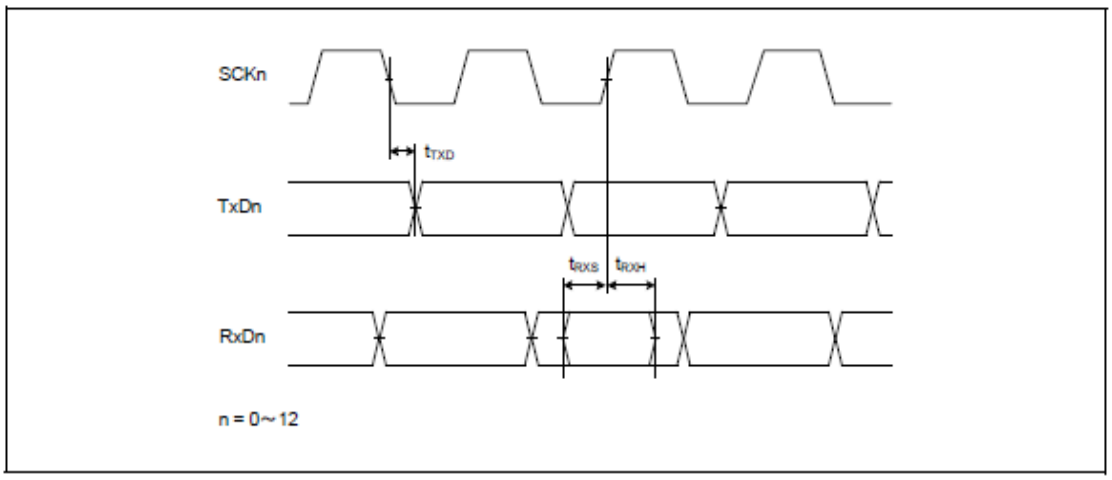


Figure 4-38. SCI Input and Output Timing / Clock-Synchronous Mode

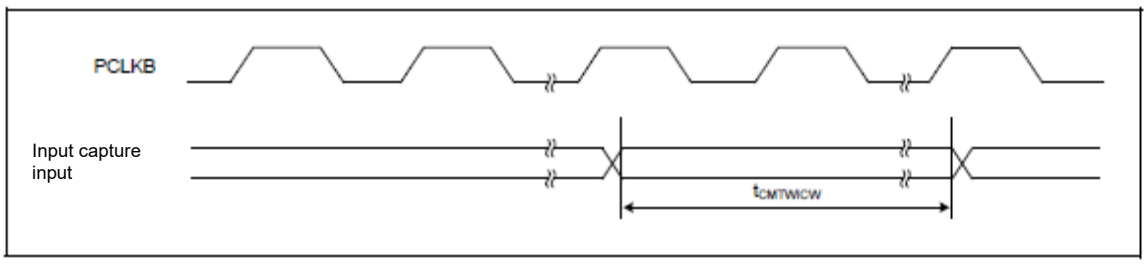
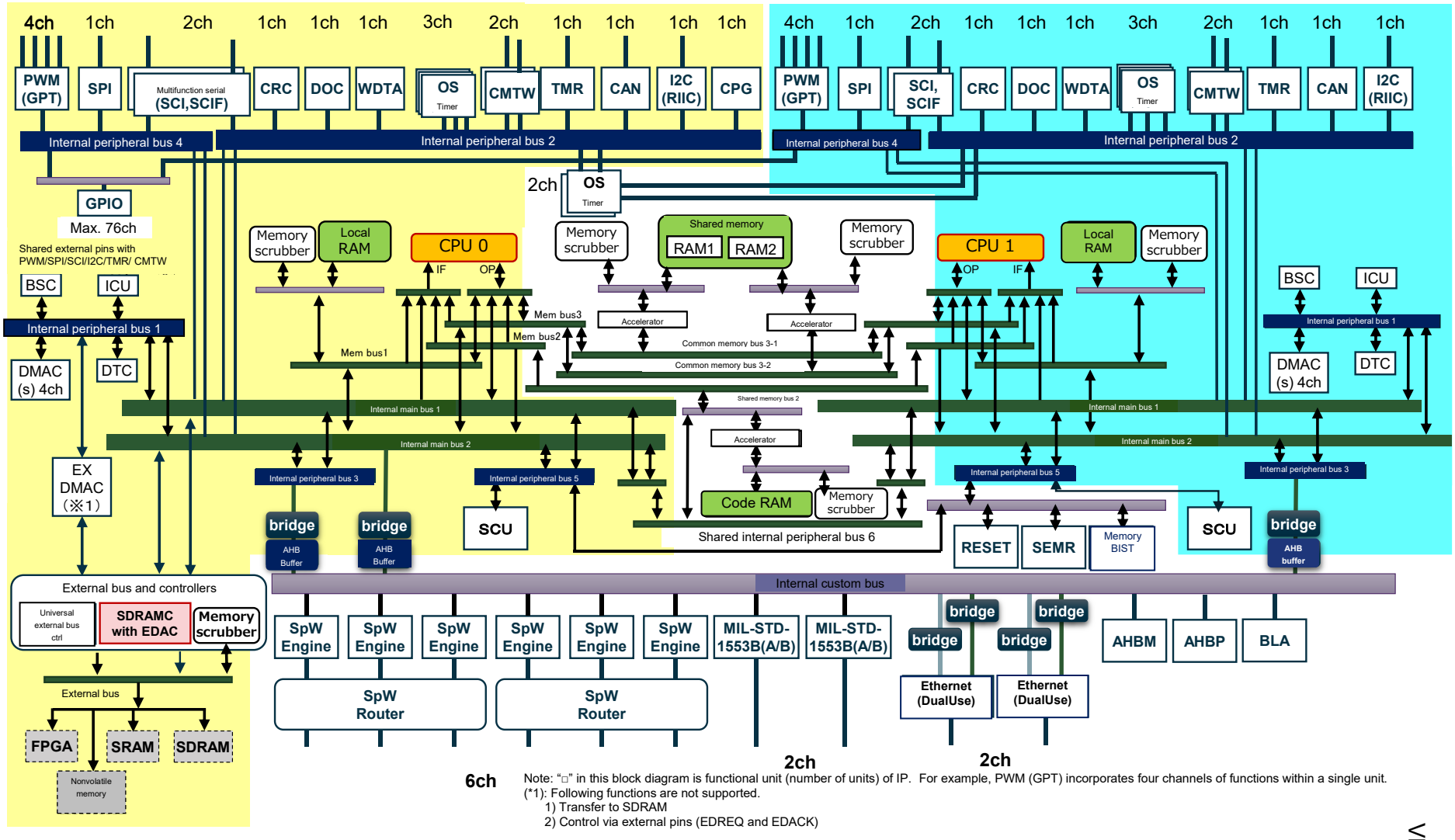


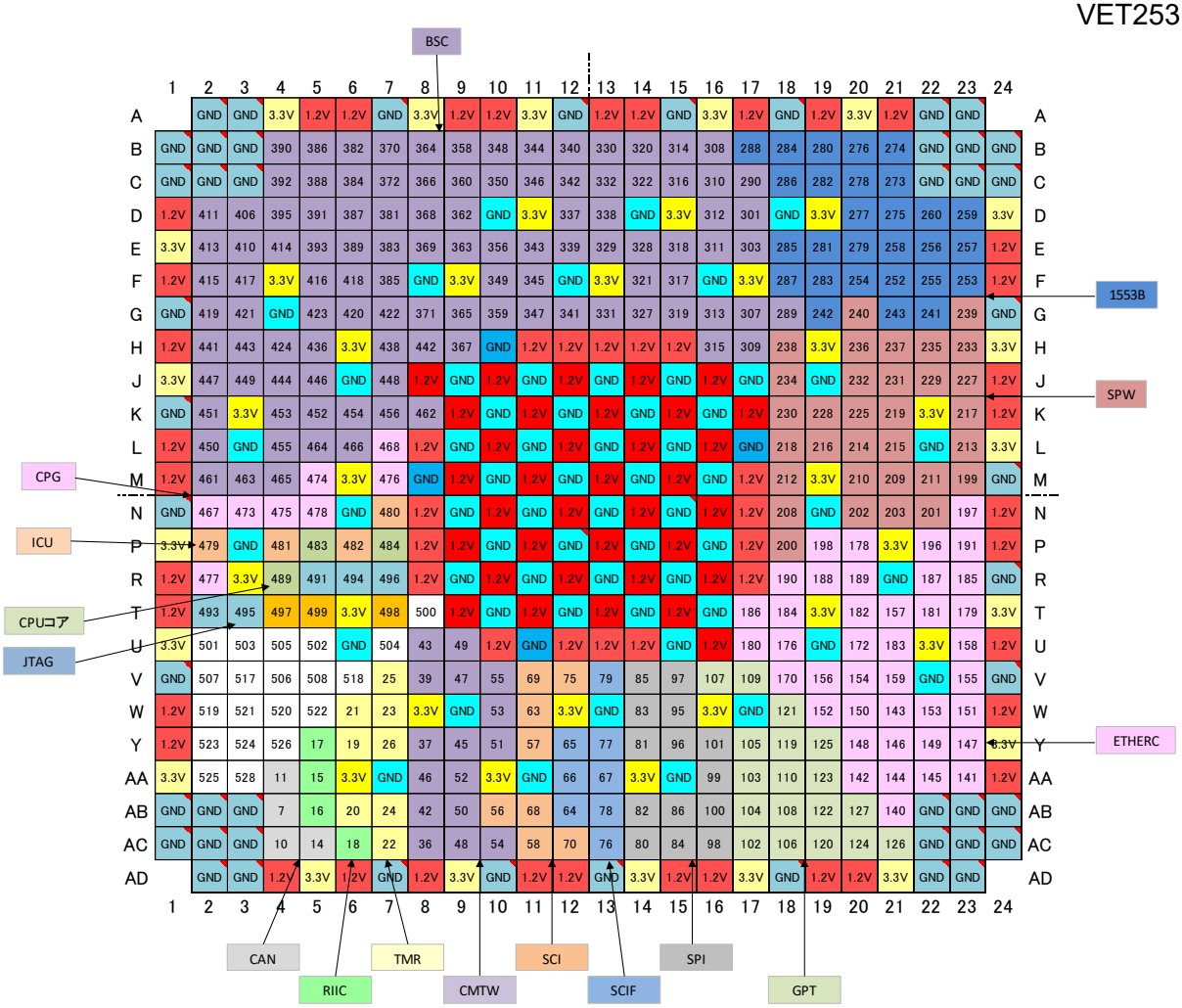
Figure 4-39. CMTW Input Capture Input Timing



Note: "□" in this block diagram is functional unit (number of units) of IP. For example, PWM (GPT) incorporates four channels of functions within a single unit.
(*1): Following functions are not supported.
1) Transfer to SDRAM
2) Control via external pins (EDREQ and EDACK)

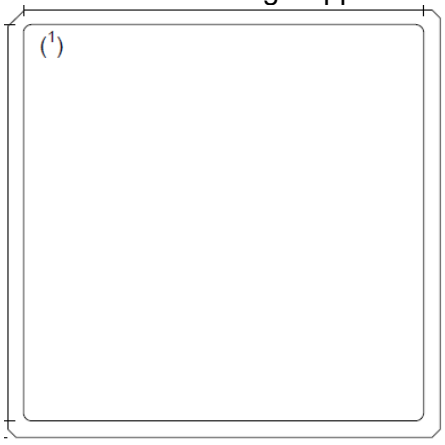
Figure 4-40. System Block Diagram

VET25311



<TOP VIEW>

[Correspondence with CBGA Package Appearance <TOP VIEW>]



Note: (1) The notch position is at the top left of the drawing.

Figure 4-41. Pin Configuration Drawing (CBGA Package)

Table 4-3. Pin-outs and Pin Functions (1/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
A2	GND	-	-	-		VSS,VSSQ
A3	GND	-	-	-		VSS,VSSQ
A4	3.3V	-	-	-		VCCQ
A5	1.2V	-	-	-		VDD
A6	1.2V	-	-	-		VDD
A7	GND	-	-	-		VSS,VSSQ
A8	3.3V	-	-	-		VCCQ
A9	1.2V	-	-	-		VDD
A10	1.2V	-	-	-		VDD
A11	3.3V	-	-	-		VCCQ
A12	GND	-	-	-		VSS,VSSQ
A13	1.2V	-	-	-		VDD
A14	1.2V	-	-	-		VDD
A15	GND	-	-	-		VSS,VSSQ
A16	3.3V	-	-	-		VCCQ
A17	1.2V	-	-	-		VDD
A18	GND	-	-	-		VSS,VSSQ
A19	1.2V	-	-	-		VDD
A20	3.3V	-	-	-		VCCQ
A21	1.2V	-	-	-		VDD
A22	GND	-	-	-		VSS,VSSQ
A23	GND	-	-	-		VSS,VSSQ
B1	GND	-	-	-		VSS,VSSQ
B2	GND	-	-	-		VSS,VSSQ
B3	GND	-	-	-		VSS,VSSQ
B4	D40	External bus	CPU0	inout	24mA	
B5	D36	External bus	CPU0	inout	24mA	
B6	D32	External bus	CPU0	inout	24mA	
B7	D28	External bus	CPU0	inout	24mA	
B8	D22	External bus	CPU0	inout	24mA	
B9	D17	External bus	CPU0	inout	24mA	
B10	D13	External bus	CPU0	inout	24mA	
B11	D9	External bus	CPU0	inout	24mA	
B12	D5	External bus	CPU0	inout	24mA	
B13	A23	External bus	CPU0	out	24mA	
B14	A17	External bus	CPU0	out	24mA	
B15	A11	External bus	CPU0	out	24mA	
B16	A5	External bus	CPU0	out	24mA	
B17	MIL 1553B_TX_DATA_B_2	MIL-1553B	Common	out	8mA	
B18	MIL 1553B_RX_DATA__BAR_B_2	MIL-1553B	Common	in	-	
B19	MIL 1553B_TX_DATA_BAR_A_2	MIL-1553B	Common	out	8mA	
B20	MIL 1553B_SUBSYSYTEM_2	MIL-1553B	Common	in	-	
B21	MIL 1553B_TX_DATA_B_1	MIL-1553B	Common	out	8mA	
B22	GND	-	-	-		VSS,VSSQ
B23	GND	-	-	-		VSS,VSSQ
B24	GND	-	-	-		VSS,VSSQ
C1	GND	-	-	-		VSS,VSSQ
C2	GND	-	-	-		VSS,VSSQ
C3	GND	-	-	-		VSS,VSSQ
C4	D42	External bus	CPU0	inout	24mA	
C5	D38	External bus	CPU0	inout	24mA	
C6	D34	External bus	CPU0	inout	24mA	
C7	D30	External bus	CPU0	inout	24mA	
C8	D24	External bus	CPU0	inout	24mA	
C9	D19	External bus	CPU0	inout	24mA	
C10	D15	External bus	CPU0	inout	24mA	
C11	D11	External bus	CPU0	inout	24mA	
C12	D7	External bus	CPU0	inout	24mA	
C13	D1	External bus	CPU0	inout	24mA	
C14	A19	External bus	CPU0	out	24mA	
C15	A13	External bus	CPU0	out	24mA	
C16	A7	External bus	CPU0	out	24mA	
C17	A1	External bus	CPU0	out	24mA	
C18	MIL 1553B_RX_STROBE_B_2	MIL-1553B	Common	out	8mA	
C19	MIL 1553B_TX_INHIBIT_A_2	MIL-1553B	Common	out	8mA	
C20	MIL 1553B_RX_DATA__BAR_A_2	MIL-1553B	Common	in	-	
C21	MIL 1553B_TX_DATA_BAR_B_1	MIL-1553B	Common	out	8mA	
C22	GND	-	-	-		VSS,VSSQ
C23	GND	-	-	-		VSS,VSSQ
C24	GND	-	-	-		VSS,VSSQ
D1	1.2V	-	-	-		VDD
D2	D47	External bus	CPU0	inout	24mA	
D3	D45	External bus	CPU0	inout	24mA	
D4	D44	External bus	CPU0	inout	24mA	
D5	D41	External bus	CPU0	inout	24mA	

Table 4-3. Pin-outs and Pin Functions (2/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
D6	D37	External bus	CPU0	inout	24mA	
D7	D31	External bus	CPU0	inout	24mA	
D8	D26	External bus	CPU0	inout	24mA	
D9	D20	External bus	CPU0	inout	24mA	
D10	GND	-	-	-		VSS,VSSQ
D11	3.3V	-	-	-		VCCQ
D12	D2	External bus	CPU0	inout	24mA	
D13	D3	External bus	CPU0	inout	24mA	
D14	GND	-	-	-		VSS,VSSQ
D15	3.3V	-	-	-		VCCQ
D16	A9	External bus	CPU0	out	24mA	
D17	A2	External bus	CPU0	out	24mA	
D18	GND	-	-	-		VSS,VSSQ
D19	3.3V	-	-	-		VCCQ
D20	MIL 1553B_RX_DATA_A_2	MIL-1553B	Common	in	-	
D21	MIL 1553B_EX_SYNC_2	MIL-1553B	Common	in	-	
D22	MIL 1553B_RX_STROBE_B_1	MIL-1553B	Common	out	8mA	
D23	MIL 1553B_TX_INHIBIT_B_1	MIL-1553B	Common	out	8mA	
D24	3.3V	-	-	-		VCCQ
E1	3.3V	-	-	-		VCCQ
E2	ALE	External bus	CPU0	out	24mA	
E3	D46	External bus	CPU0	inout	24mA	
E4	BC0	External bus	CPU0	out	24mA	
E5	D43	External bus	CPU0	inout	24mA	
E6	D39	External bus	CPU0	inout	24mA	
E7	D33	External bus	CPU0	inout	24mA	
E8	D27	External bus	CPU0	inout	24mA	
E9	D21	External bus	CPU0	inout	24mA	
E10	D16	External bus	CPU0	inout	24mA	
E11	D8	External bus	CPU0	inout	24mA	
E12	D4	External bus	CPU0	inout	24mA	
E13	A22	External bus	CPU0	out	24mA	
E14	A21	External bus	CPU0	out	24mA	
E15	A15	External bus	CPU0	out	24mA	
E16	A8	External bus	CPU0	out	24mA	
E17	A3	External bus	CPU0	out	24mA	
E18	MIL 1553B_TX_INHIBIT_B_2	MIL-1553B	Common	out	8mA	
E19	MIL 1553B_RX_STROBE_A_2	MIL-1553B	Common	out	8mA	
E20	MIL 1553B_TX_DATA_A_2	MIL-1553B	Common	out	8mA	
E21	MIL 1553B_RX_DATA__BAR_B_1	MIL-1553B	Common	in	-	
E22	MIL 1553B_TX_INHIBIT_A_1	MIL-1553B	Common	out	8mA	
E23	MIL 1553B_RX_DATA_B_1	MIL-1553B	Common	in	-	
E24	1.2V	-	-	-		VDD
F1	1.2V	-	-	-		VDD
F2	BC1	External bus	CPU0	out	24mA	
F3	BC3	External bus	CPU0	out	24mA	
F4	3.3V	-	-	-		VCCQ
F5	BC2	External bus	CPU0	out	24mA	
F6	CAS#	External bus	CPU0	out	24mA	
F7	D35	External bus	CPU0	inout	24mA	
F8	GND	-	-	-		VSS,VSSQ
F9	3.3V	-	-	-		VCCQ
F10	D14	External bus	CPU0	inout	24mA	
F11	D10	External bus	CPU0	inout	24mA	
F12	GND	-	-	-		VSS,VSSQ
F13	3.3V	-	-	-		VCCQ
F14	A18	External bus	CPU0	out	24mA	
F15	A14	External bus	CPU0	out	24mA	
F16	GND	-	-	-		VSS,VSSQ
F17	3.3V	-	-	-		VCCQ
F18	MIL 1553B_TX_DATA_BAR_B_2	MIL-1553B	Common	out	8mA	
F19	MIL 1553B_RX_DATA_B_2	MIL-1553B	Common	in	-	
F20	MIL 1553B_TX_DATA_BAR_A_1	MIL-1553B	Common	out	8mA	
F21	MIL 1553B_RX_DATA__BAR_A_1	MIL-1553B	Common	in	-	
F22	MIL 1553B_RX_STROBE_A_1	MIL-1553B	Common	out	8mA	
F23	MIL 1553B_TX_DATA_A_1	MIL-1553B	Common	out	8mA	
F24	1.2V	-	-	-		VDD
G1	GND	-	-	-		VSS,VSSQ
G2	CKE	External bus	CPU0	out	24mA	
G3	CS2#	External bus	CPU0	out	24mA	
G4	GND	-	-	-		VSS,VSSQ
G5	CS4#	External bus	CPU0	out	24mA	
G6	CS1#	External bus	CPU0	out	24mA	
G7	CS3#	External bus	CPU0	out	24mA	
G8	D29	External bus	CPU0	inout	24mA	
G9	D23	External bus	CPU0	inout	24mA	
G10	D18	External bus	CPU0	inout	24mA	

Table 4-3. Pin-outs and Pin Functions (3/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
G11	D12	External bus	CPU0	inout	24mA	
G12	D6	External bus	CPU0	inout	24mA	
G13	D0	External bus	CPU0	inout	24mA	
G14	A20	External bus	CPU0	out	24mA	
G15	A16	External bus	CPU0	out	24mA	
G16	A10	External bus	CPU0	out	24mA	
G17	A4	External bus	CPU0	out	24mA	
G18	A0	External bus	CPU0	out	24mA	
G19	MIL 1553B_SUBSYSYTEM_1	MIL-1553B	Common	in	-	
G20	GPIO_2_11	SpaceWire	Common	in	-	Channels 4 to 6 (common)
G21	MIL 1553B_RX_DATA_A_1	MIL-1553B	Common	in	-	
G22	MIL 1553B_EX_SYNC_1	MIL-1553B	Common	in	-	
G23	GPIO_2_10	SpaceWire	Common	in	-	Channels 4 to 6 (common)
G24	GND	-	-	-		VSS,VSSQ
H1	1.2V	-	-	-		VDD
H2	DQM0	External bus	CPU0	out	24mA	
H3	DQM2	External bus	CPU0	out	24mA	
H4	CS5#	External bus	CPU0	out	24mA	
H5	CS6#	External bus	CPU0	out	24mA	
H6	3.3V	-	-	-		VCCQ
H7	CS7#	External bus	CPU0	out	24mA	
H8	DQM1	External bus	CPU0	out	24mA	
H9	D25	External bus	CPU0	inout	24mA	
H10	GND	-	-	-		VSS,VSSQ,VBN
H11	1.2V	-	-	-		VDD
H12	1.2V	-	-	-		VDD
H13	1.2V	-	-	-		VDD
H14	1.2V	-	-	-		VDD, VBP
H15	1.2V	-	-	-		VDD
H16	A12	External bus	CPU0	out	24mA	
H17	A6	External bus	CPU0	out	24mA	
H18	GPIO_2_01	SpaceWire	Common	in	-	Channels 4 to 6 (common)
H19	3.3V	-	-	-		VCCQ
H20	D_OUT(5)	SpaceWire	Common	out	8mA	
H21	GPIO_2_00	SpaceWire	Common	in	-	Channels 4 to 6 (common)
H22	D_IN(5)	SpaceWire	Common	in	-	
H23	S_IN(5)	SpaceWire	Common	in	-	
H24	3.3V	-	-	-		VCCQ
J1	3.3V	-	-	-		VCCQ
J2	DQM5	External bus	CPU0	out	24mA	
J3	RD#	External bus	CPU0	out	24mA	
J4	DQM3	External bus	CPU0	out	24mA	
J5	DQM4	External bus	CPU0	out	24mA	
J6	GND	-	-	-		VSS,VSSQ
J7	RAS#	External bus	CPU0	out	24mA	
J8	1.2V	-	-	-		VDD
J9	GND	-	-	-		VSS,VSSQ
J10	1.2V	-	-	-		VDD
J11	GND	-	-	-		VSS,VSSQ
J12	1.2V	-	-	-		VDD
J13	GND	-	-	-		VSS,VSSQ
J14	1.2V	-	-	-		VDD
J15	GND	-	-	-		VSS,VSSQ
J16	1.2V	-	-	-		VDD
J17	GND	-	-	-		VSS,VSSQ
J18	S_OUT(5)	SpaceWire	Common	out	8mA	
J19	GND	-	-	-		VSS,VSSQ
J20	D_OUT(4)	SpaceWire	Common	out	8mA	
J21	D_IN(4)	SpaceWire	Common	in	-	
J22	S_IN(4)	SpaceWire	Common	in	-	
J23	D_IN(3)	SpaceWire	Common	in	-	
J24	1.2V	-	-	-		VDD
K1	GND	-	-	-		VSS,VSSQ
K2	SDCS#	External bus	CPU0	out	24mA	
K3	3.3V	-	-	-		VCCQ
K4	SDCS2#	External bus	CPU0	out	24mA	
K5	SDCS1#	External bus	CPU0	out	24mA	
K6	SDCS3#	External bus	CPU0	out	24mA	
K7	WE#	External bus	CPU0	out	24mA	
K8	WR1#	External bus	CPU0	out	24mA	
K9	1.2V	-	-	-		VDD
K10	GND	-	-	-		VSS,VSSQ
K11	1.2V	-	-	-		VDD
K12	GND	-	-	-		VSS,VSSQ
K13	1.2V	-	-	-		VDD
K14	GND	-	-	-		VSS,VSSQ
K15	1.2V	-	-	-		VDD

Table 4-3. Pin-outs and Pin Functions (4/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
K16	GND	-	-	-		VSS,VSSQ
K17	1.2V	-	-	-		VDD
K18	S_OUT(4)	SpaceWire	Common	out	8mA	
K19	D_OUT(3)	SpaceWire	Common	out	8mA	
K20	S_OUT(3)	SpaceWire	Common	out	8mA	
K21	S_IN(3)	SpaceWire	Common	in	-	
K22	3.3V	-	-	-		VCCQ
K23	GPIO_1_10	SpaceWire	Common	in	-	Channels 1 to 3 (common)
K24	1.2V	-	-	-		VDD
L1	1.2V	-	-	-		VDD
L2	SDCLK	External bus	CPU0	out	24mA	
L3	GND	-	-	-		VSS,VSSQ
L4	WAIT#	External bus	CPU0	in	-	
L5	WR3#	External bus	CPU0	out	24mA	
L6	CS_BSW[1]	External bus	CPU0	in	-	Initial bus width setting for external bus area 1
L7	PLL_SEL[0]	CPG	Common	in	-	
L8	1.2V	-	-	-	-	VDD
L9	GND	-	-	-		VSS,VSSQ
L10	1.2V	-	-	-		VDD
L11	GND	-	-	-		VSS,VSSQ
L12	1.2V	-	-	-		VDD
L13	GND	-	-	-		VSS,VSSQ
L14	1.2V	-	-	-		VDD
L15	GND	-	-	-		VSS,VSSQ
L16	1.2V	-	-	-		VDD
L17	GND	-	-	-		VSS,VSSQ,VBN
L18	GPIO_1_11	SpaceWire	Common	in	-	Channels 1 to 3 (common)
L19	GPIO_1_01	SpaceWire	Common	in	-	Channels 1 to 3 (common)
L20	D_OUT(2)	SpaceWire	Common	out	8mA	
L21	GPIO_1_00	SpaceWire	Common	in	-	Channels 1 to 3 (common)
L22	GND	-	-	-		VSS,VSSQ
L23	D_IN(2)	SpaceWire	Common	in	-	
L24	3.3V	-	-	-		VCCQ
M1	1.2V	-	-	-		VDD
M2	WR0#	External bus	CPU0	out	24mA	
M3	WR2#	External bus	CPU0	out	24mA	
M4	CS_BSW[0]	External bus	CPU0	in	-	Initial bus width setting for external bus area 1
M5	PLL_SEL[2]	CPG	Common	in	-	
M6	3.3V	-	-	-	-	VCCQ
M7	PLL_SEL[4]	CPG	Common	in	-	
M8	GND	-	-	-	-	VSS,VSSQ
M9	1.2V	-	-	-	-	VDD
M10	GND	-	-	-	-	VSS,VSSQ
M11	1.2V	-	-	-	-	VDD
M12	GND	-	-	-	-	VSS,VSSQ
M13	1.2V	-	-	-	-	VDD
M14	GND	-	-	-	-	VSS,VSSQ
M15	1.2V	-	-	-	-	VDD
M16	GND	-	-	-	-	VSS,VSSQ
M17	1.2V	-	-	-	-	VDD
M18	S_OUT(2)	SpaceWire	Common	out	8mA	
M19	3.3V	-	-	-	-	VCCQ
M20	D_OUT(1)	SpaceWire	Common	out	8mA	
M21	D_IN(1)	SpaceWire	Common	in	-	
M22	S_IN(2)	SpaceWire	Common	in	-	
M23	S_IN(0)	SpaceWire	Common	in	-	
M24	GND	-	-	-	-	VSS,VSSQ
N1	GND	-	-	-	-	VSS,VSSQ
N2	EXT_CLK	CPG	Common	in	-	
N3	PLL_SEL[1]	CPG	Common	in	-	
N4	PLL_SEL[3]	CPG	Common	in	-	
N5	JTAG_CLK	CPG	Common	in	-	TCK
N6	GND	-	-	-	-	VSS,VSSQ
N7	IRQ1	External interrupt	Common	in	-	
N8	1.2V	-	-	-	-	VDD
N9	GND	-	-	-	-	VSS,VSSQ
N10	1.2V	-	-	-	-	VDD
N11	GND	-	-	-	-	VSS,VSSQ
N12	1.2V	-	-	-	-	VDD
N13	GND	-	-	-	-	VSS,VSSQ
N14	1.2V	-	-	-	-	VDD
N15	GND	-	-	-	-	VSS,VSSQ
N16	1.2V	-	-	-	-	VDD
N17	1.2V	-	-	-		VDD

Table 4-3. Pin-outs and Pin Functions (5/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
N18	S_OUT(1)	SpaceWire	Common	out	8mA	
N19	GND	-	-	-	-	VSS,VSSQ
N20	D_OUT(0)	SpaceWire	Common	out	8mA	
N21	S_IN(1)	SpaceWire	Common	In	-	
N22	D_IN(0)	SpaceWire	Common	In	-	
N23	clk_gptp_extern_1	Ethernet	Common	In	-	gPTP function
N24	1.2V	-	-	-	-	VDD
P1	3.3V	-	-	-	-	VCCQ
P2	NMI	External interrupt	CPU0	In	-	
P3	GND	-	-	-	-	VSS,VSSQ
P4	IRQ2	External interrupt	Common	In	-	
P5	MD[0]	System	Common	In	-	
P6	IRQ3	External interrupt	Common	In	-	
P7	MD[1]	System	Common	In	-	
P8	1.2V	-	-	-		VDD
P9	1.2V	-	-	-	-	VDD
P10	GND	-	-	-	-	VSS,VSSQ
P11	1.2V	-	-	-	-	VDD
P12	GND	-	-	-	-	VSS,VSSQ
P13	1.2V	-	-	-	-	VDD
P14	GND	-	-	-	-	VSS,VSSQ
P15	1.2V	-	-	-	-	VDD
P16	GND	-	-	-	-	VSS,VSSQ
P17	1.2V	-	-	-	-	VDD
P18	S_OUT(0)	SpaceWire	Common	out	8mA	
P19	avb_pt_capture_1	Ethernet	Common	in	-	gPTP function
P20	clk_miitx_clk_1	Ethernet	Common	in	-	
P21	3.3V	-	-	-	-	VCCQ
P22	clk_miirx_clk_1	Ethernet	Common	in	-	
P23	avd_miirx_err_1	Ethernet	Common	in	-	
P24	1.2V	-	-	-	-	VDD
R1	1.2V	-	-	-	-	VDD
R2	USER_CLK	CPG	Common	out	-	
R3	3.3V	-	-	-	-	VCCQ
R4	RES#	System	Common	in	-	
R5	TRST#	_JTAG for CPU	Common	in	-	
R6	TDI	_JTAG for CPU	Common	in	-	
R7	TDO	_JTAG for CPU	Common	out	8mA	
R8	1.2V	-	-	-	-	VDD
R9	GND	-	-	-	-	VSS,VSSQ
R10	1.2V	-	-	-	-	VDD
R11	GND	-	-	-	-	VSS,VSSQ
R12	1.2V	-	-	-	-	VDD
R13	GND	-	-	-	-	VSS,VSSQ
R14	1.2V	-	-	-	-	VDD
R15	GND	-	-	-	-	VSS,VSSQ
R16	1.2V	-	-	-	-	VDD
R17	1.2V	-	-	-		VDD, VBP
R18	avd_miirx_rxd0_1	Ethernet	Common	in	-	
R19	avd_miitx_crs_1	Ethernet	Common	in	-	
R20	fet_miitx_err_1	Ethernet	Common	out	8mA	
R21	GND	-	-	-	-	VSS,VSSQ
R22	avd_miirx_dv_1	Ethernet	Common	in	-	
R23	avd_miitx_col_1	Ethernet	Common	in	-	
R24	GND	-	-	-	-	VSS,VSSQ
T1	1.2V	-	-	-	-	VDD
T2	EMLE	_JTAG for CPU	Common	in	-	
T3	TMS	_JTAG for CPU	Common	in	-	
T4	Reserved	-	-	-	-	
T5	Reserved	-	-	-	-	
T6	3.3V	-	-	-	-	VCCQ
T7	Reserved	-	-	-	-	
T8	Reserved	-	-	-	-	
T9	1.2V	-	-	-	-	VDD
T10	GND	-	-	-	-	VSS,VSSQ
T11	1.2V	-	-	-	-	VDD
T12	GND	-	-	-	-	VSS,VSSQ
T13	1.2V	-	-	-	-	VDD
T14	GND	-	-	-	-	VSS,VSSQ
T15	1.2V	-	-	-	-	VDD

Table 4-3. Pin-outs and Pin Functions (6/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
T16	GND	-	-	-	-	VSS,VSSQ
T17	fet_miitx_txd2_1	Ethernet	Common	out	8mA	
T18	avd_miirx_rxd1_1	Ethernet	Common	in	-	
T19	3.3V	-	-	-	-	VCCQ
T20	avd_miirx_rxd2_1	Ethernet	Common	in	-	
T21	clk_miirx_clk_0	Ethernet	Common	in	-	
T22	fet_miitx_txd0_1	Ethernet	Common	out	8mA	
T23	avd_miirx_rxd3_1	Ethernet	Common	in	-	
T24	3.3V	-	-	-	-	VCCQ
U1	3.3V	-	-	-	-	VCCQ
U2	Reserved	-	-	-	-	
U3	Reserved	-	-	-	-	
U4	Reserved	-	-	-	-	
U5	Reserved	-	-	-	-	
U6	GND	-	-	-	-	VSS,VSSQ
U7	Reserved	-	-	-	-	
U8	TIC0_CPU0_2/PORT_K(4)	CMTW	CPU0	inout	8mA	
U9	TOC0_CPU1_1/PORT_L(1)	CMTW	CPU1	inout	8mA	
U10	1.2V	-	-	-	-	VDD
U11	GND	-	-	-	-	VSS,VSSQ
U12	1.2V	-	-	-	-	VDD
U13	1.2V	-	-	-		VDD
U14	1.2V	-	-	-	-	VDD
U15	GND	-	-	-	-	VSS,VSSQ
U16	1.2V	-	-	-	-	VDD
U17	fet_miitx_txd1_1	Ethernet	Common	out	8mA	
U18	fec_miimg_crxmdc_1	Ethernet	Common	out	8mA	
U19	GND	-	-	-	-	VSS,VSSQ
U20	fet_miitx_txd3_1	Ethernet	Common	out	8mA	
U21	fet_miitx_en_1	Ethernet	Common	out	8mA	
U22	3.3V	-	-	-	-	VCCQ
U23	clk_gptp_extern_0	Ethernet	Common	in	-	gPTP function
U24	1.2V	-	-	-	-	VDD
V1	GND	-	-	-	-	VSS,VSSQ
V2	Reserved	-	-	-	-	
V3	Reserved	-	-	-	-	
V4	Reserved	-	-	-	-	
V5	Reserved	-	-	-	-	
V6	Reserved	-	-	-	-	
V7	TMRI0_CPU1/PORT_J(2)	TMR	CPU1	inout	8mA	Shared pins with TMRI1_CPU1
V8	TIC1_CPU0_1/PORT_K(2)	CMTW	CPU0	inout	8mA	
V9	TOC1_CPU0_2/PORT_K(7)	CMTW	CPU0	inout	8mA	
V10	TOC1_CPU1_2/PORT_L(7)	CMTW	CPU1	inout	8mA	
V11	SS1_0#/CTS1_0#/ RTS1_0#/PORT_H(1)	SCI	CPU1	inout	8mA	
V12	TXD0_CPU1/PORT_H(3)	SCI	CPU1	inout	8mA	TXD0_1/SDA0_1/MOSI0_1
V13	TXD1_CPU1/PORT_H(7)	SCIF	CPU1	inout	8mA	TXD1_1/SDA1_1/MOSI1_1
V14	RSPCK/PORT_C(5)	SPI	CPU0	inout	8mA	
V15	SSL1/PORT_D(2)	SPI	CPU1	inout	8mA	
V16	GTIOC2A/PORT_A(5)	GPT	CPU0	inout	8mA	
V17	GTIOC3A/PORT_A(7)	GPT	CPU0	inout	8mA	
V18	fec_miimg_cxrmdo/mdi_1	Ethernet	Common	inout	8mA	
V19	avd_miirx_err_0	Ethernet	Common	in	-	
V20	fet_miitx_err_0	Ethernet	Common	out	8mA	
V21	avb_pt_capture_0	Ethernet	Common	in	-	gPTP function
V22	GND	-	-	-	-	VSS,VSSQ
V23	avd_miirx_rxd0_0	Ethernet	Common	in	-	
V24	GND	-	-	-	-	VSS,VSSQ
W1	1.2V	-	-	-	-	VDD
W2	Reserved	-	-	-	-	
W3	Reserved	-	-	-	-	
W4	Reserved	-	-	-	-	
W5	Reserved	-	-	-	-	
W6	TMRI0_CPU0/PORT_I(2)	TMR	CPU0	inout	8mA	Shared pins with TMRI1_CPU0
W7	TMO0_CPU1/PORT_J(0)	TMR	CPU1	inout	8mA	
W8	3.3V	-	-	-	-	VCCQ
W9	GND	-	-	-	-	VSS,VSSQ
W10	TOC0_CPU1_2/PORT_L(5)	CMTW	CPU1	inout	8mA	
W11	TXD0_CPU0/PORT_G(3)	SCI	CPU0	inout	8mA	TXD0_0/SDA0_0/MOSI0_0
W12	3.3V	-	-	-	-	VCCQ
W13	GND	-	-	-	-	VSS,VSSQ
W14	MOSI/PORT_C(3)	SPI	CPU0	inout	8mA	
W15	SSL3/PORT_D(0)	SPI	CPU1	inout	8mA	
W16	3.3V	-	-	-	-	VCCQ
W17	GND	-	-	-	-	VSS,VSSQ
W18	GTIOC0B/PORT_B(2)	GPT	CPU1	inout	8mA	
W19	avd_miirx_dv_0	Ethernet	Common	in	-	

Table 4-3. Pin-outs and Pin Functions (7/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
W20	avd_miitx_col_0	Ethernet	Common	in	-	
W21	clk_miitx_clk_0	Ethernet	Common	in	-	
W22	avd_miitx_crs_0	Ethernet	Common	in	-	
W23	fet_miitx_txd2_0	Ethernet	Common	out	8mA	
W24	1.2V	-	-	-	-	VDD
Y1	1.2V	-	-	-	-	VDD
Y2	Reserved	-	-	-	-	
Y3	Reserved	-	-	-	-	
Y4	Reserved	-	-	-	-	
Y5	SCL1（FM+)/PORT_F(0)	I2C	CPU1	inout	8mA	For the I2C function, output is LOW / High-Z.
Y6	TMO0_CPU0/PORT_I(0)	TMR	CPU0	inout	8mA	
Y7	TMO1_CPU1/PORT_J(3)	TMR	CPU1	inout	8mA	
Y8	TOC0_CPU0_1/PORT_K(1)	CMTW	CPU0	inout	8mA	
Y9	TOC0_CPU0_2/PORT_K(5)	CMTW	CPU0	inout	8mA	
Y10	TOC1_CPU1_1/PORT_L(3)	CMTW	CPU1	inout	8mA	
Y11	SS0_0#/CTS0_0#/RTS0_0#/PORT_G(1)	SCI	CPU0	inout	8mA	
Y12	SS0_1#/CTS0_1#/RTS0_1#/PORT_G(5)	SCIF	CPU0	inout	8mA	
Y13	SS1_1#/CTS1_1#/RTS1_1#/PORT_H(5)	SCIF	CPU1	inout	8mA	
Y14	SSL2/PORT_C(1)	SPI	CPU0	inout	8mA	
Y15	SSL2/PORT_D(1)	SPI	CPU1	inout	8mA	
Y16	SSL0/PORT_D(6)	SPI	CPU1	inout	8mA	
Y17	GTIOC1A/PORT_A(3)	GPT	CPU0	inout	8mA	
Y18	GTETRG/PORT_B(0)	GPT	CPU1	inout	8mA	Channels 1 to 4 (common)
Y19	GTIOC2B/PORT_B(6)	GPT	CPU1	inout	8mA	
Y20	fet_miitx_en_0	Ethernet	Common	out	8mA	
Y21	fet_miitx_txd0_0	Ethernet	Common	out	8mA	
Y22	avd_miirx_rxd1_0	Ethernet	Common	in	-	
Y23	avd_miirx_rxd2_0	Ethernet	Common	in	-	
Y24	3.3V	-	-	-	-	VCCQ
AA1	3.3V	-	-	-	-	VCCQ
AA2	Reserved	-	-	-	-	
AA3	Reserved	-	-	-	-	
AA4	CTX1	CAN	CPU1	out	8mA	
AA5	SCL0 (FM+) / PORT_E(0)	I2C	CPU0	inout	8mA	For the I2C function, output is LOW / High-Z.
AA6	3.3V	-	-	-	-	VCCQ
AA7	GND	-	-	-	-	VSS,VSSQ
AA8	TIC1_CPU0_2/PORT_K(6)	CMTW	CPU0	inout	8mA	
AA9	TIC0_CPU1_2/PORT_L(4)	CMTW	CPU1	inout	8mA	
AA10	3.3V	-	-	-	-	VCCQ
AA11	GND	-	-	-	-	VSS,VSSQ
AA12	RXD1_CPU0/PORT_G(6)	SCIF	CPU0	inout	8mA	RXD1_0/SCL1_0/MISO1_0
AA13	TXD1_CPU0/PORT_G(7)	SCIF	CPU0	inout	8mA	TXD1_0/SDA1_0/MOSI1_0
AA14	3.3V	-	-	-	-	VCCQ
AA15	GND	-	-	-	-	VSS,VSSQ
AA16	MISO/PORT_D(4)	SPI	CPU1	inout	8mA	
AA17	GTIOC0A/PORT_A(1)	GPT	CPU0	inout	8mA	
AA18	GTIOC3B/PORT_A(8)	GPT	CPU0	inout	8mA	
AA19	GTIOC1B/PORT_B(4)	GPT	CPU1	inout	8mA	
AA20	fec_miimg_crxmdc_0	Ethernet	Common	out	8mA	
AA21	avd_miirx_rxd3_0	Ethernet	Common	in	-	
AA22	fet_miitx_txd1_0	Ethernet	Common	out	8mA	
AA23	fet_miitx_txd3_0	Ethernet	Common	out	8mA	
AA24	1.2V	-	-	-	-	VDD
AB1	GND	-	-	-	-	VSS,VSSQ
AB2	GND	-	-	-	-	VSS,VSSQ
AB3	GND	-	-	-	-	VSS,VSSQ
AB4	CTX0	CAN	CPU0	out	8mA	
AB5	SDA0 (FM+) / PORT_E(1)	I2C	CPU0	inout	8mA	For the I2C function, output is LOW / High-Z.
AB6	TMCI0_CPU0/PORT_I(1)	TMR	CPU0	inout	8mA	Shared pins with TMCI1_CPU0
AB7	TMCI0_CPU1/PORT_J(1)	TMR	CPU1	inout	8mA	Shared pins with TMCI1_CPU1
AB8	TOC1_CPU0_1/PORT_K(3)	CMTW	CPU0	inout	8mA	
AB9	TIC1_CPU1_1/PORT_L(2)	CMTW	CPU1	inout	8mA	
AB10	SCK0_CPU0/PORT_G(0)	SCI	CPU0	inout	8mA	
AB11	SCK0_CPU1/PORT_H(0)	SCI	CPU1	inout	8mA	
AB12	SCK1_CPU0/PORT_G(4)	SCIF	CPU0	inout	8mA	
AB13	RXD1_CPU1/PORT_H(6)	SCIF	CPU1	inout	8mA	RXD1_1/SCL1_1/MISO1_1
AB14	SSL1/PORT_C(2)	SPI	CPU0	inout	8mA	
AB15	SSL0/PORT_C(6)	SPI	CPU0	inout	8mA	
AB16	RSPCK/PORT_D(5)	SPI	CPU1	inout	8mA	
AB17	GTIOC0B/PORT_A(2)	GPT	CPU0	inout	8mA	
AB18	GTIOC2B/PORT_A(6)	GPT	CPU0	inout	8mA	
AB19	GTIOC1A/PORT_B(3)	GPT	CPU1	inout	8mA	
AB20	GTIOC3B/PORT_B(8)	GPT	CPU1	inout	8mA	
AB21	fec_miimg_cxrmdo/mdi_0	Ethernet	Common	inout	8mA	

Table 4-3. Pin-outs and Pin Functions (8/8)

CBGA Pin No.	Pin name	Function	CPU	Input / output direction	Drive capability	Remarks
AB22	GND	-	-	-	-	VSS,VSSQ
AB23	GND	-	-	-	-	VSS,VSSQ
AB24	GND	-	-	-	-	VSS,VSSQ
AC1	GND	-	-	-	-	VSS,VSSQ
AC2	GND	-	-	-	-	VSS,VSSQ
AC3	GND	-	-	-	-	VSS,VSSQ
AC4	CRX0	CAN	CPU0	in	-	
AC5	CRX1	CAN	CPU1	in	-	
AC6	SDA1(FM+)/PORT_F(1)	I2C	CPU1	inout	8mA	For the I2C function, output is Low / High-Z.
AC7	TMO1_CPU0/PORT_I(3)	TMR	CPU0	inout	8mA	
AC8	TIC0_CPU0_1/PORT_K(0)	CMTW	CPU0	inout	8mA	
AC9	TIC0_CPU1_1/PORT_L(0)	CMTW	CPU1	inout	8mA	
AC10	TIC1_CPU1_2/PORT_L(6)	CMTW	CPU1	inout	8mA	
AC11	RXD0_CPU0/PORT_G(2)	SCI	CPU0	inout	8mA	RXD0_0/SCL0_0/MISO0_0
AC12	RXD0_CPU1/PORT_H(2)	SCI	CPU1	inout	8mA	RXD0_1/SCL0_1/MISO0_1
AC13	SCK1_CPU1/PORT_H(4)	SCIF	CPU1	inout	8mA	
AC14	SSL3/PORT_C(0)	SPI	CPU0	inout	8mA	
AC15	MISO/PORT_C(4)	SPI	CPU0	inout	8mA	
AC16	MOSI/PORT_D(3)	SPI	CPU1	inout	8mA	
AC17	GTETRG/PORT_A(0)	GPT	CPU0	inout	8mA	Channels 1 to 4 (common)
AC18	GTIOC1B/PORT_A(4)	GPT	CPU0	inout	8mA	
AC19	GTIOC0A/PORT_B(1)	GPT	CPU1	inout	8mA	
AC20	GTIOC2A/PORT_B(5)	GPT	CPU1	inout	8mA	
AC21	GTIOC3A/PORT_B(7)	GPT	CPU1	inout	8mA	
AC22	GND	-	-	-	-	VSS,VSSQ
AC23	GND	-	-	-	-	VSS,VSSQ
AC24	GND	-	-	-	-	VSS,VSSQ
AD2	GND	-	-	-	-	VSS,VSSQ
AD3	GND	-	-	-	-	VSS,VSSQ
AD4	1.2V	-	-	-	-	VDD
AD5	3.3V	-	-	-	-	VCCQ
AD6	1.2V	-	-	-	-	VDD
AD7	GND	-	-	-	-	VSS,VSSQ
AD8	1.2V	-	-	-	-	VDD
AD9	3.3V	-	-	-	-	VCCQ
AD10	GND	-	-	-	-	VSS,VSSQ
AD11	1.2V	-	-	-	-	VDD
AD12	1.2V	-	-	-	-	VDD
AD13	GND	-	-	-	-	VSS,VSSQ
AD14	3.3V	-	-	-	-	VCCQ
AD15	1.2V	-	-	-	-	VDD
AD16	1.2V	-	-	-	-	VDD
AD17	3.3V	-	-	-	-	VCCQ
AD18	GND	-	-	-	-	VSS,VSSQ
AD19	1.2V	-	-	-	-	VDD
AD20	1.2V	-	-	-	-	VDD
AD21	3.3V	-	-	-	-	VCCQ
AD22	GND	-	-	-	-	VSS,VSSQ
AD23	GND	-	-	-	-	VSS,VSSQ

4.2 Mechanical and Thermal Characteristics

The mechanical and thermal (environmental resistance) characteristics specified in the detail specification are listed in Table 4-4.

Table 4-4. Mechanical and Thermal Characteristics

Item		Performances
Temperature	Temperature cycling	10 minutes each at -65°C and +150°C, 100 cycles
	Thermal shock	5 minutes at -55°C and +125°C, 15 cycles
	Solderability	(1) Within the temperature profile range for reference specified in paragraph 5.7.1, “Total heating process” (Sn63/Pb37 or Sn60/Pb40 solder alloys specified in “IV Actual heating period” in Table 5-3 of JERG-0-043E are applied). (2) The number of heating cycles is two.
Moisture resistance		80%RH to 98%RH, -10°C to +65°C, 10 cycles
Mechanical Environment	Vibration	20Hz to 2000Hz, 20G, four minutes/times, four times/direction, three directions (X, Y and Z) (1)
	Shock	1500G, 0.5ms, five times, six directions (X1, X2, Y1, Y2, Z1 and Z2) (1)
	Constant acceleration	5000G, one minute, Y1 direction (1)
	Solder ball pull test	JESD22-B115A (Pull strength requirements are as follows) (1) For eutectic solder ball: 40.0MPa as a minimum. (2) For high-temperature solder ball: 19.7MPa as a minimum.
Others	Electrostatic discharge sensitivity test	(1) HBM MIL-STD-883L Method 3015.9 (ANSI/ESDA/JEDEC JS-001) Discharge capacitance: 100pF, discharge resistance: 1.5kΩ, ±2000V (2) MM JEDEC JESD22-A115C Discharge capacitance: 200pF, discharge resistance: 0Ω, ±300V (3) CDM ANSI/ESDA/JEDEC JS-002-2018 ±750V

Note:

(1) The definition of direction shall be in accordance with paragraph C.2.2, Appendix C of JAXA-QTS-2010D.

5. CHARACTERISTICS IN VARIOUS ENVIRONMENTS

Results of qualification tests for JAXA-developed parts using QM and characteristics evaluation tests are as follows.

a) Electrical characteristics
Output characteristics (VOH/L) are shown in Figure 5-1.

b) Current consumption
Temperature characteristics of quiescent power supply current (IDDQ) are shown in Figure 5-2.
Frequency characteristics of current consumption (in operation) are shown in Figure 5-3.
Temperature characteristics of current consumption (in operation) are shown in Figure 5-4.
Design values of current consumption are shown in Table 5-1.
Frequency characteristics and temperature characteristics of power consumption (in CoreMark execution) are as follows.
   1) 1-core, Coremark execution (CPU0: CoreMark execution, CPU1: sleep)
   T_j=40°C: Figure 5-5, T_j= room temperature: Figure 5-6. T_j=+125°C: Figure 5-7
   2) 2-core, CoreMark execution
   T_j=40°C: Figure 5-8, T_j= room temperature: Figure 5-9. T_j=+125°C: Figure 5-10

c) Measurement results of input and output characteristics (VIH/L and VOH/L) and current consumption (IDDQ) at screening (Burn-in test (+125°C, 240 hours)) and qualification tests for JAXA-developed parts, group C, subgroup 1 (Steady state life test (+125°C, 2000 hours)) are shown in Figures 5-11 to 5-13.

d) Measurement results of input and output characteristics (VIH/L and VOH/L) and current consumption (IDDQ) at qualification tests for JAXA-developed parts, group E tests, subgroup 1 (Steady state total ionizing dose test (TID test)) are shown in Figures 5-14 to 5-16.

e) SEE resistance at qualification tests for JAXA-developed parts, group E tests, subgroup 2 (Single event test) is shown in Table 5-2.
   1) Test conditions are shown in Table 5-4.
   2) Cross section curve and cross section of No.1 SEU (1) (without scrubbing) in Table 5-4 are shown in Figure 5-17 and Table 5-5, respectively.
   3) The comparison between the calculated values and test results for No.2 SEU (2) (with scrubbing) in Table 5-4 is shown in Figure 5-18.
   The calculated value indicates the number of SEUs occurring in the SRAM when the scrubbing function operates as required (the number of occurrences where 2 or more bits per word of SEUs occur that are not repairable by read-modify-write). Since the calculated values match the test results, it is considered that the scrubbing function worked as required in the sample.
   4) Cross section curve and cross section of No.3 SEU (3) (logic section) in Table 5-4 are shown in Figure 5-19 and Table 5-6, respectively.
   5) For test results of No.4 SEL in Table 5-4, no errors were detected at LET = 88 (MeV/(mg/cm^2)).

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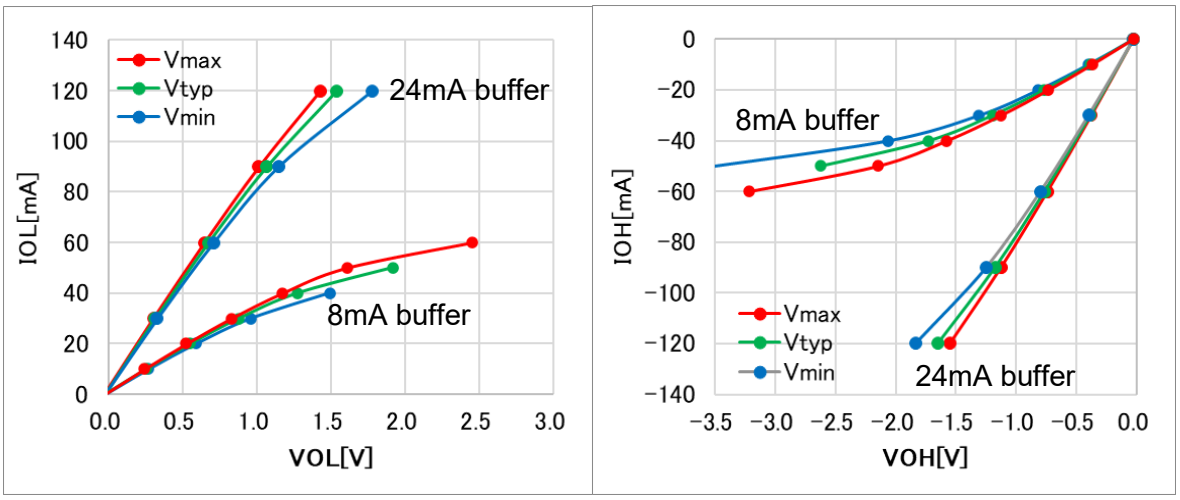
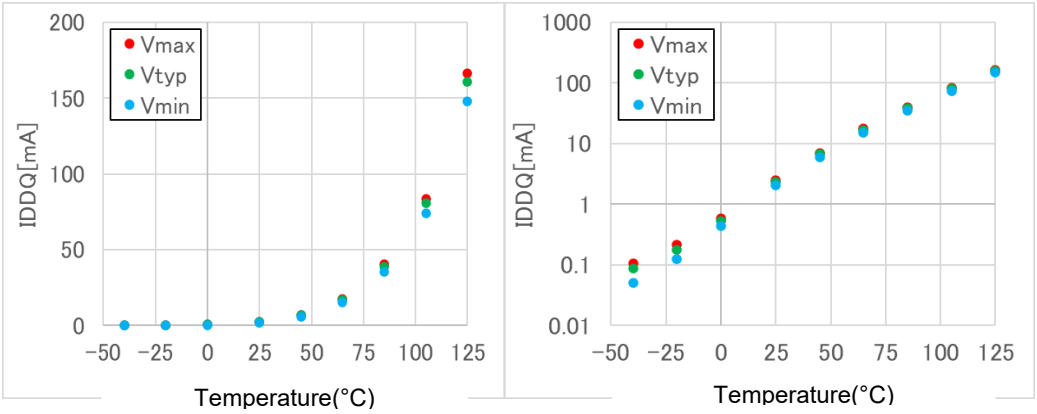
f) Proton resistance at various characteristics evaluation tests are shown in Figure 5-20 and Table 5-6.



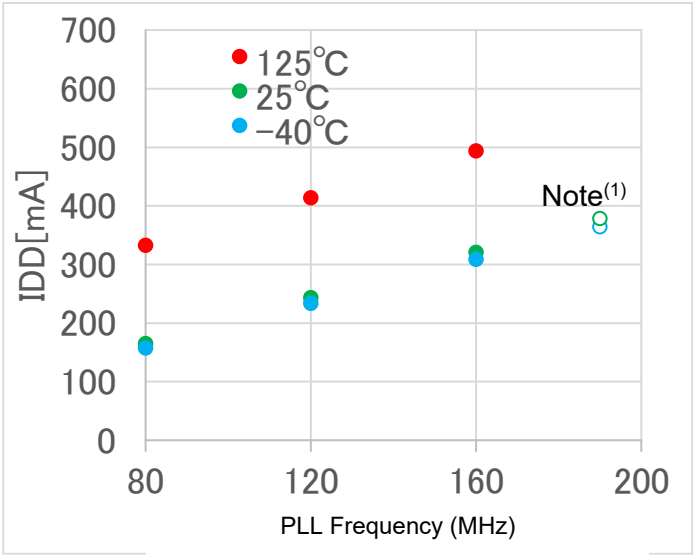
(a) VOL-IOL Characteristics (b) VOH-IOH Characteristics

Figure 5-1. Output Characteristics (VOH/L)



(a) Linear scale on the vertical axis. (b) Logarithmic scale on the vertical axis.

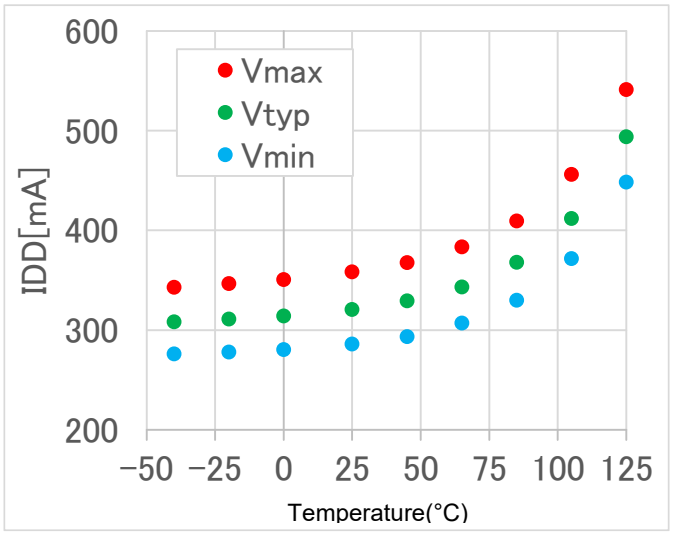
Figure 5-2. Temperature Characteristics of Quiescent Current



Vtyp (VCCQ=3.3V, VDD=1.2V), Entire MPU (using 2 cores)

Note: (1) Extrapolated values of the 190 MHz IDD at 25°C and -40°C

Figure 5-3. Frequency Characteristics of VDD Current Consumption (in Operation)



160MHz, Entire MPU (using 2 cores)

Note: Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),

Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V)

Figure 5-4. Temperature Characteristics of VDD Current Consumption (in Operation)

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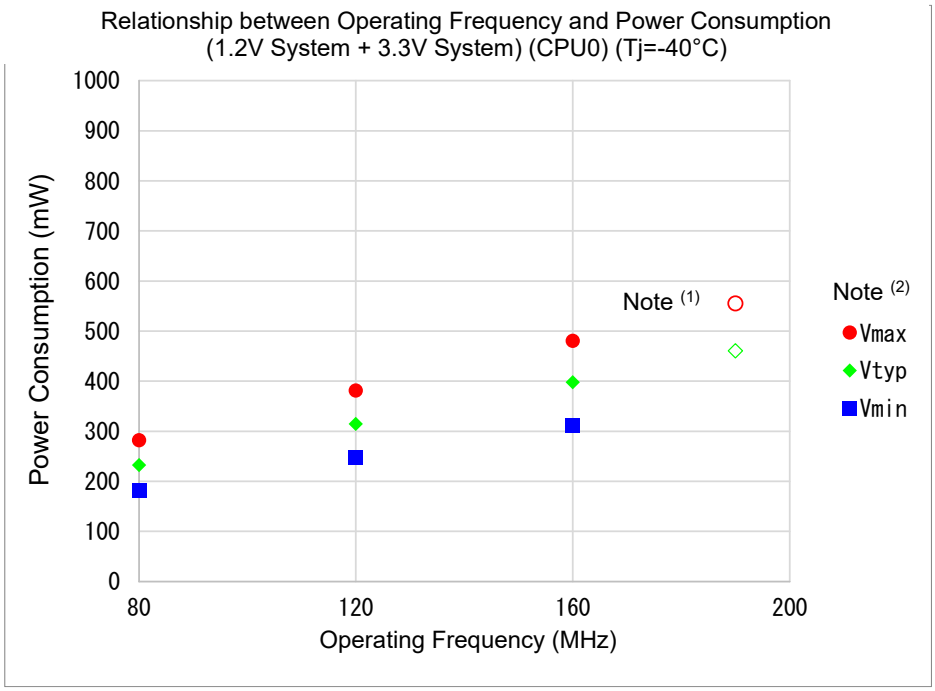
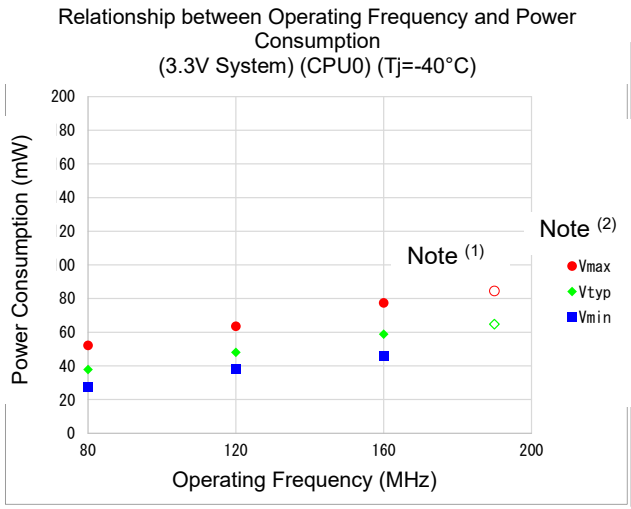
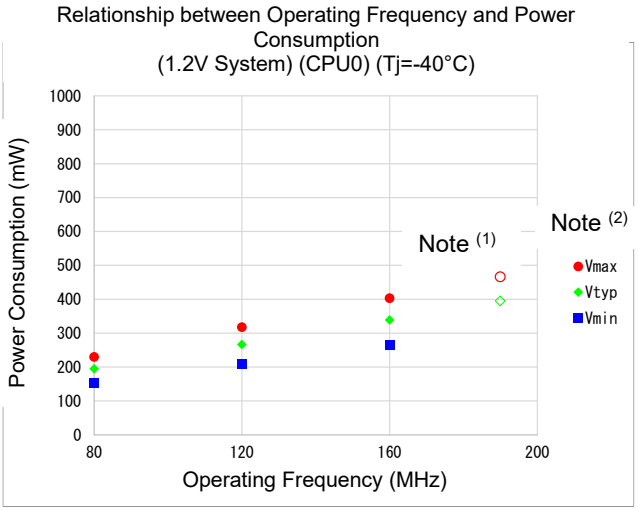
Table 5-1. Design Values of Current Consumption

Item	Symbol	Conditions	Min.	Typ.	Max	Unit	Remarks
Quiescent current	IDDQ(VDD)	VDD=1.2V, Tj=25°C	-	2.4	-	mA	Design value
		VDD=1.29V, Tj=125°C	-	-	416	mA	Design value
	IDDQ(VCCQ)	VCCQ=3.6V, Tj=125°C	-	-	40	uA	Design value
Operating current	IDD(VCCQ)	VCCQ=3.6V, Tj=125°C	-	-	45	mA	Design value







Notes: (1) Extrapolated values of the 190 MHz IDD at 25°C and -40°C.

Notes: (2) Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-5. Power Consumption (CoreMark Execution)
(1-core, CoreMark Execution, Tj = -40°C)

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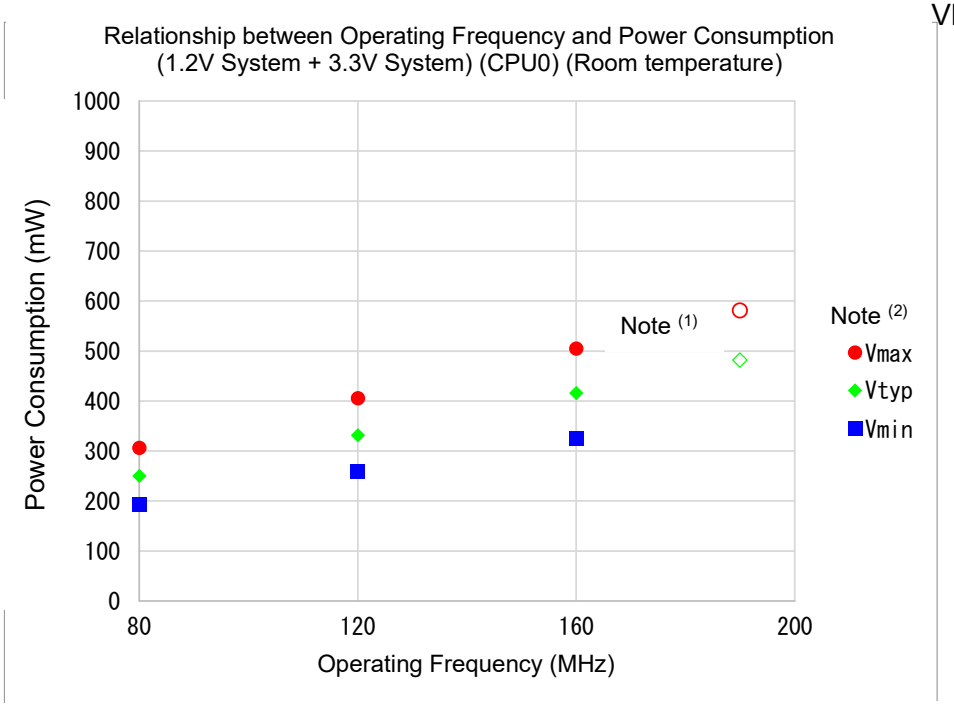

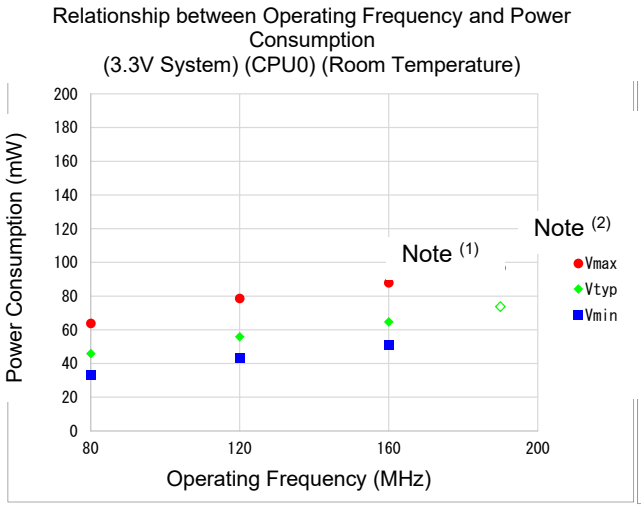

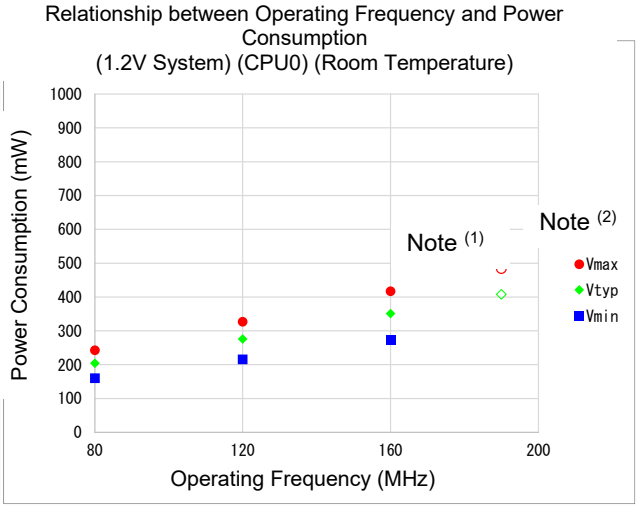

Notes: (1) Extrapolated values of the 190 MHz IDD at 25°C and -40°C.

Notes: (2) Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-6. Power Consumption (CoreMark Execution)
(1-core, CoreMark Execution, Tj = Room Temperature)

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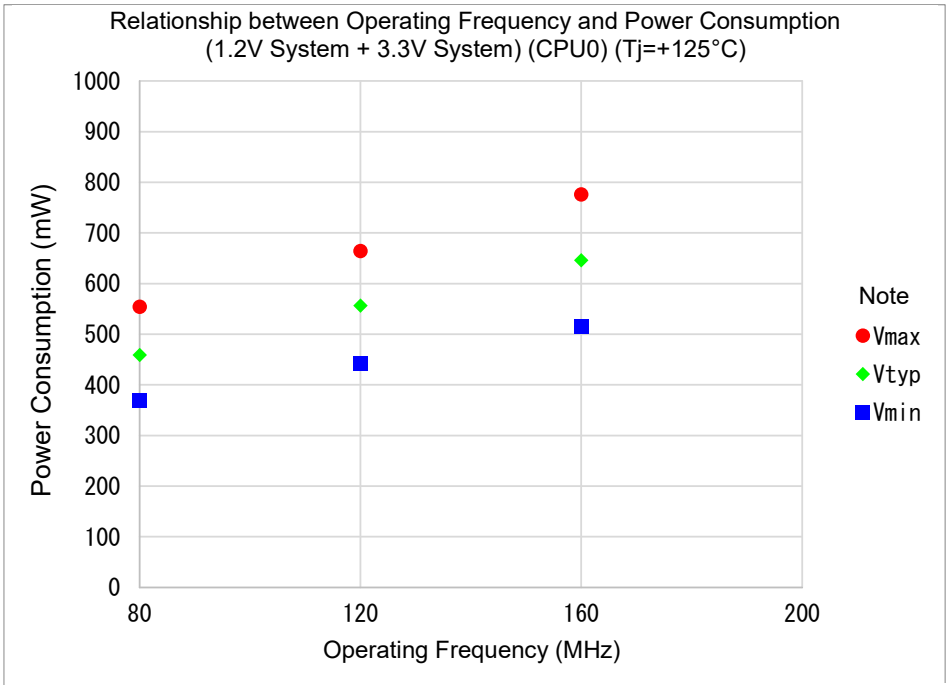
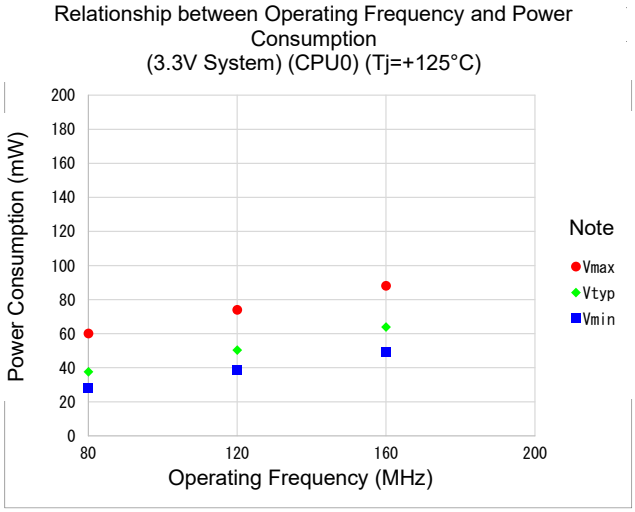
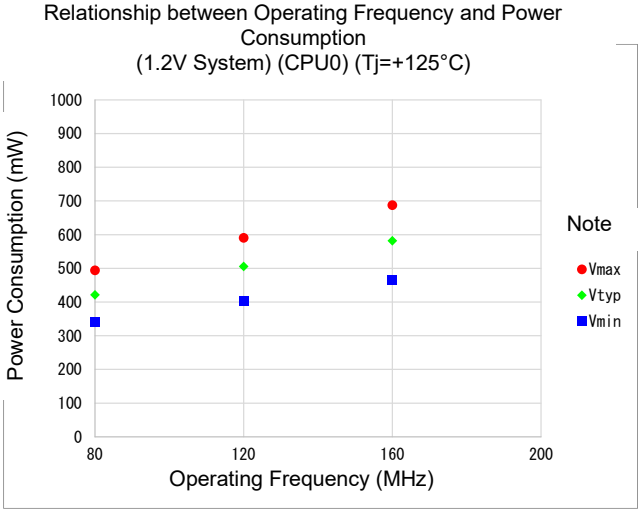
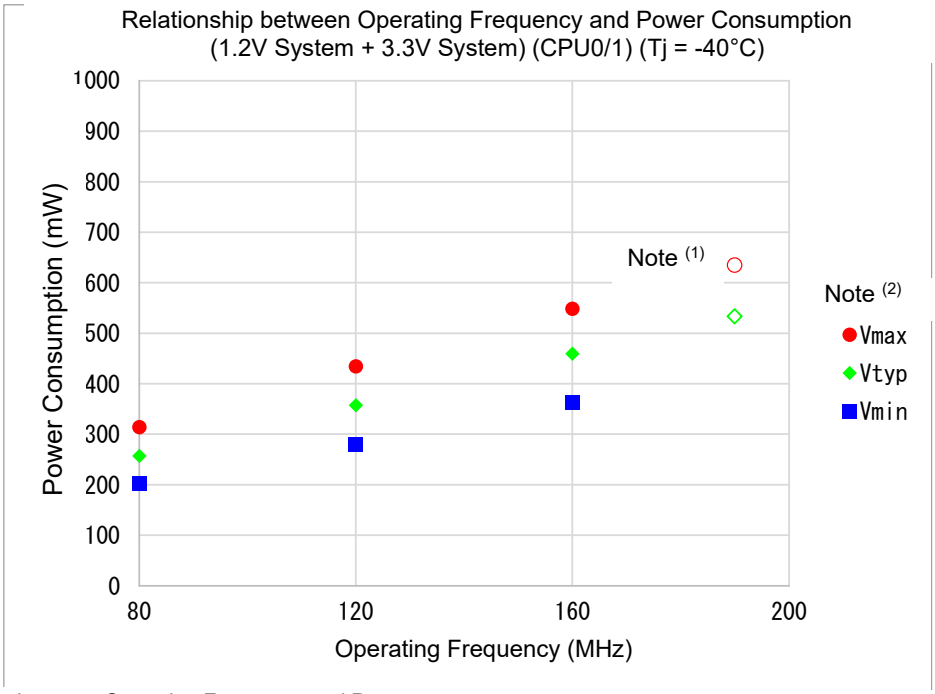


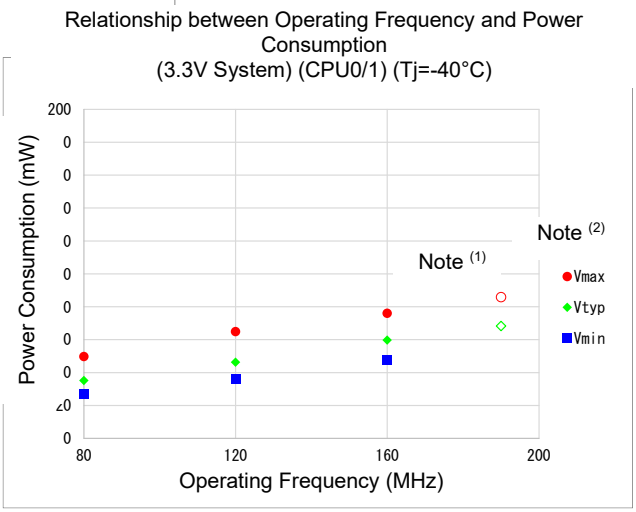


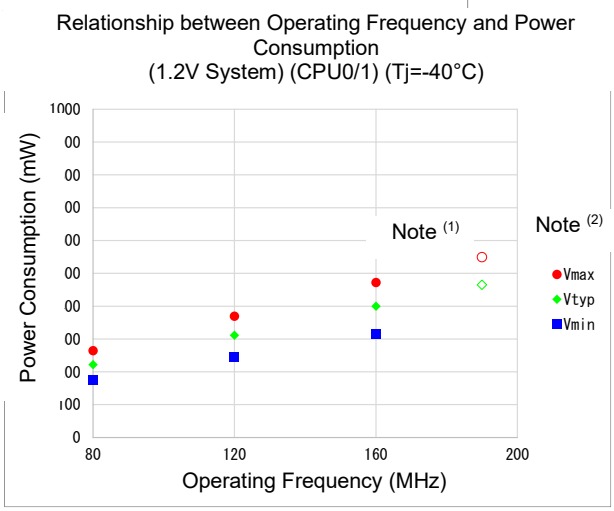


Note: Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-7. Power Consumption (CoreMark Execution)
(1-core, CoreMark Execution, Tj = +125°C)



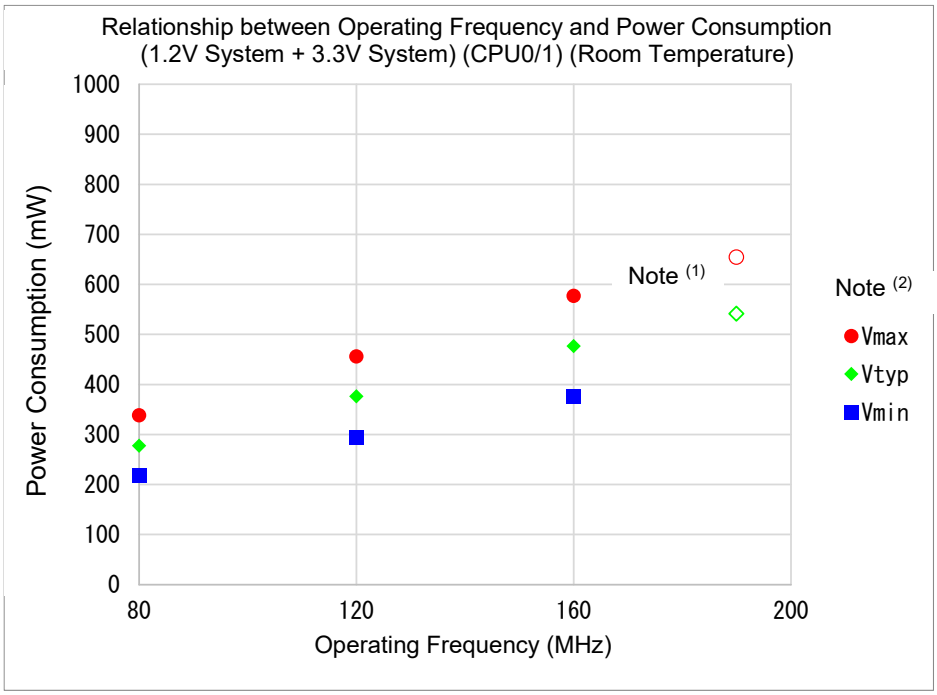


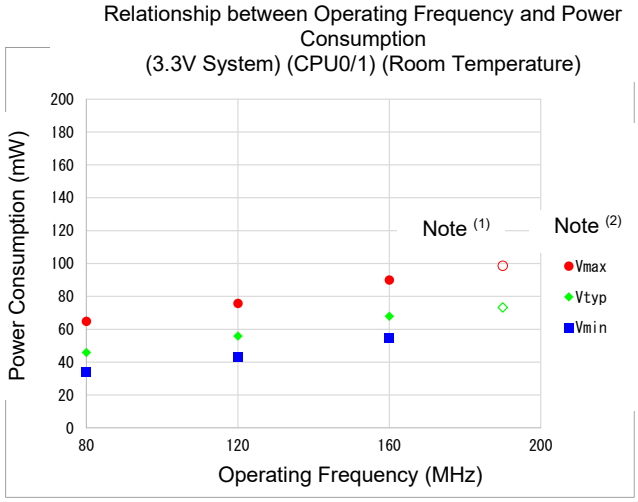


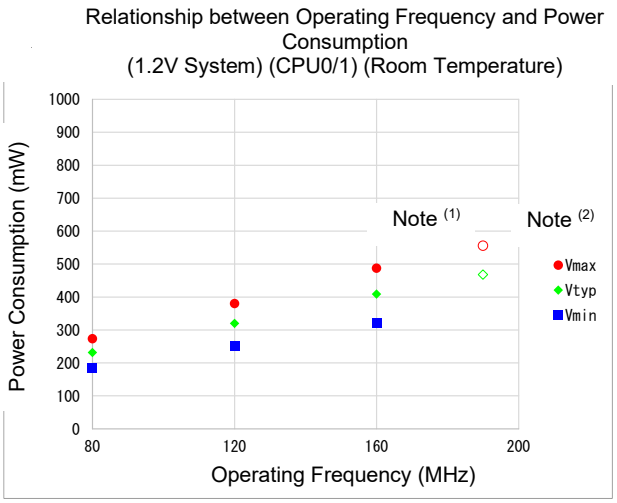
Notes: (1) Extrapolated values of the 190 MHz IDD at 25°C and -40°C.

Notes: (2) Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-8. Power Consumption (CoreMark Execution)
(2-core, CoreMark Execution, Tj = -40°C)







Notes: (1) Extrapolated values of the 190 MHz IDD at 25°C and -40°C.

Notes: (2) Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-9. Power Consumption (CoreMark Execution)
(2-core, CoreMark Execution, Tj = Room Temperature)

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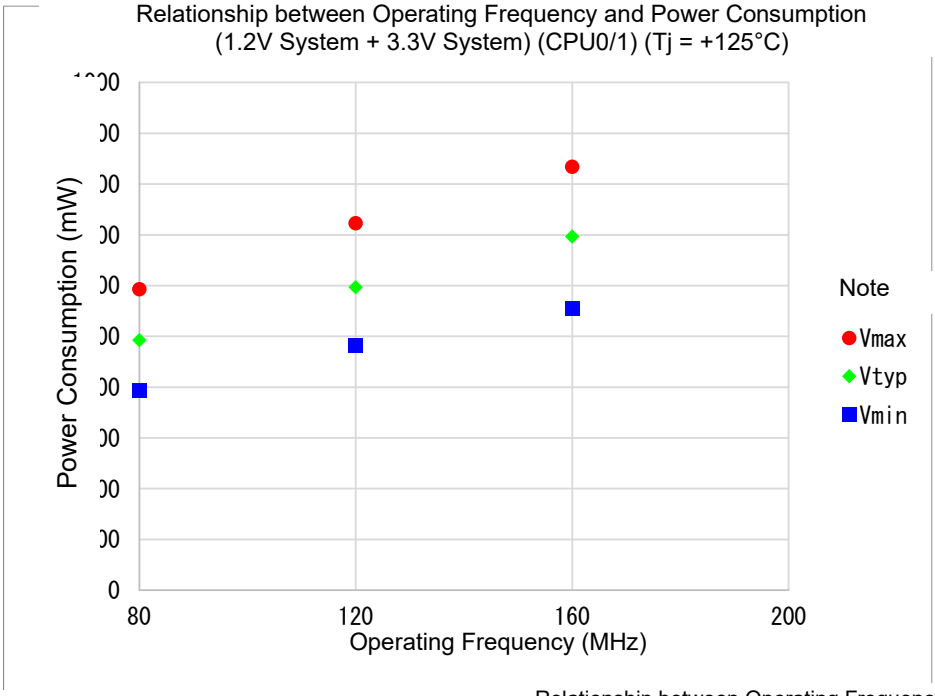
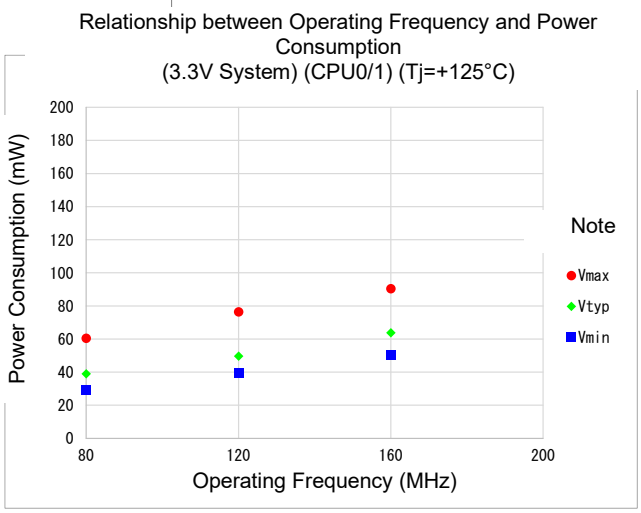
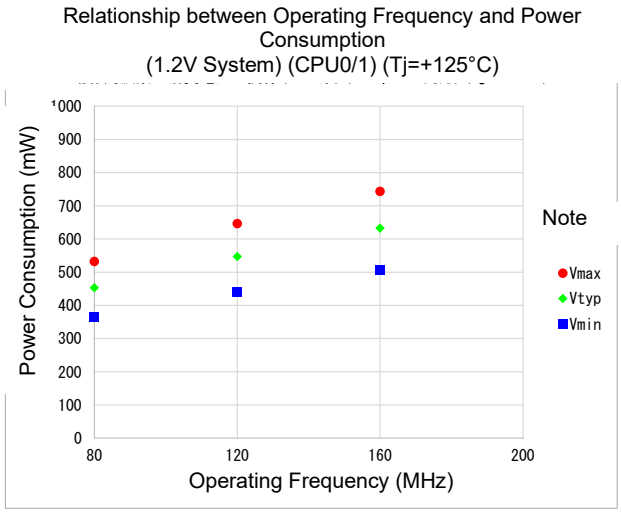
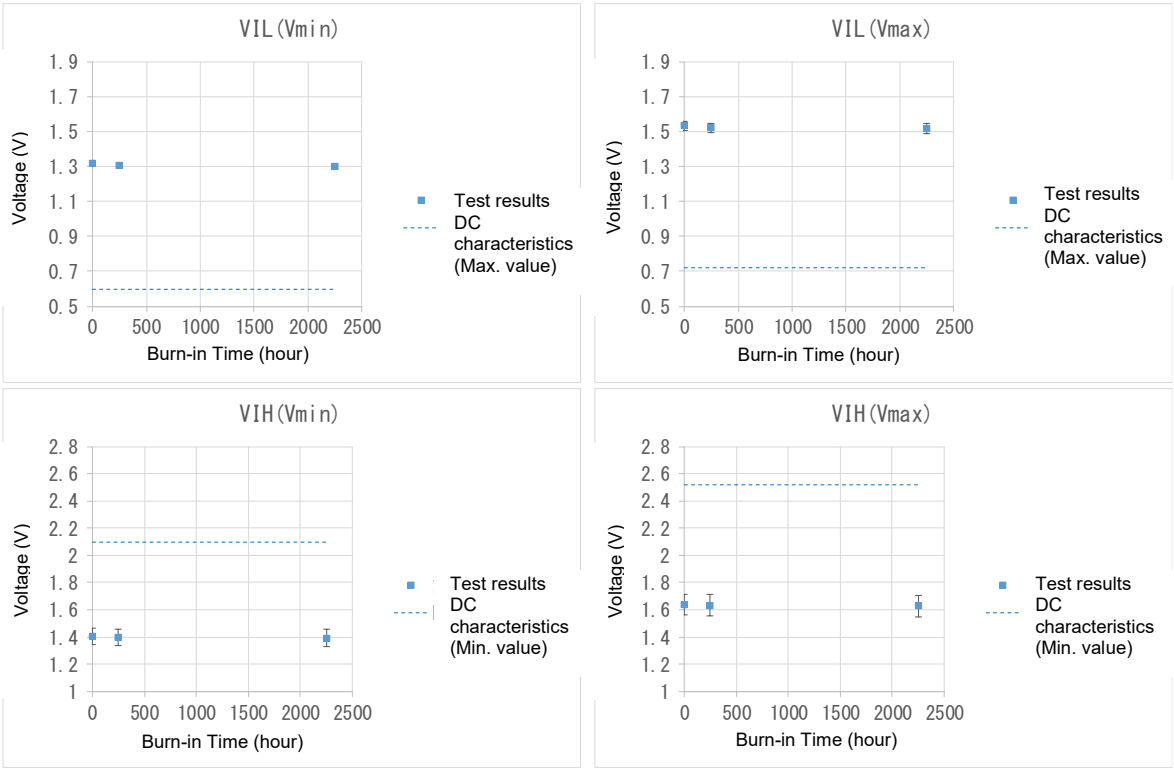






Note: Power supply voltage condition: Vmax (VCCQ=3.6V, VDD=1.29V),
Vtyp (VCCQ=3.3V, VDD=1.2V), Vmin (VCCQ=3.0V, VDD=1.11V).

Figure 5-10. Power Consumption (CoreMark Execution)
(2-core, CoreMark Execution, Tj = +125°C)



Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-11. Input Characteristics (VIL/VIH) at Screening (Burn-in) and Group C, Subgroup 1 Test (Steady State Life Test)

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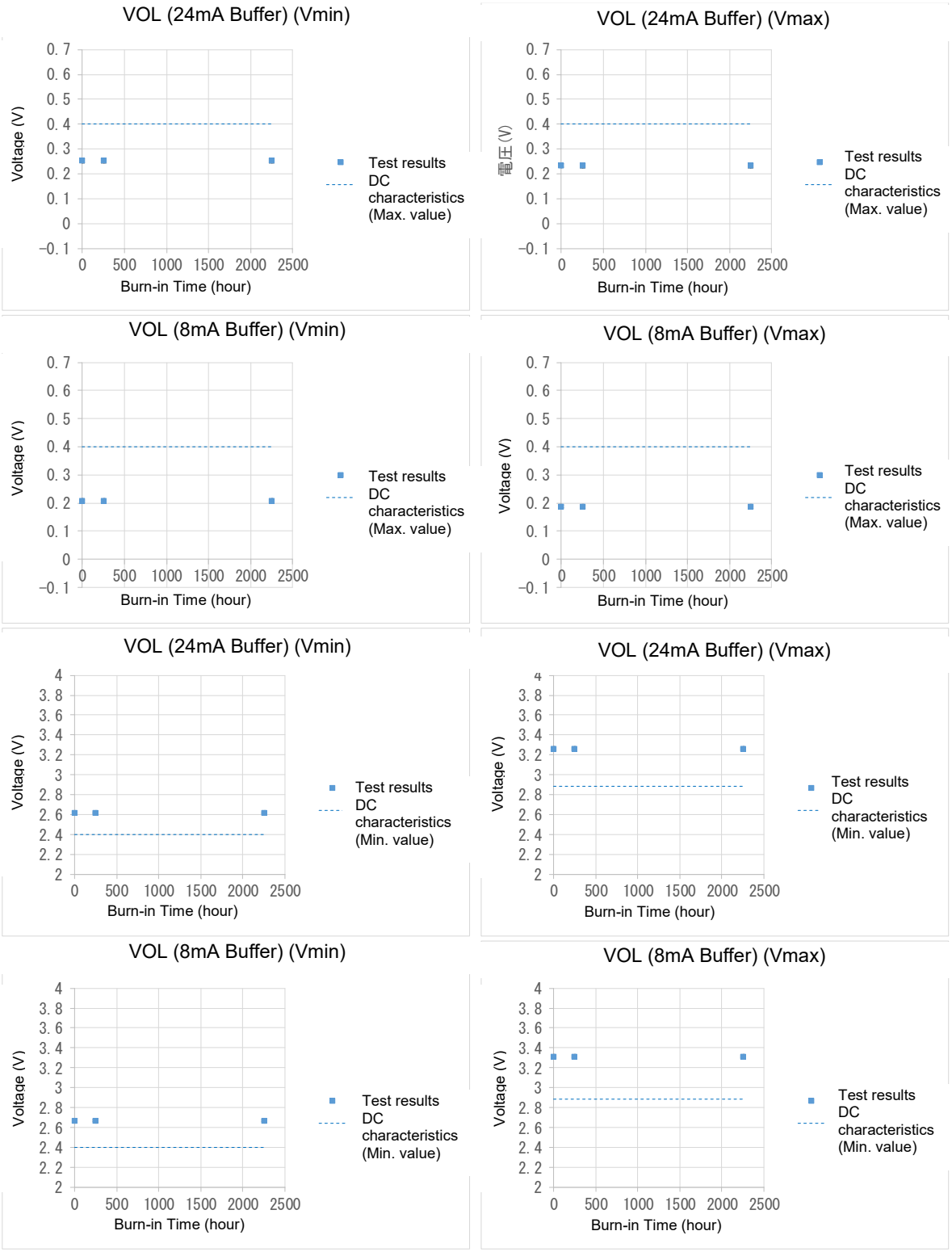
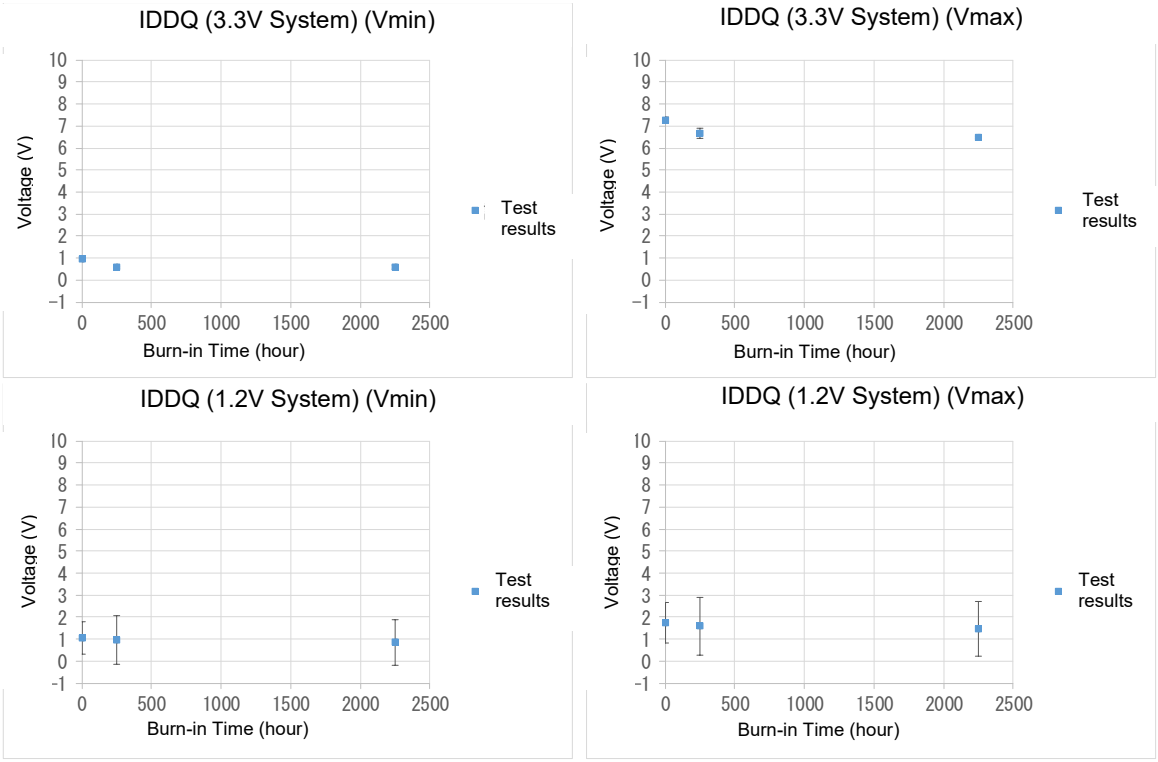


Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-12. Output Characteristics (VOL/VOH) at Screening (Burn-in) and Group C, Subgroup 1 Test (Steady State Life Test)

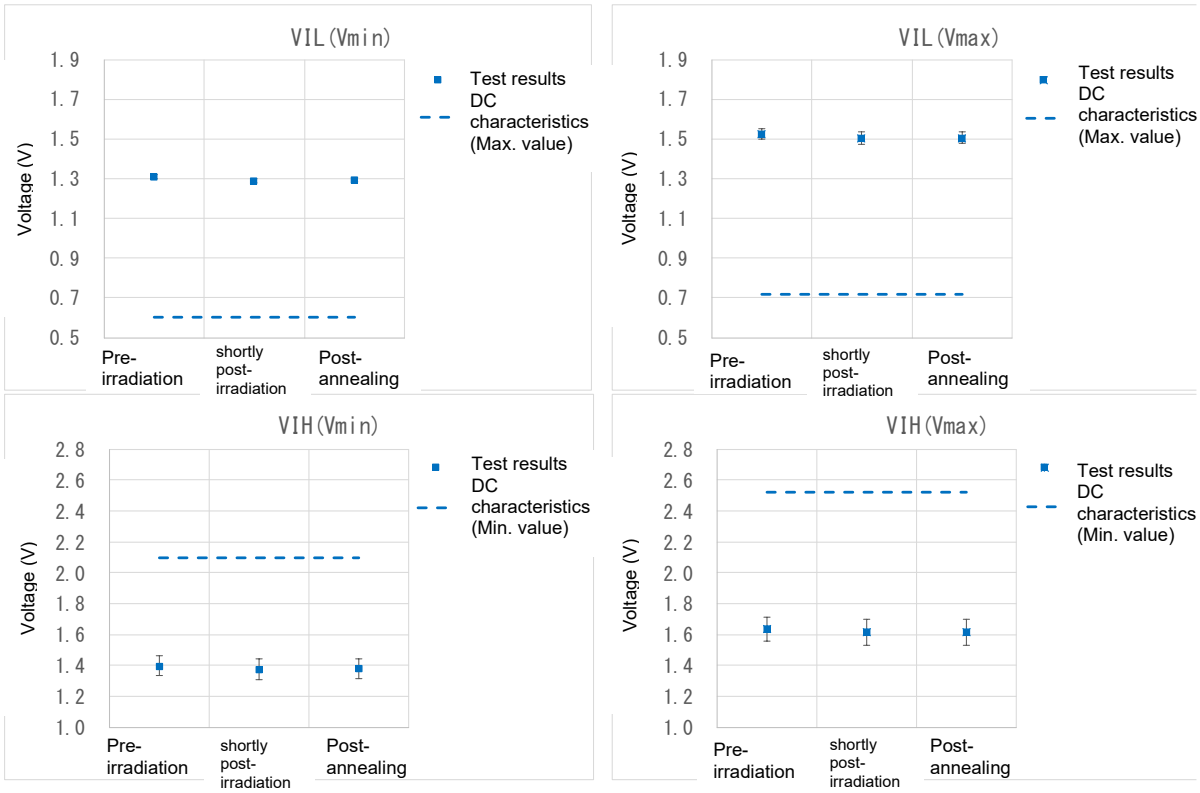
VET25311



Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-13. Current Consumption (IDDQ) at Screening (Burn-in) and Group C, Subgroup 1 Test (Steady State Life Test)

VET25311



Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-14. Input Characteristics (VIL/VIH) at Group E, Subgroup 1 Test
(Steady-State Total Ionizing Dose Test (TID Test))

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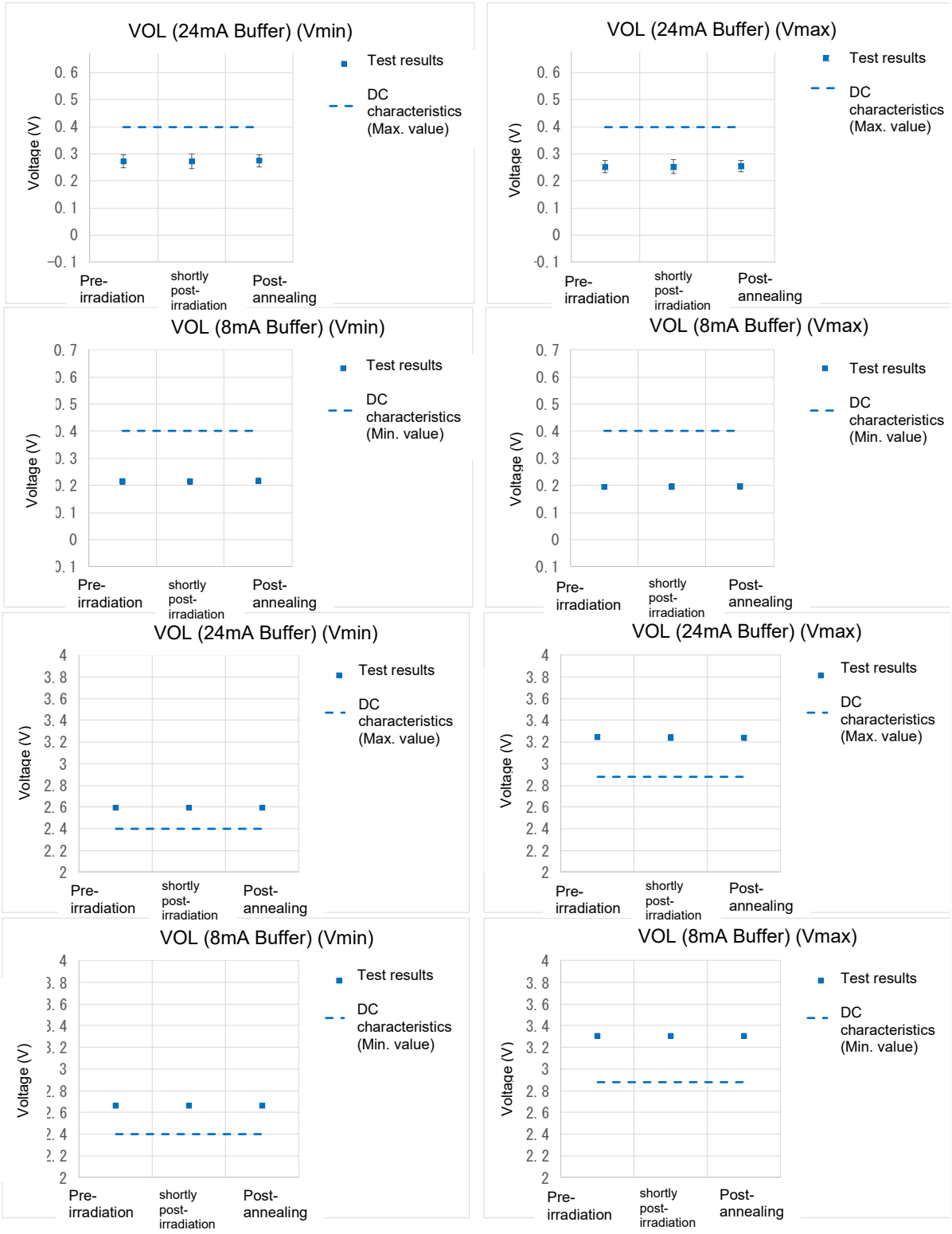
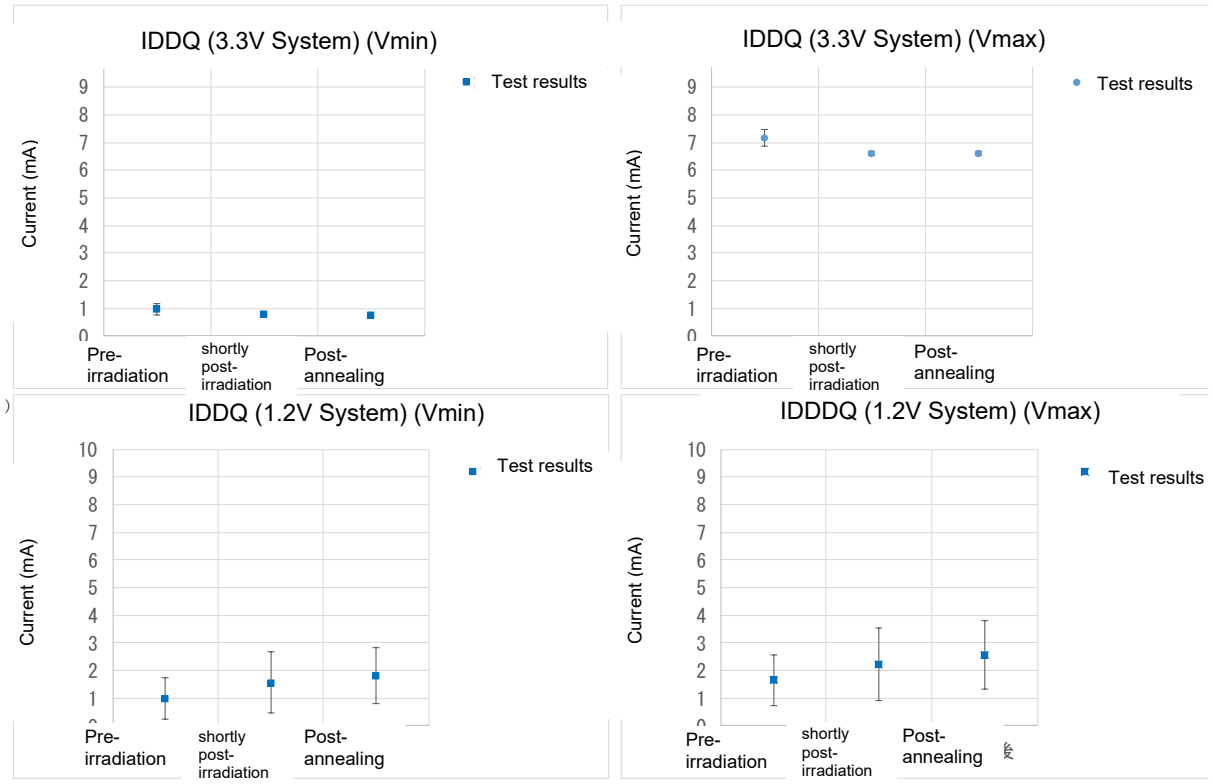


Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-15. Output Characteristics (VOL/VOH) at Group E, Subgroup 1 Test (Steady-State Total Ionizing Dose Test (TID Test))



Note: Power supply voltage condition: Vmin (VCCQ=3.0V, VDD=1.11V),
Vmax (VCCQ=3.6V, VDD=1.29V).

Figure 5-16. Current Consumption (IDDQ) at Group E, Subgroup 1 Test
(Steady-State Total Ionizing Dose Test (TID Test))

Table 5-2. Group E, Subgroup 2, Single Event Effects Test (SEE Hardness)

	Evaluation block		Saturated cross section (1)	LET Threshold (MeV/(mg/cm^2))	Corresponding test results
SEU	Memory section	Local RAM	No errors	- (2)	Tabel 5-4, No.1 SEU (1)
		Code RAM and shared memory	7.7x10^{-10} (cm^2/bit)	≧ 25 (3)	Table 5-4, No.1 SEU (1)
				≧ 40 (4)	Table 5-4, No.2 SEU (2)
	Logic section	Quicksort program operation as a representative example (operational frequency is 200MHz)	2.1x10^{-7} (cm^2/device) (5)	≧ 7 (5)	Table 5-4, No.3 SEU (3)
SEL	IO section	-	No errors	- (6)	Table 5-4, No.4 SEL
	Memory section (7) Logic section (7)	-	-	-	-

Notes (1): Defined as the mean value of test results.
(2): Since the errors were not detected at LET=0.8, 4, 7, 17, 41 and 68, LET threshold was not defined.
(3): In the case of using the scrubbing function on an ISS orbit with a scrubbing period of 327,680 seconds.
(4): In the case of using the scrubbing function at on GEO orbit with a scrubbing period of 1,310 seconds.
(5): For reference, on-orbit error count and error rate calculated from SEU logic section test results are shown in Table 5-3.
(6): Since the errors were not detected at LET=88, LET threshold was not defined.
(7): Since this IC has SOI structure and no parasitic thyristor is formed, the test results indicate latch-up-free.

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Table 5-3. (Reference Information) On-orbit Error Count and Error Rate Calculated from SEU Logic Section Test Results

Saturated cross section (cm^2/device)	LET threshold (MeV/(mg/cm^2))
2.1×10^{-7}	7

Orbit	Aluminium thickness: 100mil (2.54mm)			
	Orbit integral flux (1/m^2/s/sr)		Orbit integral flux (1/cm^2/day)	
	SolarMin	SolarMax	SolarMin	SolarMax
ISS	7.93E-04	9.99E-05	8.61E-02	1.08E-02
GEO	1.93E-02	2.37E-03	2.10E+00	2.57E-01

Calculation results for the error count and error ratio			
Error count (error / day)		Error ratio (FIT)	
SolarMin	SolarMax	SolarMin	SolarMax
1.81E-08	2.28E-09	0.8	0.1
4.40E-07	5.40E-08	18.3	2.3

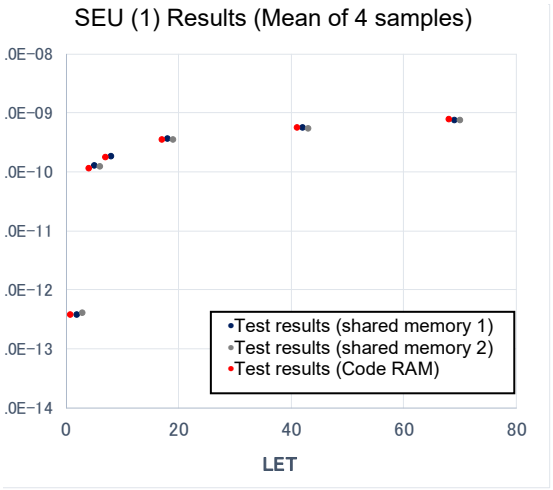
Table 5-4. Test Conditions of Group E, Subgroup 2, Single Event Effects Test

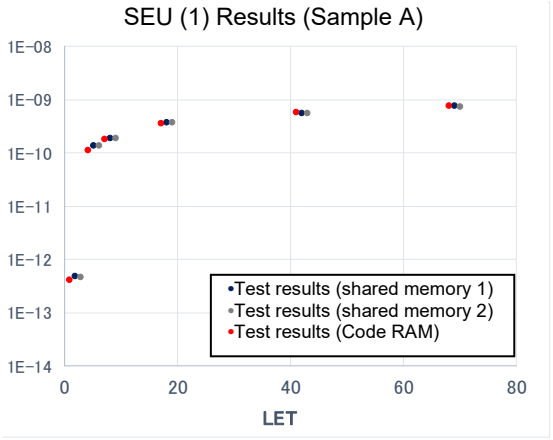
No.	Item	Sample conditions				Irradiation conditions		
		Operating condition	Poer supply voltage (1)	Board surface temperature	Number of test samples (2)	Ionic species (LET) (3)(4)	Irradiation angle (5)	Fluence [ions/cm^2]
1	SEU (1) (without error correcting)	The operation for local RAM, code RAM and shared memory shall not use the scrubbing function.	VCCQ= 3.3V VDD= 1.2V	Room temperature	4	Xe(68) Xe(41) Kr(17) Ar(7) Ar(4)	0°	Minimum of 1×10^6
						C(0.8)		Minimum of 2×10^7
2	SEU (2) (with error correcting)	The operation for local RAM, code RAM and shared memory shall use the scrubbing function.	VCCQ= 3.3V VDD= 1.2V	Room temperature	4	Xe(41)	0°	Minimum of 1×10^6
3	SEU (3) (Logic section)	The operation shall perform a sort calculation on the logic section.	VCCQ= 3.3V VDD= 1.2V	Room temperature	4	Xe(68) Xe(41) Kr(17) Ar(7) Ar(4)	0°	Minimum of 1×10^7
4	SEL	Same operational state as SEU (1) (without error correcting)	VCCQ= 3.6V VDD= 1.3V	+120°C	4	Os(88)	0°	Minimum of 1×10^8

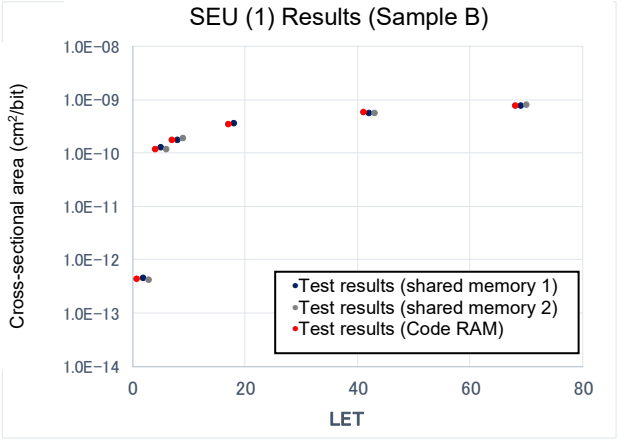
Notes (1): Setting value for power supply voltage during testing.
(2): Samples for Tests SEU (1), SEU (2), SEU (3) and SEL may be shared among each other.
(3): The unit of LET is MeV/(mg/cm^2), and the same applies to the following in this document.
(4): Irradiation facilities are shown below.

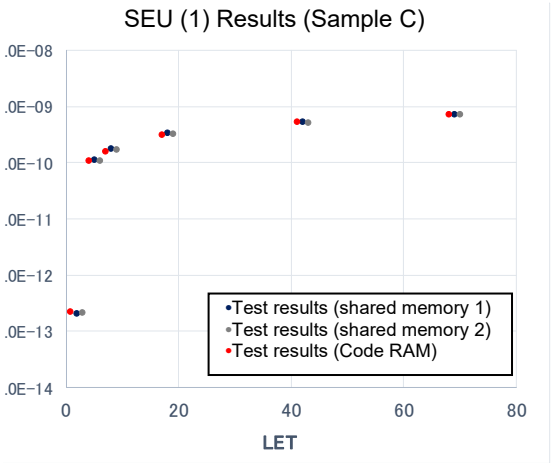
a) For Os(88), Ion Irradiation Research Facility TIARA,
Takasaki Institute for Advanced Quantum Science,
National Institutes for Quantum Science and Technology
b) Except for Os(88), ESA Course, Azimuthally Varying Field (AVF) Ring Cyclotron & RIKEN Ring Cyclotron (RRC),
RIKEN Nishina Center for Accelerator-Based Science,
National Research and Development Institute

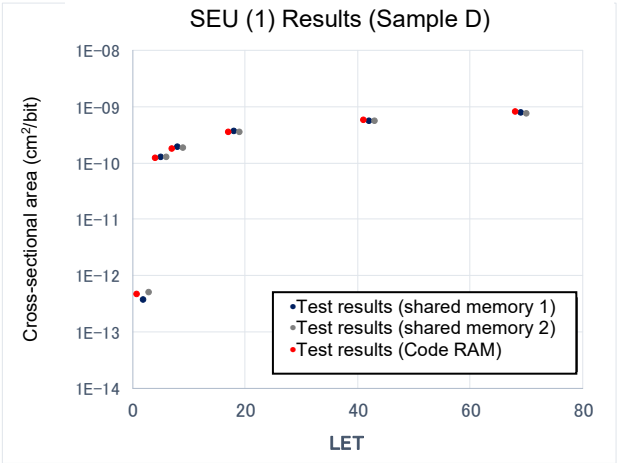
(5): The irradiation angle of 0° is defined as the case where the beam is incident parallel to the direction perpendicular to the semiconductor chip surface of the test sample, and where the beam is incident from the BEOL side of the semiconductor chip toward the substrate side.











Note: In order to easily verify the test results, shared memory 1 is plotted with LET incremented by +1, and shared memory 2 is plotted with LET incremented by +2.

Figure 5-17. SEU(1) Cross-Section Curve

Table 5-5. SEU(1) Cross-Sectional Area (1/2)

Ionic species	LET	Cross-sectional areas (cm^2/bit)			
		Mean of 4 samples			
		Local RAM	Shared memory 1	Shared memory 2	Code RAM
Xe	68	No errors	7.7E-10	7.6E-10	7.7E-10
Xe	41	No errors	5.6E-10	5.5E-10	5.7E-10
Kr	17	No errors	3.7E-10	3.6E-10	3.5E-10
Ar	7	No errors	1.9E-10	1.8E-10	1.8E-10
Ar	4	No errors	1.3E-10	1.2E-10	1.2E-10
C	0.8	No errors	3.8E-13	4.0E-13	3.8E-13

Ionic species	LET	Cross-sectional areas (cm^2/bit)							
		Sample A				Sample B			
		Local RAM	Shared memory 1	Shared memory 2	Code RAM	Local RAM	Shared memory 1	Shared memory 2	Code RAM
Xe	68	No errors	7.6E-10	7.4E-10	7.7E-10	No errors	7.8E-10	8.0E-10	7.8E-10
Xe	41	No errors	5.6E-10	5.5E-10	5.8E-10	No errors	5.7E-10	5.7E-10	5.9E-10
Kr	17	No errors	3.8E-10	3.8E-10	3.6E-10	No errors	3.7E-10	3.6E-10	3.5E-10
Ar	7	No errors	1.9E-10	1.9E-10	1.8E-10	No errors	1.8E-10	1.9E-10	1.8E-10
Ar	4	No errors	1.4E-10	1.4E-10	1.2E-10	No errors	1.3E-10	1.2E-10	1.2E-10
C	0.8	No errors	4.8E-13	4.7E-13	4.1E-13	No errors	4.6E-13	4.3E-13	4.4E-13

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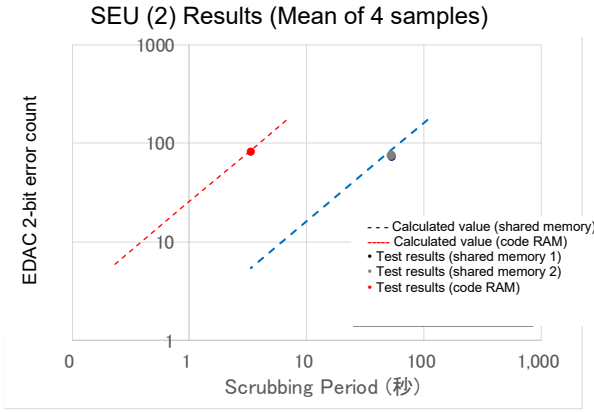
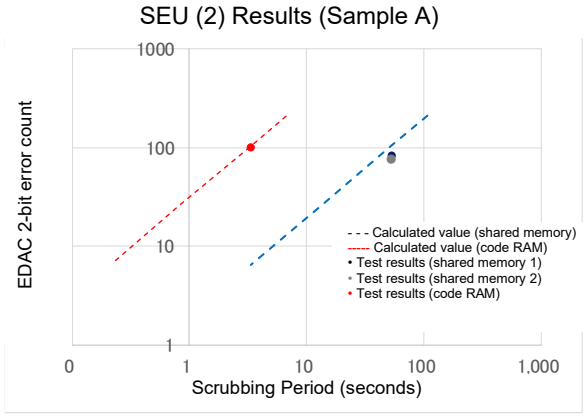
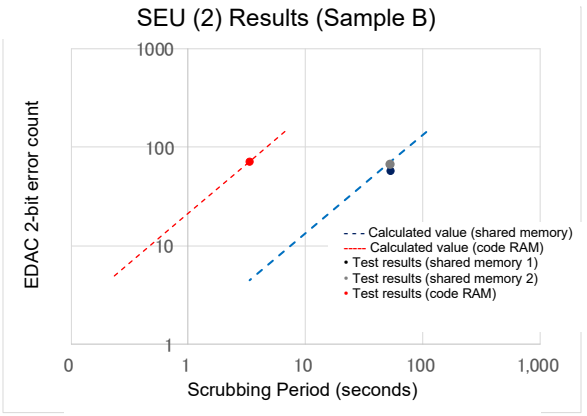
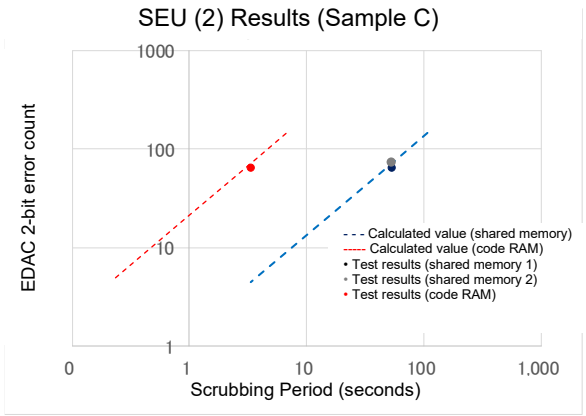
Table 5-5. SEU(1) Cross-Sectional Area (2/2)

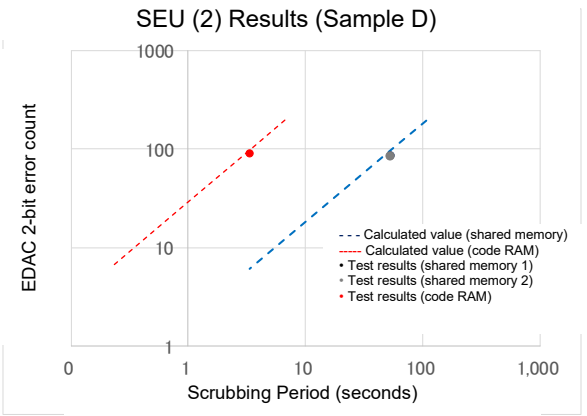
Ionic species	LET	Cross-sectional areas (cm^2/bit)							
		Sample C				Sample D			
		Local RAM	Shared memory 1	Shared memory 2	Code RAM	Local RAM	Shared memory 1	Shared memory 2	Code RAM
Xe	68	No errors	7.4E-10	7.3E-10	7.4E-10	No errors	7.8E-10	7.7E-10	8.1E-10
Xe	41	No errors	5.4E-10	5.1E-10	5.4E-10	No errors	5.7E-10	5.5E-10	5.8E-10
Kr	17	No errors	3.4E-10	3.3E-10	3.2E-10	No errors	3.7E-10	3.6E-10	3.6E-10
Ar	7	No errors	1.8E-10	1.7E-10	1.6E-10	No errors	2.0E-10	1.9E-10	1.8E-10
Ar	4	No errors	1.2E-10	1.1E-10	1.1E-10	No errors	1.3E-10	1.3E-10	1.2E-10
C	0.8	No errors	2.1E-13	2.2E-13	2.2E-13	No errors	3.7E-13	5.0E-13	4.7E-13







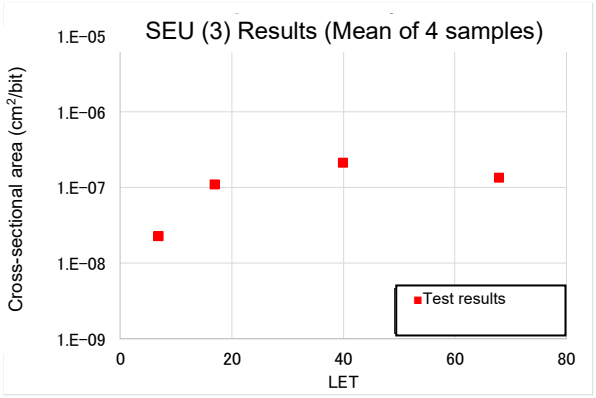


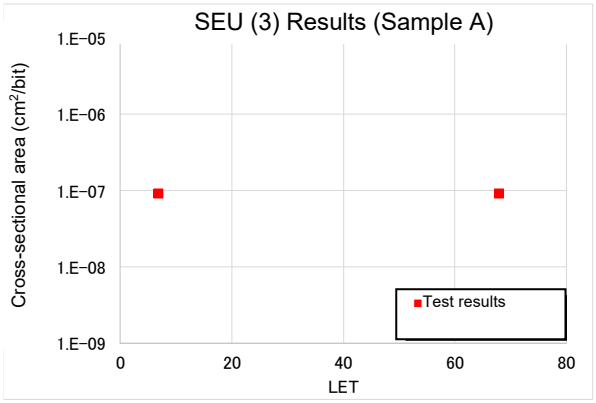


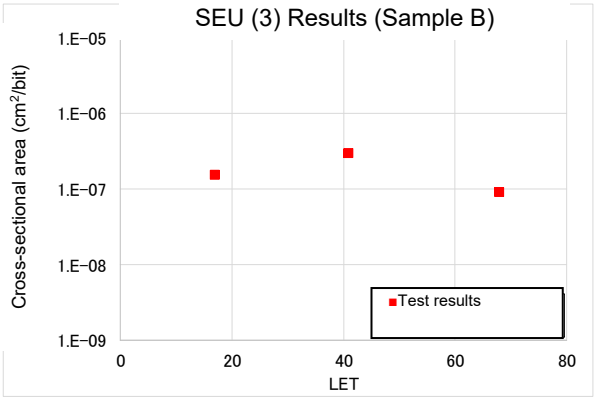
Note: (1) The test results represent the error count measured in single event tests (the number of events where 2 or more bits per word of SEU occur that cannot be corrected by read-modify-write).

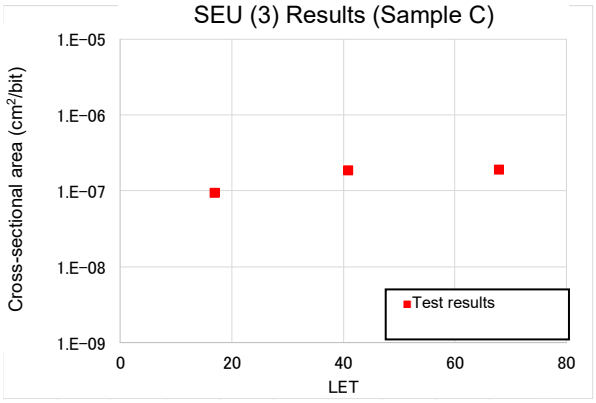
(2) The calculated value represents the relationship between the Scrubbing Period and the number of errors (defined as in the test results above) when the scrubbing function operates as required, based on the reverse cross sectional area for the single-event test's Flux, irradiation time and test LET.

Figure 5-18. SEU(2) Comparison of Test Data and Calculation Results









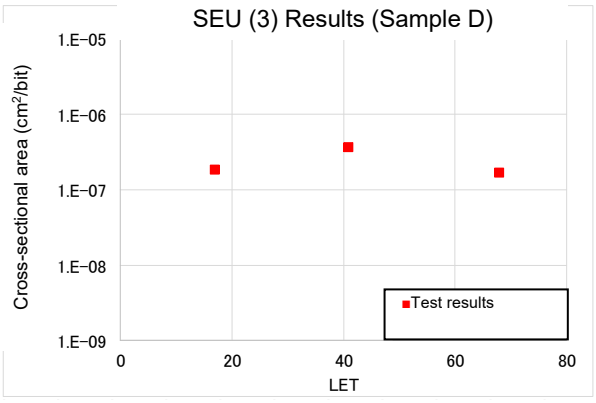


Figure 5-19. SEU(3) Cross-Section Curve

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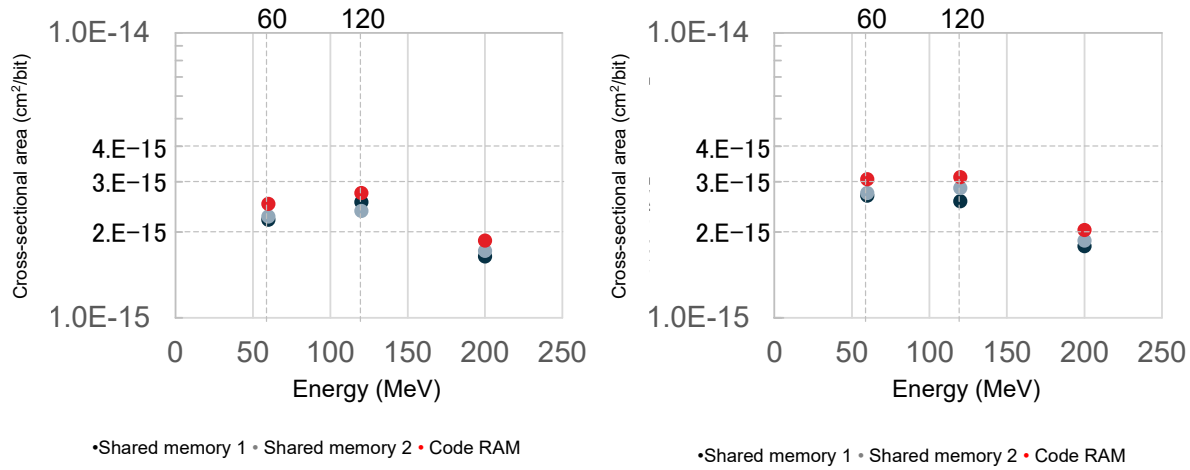
Table 5-6. SEU(3) Cross-Sectional Area

Ionic species	LET	Cross-sectional Areas (cm^2/device)				
		Mean of 4 samples	Sample A	Sample B	Sample C	Sample D
Xe	68	1.3E-07	8.9E-08	8.9E-08	1.9E-07	1.7E-07
Xe	41	2.1E-07	No errors	2.9E-07	1.8E-07	3.6E-07
Kr	17	1.1E-07	No errors	1.5E-07	9.2E-08	1.8E-07
Ar	7	2.2E-08	8.8E-08	No errors	No errors	No errors
Ar	4	No errors	No errors	No errors	No errors	No errors



(a) Sample A (b) Sample B

Figure 5-20. Proton Resistance

Table 5-6. Proton Resistance

Energy (MeV)	Cross-sectional Area (cm^2/bit)					
	Sample A			Sample B		
	Shared memory 1	Shared memory 2	Code RAM	Shared memory 1	Shared memory 2	Code RAM
200	1.6E-15	1.7E-15	1.9E-15	1.8E-15	1.9E-15	2.0E-15
120	2.5E-15	2.4E-15	2.7E-15	2.6E-15	2.8E-15	3.1E-15
60	2.2E-15	2.3E-15	2.5E-15	2.7E-15	2.7E-15	3.1E-15

Notes: (1) Sample size is 2 from the same lot.

(2) Code RAM, shared memory 1 and shared memory 2 were evaluated.

(3) Evaluation conditions are room temperature and Vtyp.

(4) The data pattern is All 0. Data pattern dependency has been confirmed in past tests to have no difference in cross-sectional area.

(5) Code RAM, shared memory 1 and shared memory 2 use the same memory macro.

(6) The capacity of each memory is shown in Table 2.1-1.

6. ENVIRONMENTAL LIMITS

Environmental limits of the ICs are as specified in this section.

6.1 Mechanical Combination Test

Table 6-1. Result of Mechanical Combination Test

Test item	Test conditions	Result [1]
Shock ↓ Vibration	1,500G: 0.5ms, 5 times each for 6 directions (X1, X2, Y1, Y2, Z1 and Z2) [2]	0/15
	20 to 2,000Hz and 20G, 4 times each for 3 directions (X, Y and Z) [2], 4 minutes / time	

Notes:

[1]: Unit: Number of failures/Total number of samples

[2]: The definition of direction shall be in accordance with paragraph B.2.2, Appendix B of JAXA-QTS-2010D.

6.2 Thermal Environmental and Moisture Resistance Combination Tests

Table 6-2. Thermal Environmental and Moisture Resistance Tests

Test item	Test conditions	Result[1]
Thermal shock ↓ Temperature cycling ↓ Moisture resistance	5 minutes each at -55°C and +125°C (5 minutes), 15 cycles	0/15
	10 minutes each at -65°C and +150°C, 100 cycles	
	RH= 80 to 98%, -10°C to +65°C, 10 cycles	

Notes:

[1]: Unit: Number of failures/Total number of samples

6.3 Radiation Hardness Test

Table 6-3. Radiation Hardness Evaluation Test

Test item	Test Conditions	Results [1]
Steady State Total Ionizing Dose Test (Total Dose Test)	Absorbed dose: 100krad (Si)	0/5

Notes:

[1]: Unit: Number of failures/Total number of samples

7. RELIABILITY

7.1 Failure Rate

The failure rates calculated using the accelerated life test results are shown in Table 7-1. The calculation conditions for the failure rate are VDD=1.2V, VCCQ=3.3V and confidence level=60%.

Table 7-1. Failure Rates based on Accelerated Test Results

Temperature (°C)	Failure Rate (FIT)	Temperature (°C)	Failure Rate (FIT)
105	760	70	18
100	464	60	6
90	166	50	2
85	98	40	0.4
80	57	20	0.02

8. STORAGE CONDITIONS

Storage conditions for ICs by the purchasers are shown below.

a) Ambient temperature: 15°C to 35°C
b) Relative humidity: 35% as a maximum
c) Pressure: 86kPa to 106kPa
d) Others: Vibration and shock shall not be applied to the ICs.

9. APPLICATION INSTRUCTIONS

a) The ICs shall be handled carefully to avoid damaging the solder balls.
During temporary storage while handling, place the package with the LID side facing down to protect the solder balls.

b) The cap on the package surface is connected to GND.

c) The solder ball attachment areas of IC package feature a dimple structure.
Therefore, since the solder balls are not able to be removed completely, it is impossible to perform rework on the solder balls.

d) Maximum number of reflow cycles shall be two.

10. OTHERS

a) Part numbers and suppliers of LSI socket are shown below.
Part number: 572BHQ10Y01G
Manufacturer: JC ELECTRONICS CORPORATION

b) Suppliers of the ICs are shown below.
Supplier: Contact information will be provided later.